SGM41603
I²C Controlled 10A Bidirectional Switched-Capacitor Converter

GENERAL DESCRIPTION

The SGM41603 is an efficient 2:1 bidirectional switched-capacitor converter with integrated power switches. It can deliver 10A in forward direction (2:1 voltage divider) and 5A in the reverse direction (1:2 voltage doubler). This device allows using a 2S Li+ power source as a 1S Li+ solution by inserting it between the 2S battery pack and charger output, and saves the existing 1S power architecture that is powered from the same battery.

This 2-phase high switching frequency (1.5MHz, MAX) and inductor-less topology allow low profile design with small footprint. The high switching frequency also reduces the size and quantity of the required capacitors. Safe operation is assured by over-voltage, under-voltage, over-current and thermal protections. Interference is also minimized by the built-in frequency dithering option. This device can achieve 98.5% efficiency which is the highest in its class. Thermal management of such a low loss device is simple, which makes it an ideal choice for industrial, consumer, and medical applications.

The I²C interface allows flexible parameter settings including OCP, OVLO, switching frequency thresholds and soft-start currents and durations. The SGM41603 is available in a Green WLCSP-2.85×2.59-42B package.

APPLICATIONS

Smartphones, Tablets, Ultrabooks
Chromebooks, DSLR and Mirrorless Cameras
Power Banks, 2S Li+ Battery Applications
Smartphone Direct Charging, Portable Printers
Portable Gaming Devices, Two-Way Radios

FEATURES

- **Bidirectional Switched Capacitor Converter**
  - **Forward Direction 2:1 Conversion, Reverse Direction 1:2 Conversion**
  - **2-Phase Interleaved Operation (90° or 180°)**
  - **8 Integrated N-Type MOSFET Switches**
  - **10A Output Current Capability**
  - **98.5% Peak Efficiency**
- **Low I_Q Current: 40μA Forward Operating**
- **6.7μA Shutdown Current**
- **I²C Interface with Interrupt Signaling**
- **Adjustable Soft-Start Current and Timeout**
- **0.25MHz to 1.5MHz Adjustable Switching Frequency**
- **Low EMI with Switching Frequency Dithering**
- **Enable Input**
- **Out-of-Audio Option at Light Load**
- **Power Good Output**
- **Programmable V1X & V2X Over-Voltage Lockout**
- **Separate OCP Adjustment for Each Direction**
- **Thermal Alarm and Protection**
- **Available in a Green WLCSP-2.85×2.59-42B Package**

TYPICAL APPLICATION

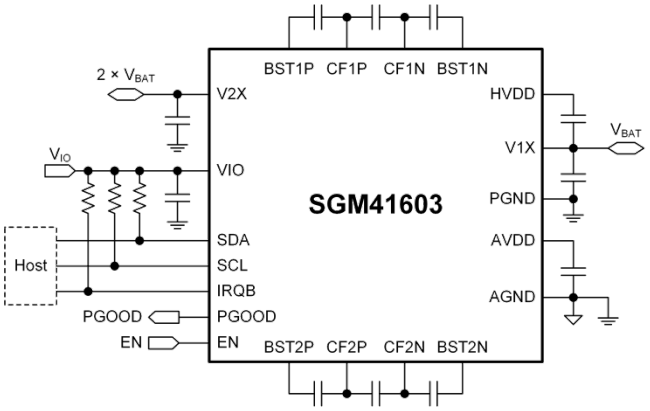


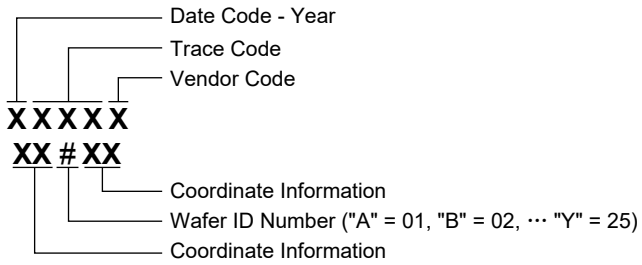
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41603	WLCSP-2.85×2.59-42B	-40℃ to +85℃	SGM41603YG/TR	064 XXXXX XX#XX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V2X to PGND ..... -0.3V to 16V
BSTxP to PGND ..... -0.3V to 16V
BSTxN to PGND ..... -0.3V to 8V
BSTxP to CFxP ..... -0.3V to 6V
BSTxN to CFxN ..... -0.3V to 6V
CFxP to PGND ..... -0.3V to (V_{V1X} + 6V)
CFxN, V1X to PGND ..... -0.3V to 6V
PGND to AGND ..... -0.3V to 0.3V
HVDD to AGND ..... -0.3V to (V_{V1X} + 6V)
AVDD, NC, IRQB, VIO to AGND ..... -0.3V to 6V
EN to AGND ..... -0.3V to 16V
SDA, SCL to AGND ..... -0.3V to (V_{VIO} + 0.3V)
PGOOD to AGND ..... -0.3V to 2.0V
V1X Continuous RMS Current (From V2X to V1X) 10A
Package Thermal Resistance
WLCSP-2.85×2.59-42B, θ_{JA} ..... 62℃/W
WLCSP-2.85×2.59-42B, θ_{JB} ..... 15.5℃/W
WLCSP-2.85×2.59-42B, θ_{JC} ..... 25.6℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

V2X ..... 5V to 11V
V1X ..... 2.8V to 5.5V
I_{V1X} (Voltage Divider Mode) ..... 0A to 10A
I_{V2X} (Voltage Doubler Mode) ..... 0A to 5A
(BST1P - CF1P), (BST1N - CF1N) ..... 0V to 5V
(CF1P - V1X), CF1N ..... 0V to 5.5V
(BST2P - CF2P), (BST2N - CF2N), ... 0V to 5V
(CF2P - V1X), CF2N ..... 0V to 5.5V
AVDD, (HVDD - V1X), VIO, EN ..... 0V to 5V
PGOOD ..... 0V to 1.8V
SDA, SCL, IRQB ..... 0V to 5V
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

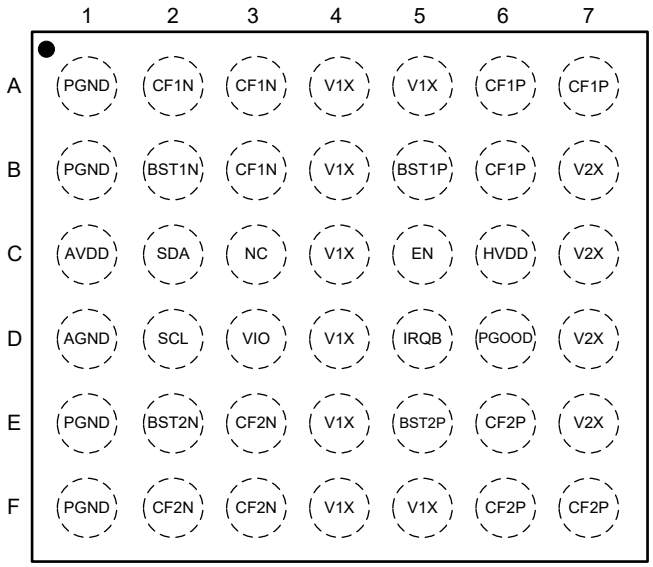
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.85×2.59-42B

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1, B1, E1, F1	PGND	P	Power Ground.
A2, A3, B3	CF1N	P	Flying Cap Phase 1 Negative Node. Connect at least two parallel 47μF capacitors between CF1P and CF1N pins as close as possible to these pins.
A4, A5, B4, C4, D4, E4, F4, F5	V1X	P	Lower Voltage (1X) Power Port. It is an input in forward mode and an output in reverse mode. A 22μF capacitor is recommended between V1X and PGND.
A6, A7, B6	CF1P	P	Flying Cap Phase 1 Positive Node. Connect at least two parallel 47μF capacitors between CF1P and CF1N pins as close as possible to these pins.
B2	BST1N	P	Bootstrap Capacitor Connection for Q_{CL1} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF1N.
B5	BST1P	P	Bootstrap Capacitor Connection for Q_{CH1} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF1P.
B7, C7, D7, E7	V2X	P	Higher Voltage (2X) Power Port. It is an input in forward and an output in reverse direction. A 22μF capacitor is recommended between V2X and PGND.
C1	AVDD	AO	5V LDO Output. Decouple AVDD to AGND with at least 1μF high quality ceramic capacitor (X5R or better). Do not connect any external load to AVDD.
C2	SDA	DIO	I²C Interface Data Line.
C3	NC	–	No Connection. Leave this pin open.
C5	EN	DI	Active High Device Enable Input.
C6	HVDD	AO	(V_{V1X} + 5V) LDO Output. Decouple HVDD to V1X with at least 1μF high quality ceramic capacitor (X5R or better). Do not connect any external load to HVDD.
D1	AGND	P	Analog Ground.
D2	SCL	DI	I²C Interface Clock Line.
D3	VIO	P	Input Voltage Supply for I/O Circuits. Bypass this pin to AGND with at least 1μF high quality ceramic capacitor (X5R or better).
D5	IRQB	DO	Open-Drain Active Low Interrupt Output. Pull it up with a 100kΩ resistor to VIO. A low on IRQB indicates a fault condition.
D6	PGOOD	DO	Power Good Output.
E2	BST2N	P	Bootstrap Capacitor Connection for Q_{CL2} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF2N.
E3, F2, F3	CF2N	P	Flying Cap Phase 2 Negative Node. Connect at least two parallel 47μF capacitors between CF2P and CF2N pins as close as possible to these pins.
E5	BST2P	P	Bootstrap Capacitor Connection for Q_{CH2} Gate Driver Supply. Place a 47nF or larger ceramic capacitor between this pin and CF2P.
E6, F6, F7	CF2P	P	Flying Cap Phase 2 Positive Node. Connect at least two parallel 47μF capacitors between CF2P and CF2N pins as close as possible to these pins.

NOTE:
1. P = Power, AI = Analog Input, AO = Analog Output, AIO = Analog Input/Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output.

ELECTRICAL CHARACTERISTICS

(V_{V2X} = 7.6V, V_{V1X} = 3.8V, C_{FLY}/phase = 3 × 47μF, V_{VIO} = 1.8V, f_{SW} = 0.25MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Global Input Supply							
Shutdown Supply Current	I_{SHDN_V2X}	EN = LOW, V_{VIO} = 0V, V_{V2X} = 8.4V	T_J= +25℃		6.70	8.60	μA
			T_J = -40℃ to +85℃		6.70	11.25	
	I_{SHDN_V1X}	EN = LOW, V_{VIO} = 0V, V_{V1X} = 4.2V	T_J = +25℃		5.80	7.15	
			T_J = -40℃ to +85℃		5.80	9.30	
Quiescent Current	I_{Q_V2X}	V_{V2X} = 8.4V, automatic mode			40		μA
	I_{Q_V1X}	V_{V1X} = 4.2V, automatic mode			84		
Shutdown VIO Current	I_{SHDN_VIO}	V_{VIO} = 5.5V	T_J = +25℃		0.2	1.3	μA
			T_J = -40℃ to +85℃		0.2	1.5	
V1X Leakage Current	I_{LK_V1X}	V_{V2X} = 4.2V, V1X_AD_EN = 0, EN = LOW, V_{VIO} = 0V (Measure at V1X pin), T_J = +25℃			0.1	1.0	μA
Input Under-Voltage Lockout							
Under-Voltage Lockout Threshold	$V2X_{UVLO\_R}$	V_{V2X} rising	T_J = +25℃	3.35	3.58	3.81	V
			T_J = -40℃ to +85℃	3.22	3.58	3.95	
	$V2X_{UVLO\_F}$	V_{V2X} falling	T_J = +25℃	2.27	2.47	2.66	
			T_J = -40℃ to +85℃	2.25	2.47	2.68	
	$V2X_{UVLO\_HYS}$	V2X UVLO hysteresis			1.10		
	$V1X_{UVLO\_R}$	V_{V1X} rising	T_J = +25℃	2.55	2.76	2.97	
			T_J = -40℃ to +85℃	2.53	2.76	2.99	
	$V1X_{UVLO\_F}$	V_{V1X} falling	T_J = +25℃	2.27	2.46	2.66	
			T_J = -40℃ to +85℃	2.25	2.46	2.68	
	$V1X_{UVLO\_HYS}$	V1X UVLO hysteresis			0.30		
Enable Inputs and Logic							
EN Deglitch Time	t_{EN_DEG}	Deglitch between V_{EN} rising above V_{IH} and starting soft-start action, when t_{EN_DEG} = 0.125ms (I^2C programmable from 0.125ms to 64ms, default 0.125ms)			0.125		ms
Logic Input Low Level	V_{IL}	EN pin, T_J = +25℃				0.80	V
Logic Input High Level	V_{IH}	EN pin, T_J = +25℃		0.82			V
EN Pull-Down Resistance	R_{EN_PD}	Pulled down to AGND, T_J = +25℃		0.95	1.20	1.50	MΩ
EN Input Leakage Current	I_{LK_EN}	EN pin connected to 16V, T_J = +25℃			0.01	0.40	μA
IRQB Pin Output High Leakage	I_{LK_IRQB}	IRQB pin, V_{IRQB} = 5.5V, T_J = +25℃			0.01	0.50	μA
AVDD Linear Regulator Output Voltage	V_{AVDD}	T_J = +25℃		4.55	4.90	5.30	V
		T_J = -40℃ to +85℃		4.50	4.90	5.35	V
HVDD Linear Regulator Output Voltage	V_{HVDD}	V_{V1X} = 1.5V			5.10		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{V2X} = 7.6V, V_{V1X} = 3.8V, C_{FLY}/phase = 3 × 47μF, V_{VIO} = 1.8V, f_{SW} = 0.25MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Switched-Capacitor Converter							
Switching Stop Deglitch Time	$t_{SW\_F\_DEG}$	Deglitch time between the time of V_{V1X} or V_{V2X} falling below its switching threshold and stopping the switching action, when $t_{SW\_F\_DEG}$ = 108μs (I^2C programmable from 0ms to 1ms, default 0ms)			108		μs
Forward Mode Soft-Start Current (all at V1X)	I_{SS_FWD}	V_{V1X} > 0.25V_{V2X} when I_{SS_FWD} = 145mA (I^2C programmable from 145mA to 580mA, 145mA per step, default 580mA)			130		mA
Reverse Mode Soft-Start Current (all at V2X)	I_{RSS_LC}	V_{V2X} < $V2X_{VALID}$ when I_{RSS_LC} = 100mA (I^2C programmable from 100mA to 250mA, default 150mA)			175		mA
	I_{RSS_HC}	V_{V2X} > $V2X_{VALID}$ when I_{RSS_HC} = 260mA (I^2C programmable from 260mA to 400mA, 20mA per step, default 260mA)			440		
Valid V2X Voltage During Soft-Start	$V2X_{VALID}$	V_{V2X} rising, threshold for entering high current soft-start, when $V2X_{VALID}$ = 5.9V (I^2C programmable from 5.5V to 5.9V, 0.4V per step, default 5.9V)	T_J = +25℃	5.670	5.880	6.085	V
			T_J = -40℃ to +85℃	5.660	5.880	6.095	
Light Load Efficiency	η_{LIGHT1_FWD}	I_{V1X} = 1mA, V_{V2X} = 7.4V, REG0x0F = 0xFD			91.3		%
	η_{LIGHT2_FWD}	I_{V1X} = 30mA, V_{V2X} = 7.4V, REG0x0F = 0xFD			97.6		%
Peak Efficiency	η_{PEAK_FWD}				98.5		%
Heavy Load Efficiency	η_{HEAVY_FWD}	I_{V1X} = 10A, V_{V2X} = 9V			95.8		%
Light Load Efficiency (Reverse)	η_{LIGHT1_RVS}	I_{V2X} = 1mA, V_{V1X} = 3.7V, REG0x0F = 0xFD			94.1		%
Heavy Load Efficiency (Reverse)	η_{HEAVY_RVS}	I_{V2X} = 5A, V_{V1X} = 4.5V			95.8		%
R_{DSON} of Q_{CH1} and Q_{CH2}	R_{DS_QCH}	T_J = +25℃			8.5	11.7	mΩ
		T_J = -40℃ to +85℃			8.5	14.5	
R_{DSON} of Q_{DH1} and Q_{DH2}	R_{DS_QDH}	T_J = +25℃			8.9	13.6	
		T_J = -40℃ to +85℃			8.9	16.5	
R_{DSON} of Q_{CL1} and Q_{CL2}	R_{DS_QCL}	T_J = +25℃			6.6	9.1	
		T_J = -40℃ to +85℃			6.6	11.5	
R_{DSON} of Q_{DL1} and Q_{DL2}	R_{DS_QDL}	T_J = +25℃			8.9	13.6	
		T_J = -40℃ to +85℃			8.9	15.5	
Switching Frequency	f_{SW}	When f_{SW} = 250kHz (I^2C programmable from 250kHz to 1.5MHz, default 250kHz)	T_J = +25℃	225	250	275	kHz
			T_J = -40℃ to +85℃	220	250	280	
Switching Frequency Dither Rate	f_{SW_DTHR}	When f_{SW_DTHR} = 3% (I^2C programmable from 3% to 12% or OFF, default 3%)	T_J = +25℃	±2.5	±3.5	±4.5	%
			T_J = -40℃ to +85℃	±2.5	±3.5	±4.5	
Active Discharge Resistance	R_{AD_V2X}	Active discharge is enabled, SCC is disabled	T_J = +25℃	8.00	9.90	12.00	kΩ
			T_J = -40℃ to +85℃	7.95	9.90	12.10	
	R_{AD_V1X}		T_J = +25℃	0.91	1.03	1.18	
			T_J = -40℃ to +85℃	0.90	1.03	1.20	

ELECTRICAL CHARACTERISTICS (continued)

(V_{V2X} = 7.6V, V_{V1X} = 3.8V, C_{FLY}/phase = 3 × 47μF, V_{VIO} = 1.8V, f_{SW} = 0.25MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Protections							
Over-Voltage Protection Threshold	$V2X_{OVP\_R}$	Rising, when $V2X_{OVP\_R}$ = 8.7V (I^2C programmable from 8.3V to 11V, default 9.5V)	T_J = +25℃	8660	8700	8740	mV
			T_J = -40℃ to +85℃	8646	8700	8757	
		Rising, $V2X_{OVP\_R\_ACC}$ when $V2X_{OVP\_R}$ = 8.7V	T_J = +25℃	-0.5		0.5	%
			T_J = -40℃ to +85℃	-0.7		0.7	
		Rising, when $V2X_{OVP\_R}$ = 11V (I^2C programmable from 8.3V to 11V, default 9.5V)	T_J = +25℃	10945	11005	11064	mV
			T_J = -40℃ to +85℃	10930	11005	11082	
		Rising, $V2X_{OVP\_R\_ACC}$ when $V2X_{OVP\_R}$ = 11V	T_J = +25℃	-0.6		0.6	%
			T_J = -40℃ to +85℃	-0.7		0.8	
	$V2X_{OVP\_HYS}$	V2X OVP Hysteresis			180		mV
	$V1X_{OVP\_R}$	Rising, when $V1X_{OVP\_R}$ = 4.35V (I^2C programmable from 4.15V to 5.5V, default 5.3V)	T_J = +25℃	4332	4350	4368	mV
			T_J = -40℃ to +85℃	4324	4350	4380	
		Rising, $V1X_{OVP\_R\_ACC}$ when $V1X_{OVP\_R}$ = 4.35V	T_J = +25℃	-0.5		0.5	%
			T_J = -40℃ to +85℃	-0.7		0.7	
		Rising, when $V1X_{OVP\_R}$ = 4.9V (I^2C programmable from 4.15V to 5.5V, default 5.3V)	T_J = +25℃	4876	4900	4924	mV
			T_J = -40℃ to +85℃	4868	4900	4935	
		Rising, $V1X_{OVP\_R\_ACC}$ when $V1X_{OVP\_R}$ = 4.9V	T_J = +25℃	-0.5		0.5	%
			T_J = -40℃ to +85℃	-0.7		0.8	
	$V1X_{OVP\_HYS}$	V1X OVP Hysteresis			90		mV
V1X OCP1 Threshold (Bidirectional)	I_{V1X_OCP1}	When I_{V1X_OCP1} = 4.2A (I^2C programmable from 4.2A to 11.6A, default 10.4A)		3900	4215	4600	mA
V1X OCP1 Accuracy	$I_{V1X\_OCP1\_ACC}$	In the entire I_{V1X_OCP1} range		-7.5		9.2	%
OCP2 Offset	$V1X_{OCP2}$	When $V1X_{OCP2}$ = 310mV (I^2C programmable from 110mV to 310mV, default 310mV)	T_J = +25℃	230	295	365	mV
			T_J = -40℃ to +85℃	225	295	370	
	$V2X_{OCP2}$	When $V2X_{OCP2}$ = 620mV (I^2C programmable from 340mV to 900mV, 40mV per step, default 620mV)	T_J = +25℃	475	605	740	
			T_J = -40℃ to +85℃	465	605	750	
Thermal Alarms and Shutdown							
Thermal Alarm at +100℃	T_{INT100}	T_J rising, +15℃ hysteresis			100		℃
Thermal Alarm at +120℃	T_{INT120}	T_J rising, +15℃ hysteresis			120		℃
Thermal Shutdown Rising Threshold	$T_{DIE\_OTP\_R}$				160		℃
Thermal Shutdown Rising Threshold Hysteresis	$T_{DIE\_OTP\_HYS}$				20		℃
SDA and SCL I/O Stage							
Input Logic Low Level		T_J = +25℃				0.4 × V_{VIO}	V
Input Logic High Level		T_J = +25℃		0.5 × V_{VIO}			V
SCL, SDA Logic Input Current		V_{SCL} = V_{SDA} = V_{VIO} = 1.8V, T_J = +25℃			0.01	1.00	μA
SCL, SDA Input Capacitance					10		pF

ELECTRICAL CHARACTERISTICS (continued)

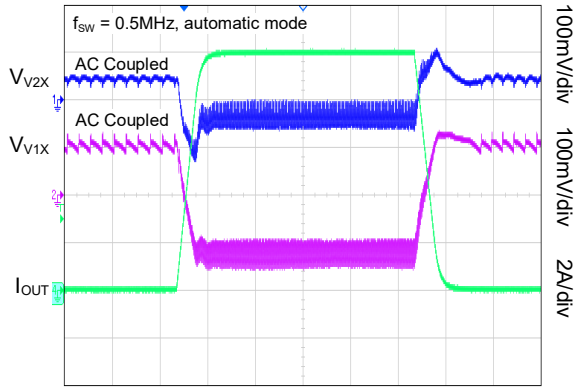
(V_{V2X} = 7.6V, V_{V1X} = 3.8V, C_{FLY}/phase = 3 × 47μF, V_{VIO} = 1.8V, f_{SW} = 0.25MHz, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Compatible Interface Timing for Standard, Fast, and Fast-Mode Plus Speeds						
Clock Frequency	f_{SCL}			1000		kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$			0.26		μs
CLK Low Period	t_{LOW}			0.5		μs
CLK High Period	t_{HIGH}			0.26		μs
Setup Time Repeated START Condition	$t_{SU;STA}$			0.26		μs
DATA Hold Time	$t_{HD:DAT}$			0		μs
DATA Valid Time	$t_{VD:DAT}$			0.45		μs
DATA Valid Acknowledge Time	$t_{VD:ACK}$			0.45		μs
DATA Setup Time	$t_{SU;DAT}$			50		ns
Setup Time for STOP Condition	$t_{SU;STO}$			0.26		μs
Bus-Free Time between STOP and START	t_{BUF}			0.5		μs

TYPICAL PERFORMANCE CHARACTERISTICS

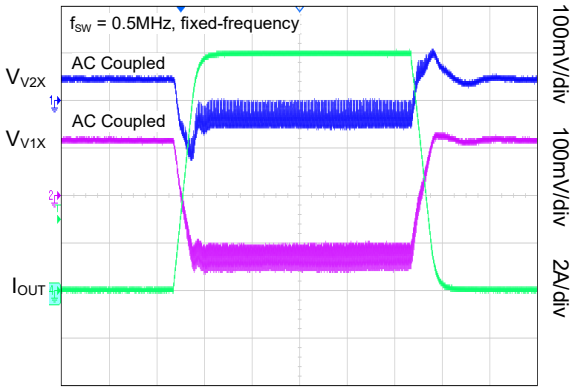
V_{V2X} = 7.4V, V_{VIO} = 1.8V, C_{FLY}/phase = 2 × 47μF, C_{V1X} = 67μF, f_{SW} = 0.5MHz, unless otherwise specified.

10A Load Transient



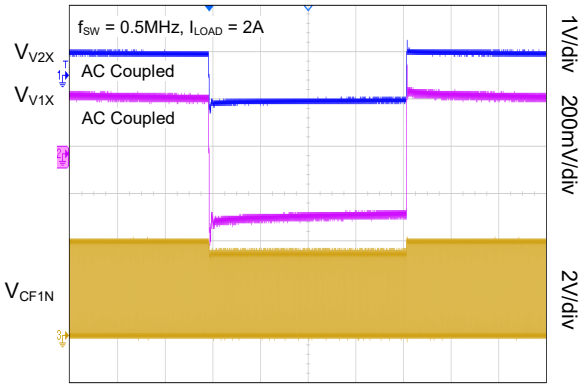
Time (100μs/div)

10A Load Transient



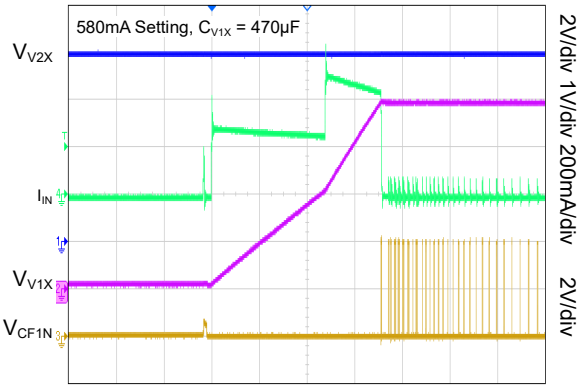
Time (100μs/div)

1V Line Transient



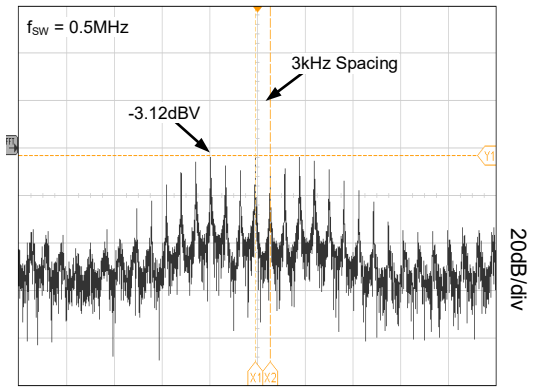
Time (2ms/div)

Soft-Start Waveform



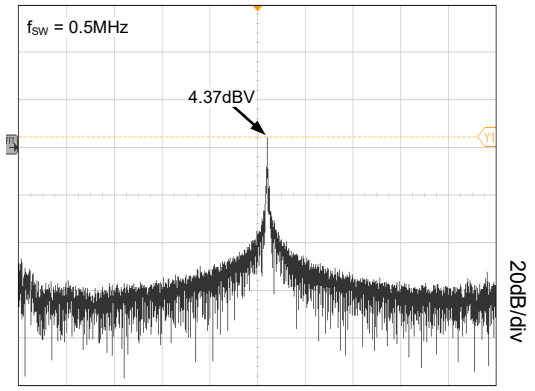
Time (2ms/div)

3% Dithering Frequency Spectrum



500kHz Center, 10kHz/div

Dithering Disabled Frequency Spectrum

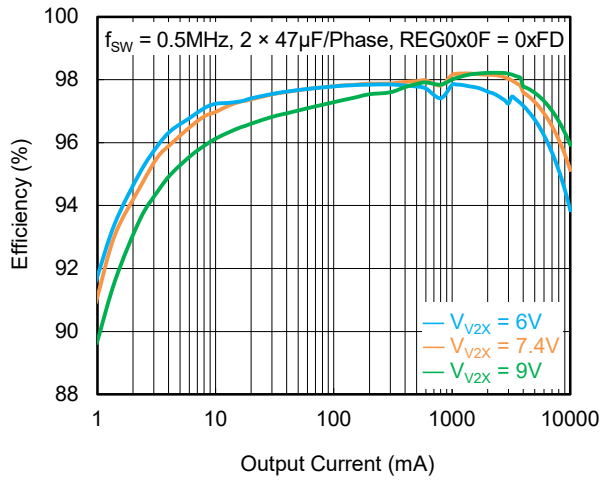


500kHz Center, 10kHz/div

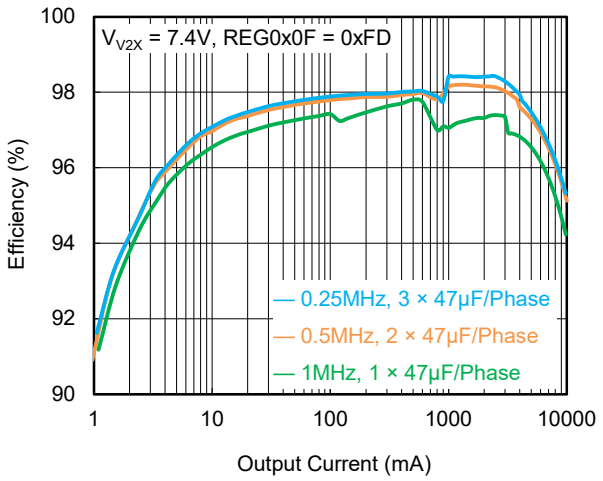
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{V2X} = 7.4V, V_{VIO} = 1.8V, C_{FLY}/phase = 2 × 47μF, C_{V1X} = 67μF, f_{SW} = 0.5MHz, unless otherwise specified.

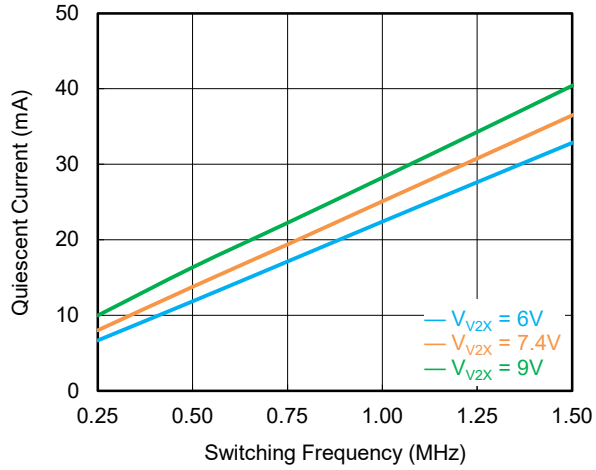
Automatic Mode Efficiency vs. Output Current



Automatic Mode Efficiency vs. Output Current



Fixed-Frequency Mode Quiescent Current vs. Switching Frequency



FUNCTIONAL BLOCK DIAGRAM

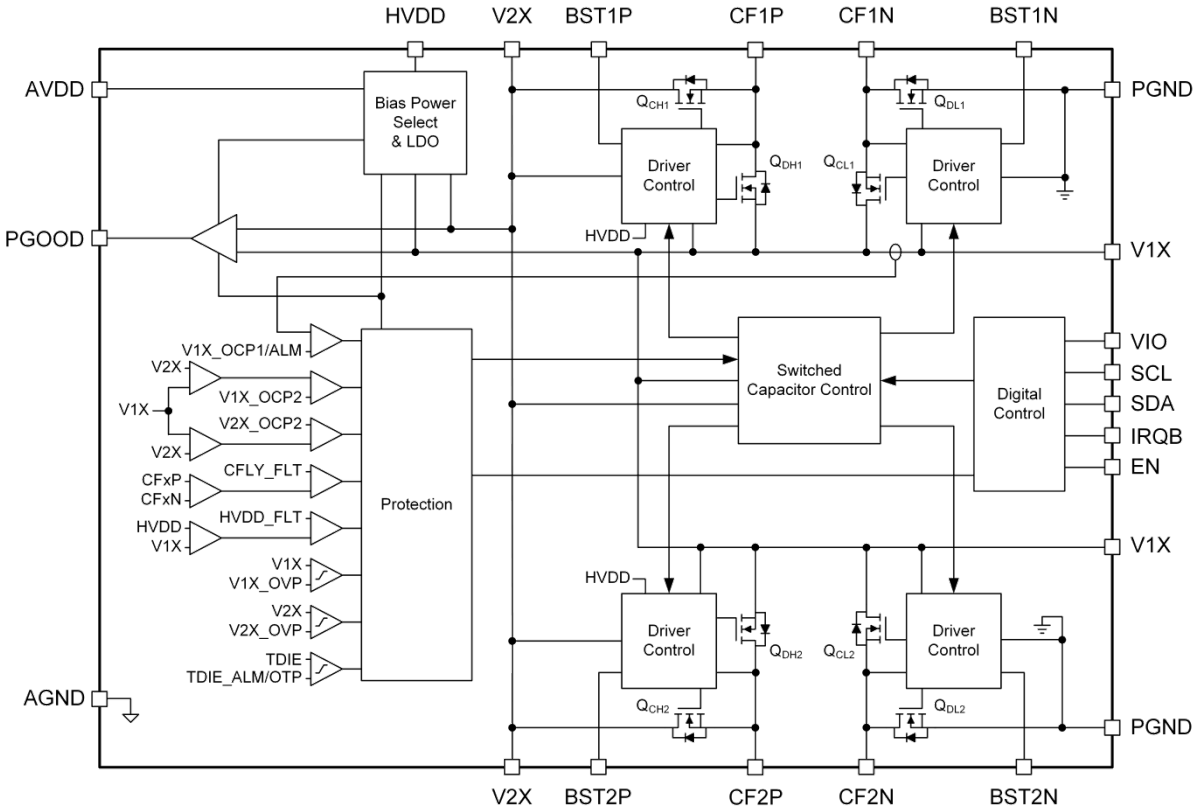


Figure 2. SGM41603 Block Diagram

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM41603 is: 0x68 (0b1101000 + W/R)

FUNCTION	FLAG	MASK	STATUS	THRESHOLD SETTING	ENABLE	DEGLITCH
V2X_OVP	0x00[7]	0x01[7]	0x02[7]	0x08[7:3]	—	—
V1X_OVP	0x00[6]	0x01[6]	0x02[6]	0x09[4:0]	—	—
V1X_OC_ALM	0x00[5]	0x01[5]	0x02[5]	0x0A[7]	—	—
V1X_OCP	0x00[4]	0x01[4]	—	V1X_OCP1: 0x0A[4:0] V1X_OCP2: 0x0B[3:0]	V1X_OCP2: 0x0B[3:0]	—
T_ALM1	0x00[3]	0x01[3]	0x02[3]	—	—	—
T_ALM2	0x00[2]	0x01[2]	0x02[2]	—	—	—
T_SHDN	0x00[1]	0x01[1]	0x02[1]	—	—	—
FSS_FLT	0x00[0]	0x01[0]	—	FWD_ISS: 0x0C[5:4] FWD_SS_T: 0x0C[2:0]	—	0x0C[2:0]
V2X_VALID_INT	0x03[7]	0x04[7]	0x02[0]	0x0D[0]	—	—
CFLY_FLT	0x03[6]	0x04[6]	—	—	—	—
HVDD_FLT	0x03[5]	0x04[5]	—	—	—	—
SW_DIR_INT	0x03[4]	0x04[4]	0x02[4]	—	—	—
RSS_FLT	0x03[2]	0x04[2]	—	RVS_ISS_HC: 0x0D[7:5] RVS_ISS_LC: 0x0D[4:3] RVS_SS_T: 0x0D[2:1]	—	0x0D[2:1]
V2X_OCP	0x03[1]	0x04[1]	—	V1X_OCP1: 0x0A[4:0] V2X_OCP2: 0x0B[7:4]	V2X_OCP2: 0x0B[7:4]	—
PWRON_INT	0x03[0]	—	—	—	—	—
RPUPD_EN	—	—	—	—	0x05[7]	—
DCVIO	—	—	—	—	0x06[7]	0x05[6:4]
EN_DEG	—	—	—	—	—	0x05[3:1]
SCC_EN	—	—	—	—	0x05[0]	—
SFT_DISCHG_T	—	—	—	—	—	0x06[5:4]
OOA_EN	—	—	—	—	0x06[3]	—
V2X_AD_EN	—	—	—	—	0x06[2]	—
V1X_AD_EN	—	—	—	—	0x06[1]	—
FIX_FREQ	—	—	—	—	0x06[0]	—
SCC_DIR	—	—	—	0x07[7:6]	—	—
DTHR	—	—	—	0x07[5:4]	0x07[5:4]	—
FREQ	—	—	—	0x07[2:0]	—	—
V2X_SW_F	—	—	—	0x08[1:0]	—	0x09[6:5]
V1X_SW_F	—	—	—	0x09[7]	—	0x09[6:5]
RESTART_EN	—	—	—	—	0x0E[3]	—
WAIT_T	—	—	—	0x0E[1:0]	—	—
F2S_DROP	—	—	—	0x0F[7:6]	—	—
SKIP_HYST	—	—	—	0x0F[1:0]	—	—
S2F_DROP	—	—	—	0x0F[5:4]	—	—
OTP_VER	—	—	—	0x10[7:4]	—	—
CHIP_VER	—	—	—	0x10[3:0]	—	—
DEVICE_ID	—	—	—	0x11[7:0] (0x03)	—	—

REGISTER MAPS (continued)

Bit Types:
R: Read only
R/W: Read/Write
RC: Read clears the bit
R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

REG0x00: INT_SRC Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V2X_OVP_INT	0	RC	V2X_OVP Fault Flag Bit 0 = No V2X_OVP fault 1 = V2X_OVP fault has occurred, or the V2X_OVP status bit is reset from '1' to '0' when the fault is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[6]	V1X_OVP_INT	0	RC	V1X_OVP Fault Flag Bit 0 = No V1X_OVP fault 1 = V1X_OVP fault has occurred, or the V1X_OVP status bit is reset from '1' to '0' when the fault is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[5]	V1X_OC_ALM_INT	0	RC	V1X Over-Current Alarm Flag Bit (including forward mode and reverse mode) 0 = No V1X over-current alarm 1 = V1X over-current alarm has occurred, or the V1X_OCP_ALM status bit has been reset from '1' to '0' when the alarm is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[4]	V1X_OCP_INT	0	RC	V1X Over-Current Fault Flag Bit (including V1X_OCP1 and V1X_OCP2) 0 = No V1X over-current fault 1 = V1X over-current fault has occurred. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[3]	T_ALM1_INT	0	RC	T_{DIE} Over 100℃ Alarm Flag Bit 0 = No T_{DIE} over 100℃ alarm 1 = T_{DIE} over 100℃ alarm has occurred, or the T_ALM1 status bit is reset from '1' to '0' when the alarm is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[2]	T_ALM2_INT	0	RC	T_{DIE} Over 120℃ Alarm Flag Bit 0 = No T_{DIE} over 120℃ alarm 1 = T_{DIE} over 120℃ alarm has occurred, or the T_ALM2 status bit is reset from '1' to '0' when the alarm is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[1]	T_SHDN_INT	0	RC	T_{DIE} Thermal Shutdown Fault Flag Bit 0 = No T_{DIE} thermal shutdown fault 1 = T_{DIE} thermal shutdown fault has occurred, or the T_SHDN status bit is reset from '1' to '0' when the fault is cleared. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[0]	FSS_FLT_INT	0	RC	Forward Mode Soft-Start Fault Flag Bit 0 = No soft-start fault 1 = Forward mode soft-start fault has occurred. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.

REGISTER MAPS (continued)

REG0x01: INT_SRC_M Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V2X_OVP_M	0	R/W	Mask Bit for the V2X_OVP Fault Interrupt 0 = V2X_OVP fault interrupt can work (default) 1 = Mask V2X_OVP fault interrupt. V2X_OVP_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[6]	V1X_OVP_M	0	R/W	Mask Bit for the V1X_OVP Fault Interrupt 0 = V1X_OVP fault interrupt can work (default) 1 = Mask V1X_OVP fault interrupt. V1X_OVP_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[5]	V1X_OC_ALM_M	0	R/W	Mask Bit for the V1X Over-Current Alarm Interrupt 0 = V1X over-current alarm interrupt can work (default) 1 = Mask V1X over-current alarm interrupt. V1X_OC_ALM_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[4]	V1X_OCP_M	0	R/W	Mask Bit for the V1X Over-Current Fault Interrupt 0 = V1X over-current fault interrupt can work (default) 1 = Mask V1X over-current fault interrupt. V1X_OCP_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.
D[3]	T_ALM1_M	0	R/W	Mask Bit for the T_{DIE} Over 100℃ Alarm Interrupt 0 = T_{DIE} over 100℃ alarm interrupt can work (default) 1 = Mask T_{DIE} over 100℃ alarm interrupt. T_ALM1_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[2]	T_ALM2_M	0	R/W	Mask Bit for the T_{DIE} Over 120℃ Alarm Interrupt 0 = T_{DIE} over 120℃ alarm interrupt can work (default) 1 = Mask T_{DIE} over 120℃ alarm interrupt. T_ALM2_INT bit sets after the alarm occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[1]	T_SHDN_M	0	R/W	Mask Bit for the T_{DIE} Thermal Shutdown Fault Interrupt 0 = T_{DIE} thermal shutdown fault interrupt can work (default) 1 = Mask T_{DIE} thermal shutdown fault interrupt. T_SHDN_INT bit sets after the fault occurs or is cleared, but no interrupt signal is sent on IRQB pin.
D[0]	FSS_FLT_M	0	R/W	Mask Bit for the Forward Mode Soft-start Fault Interrupt 0 = Soft-start fault interrupt can work (default) 1 = Mask forward mode soft-start fault interrupt. FSS_FLT_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.

REGISTER MAPS (continued)

REG0x02: STATUS Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V2X_OVP	0	R	V2X_OVP Fault Status Bit 0 = No V2X_OVP fault 1 = Device is in V2X_OVP fault status.
D[6]	V1X_OVP	0	R	V1X_OVP Fault Status Bit 0 = No V1X_OVP fault 1 = Device is in V1X_OVP fault status.
D[5]	V1X_OC_ALM	0	R	V1X Over-Current Alarm Status Bit 0 = No V1X over-current alarm 1 = Device is in V1X over-current alarm status.
D[4]	SW_DIR	0	R	SCC Switching Direction Status Bits 0 = Forward direction 1 = Reverse direction
D[3]	T_ALM1	0	R	T_{DIE} Over 100℃ Alarm Status Bit 0 = No T_{DIE} over 100℃ alarm 1 = Device is in T_{DIE} over 100℃ alarm status.
D[2]	T_ALM2	0	R	T_{DIE} Over 120℃ Alarm Status Bit 0 = No T_{DIE} over 120℃ alarm 1 = Device is in T_{DIE} over 120℃ alarm status.
D[1]	T_SHDN	0	R	T_{DIE} Thermal Shutdown Fault Status Bit 0 = No T_{DIE} thermal shutdown fault 1 = Device is in T_{DIE} thermal shutdown fault status.
D[0]	V2X_VALID	0	R	V_{V2X} above $V2X_{VALID}$ Threshold Status Bit (update only during reverse direction soft-start) 0 = V_{V2X} < $V2X_{VALID}$ 1 = V_{V2X} > $V2X_{VALID}$

REGISTER MAPS (continued)

REG0x03: INT_SRC2 Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V2X_VALID_INT	0	RC	V2X_VALID Status Change Event Flag Bits 0 = No V2X_VALID status change event 1 = V2X_VALID status change event has occurred. When the V2X_VALID status bit has changed, it generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[6]	CFLY_FLT_INT	0	RC	C_{FLY} Charging Fault Flag Bit 0 = No C_{FLY} charging fault 1 = C_{FLY} charging fault has occurred. It generates an interrupt on IRQB pin. Read this bit to reset it to 0.
D[5]	HVDD_FLT_INT	0	RC	HVDD Charging Fault Flag Bit 0 = No HVDD charging fault 1 = HVDD charging fault has occurred. It generates an interrupt on IRQB pin. Read this bit to reset it to 0.
D[4]	SW_DIR_INT	0	RC	SCC Switching Direction Transition Event Flag Bit 0 = No SCC switching direction transition event 1 = SCC switching direction transition event has occurred. When the SW_DIR status bit is changed, it generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[3]	Reserved	0	R	Reserved
D[2]	RSS_FLT_INT	0	RC	Reverse Mode Soft-Start Fault Flag Bit 0 = No reverse mode soft-start fault 1 = Reverse mode soft-start fault has occurred. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[1]	V2X_OCP_INT	0	RC	V2X Over-Current Fault Flag Bit (including V1X_OCP1 during reverse mode and V2X_OCP2) 0 = No V2X over-current fault 1 = V2X over-current fault has occurred. It generates an interrupt on IRQB pin if unmasked. Read this bit to reset it to 0.
D[0]	PWRON_INT	0	RC	Device Power-on Event Flag Bit (V_{V1X} or V_{V2X} rising above its UVLO threshold and I^2C communication ready) 0 = No device power-on event 1 = Device power-on event has occurred. It generates an interrupt on IRQB pin. Read this bit to reset it to 0.

REGISTER MAPS (continued)

REG0x04: INT_SRC2_M Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V2X_VALID_M	0	R/W	Mask Bit for the V2X_VALID Status Change Event Interrupt 0 = V2X_VALID status change event interrupt can work (default) 1 = Mask V2X_VALID status change event interrupt. V2X_VALID_INT bit sets after the event occurs, but no interrupt signal is sent on IRQB pin.
D[6]	CFLY_FLT_M	0	R/W	Mask Bit for the C_{FLY} Charging Fault Interrupt 0 = C_{FLY} charging fault interrupt can work (default) 1 = Mask C_{FLY} charging fault interrupt. CFLY_FLT_INT bit sets after the fault occurs, but no interrupt signal is sent on IRQB pin.
D[5]	HVDD_FLT_M	0	R/W	Mask Bit for the HVDD Charging Fault Interrupt 0 = HVDD charging fault interrupt can work (default) 1 = Mask HVDD charging fault interrupt. HVDD_FLT_INT bit sets after the fault occurs, but no interrupt signal is sent on IRQB pin.
D[4]	SW_DIR_M	0	R/W	Mask Bit for the SCC Switching Direction Transition Event Interrupt 0 = SCC switching direction transition event interrupt can work (default) 1 = Mask SCC switching direction transition event interrupt. SW_DIR_INT bit sets after the event occurs, but no interrupt signal is sent on IRQB pin.
D[3]	Reserved	0	R	Reserved
D[2]	RSS_FLT_M	0	R/W	Mask Bit for the Reverse Mode Soft-Start Fault Interrupt 0 = Reverse Mode soft-start fault interrupt can work (default) 1 = Mask reverse mode soft-start fault interrupt. RSS_FLT_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.
D[1]	V2X_OCP_M	0	R/W	Mask Bit for the V2X Over-Current Fault Interrupt 0 = V2X over-current fault interrupt can work (default) 1 = Mask V2X over-current fault interrupt. V2X_OCP_INT bit sets after the fault, but no interrupt signal is sent on IRQB pin.
D[0]	Reserved	0	R	Reserved

REG0x05: EN_CFG0 Register Address [reset = 0xB0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	RPUPD_EN	1	R/W	Enable Bit of EN Pin Input Pull-down Resistor Activation 0 = Disabled 1 = Enabled (default)
D[6:4]	OFF_DEG[2:0]	011	R/W	Setting Bits of V_{VIO} Power-off Deglitch Time t_{OFF_DEG} 000 = No deglitch 001 ~ 111: $t_{OFF\_DEG} = 2^{(OFF\_DEG[2:0] - 1)} \times 8ms$ Default: t_{OFF_DEG} = 32ms (011)
D[3:1]	EN_DEG[2:0]	000	R/W	Setting Bits of EN Pin Input High Deglitch Time t_{EN_DEG} 000 = 0.125ms 001 ~ 111: $t_{EN\_DEG} = 2^{(EN\_DEG[2:0] - 1)} \times 1ms$ Default: t_{EN_DEG} = 0.125ms (000)
D[0]	SCC_EN	0	R/W	Switched Capacitor Converter Enable Bit 0 = Disabled (default) 1 = Enabled. If an HVDD or C_{FLY} charging fault occurs, device returns to standby mode and this bit is automatically reset to 0.

REGISTER MAPS (continued)

REG0x06: SCC_CFG1 Register Address [reset = 0x16]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	DCVIO	0	R/W	Enable Bit of VIO_OK to Turn-off Switched Capacitor Converter 0 = Enabled. SCC turns off if V_{VIO} falls below V_{IO_OK} with t_{OFF_DEG}. (default) 1 = Disabled. VIO_OK has no effect on the SCC output state.
D[6]	Reserved	0	R	Reserved
D[5:4]	SFT_DISCHG_T[1:0]	01	R/W	Setting Bits of Soft-Discharge Time t_{SFT_DISCHG} 00 = 50ms 01 = 100ms (default) 10 = 200ms 11 = 300ms
D[3]	OOA_EN	0	R/W	Skip Out-of-Audio (OOA) Mode Disable: 0 = Out-of-audio mode is disabled when converter is in Skip mode. (default) 1 = Out-of-audio mode is enabled when converter is in Skip mode, and the pulse skipping frequency is maintained above 30kHz.
D[2]	V2X_AD_EN	1	R/W	V2X Active Discharge Enable Bit 0 = Disabled 1 = Enabled (default)
D[1]	V1X_AD_EN	1	R/W	V1X Active Discharge Enable Bit 0 = Disabled 1 = Enabled (default)
D[0]	FIX_FREQ	0	R/W	Fixed Frequency Operation Mode Enable Bit 0 = Disabled (default) 1 = Enabled

REG0x07: SCC_CFG2 Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	SCC_DIR[1:0]	00	R/W	SCC Converter Operating Direction Control Bits 00 = Forward direction (default) 01 = Bidirectional 10 or 11 = invalid (not allowed) These bits are forbidden to be changed during switching.
D[5:4]	DTHR[1:0]	00	R/W	Setting Bits of Switching Frequency Dithering Enable and Ratio 00 = Dithering varies switching frequency between ±3% (default) 01 = Dithering varies switching frequency between ±6% 10 = Dithering varies switching frequency between ±12% 11 = Dithering is OFF (Disabled)
D[3]	PH_DEL	0	R/W	Setting Bit of Phase Delay Between Phase-A and Phase-B 0 = 180 degree delay (default) 1 = 90 degree delay
D[2:0]	FREQ[2:0]	000	R/W	SCC Switching Frequency Setting Bits 000 = 250kHz (default) 001 = 500kHz 010 = 750kHz 011 = 1000kHz 100 = 1200kHz 101 ~ 111 = 1500kHz

REGISTER MAPS (continued)

REG0x08: V2X_OVP_SW Register Address [reset = 0x90]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	V2X_OVP_R[4:0]	1 0010	R/W	Setting Bits of V_{V2X} OVP Protection Rising Threshold $V2X_{OVP\_R}$ 0 0000 ~ 0 1100: $V2X_{OVP\_R}$ = 8.3V + V2X_OVP_R[4:0] × 0.05V 0 1101 ~ 1 0010: $V2X_{OVP\_R}$ = 7.7V + V2X_OVP_R[4:0] × 0.10V 1 0011 ~ 1 1000: $V2X_{OVP\_R}$ = 5.0V + V2X_OVP_R[4:0] × 0.25V 1 1001 ~ 1 1111: $V2X_{OVP\_R}$ = 11V Default: $V2X_{OVP\_R}$ = 9.5V (1 0010)
D[2]	Reserved	0	R	Reserved
D[1:0]	V2X_SW_F[1:0]	00	R/W	Setting Bits of V_{V2X} Falling Threshold ($V2X_{SW\_F}$) to Exit Switching 00 = 5.0V (default) 01 = 5.1V 10 = 5.2V 11 = 5.3V

REG0x09: V1X_OVP_SW Register Address [reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	V1X_SW_F	0	R/W	Setting Bit of V_{V1X} Falling Threshold ($V1X_{SW\_F}$) to Exit Switching 0 = 2.8V (default) 1 = 2.9V
D[6:5]	SW_F_DEG[1:0]	00	R/W	Setting Bits of Deglitching Time ($t_{SW\_F\_DEG}$) for V_{V1X} or V_{V2X} to Exit Switching 00 = 0s (default) 01 = 108μs 10 = 500μs 11 = 1ms
D[4:0]	V1X_OVP_R[4:0]	1 0101	R/W	Setting Bits of V_{V1X} OVP Protection Rising Threshold $V1X_{OVP\_R}$ 0 0000 ~ 0 1100: $V1X_{OVP\_R}$ = 4.15V + V1X_OVP_R[4:0] × 0.025V 0 1101 ~ 1 0111: $V1X_{OVP\_R}$ = 3.20V + V1X_OVP_R[4:0] × 0.1V 1 1000 ~ 1 1111: $V1X_{OVP\_R}$ = 5.5V Default: $V1X_{OVP\_R}$ = 5.3V (1 0101)

REG0x0A: OCP1 Register Address [reset = 0x9D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	OCP_ALM_TH	1	R/W	V1X Over-Current Alarm Threshold Setting Bit 0 = 80% of I_{V1X_OCP1} 1 = 90% of I_{V1X_OCP1} (default)
D[6:5]	Reserved	00	R	Reserved
D[4:0]	V1X_OCP1[4:0]	1 1101	R/W	Setting Bits of V1X OCP1 Protection Threshold I_{V1X_OCP1} 0 0000 ~ 1 1011: I_{V1X_OCP1} = 4.2A + V1X_OCP1[4:0] × 0.2A 1 1100 = 10A 1 1101 = 10.4A (default) 1 1110 = 11A 1 1111 = 11.6A

REG0x0B: OCP2 Register Address [reset = 0x7E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	V2X_OCP2[3:0]	0111	R/W	Setting Bits of V2X OCP2 Protection Threshold $V2X_{OCP2}$ 0000 ~ 1110: $V2X_{OCP2}$ = 340mV + V2X_OCP2 [3:0] × 40mV 1111 = OFF Default: $V2X_{OCP2}$ = 620mV (0111)
D[3:0]	V1X_OCP2[3:0]	1110	R/W	Setting Bits of V1X OCP2 Protection Threshold $V1X_{OCP2}$ 0000 ~ 1101: $V1X_{OCP2}$ = 110mV + V1X_OCP2 [3:0] × 10mV 1110 = 310mV (default) 1111 = OFF

REGISTER MAPS (continued)

REG0x0C: FWD_SS_CFG Register Address [reset = 0x31]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:4]	FWD_ISS[1:0]	11	R/W	Setting Bits of Forward Mode Soft-Start Current I_{SS_FWD} (total at V1X) 00 = 145mA 01 = 290mA 10 = 435mA 11 = 580mA (default)
D[3]	Reserved	0	R	Reserved
D[2:0]	FWD_SS_T[2:0]	001	R/W	Setting Bits of Forward Mode Soft-Start Time t_{SS_FWD} t_{SS_FWD} = 62.5ms + FWD_SS_T [2:0] × 62.5ms Default: t_{SS_FWD} = 125ms (001)

REG0x0D: RVS_SS_CFG Register Address [reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	RVS_ISS_HC[2:0]	000	R/W	Setting Bits of Reverse Mode High Soft-Start Current I_{RSS_HC} (total at V2X) 000 ~ 111: I_{RSS_HC} = 260mA + V2X_ISS_HC[2:0] × 20mA Default: I_{RSS_HC} = 260mA (000)
D[4:3]	RVS_ISS_LC[1:0]	01	R/W	Setting Bits of Reverse Mode Low Soft-Start Current I_{RSS_LC} (total at V2X) 00 = 100mA 01 = 150mA (default) 10 = 200mA 11 = 250mA
D[2:1]	RVS_SS_T[1:0]	11	R/W	Setting Bits Reverse Mode Soft-Start Time t_{SS_RVS} t_{SS_RVS} = 10min + RVS_SS_T [1:0] × 10min Default: t_{SS_RVS} = 40min (11)
D[0]	V2X_VALID_TH	1	R/W	Setting Bit of V2X Valid Threshold ($V2X_{VALID}$) during V2X Soft-start 0 = 5.5V 1 = 5.9V (default)

REG0x0E: REQNFLT_CFG Register Address [reset = 0x1A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R	Reserved
D[5:4]	DEEP_SKIP[1:0]	01	R/W	Setting Bits of Deglitch Time for Entry to Deep Skip Mode 00 = 24μs 01 = 48μs (default) 10 = 96μs 11 = 120μs
D[3]	RESTART_EN	1	R/W	Enable Bit of Restart after Faults 0 = Disabled 1 = Enabled (default)
D[2]	Reserved	0	R	Reserved
D[1:0]	WAIT_T[1:0]	10	R/W	Setting Bits of Restart Wait Time after Faults 00 = 0.25sec 01 = 0.38sec 10 = 0.5sec (default) 11 = 0.75sec

REGISTER MAPS (continued)

REG0x0F: SKIP_CFG Register Address [reset = 0x41]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	F2S_DROP[1:0]	01	R/W	Setting Bits of Threshold for Quitting Fixed f_{SW} Mode and Entering Skip Mode (In forward mode, device enters skip mode when V_{V1X} exceeds $V_{V2X}/2$ - ΔV_{F2S_FWD} threshold, where ΔV_{F2S_FWD} = F2S_DROP[1:0] × 10mV + 10mV) 00 = 10mV 01 = 20mV (default) 10 = 30mV 11 = 40mV
D[5:4]	S2F_DROP[1:0]	00	R/W	Setting Bits of Threshold for Quitting Skip Mode and Entering Fixed f_{SW} Mode (In forward mode, device enters fixed f_{SW} mode when V_{V1X} falls below the $V_{V2X}/2$ - ΔV_{S2F_FWD} threshold, where ΔV_{S2F_FWD} = ΔV_{F2S_FWD} + S2F_DROP[1:0] × 5mV + 10mV) 00 = 10mV (default) 01 = 15mV 10 = 20mV 11 = 25mV
D[3:2]	SAG_FWD[1:0]	00	R/W	Setting Bits of Allowed Voltage Sag Threshold before Entering Fixed f_{SW} Mode (ΔV_{SAG_FWD} in forward operation skip mode) 00 = 5mV (default) 01 = 10mV 10 = 15mV 11 = 20mV
D[1:0]	SKIP_HYST[1:0]	01	R/W	Setting Bits of Hysteresis ΔV_{SKP_FWD} during Skip Mode (ΔV_{SKP_FWD} in forward operation skip mode) 00 = 2mV 01 = 4mV (default) 10 = 6mV 11 = 8mV

REG0x10: CHIP_REV Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	OTP_VER[3:0]	0000	R	OTP Receipt Version
D[3:0]	CHIP_VER[3:0]	0000	R	IC Version

REG0x11: DEVICE_ID Register Address [reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE_ID[7:0]	0000 0011	R/W	Device ID 0000 0011 = SGM41603

TYPICAL APPLICATION CIRCUITS

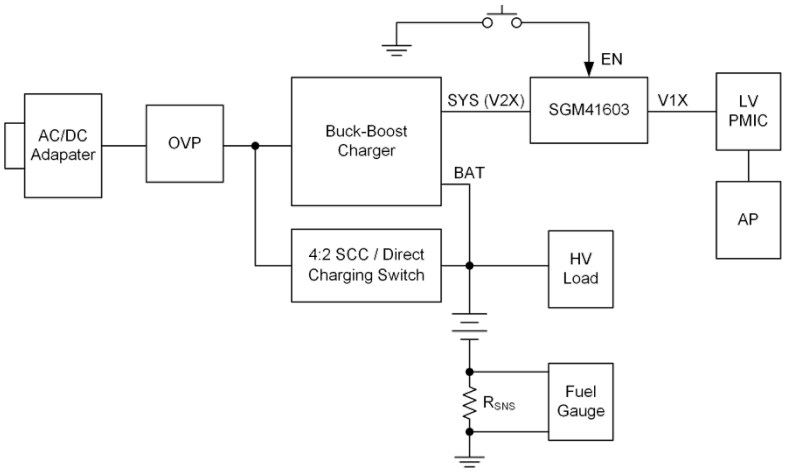


Figure 3. Typical Application Circuit 1

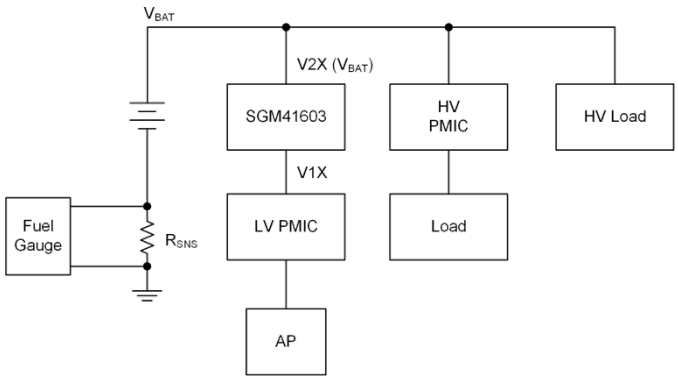


Figure 4. Typical Application Circuit 2

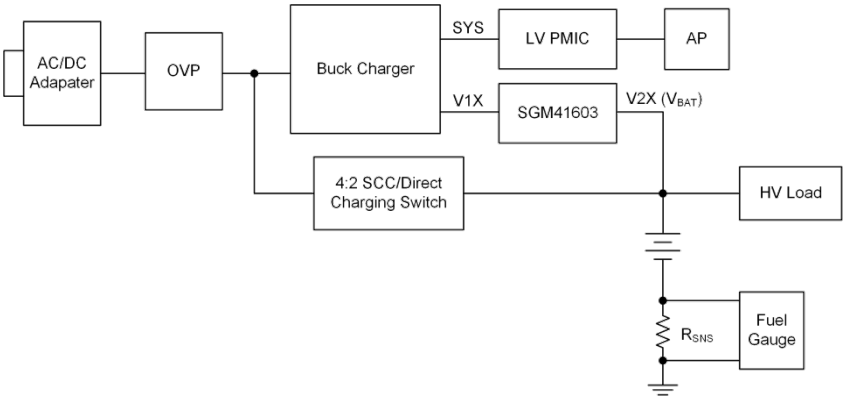


Figure 5. Typical Application Circuit 3

DETAILED DESCRIPTION

New electronic devices require more electric current and this demand is constantly increasing with every new generation of the equipment. Higher current requires larger batteries to keep the portable device running. Larger batteries in turn need higher charging currents to keep the charge time reasonably short. To reduce the charge current losses, it is preferred to have battery cells in series rather than in parallel, but the battery pack voltage will be higher. However, even for some low-voltage applications, it is beneficial to configure the batteries as 2-series (2S) cell and use an efficient 2-to-1 bidirectional voltage converter to interface the battery for powering the LV system. It is much faster to charge a 2S battery compared to a 2-parallel battery (2P) with the same current. To power the system the converter acts as a current-doubler and delivers double current to the system as if the source is 2P, but during charge the charging current is almost half. The SGM41603 is an ultra-efficient switched-capacitor (inductor-less) converter with small solution size that perfectly fits such job.

The Switched-Capacitor Converter (SCC)

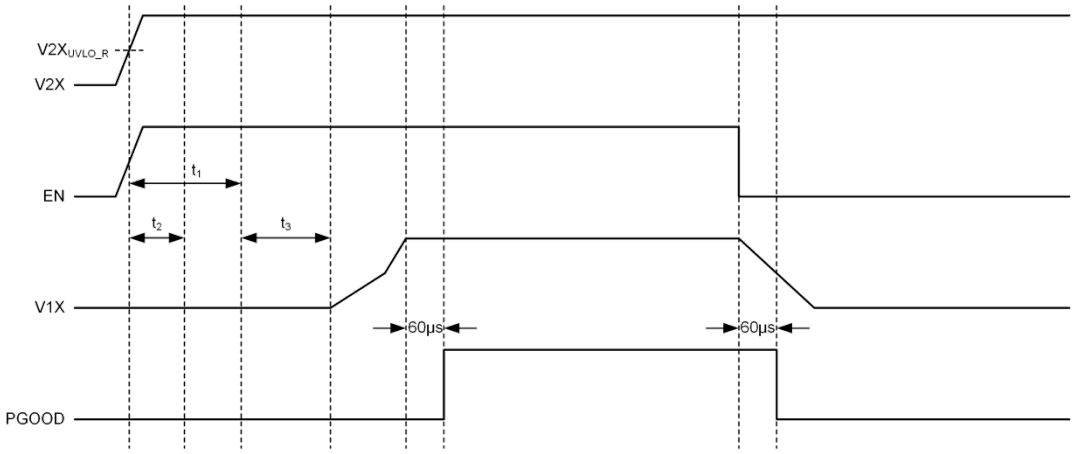
A switched-capacitor converter uses capacitors as energy storage and transfer element for DC/DC conversion. Compared to converters that use inductors (like Buck converter), the SCC provides higher efficiency, smaller solution size and lower cost. The SGM41603 is a dual phase bidirectional 2:1 SCC with 10A output current capability in forward mode. In forward direction, half of the input voltage ($1/2 \times V_{V2X}$) is generated on the output (V1X). In the reverse direction, the doubled input voltage ($2 \times V_{V1X}$) is generated on the output (V2X) with 5A capability. The converter operates with a fixed 50% duty cycle. When SCC_DIR[1:0] = 00 (default), the SGM41603 is configured as a voltage divider and can only work in forward direction. When SCC_DIR[1:0] = 01, the SGM41603 works in bidirectional mode and the change between forward and reverse directions is automatic. To reduce the output voltage and current ripples, the converter is composed of two phases (90° or 180° phase delay selectable).

Enable Input (EN)

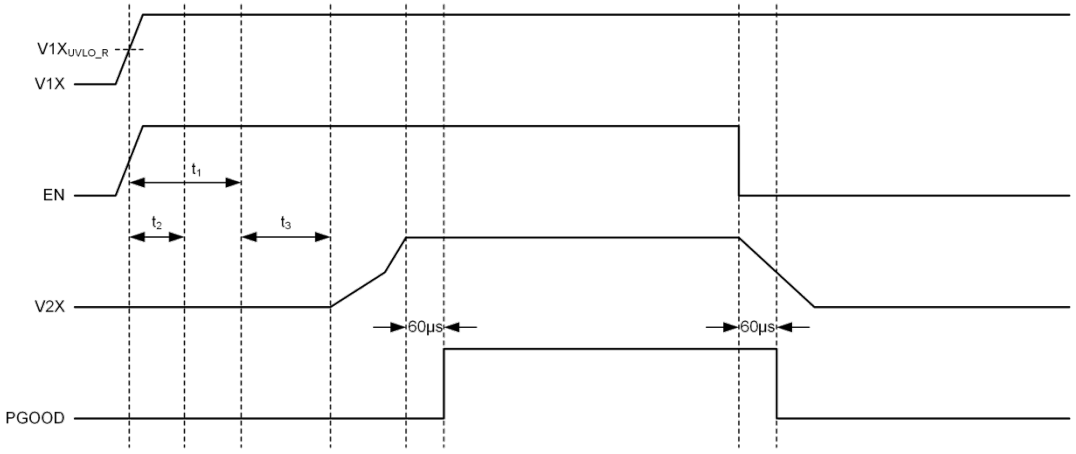
The EN pin is an active high enable input for the SGM41603. When EN is pulled high and after the deglitch time (t_{EN_DEG}), first the soft discharge is activated for t_{SFT_DISCHG} and then the soft-start is initiated. The SCC full activation occurs only after a successful soft-start. If EN is pulled low while VIO is invalid, the SCC turns off right away. The t_{EN_DEG} deglitch time and t_{SFT_DISCHG} soft-discharge-time are I²C programmable. See Figure 6 for enable and soft-start timings in bidirectional mode. In this figure:

- t_1 is the EN deglitch time (EN_DEG[2:0] in REG0x05) and can be set from 0.125ms to 64ms (default 0.125ms).
- t_2 is the standby time which is 125μs (minimum time in STANDBY state).
- t_3 is the soft-discharge time (SFT_DISCHG_T[1:0] in REG0x06) that can be set from 50ms to 300ms (default 100ms).

DETAILED DESCRIPTION (continued)



a. Forward Direction



b. Reverse Direction

Figure 6. EN, Soft-Start and Power Good Timings for Bidirectional Mode (t_1: EN Deglitch Time; t_2: Standby Time; t_3: Soft Discharge Time)

DETAILED DESCRIPTION (continued)

Enable/Disable by EN and V_{IO}

After being enabled, if EN goes low but a valid VIO voltage is present, the device remains enabled and holds the output. In this case EN can be used as a push-button to control operation. If EN goes low while VIO is invalid, the device will disable. When the output is on hold, the converter can be turned off by turning the VIO regulator off (if the DCVIO bit in REG0x06 is set to 0). When V_{VIO} goes low, the converter turns off after t_{OFF_DEG} deglitch time. Because V_{VIO} is usually the IO voltage rail of the system, this feature allows enabling the device conveniently by a push-button (and disable by system shutdown). See Figure 7 for the enable timing when the DCVIO bit is set in forward direction. In this figure, t_1 shows the t_{EN_DEG} deglitch time (EN_DEG[2:0] in REG0x05) and is adjustable from 0.125ms (default) to 64ms by I²C. t_2 is the VIO power-off deglitch time, (OFF_DEG[2:0] in REG0x05) and is programmable from 0ms to 512ms (default 32ms).

Enable/Disable by I²C

In applications that VIO can be turned on before enabling the IC, the host can enable the device output by setting SCC_EN bit to 1 in REG0x05 even if EN is low. The host can reset SCC_EN to 0, to disable the output (See Figure 8).

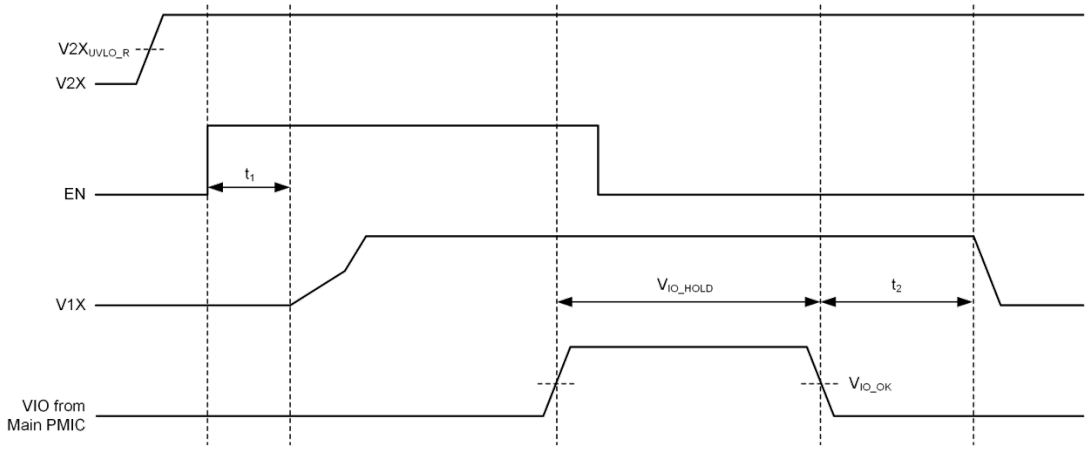


Figure 7. Enable Timing Waveform with VIO Hold when Enabled DCVIO (Forward Direction)

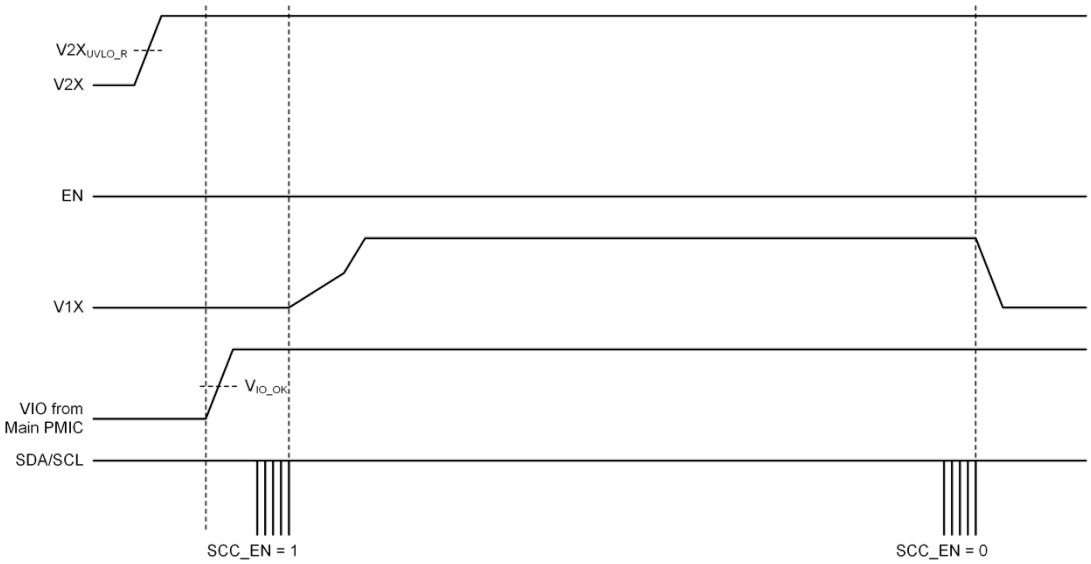


Figure 8. Enable Timing Waveform with I²C Command (Forward Direction)

DETAILED DESCRIPTION (continued)

Charge System with SGM41603

A charge system for 2-cell batteries can be implemented with the SGM41603 along with a Buck converter and a host. All protection functions must be set before enabling the SGM41603 by the host. The host must also watch the IRQB interrupts during charge and communicate with the Buck charger to control the charge current.

The block diagram of a charge system is shown in Figure 9. In this system, the Buck switching charger (SGM41516D) powers the SGM41603 (SCC) and the load system. The SCC interface acts like an interface between the 2-cell battery and the system, and provides high charging current for the batteries. The communication between devices is through I^2C.

Before soft starting SGM41603 in reverse direction (charging the battery), the charging current limit must be set in the Buck charger. Charge can be terminated by the Buck charger or by triggering a V2X over-voltage protection.

Startup and Soft-Start in Forward Direction

During the startup of SGM41603 in forward direction, the C_{FLY} capacitors appear in parallel with the output (V1X) capacitor. In normal operation, the capacitors are charged to a voltage near the final value (V_{V2X}/2 - 20mV) with a soft-start current that is adjustable from 145mA to 580mA via I^2C. If within t_{SS_FWD} (soft-start time) and for 10 successive tries, the output does not reach near V_{V2X}/2 voltage, an FSS_FLT_INT (Forward Mode Soft-Start Fault) interrupt will be generated and the device returns back to the STANDBY state. But if the soft-start is successful, normal operation will begin. The t_{SS_FWD} soft-start time can be set by I^2C.

Startup and Soft-Start in Reverse Direction

During reverse direction startup, the Buck charger sets the V1X current limit. When the PoorSRC qualification timer expires (t_{SFT_DISCHG}) for V1X/V2X, and the following two conditions are met for V1X, then V2X charging will start with the I_{RSS_LC} current.

1. V_{V1X} > ($V1X_{SW\_F}$ + 0.2V) and
2. V_{V1X} > (V_{V2X}/2 + 30mV)

The soft-start current will increase to I_{RSS_HC} when V2X voltage exceeds the $V2X_{VALID}$ threshold. Finally, if V2X reaches to ($2V_{V1X}$ - $V2X_{OCP2}$ + 20mV) threshold, the converter starts full switching as a 1:2 SCC. The t_{SFT_DISCHG}, I_{RSS_LC}, $V2X_{VALID}$ and I_{RSS_HC} parameters are I^2C adjustable.

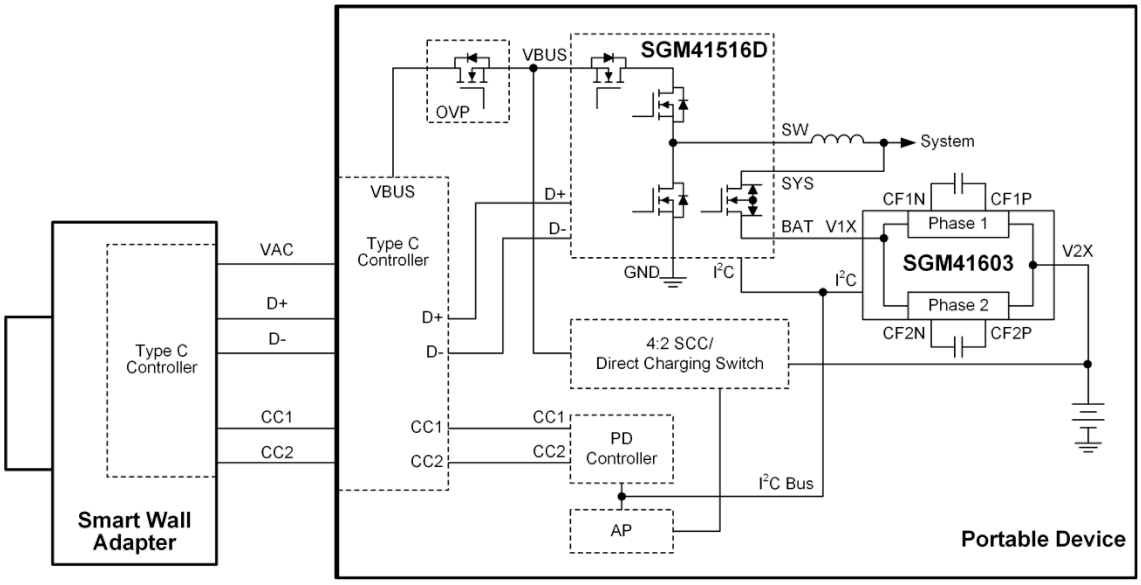


Figure 9. A Simplified Charge System with SGM41603

DETAILED DESCRIPTION (continued)

PGOOD

PGOOD is a push-pull power good indicator output with 200μA capability. After soft-start, the PGOOD goes to high state (1.8V) and remains high while the converter is operating normally. An external RC filter (1kΩ, 10nF) should be connected to PGOOD if this pin is used.

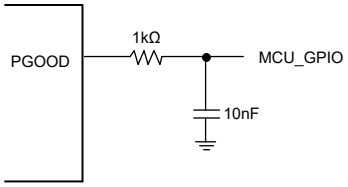


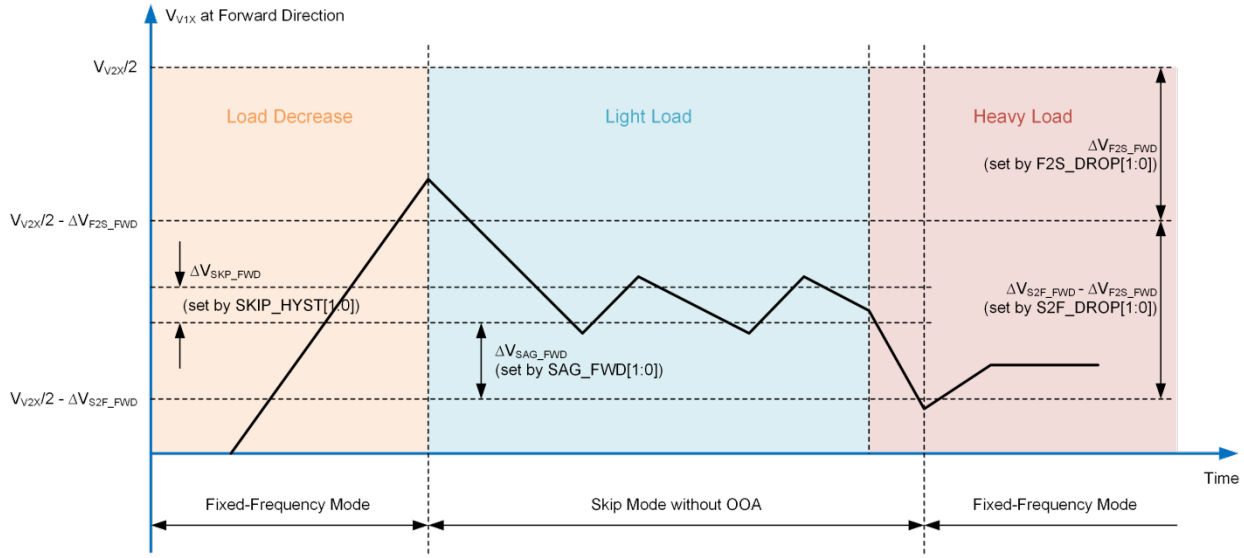
Figure 10. PGOOD Filter Example Circuit

Skip Mode and Fixed-Frequency Mode

In normal operation, the converter operates with 50% duty cycle and the switching frequency is set by the SCC_CFG2 register (REG0x07).

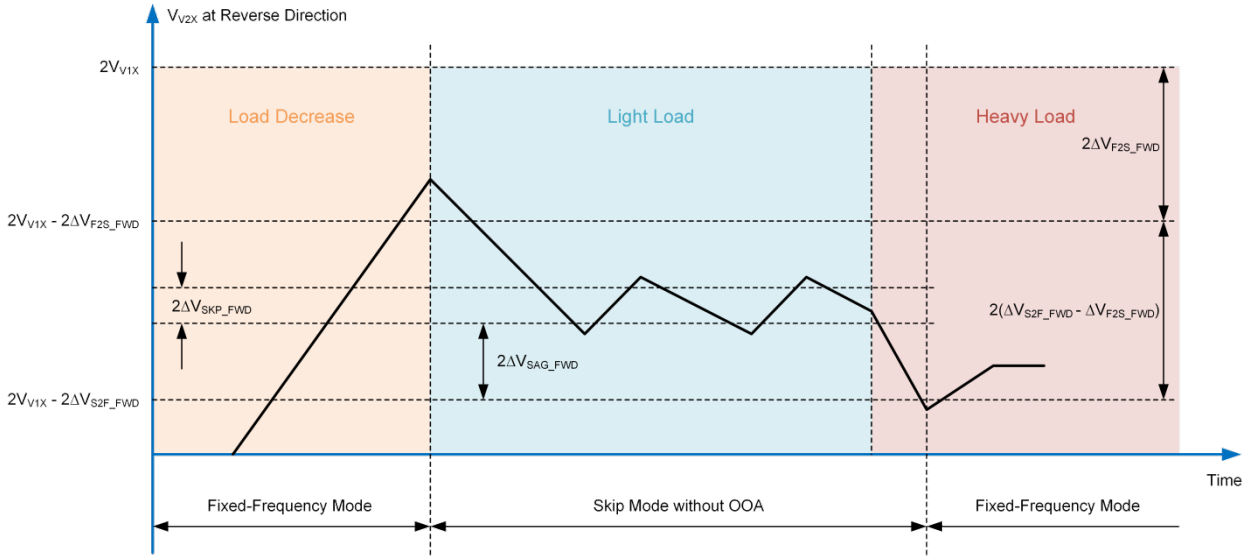
In the fixed-frequency mode, the converter generates unregulated outputs (V_{V2X}/2 at the V1X pin in forward mode or 2×V_{V1X} at the V2X pin in reverse mode).

By setting the FIX_FREQ bit in REG0x06 to 0, the device is allowed for automatic entry to skip mode at light load. To keep the device in fixed frequency mode and avoid skip mode, the FIX_FREQ bit must be set to 1. Figure 11 illustrates the skip mode operation. For example, when the V_{V1X} output exceeds the (V_{V2X}/2 - ΔV_{F2S_FWD}) threshold in forward mode, the device enters skip mode. It will return to fixed frequency mode when V_{V1X} falls below the (V_{V2X}/2 - ΔV_{S2F_FWD}) threshold. Similar behavior occurs in reverse mode. The skip mode saves power at light loads and keeps the high efficiency over the entire load range, and simultaneously maintains the V_{V1X} output near V_{V2X}/2.



a. Forward Direction

DETAILED DESCRIPTION (continued)



b. Reverse Direction

Figure 11. SGM41603 Skip Mode Operation

Out-of-Audio (OOA) Mode

When the SCC operates in skip mode, the skip frequency can fall in the audio range (20Hz to 20kHz). This can generate audible noise in multilayer chip capacitor. The SGM41603 offers an Out-of-Audio (OOA) Mode feature that if enabled, keeps the minimum skip frequency above 30kHz.

Operating details for the OOA mode during skip interval is illustrated in Figure 12. During skip mode, the maximum skip interval does not exceed t_{OOA} when OOA is enabled.

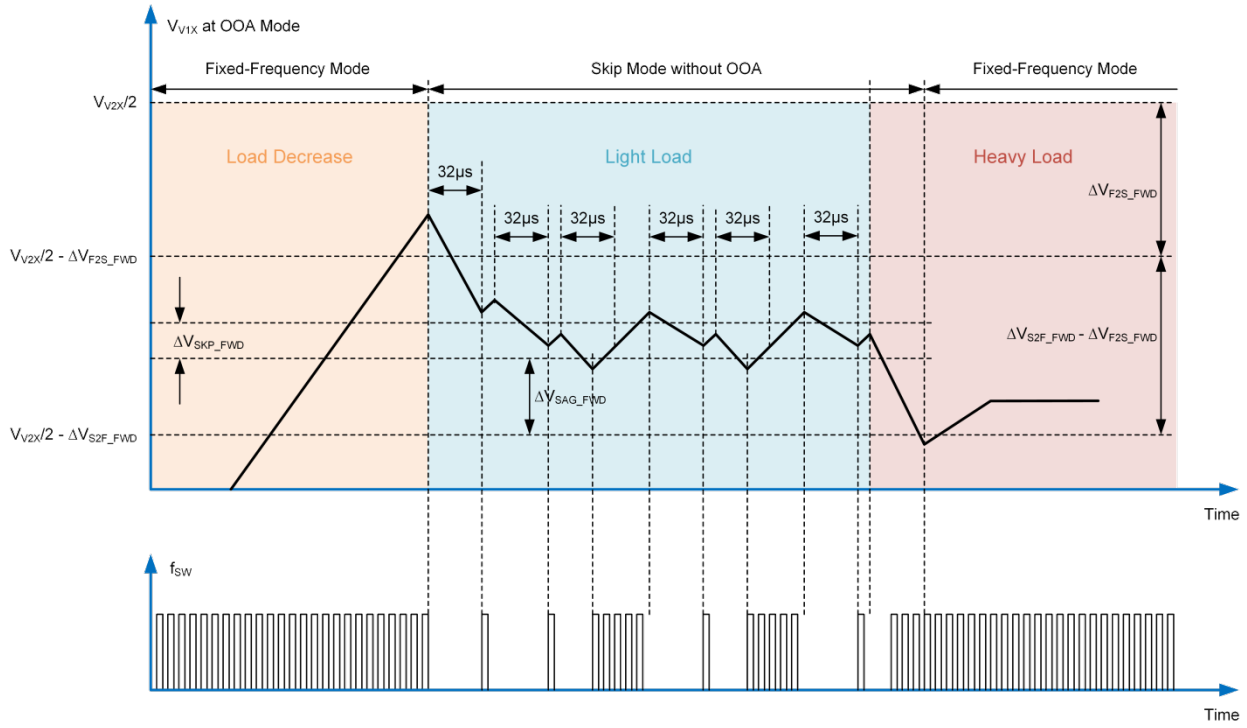


Figure 12. Skip Mode with Out-of-Audio (OOA) Operation at 500kHz

DETAILED DESCRIPTION (continued)

Under-Voltage Lockout (UVLO)

The SGM41603 will shut down if a UVLO event occurs in which V_{V2X} falls below $V2X_{UVLO\_F}$ and V_{V1X} falls below $V1X_{UVLO\_F}$. It will not restart until one of the port voltages exceeds its UVLO threshold (either V_{V2X} exceeds the $V2X_{UVLO\_R}$ threshold or V_{V1X} exceeds the $V1X_{UVLO\_R}$ threshold).

Frequency Dithering

The fixed switching frequency of the switching converter generates high peaks in EMI emission spectrum. By enabling the frequency dithering, this frequency is cyclically varied in a narrow band around the set frequency such that the emitted energy is distributed over a wider frequency range and the emission peaks are reduced. This feature is configurable via I²C and can be disabled or set to 3%, 6% or 12% of the switching frequency in the whole synthesized switching frequency range (0.25MHz to 1.5MHz).

Over-Current Protections

The SGM41603 has two layers of over-current protection in forward direction. The V1X output current is monitored for I_{V1X_OCP1} over-current protection. For a faster short-circuit protection, the V1X and V2X are also sensed for drops ($V1X_{OCP2}$). The output is disabled if the V1X output current exceeds I_{V1X_OCP1} or if V_{V1X} falls below (V_{V2X}/2 - $V1X_{OCP2}$). I_{V1X_OCP1} can be set from 4.2A to 9.6A in 0.2A steps or to 10.0A, 10.4A, 11.0A, and 11.6A values through I²C. $V1X_{OCP2}$ can be turned off or adjusted from 110mV to 240mV in 10mV steps and to 310mV.

In reverse direction, not only the V1X input current is monitored for detecting I_{V1X_OCP1} over-current, but also the V1X and the V2X are sensed for drops for faster short-circuit protection ($V2X_{OCP2}$). The output will disable if V_{V2X} falls below ($2V_{V1X}$ - $V2X_{OCP2}$). The $V2X_{OCP2}$ can be set from 340mV to 900mV in 40mV steps or turned off.

High Current Alarm (OCP_{ALM})

When V1X current (in or out) exceeds the OCP_{ALM} threshold (80% or 90% of the I_{V1X_OCP}), the V1X_OC_ALM_INT interrupt bit and V1X_OC_ALM status bits are set. The OCP_{ALM} can be set to 80% or 90% (default). The V1X_OC_ALM bit resets when the V1X current falls below 75% or 85% (default) of the I_{V1X_OCP}.

Over-Temperature Alarms and Fault

The die temperature (T_J) is monitored for thermal protection. If T_J exceeds +160℃ (T_{SHDN}), the device enters in the thermal shutdown state and the T_SHDN_INT interrupt bit is set. If T_J falls for around 20℃, the thermal shutdown will terminate and SCC can be enabled again.

Two additional alarming comparators that trip at +100℃ and +120 ℃ can set the T_ALM1 and T_ALM2 interrupts respectively.

Over-Voltage Lockout Protections for V2X and V1X

The SCC output will disable if an over-voltage occurs on V1X or V2X. For V_{V2X}, the $V2X_{OVP\_R}$ over-voltage threshold is adjustable from 8.3V to 11V in REG0x08[7:3] with 9.5V default value. For V_{V1X} the $V1X_{OVP\_R}$ is adjustable from 4.15V to 5.5V in REG0x09[4:0] with 5.3V default value.

Auto Restart Features after Faults

Two after-fault auto restart features are included in this device. Since the SGM41603 is usually the system power supply, in most applications it cannot be re-enabled externally after a fault (the auto restart feature is essential). After any fault, the switcher is off, and if all following conditions are valid:

(1) the fault condition is removed
(2) EN is higher than V_{IH} or SCC_EN = 1
(3) RESTART_EN bit is 1
(4) At least one of the V1X or V2X voltages is above its switching start threshold (($V1X_{SW\_F}$ + 0.2V) or ($V2X_{SW\_F}$ + 0.2V) respectively)

then after a wait time (adjustable by WAIT_T[1:0] bits) the device conducts an active discharge if enabled and initiates a soft-start.

Note that if RESTART_EN is 0, the EN pin must be toggled to enable the output after a fault power-down.

DETAILED DESCRIPTION (continued)

I²C Interface

The SGM41603 acts as an I²C Slave Transmitter/Receiver at the following slave addresses:

Slave Address (7 bit): 1101 000
Slave Address (Write): 1101 0000 (0xD0)
Slave Address (Read): 1101 0001 (0xD1)

I²C System Configuration

A “Transmitter” is a device on the I²C bus that generates a ″message″ on the bus. A “Receiver” is a device that receives that message from the bus. The “Master” is the device that controls the messaging, and a “Slave” is any device that is controlled by the ″Master″.

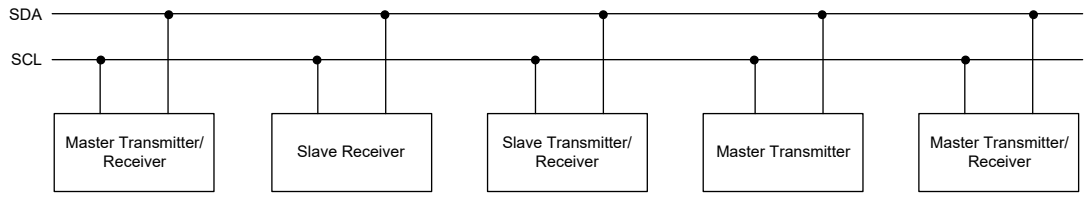


Figure 13. Configurations of the I²C Devices

Start and Stop Conditions

When the bus is free (idle) both SDA and SCL remain high. A START (S) condition is sent by master at the beginning of a transaction with a high-to-low transition on the SDA line while the SCL is high and all slaves will detect that. Similarly, one (or more) STOP (P) condition is sent by master with a low-to-high transition of the SDA line while the SCL is high to terminate the transaction and release the bus (see Figure 14). It is recommended to initiate the bus by sending a STOP condition after power-up. The master may not release the bus after a complete transaction with the slave and send a repeated START (Sr) to initiate a new data exchange with the slave.

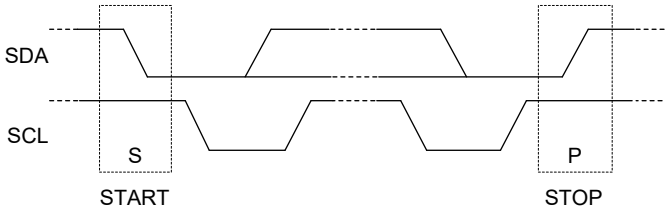


Figure 14. I²C Bus in START and STOP Conditions

Bit Transfer

With each clock pulse one data bit can be transferred as shown in Figure 15. The data on SDA line must remain stable (setup and hold times must be met) during the high time of the clock (SDA transitions during CLK high time are interpreted as a control signal).

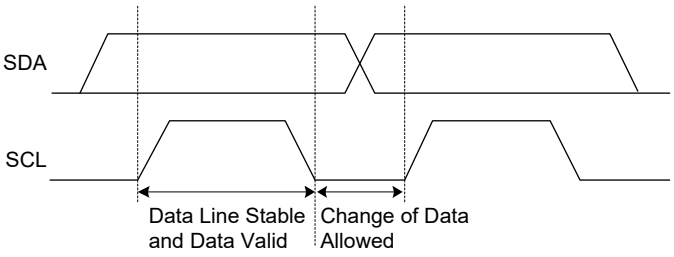


Figure 15. I²C Bus Bit Transfer

DETAILED DESCRIPTION (continued)

I²C Data Format and Acknowledge

The data is transmitted one byte at a time. After detecting the START condition, the transmitter will send one byte (8-bit) of data, bit by bit starting from the Most Significant Bit (MSB). With each SCL pulse a new bit is placed on the SDA line. After sending the 8th bit, the transmitter releases the SDA line during the 9th SCL pulse in order to receive an acknowledge bit from the receiver. Therefore, a total of 9 bits is exchanged for each byte. The number of bytes in one transaction is not limited. After sending the ACK bit, if the receiver is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the sender in wait state (clock stretching). When it is ready for another byte of data, it releases the clock line and the data transfer can continue with clocks generated by the master.

The 9th bit is the receiver response (slave or master) to show that the byte is received. Sending a low during the 9th clock cycle is interpreted as ACK. If the receiver responds a high or does not respond at all, the sender will receive a high for the 9th bit that is considered as Not ACK (= NCK). An NCK means that the receiver is not expecting more data. Therefore, the response of the receiver to the last byte in a transaction is an NCK. It can also show that there is a problem in the communication link (rare). After the 9th bit, a STOP or a Repeated START (Sr) should be sent by master. A master receiver must signal an end of data (NCK) to the transmitter on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

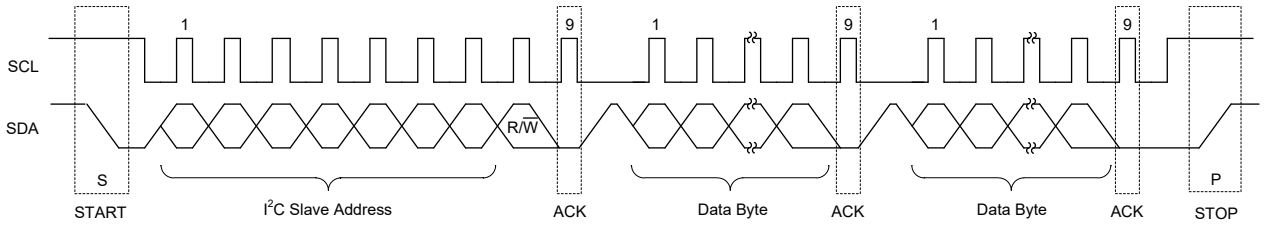


Figure 16. I²C Data Transfer and Acknowledge Bit

DETAILED DESCRIPTION (continued)

Master Transmits Protocol (Write Mode)

Figure 17 shows how the master writes to (R/$\overline{W}$ = 0) a slave register at a specific register address, or group of register in the successive addresses.

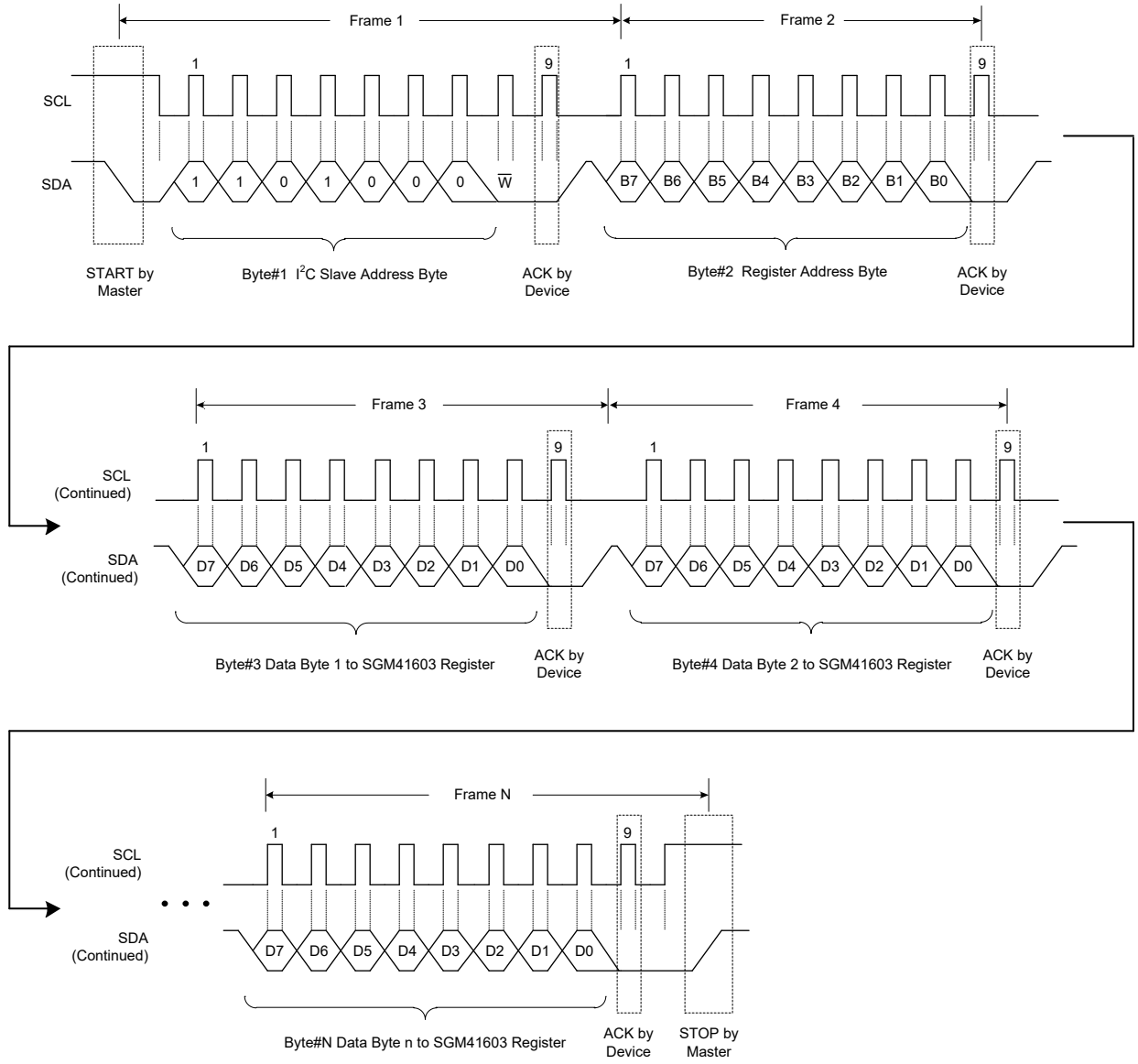


Figure 17. I²C Write Protocol Master Transmits

DETAILED DESCRIPTION (continued)

Master Reads from Slave after Setting Register Address (Write Register Address and Read Data)

Figure 18 shows how master should read a specific register (it must first write the required register address).

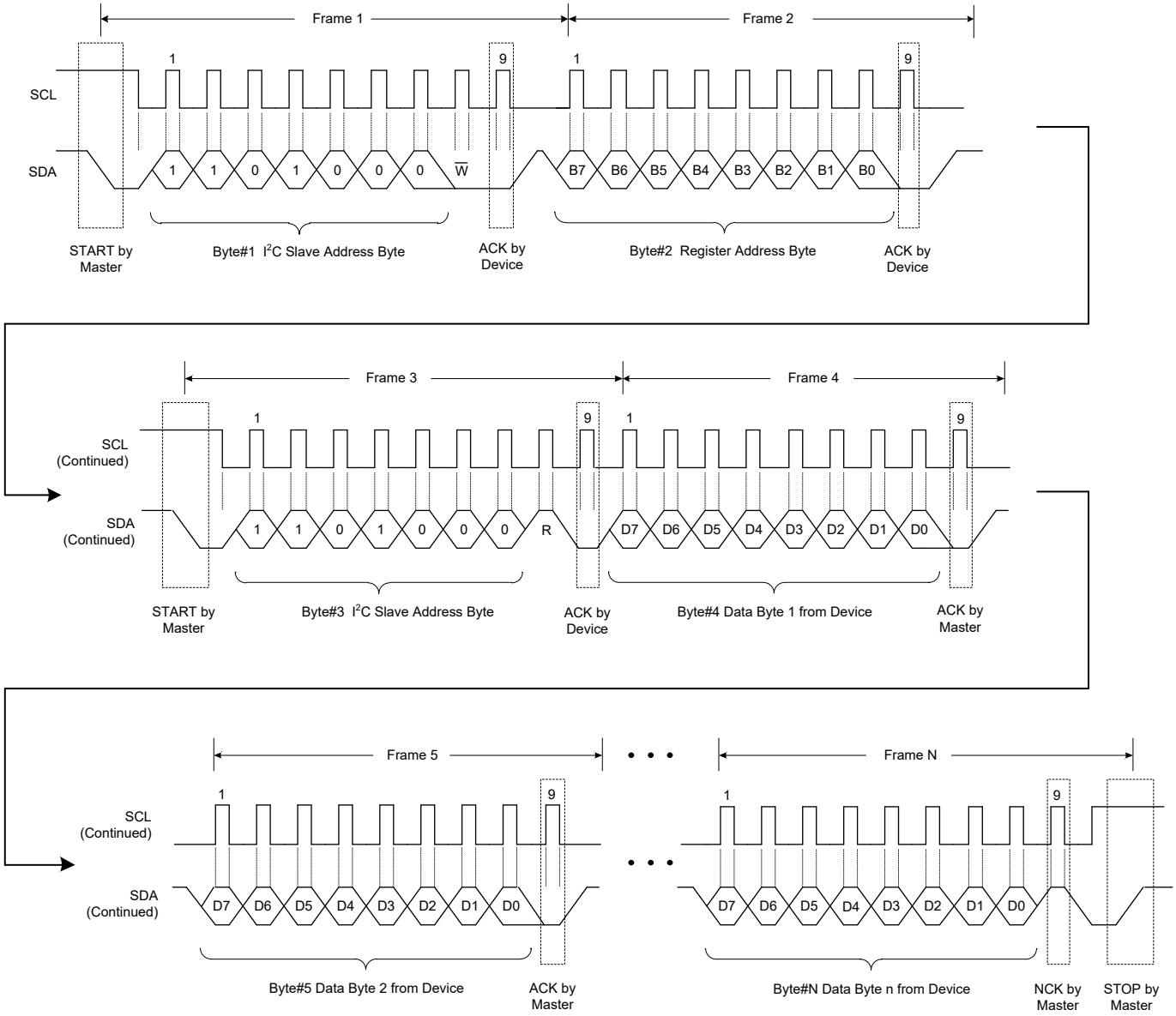


Figure 18. I²C Read Protocol (Master Reads after Setting Register Address)

DETAILED DESCRIPTION (continued)

Block Read: Master Reads Register Data without Setting Register Address (Read Mode)

The format given in Figure 19 can be used to read registers continuously starting from the first register address.

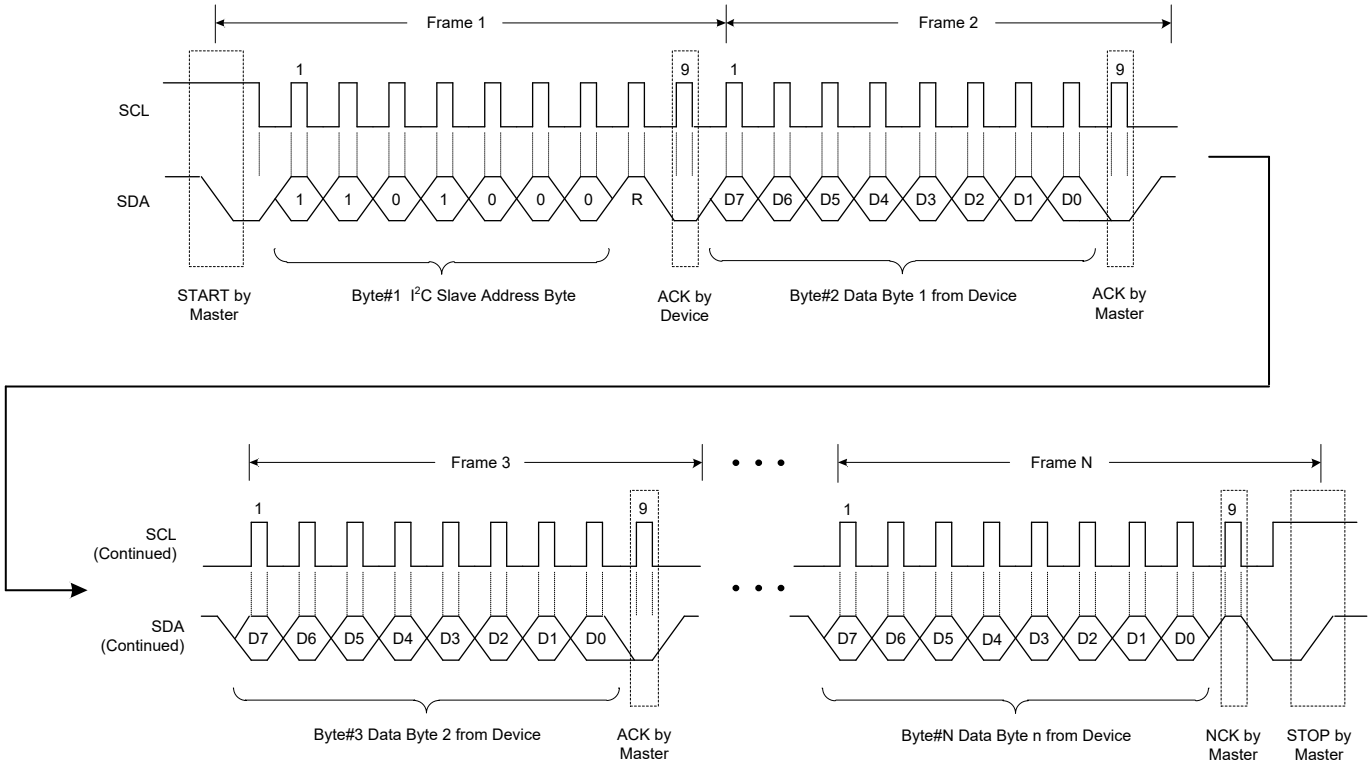


Figure 19. I²C Master Block Read Starting from the First Register

APPLICATION INFORMATION

Input Capacitor Selection (C_{V2X} or C_{V1X})

Two factors should be considered when choosing the input capacitor. One is that it must be chosen to support the maximum expected input surge voltage with adequate design margin. The other is that it is required to reduce peak currents drawn from the input source and reduce input noise.

The selection of C_{V2X} and C_{V1X} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the operation is stable. For most applications, ceramic capacitor which has total capacitance greater than 22μF with X5R or better grade can obtain stable performance.

A good design should consider the DC bias effect on a ceramic capacitor: as the applied voltage approaches the rated value, the capacitance value decreases. The X5R and X7R type capacitors should be the primary choices due to their stability versus both DC bias and temperature. For all ceramic capacitors, the DC bias effect is even more pronounced on smaller case sizes, so a good design will use the largest affordable case size. Also, it is advisable to select input capacitors with plenty of design margin in the voltage rating to accommodate the worst-case transient input voltage.

Flying Capacitor Selection (C_{FLY})

To select the capacitance of the flying capacitors, current rating and ESR are critical parameters. Moreover, these capacitors are biased to V1X voltage and their voltage rating should be high enough to avoid capacitance drop due to DC bias. The C_{FLY} is selected in a trade-off between efficiency and power density. Smaller C_{FLY} capacitance increases the output voltage/current ripples and reduces efficiency. A large C_{FLY} reduces the output ripples and improves efficiency. The C_{FLY} per phase can be calculated based on the equation below:

$$C_{FLY} = \frac{I_{V1X}}{4f_{SW}V_{CFLY\_RPP}}$$

To start, set the voltage ripple to 2% of the output voltage:

$$C_{FLY} = \frac{I_{V1X}}{8\%f_{SW}V_{V1X}} \quad (1)$$

where

I_{V1X} is the V1X input/output current;

f_{SW} is the switching frequency;

V_{CFLY_RPP} is the peak-to-peak voltage ripple over C_{FLY}.

The switching frequency can be set using the FREQ[2:0] bits in REG0x07 (default value is 250kHz). A lower switching frequency improves efficiency at light load but will also increase voltage/current ripples.

Output Capacitor Design (C_{V2X} or C_{V1X})

The C_{V2X} or C_{V1X} output capacitor selection is similar to the C_{FLY} capacitor selection. More output capacitors result in smaller output voltage ripple. Because of the lower RMS current, the output capacitor value can be much less than the C_{FLY} capacitor, and can be calculated based on the equation below:

$$C_{V1X} = \frac{I_{V1X}t_{DEAD}}{0.5V_{V1X\_RPP}} \quad (2)$$

$$C_{V2X} = \frac{I_{V2X}t_{DEAD}}{0.5V_{V2X\_RPP}} \quad (3)$$

where

t_{DEAD} is the deadtime between 2-phase.

V_{V1X_RPP} is the peak-to-peak output voltage ripple which can be set as 2% of V_{V1X}.

V_{V2X_RPP} is the peak-to-peak output voltage ripple which can be set as 2% of V_{V2X}.

Considered the bias voltage derating for the capacitors, as the C_{OUT} may be biased to the battery voltage, and this will affect their effective capacitance, a typical 22μF ceramic capacitor with X5R or better grade can be placed as close to the V2X or V1X pins as possible to obtain stable performance.

External Bootstrap Capacitors Selection (C_{BSTxP} and C_{BSTxN})

The bootstrap capacitors, C_{BSTxP} and C_{BSTxN}, provide the gate driver voltage for internal charging phase switching FETs Q_{CHx} and Q_{CLx}. A 47nF low ESR ceramic capacitor is recommended to be connected between the BSTxP pin and the CFxP pin, and between the BSTxN pin and the CFxN pin.

APPLICATION INFORMATION (continued)

PCB Layout Guidelines

For a stable and high-performance design the following guidelines are considered in the design of the PCB layout:

1. Avoid connectors as much as possible to minimize losses and hot spots.
2. Use short and wide traces for high current paths like V1X and V2X.
3. V1X and V2X pins must be bypassed to GND by ceramic capacitors placed as close as possible to these pins.
4. CFLY capacitors must be placed as close as possible to the device pins with minimal copper connection areas to reduce switching noise and EMI.
5. Use symmetrical power traces across the two phases as much as possible. For example, place the CF1P and the CF1N symmetrically, and route V1X trace symmetrically on both phases.
6. Vias are inevitable for connection of the inner pins (under the device), especially for BSTxP/N and HVDD. Use wide and short traces in the connecting layer to connect these pins and minimize the path length to the corresponding capacitors.
7. Use solid (filled) thermal vias for better heat dissipation.
8. Refer or decouple quiet signals to the AGND pin and power signals to the PGND pins (nearest pins).
9. Avoid interrupting or breaking the power planes by signal traces as much as possible.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

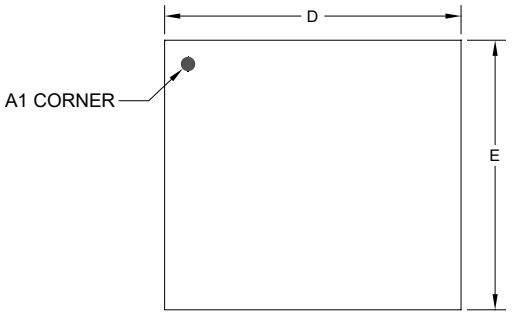
MARCH 2025 – REV.A.1 to REV.A.2	Page
Updated Features section	1
Added package thermal resistance	2
Updated Electrical Characteristics section	5, 7
Deleted t_{DT_C2D} and t_{DT_D2C} parameters	6

JUNE 2023 – REV.A to REV.A.1	Page
Updated Functional Block Diagram section	11

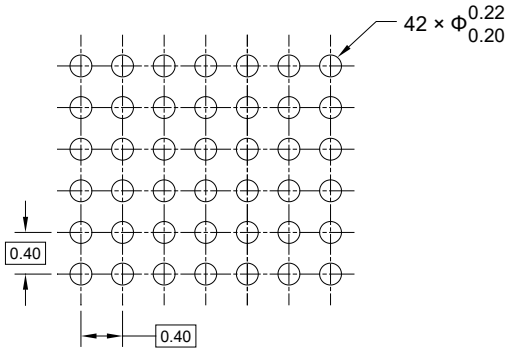
Changes from Original (MARCH 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

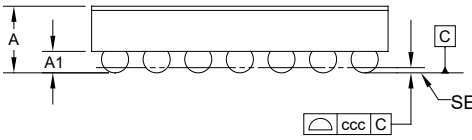
WLCSP-2.85×2.59-42B



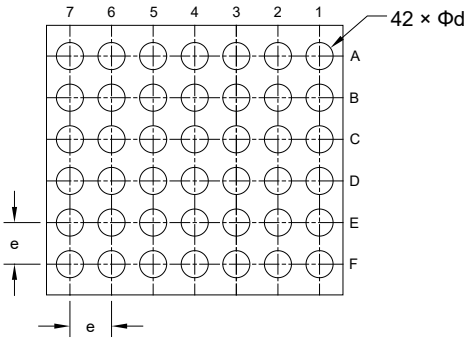
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



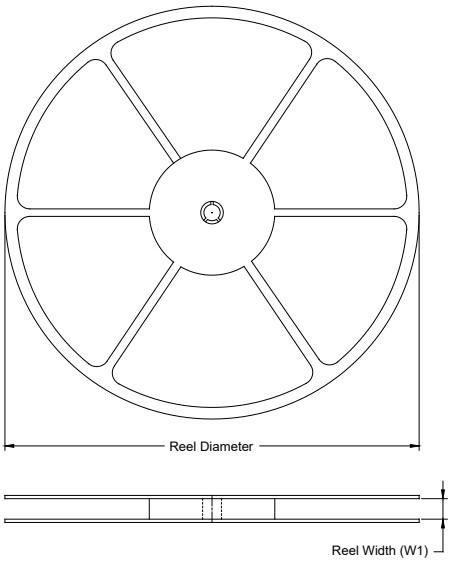
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.602	0.640	0.678
A1	0.186	0.206	0.226
D	2.823	2.853	2.883
E	2.563	2.593	2.623
d	0.240	0.260	0.280
e	0.400 BSC		
ccc	-	0.050	-

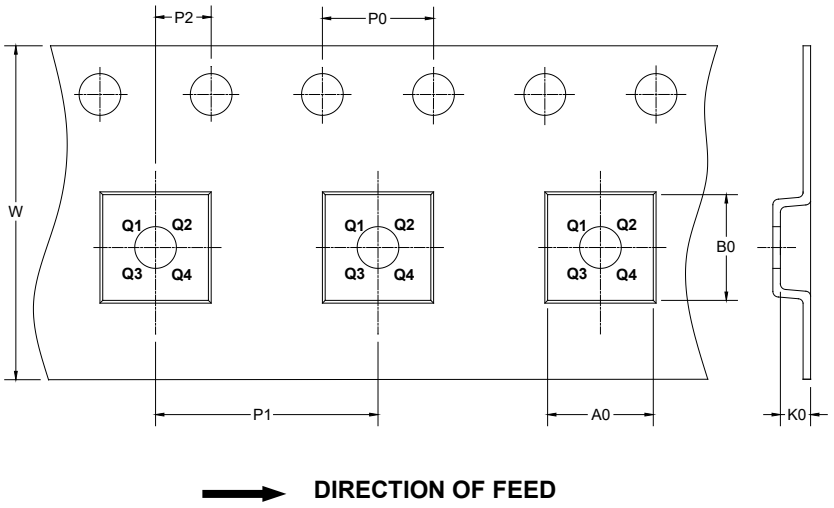
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



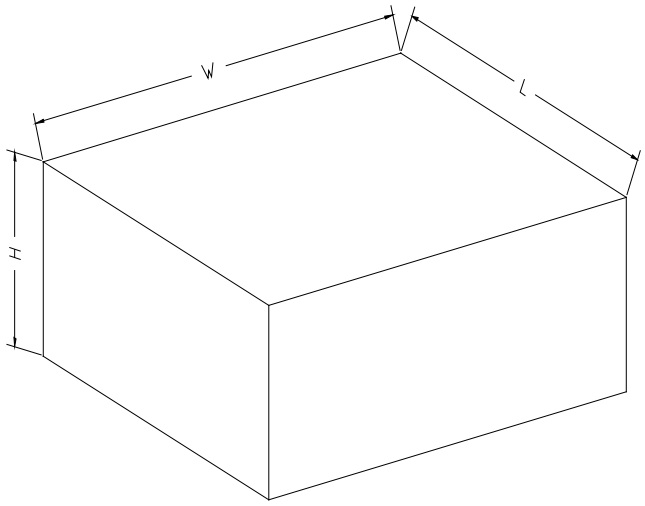
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.85×2.59-42B	13″	12.4	2.70	3.00	0.80	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002