SGM61620

4.2V to 60V, 2A Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61620 is a fully-integrated, synchronous, rectified, Buck converter. It offers a very compact solution to provide a 2A continuous current over a wide input voltage range from 4.2V to 60V. Reduced size and cost of over-voltage and surge protection solutions due to input voltage transient tolerances up to 65V.

The SGM61620 features 400kHz operating frequency, which is suitable for high efficiency. Integration and internal compensation eliminates many external components and the pin out is optimized to simplify PCB layout.

The EN pin employs an enable divider to establish a precision threshold that simplifies UVLO adjustment and device on/off control. The power-good output is designed with built-in filtering and delay to provide a true indicator of system status.

The SGM61620A operates in power save mode (PSM), which maintains high efficiency during light load operation.

Protection features include current limit, hiccup mode short-circuit protection and thermal shutdown with auto recovery.

The SGM61620 is available in a Green SOIC-8 (Exposed Pad) package.

FEATURES

- **4.2V to 60V Input Voltage Range**
- **Input Transient Protection up to 65V**
- **1V to 95% of V_{IN} Output Voltage Range**
- **Fixed 400kHz Switching Frequency**
- **PSM Mode Option for Higher Light Load Efficiency**
  SGM61620A: PSM Version
- **32μA (TYP) Operating Quiescent Current**
- **Internal Compensation**
- **Power-Good Flag and Precision Enable**
- **Full Protection Features: Hiccup Mode Short-Circuit Protection, Thermal Shutdown with Auto Recovery and Cycle-by-Cycle Current Limit**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Industrial Power Supplies
Telecom and Datacom Systems
General Purpose Wide V_{IN} Regulation

SIMPLIFIED SCHEMATIC

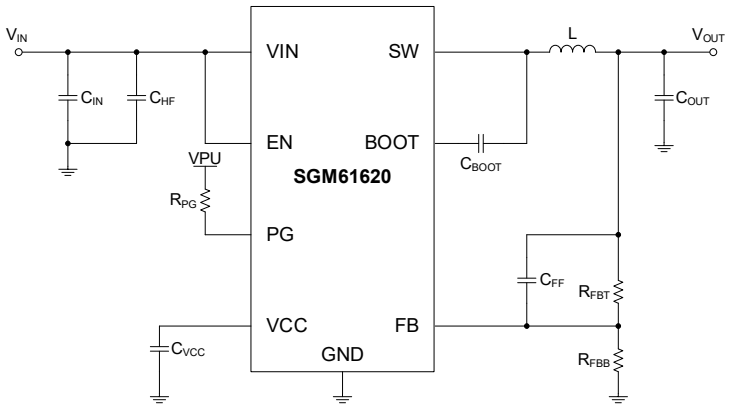


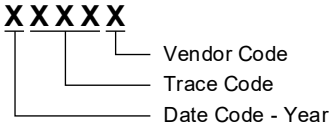
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61620A	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61620AXPS8G/TR	SGM 0IGXPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- VIN to GND ..... -0.3V to 65V
- EN to GND ..... -0.3V to 65V
- FB to GND ..... -0.3V to 5.5V
- PG to GND ..... -0.3V to 20V

Output Voltage
- SW to GND ..... -0.3V to 65V
- SW to GND, Less than 10ns Transient ..... -3.5V to 65V
- BOOT to SW ..... -0.3V to 5.5V
- VCC to GND ..... -0.3V to 5.5V

Package Thermal Resistance
- SOIC-8 (Exposed Pad), θ_{JA} ..... 34.1℃/W
- SOIC-8 (Exposed Pad), θ_{JB} ..... 8.8℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 41.9℃/W
- SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 3.5℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±3000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage
- VIN to GND ..... 4.2V to 60V
- EN to GND ..... 0V to 60V
- PG to GND ..... 0V to 18V

Output Current, I_{OUT} ..... 0A to 2A

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

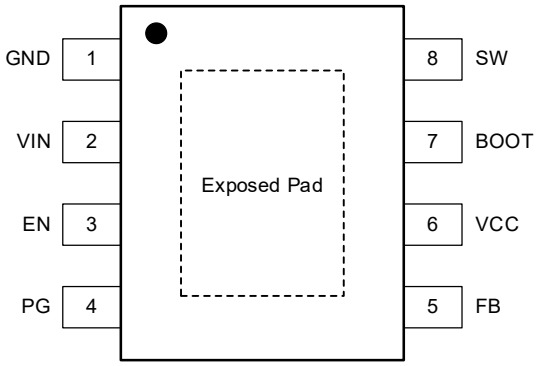
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	GND	G	Power and Analog Ground. Ground reference for internal references, logic and regulated output voltage. For the reason, care must be taken in PCB layout.
2	VIN	P	Power Supply Input Pin. It requires a high-quality decoupling capacitor or capacitors directly to this pin and GND to reduce switching spikes.
3	EN	A	Enable Input to Regulator. Pull this pin below the low threshold to shut the chip down. Pull it above the high threshold enables the chip. The pin can be connected directly to VIN. It cannot be left floating.
4	PG	A	Open-Drain Output for Power-Good Flag. Connect to suitable voltage supply through a current limiting resistor. High = power ok, low = power bad. Flag pulls low when EN = low. It can be left open when not used.
5	FB	A	Feedback Input. Connect the midpoint of the feedback resistor divider. It cannot be left floating. Do not connect this pin directly to GND.
6	VCC	P	LDO (Internal Bias) Output. This pin is provided for bypassing to GND only. Do not add load on the VCC pin.
7	BOOT	P	Bootstrap Input for Internal High-side Driver. Connect a high-quality 100nF capacitor as close as possible to the IC between this pin and the SW pin.
8	SW	P	Switching Node. Output of the internal power switchers.
—	Exposed Pad	G	Thermal Exposed Pad. Connect to ground plane on PCB. It is the main thermal relief path for the die.

NOTE: G = ground, P = power, A = analog.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 24V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VIN Pin)						
Operating Quiescent Current (Non-Switching)	I_{Q_NONSW}	V_{EN} = 3.3V, V_{FB} = 1.05V (PSM variant only)		32	50	μA
Shutdown Quiescent Current; Measured at VIN Pin	I_{SD}	V_{EN} = 0V		2		μA
Enable (EN Pin)						
Enable Input High Threshold for V_{CC} Output	$V_{EN\_VCC\_H}$	V_{ENABLE} rising			1.14	V
Enable Input Low Threshold for V_{CC} Output	$V_{EN\_VCC\_L}$	V_{ENABLE} falling	0.3			V
Enable Input High Level for V_{OUT}	$V_{EN\_VOUT\_H}$	V_{ENABLE} rising	1.15	1.21	1.27	V
Enable Input Hysteresis for V_{OUT}	$V_{EN\_VOUT\_HYS}$	Hysteresis below $V_{EN\_VOUT\_H}$, falling		150		mV
Enable Input Leakage Current	I_{LKG_EN}	V_{EN} = 3.3V		2.2		nA
Internal LDO (VCC Pin)						
Internal V_{CC} Voltage	V_{CC}	V_{IN} = 6V to 60V	4.45	4.7	4.95	V
Internal V_{CC} Rising Under-Voltage Lockout	$V_{CC\_UVLO\_R}$	V_{CC} rising	3.5	3.8	4.1	V
Internal V_{CC} Falling Under-Voltage Lockout	$V_{CC\_UVLO\_F}$	V_{CC} falling	3.0	3.25	3.5	V
Voltage Reference (FB Pin)						
Feedback Voltage	V_{FB}		0.985	1	1.012	V
Feedback Leakage Current	I_{LKG_FB}	V_{FB} = 1V		2.8		nA
Current Limits and Hiccup						
High-side Current Limit	I_{HS_LIMIT}	V_{IN} = 24V, V_{OUT} = 5V, L = 10μH	2.4	3.0	3.6	A
Low-side Current Limit (1)	I_{LS_LIMIT}	T_J = +25℃	1.85	2.25	2.70	A
Zero Cross Detector Threshold	I_{L_ZC}	PSM variants only		0.07		A
Minimum Inductor Peak Current (2)	I_{PEAK_MIN}			0.6		A
Power Good (PG Pin)						
Power-Good Upper Threshold - Falling	$V_{PG\_HIGH\_DN}$	% of FB voltage	105	110	115	%
Power-Good Lower Threshold - Falling	$V_{PG\_LOW\_DN}$	% of FB voltage	87	91	95	%
Power-Good Hysteresis (Rising & Falling)	V_{PG_HYS}	% of FB voltage		2		%
Minimum Input Voltage for Proper Power-Good Function	V_{PG_VALID}				2	V
Power-Good On-Resistance	R_{PG}	V_{EN} = 0V		40	50	Ω
MOSFETs						
High-side MOSFET On-Resistance	R_{DSON_HS}	I_{OUT} = 0.5A		240	460	mΩ
Low-side MOSFET On-Resistance	R_{DSON_LS}	I_{OUT} = 0.5A		160	310	mΩ

NOTE:

1. The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

2. Guaranteed by design, not tested in production.

TIMING REQUIREMENTS

(T_J = -40℃ to +125℃, V_{IN} = 24V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Switch On Time	t_{ON_MIN}			150		ns
Minimum Switch Off Time	t_{OFF_MIN}			90		ns
Maximum Switch On Time	t_{ON_MAX}			6.8		μs
Internal Soft-Start Time	t_{SS}		3	5	7	ms

SWITCHING CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Internal Oscillator Frequency	f_{OSC}		340	400	460	kHz

SYSTEM CHARACTERISTICS (1)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{IN}		4.2		60	V
Adjustable Output Voltage Regulation	V_{OUT}	PSM operation	-0.04		0.8	%
Input Supply Current when in Regulation	I_{SUPPLY}	V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A, R_{FBT} = 1MΩ, PSM variant		32		μA
Maximum Switch Duty Cycle	D_{MAX}			98.5		%
FB Pin Voltage Required to Trip Short-Circuit Hiccup Mode	V_{HC}			0.4		V
Dead Time DRVH Off to DRVL On	t_{DF}			11.5		ns
Dead Time DRVL Off to DRVH On	t_{DR}			13.4		
Thermal Shutdown Temperature	T_{SD}	Shutdown temperature		165		℃
		Recovery temperature		150		℃

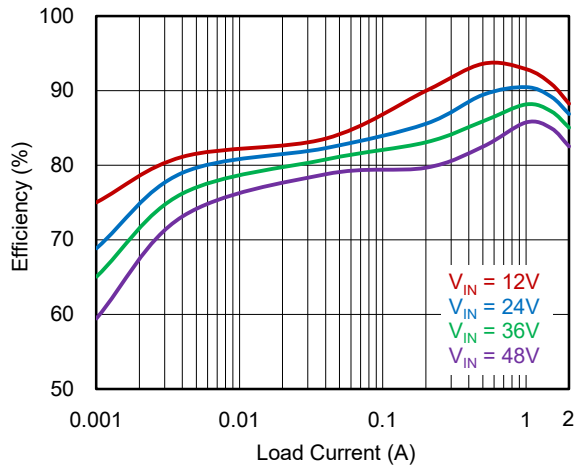
NOTE:

1. Guaranteed by design, not tested in production.

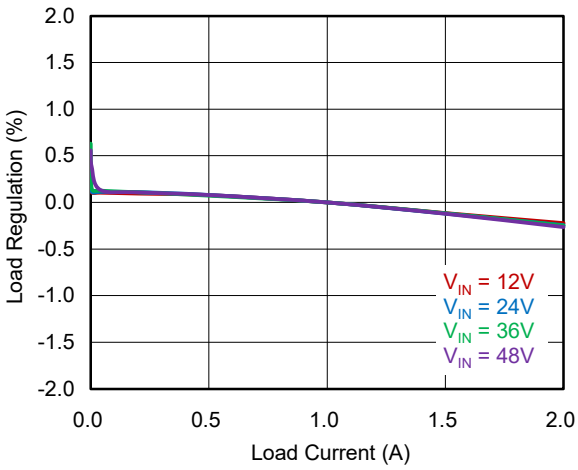
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, the corresponding BOM can be found in Table 1, unless otherwise noted.

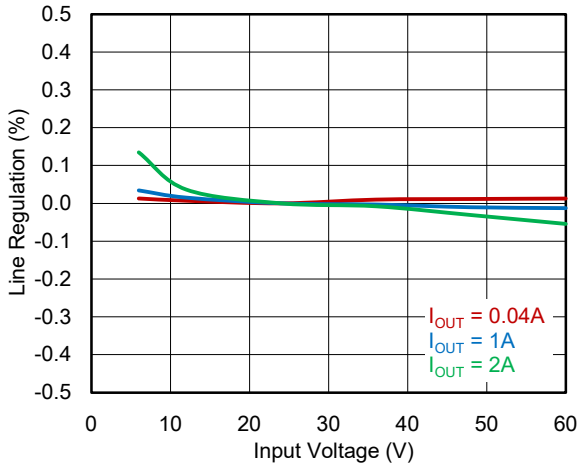
Efficiency vs. Load Current



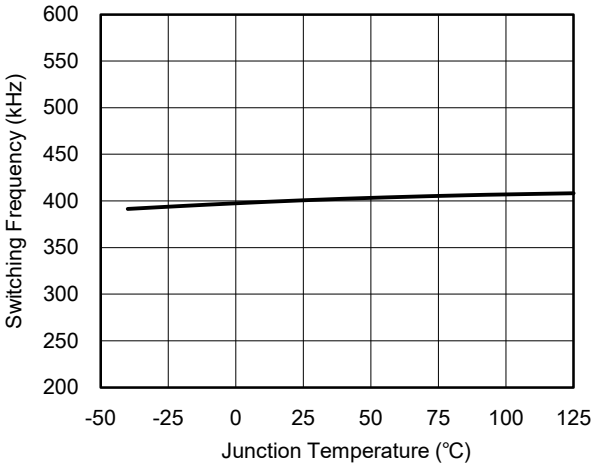
Load Regulation



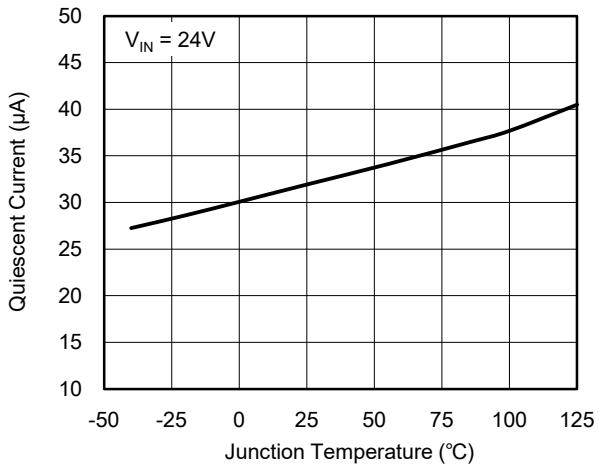
Line Regulation



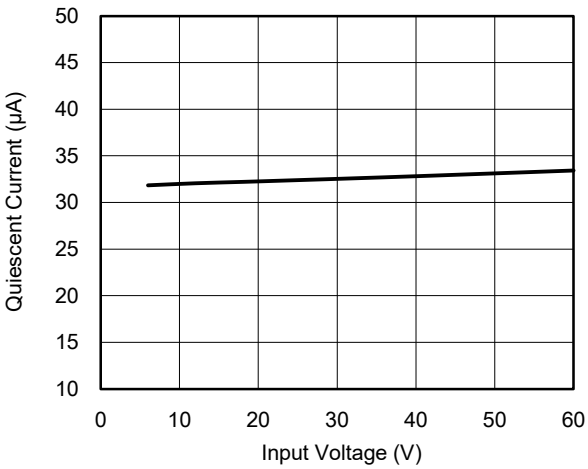
Switching Frequency vs. Junction Temperature



Quiescent Current vs. Junction Temperature



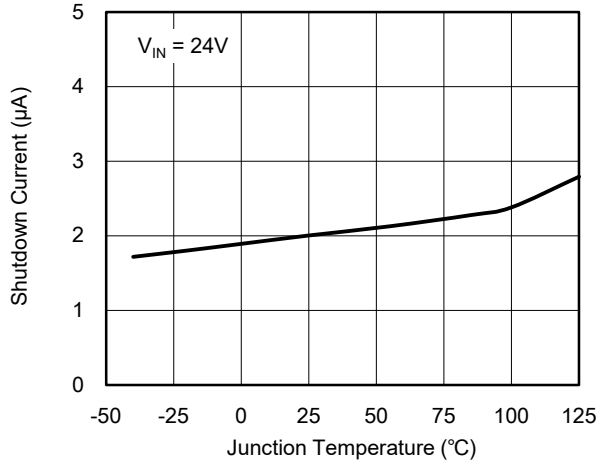
Quiescent Current vs. Input Voltage



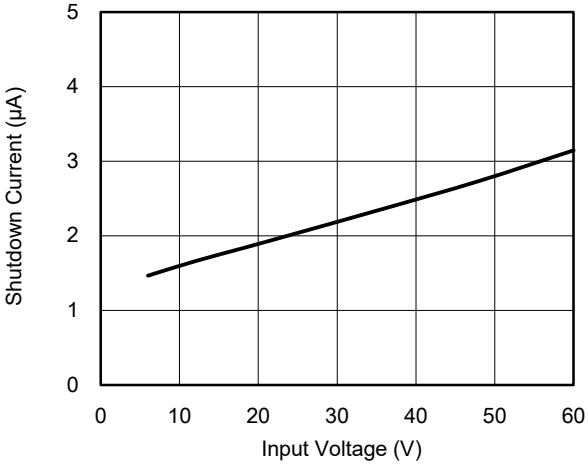
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, the corresponding BOM can be found in Table 1, unless otherwise noted.

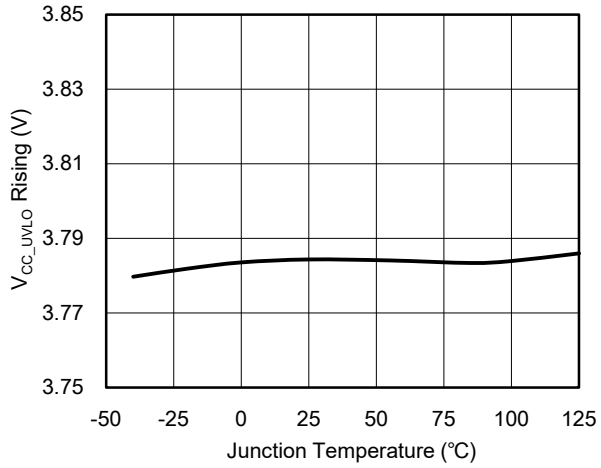
Shutdown Current vs. Junction Temperature



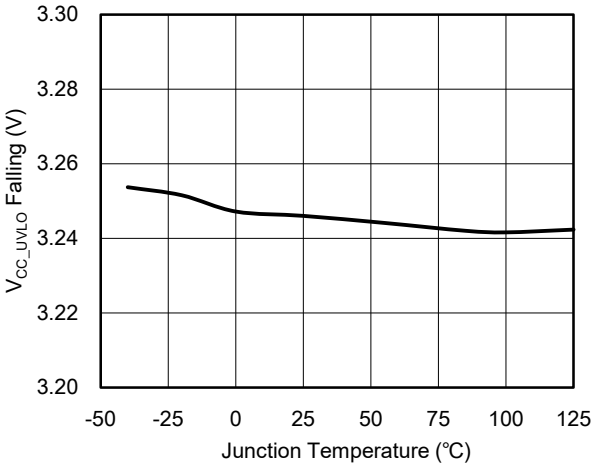
Shutdown Current vs. Input Voltage



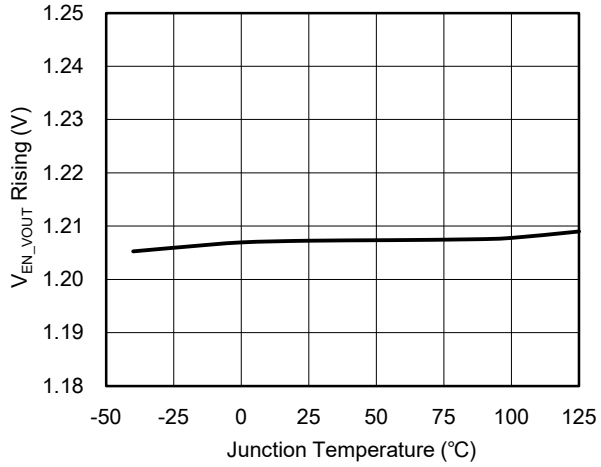
V_{CC_UVLO} Rising vs. Junction Temperature



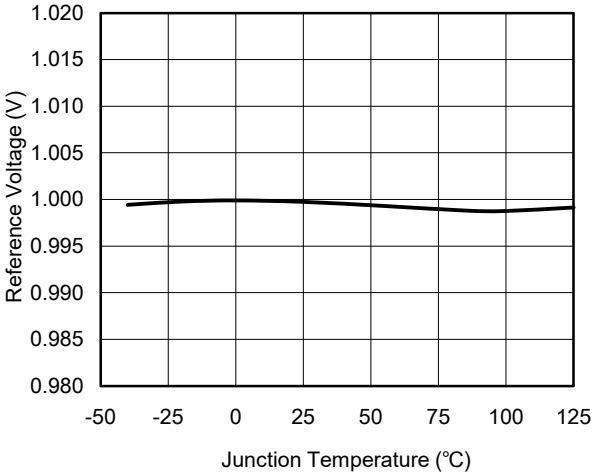
V_{CC_UVLO} Falling vs. Junction Temperature



V_{EN_VOUT} Rising vs. Junction Temperature



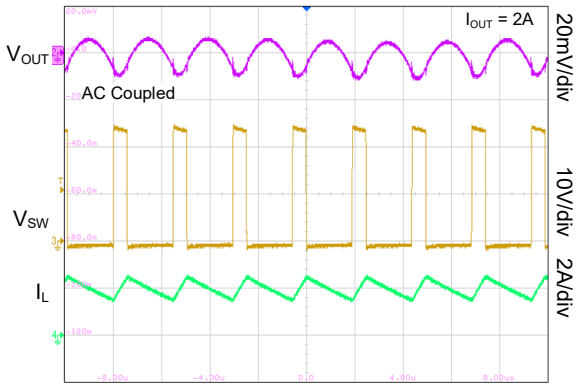
Reference Voltage vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

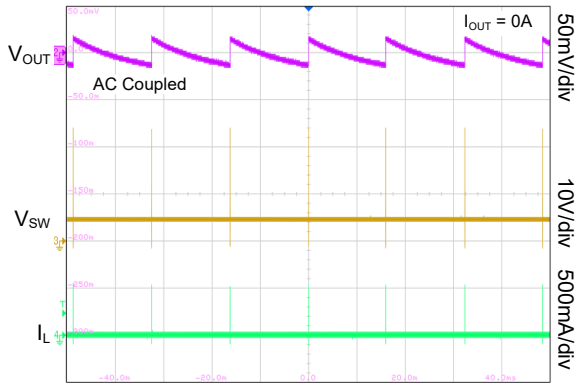
T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, the corresponding BOM can be found in Table 1, unless otherwise noted.

CCM Mode



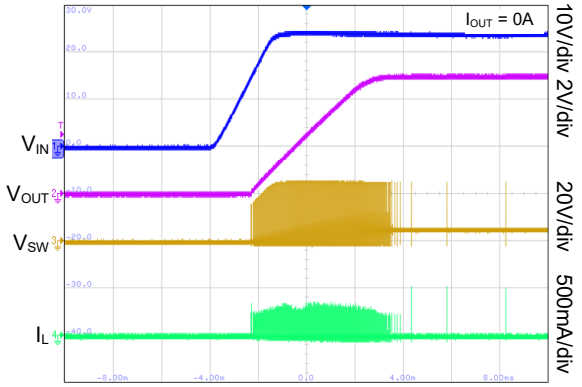
Time (2μs/div)

PSM Mode



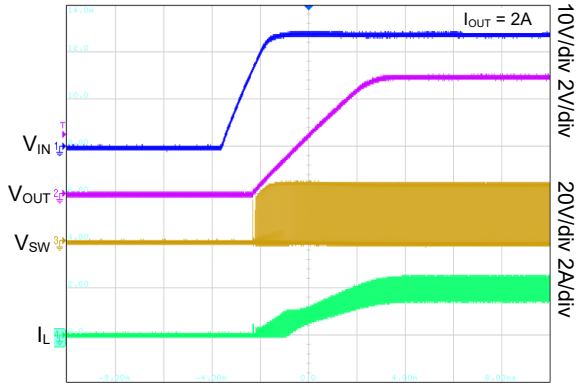
Time (10ms/div)

Start-Up by VIN



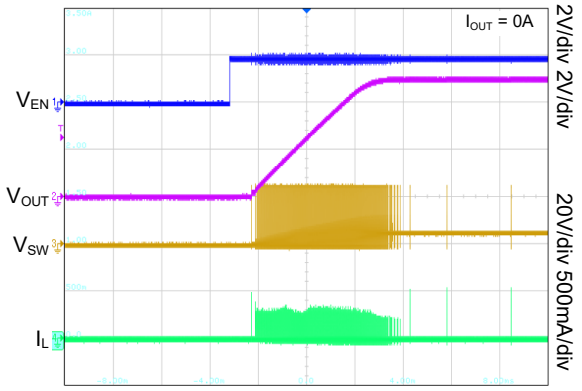
Time (2ms/div)

Start-Up by VIN



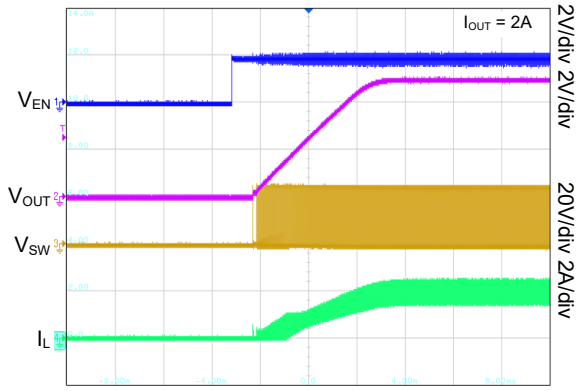
Time (2ms/div)

Start-Up by EN



Time (2ms/div)

Start-Up by EN

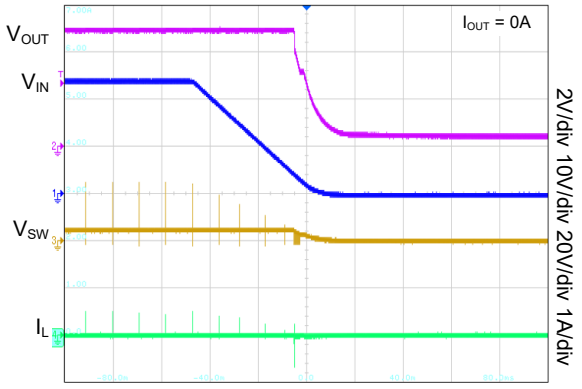


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

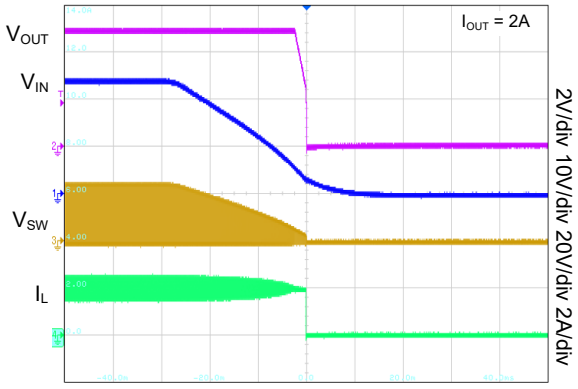
T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, the corresponding BOM can be found in Table 1, unless otherwise noted.

Shutdown by VIN



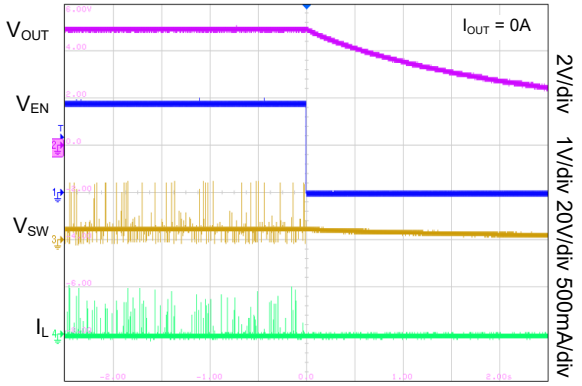
Time (20ms/div)

Shutdown by VIN



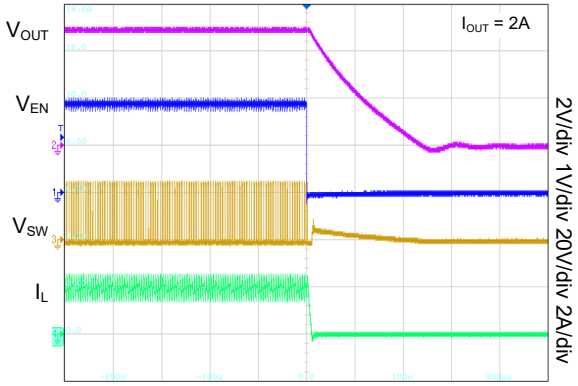
Time (10ms/div)

Shutdown by EN



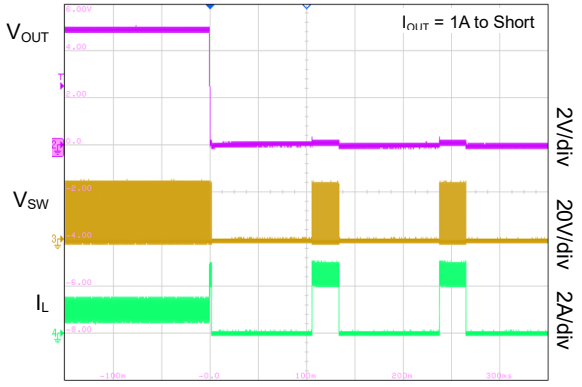
Time (500ms/div)

Shutdown by EN



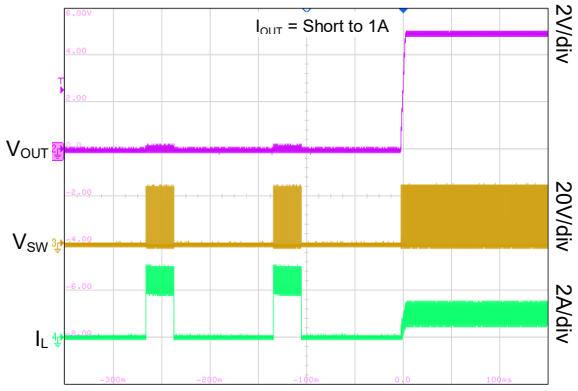
Time (50μs/div)

SCP Entry



Time (50ms/div)

SCP Recovery

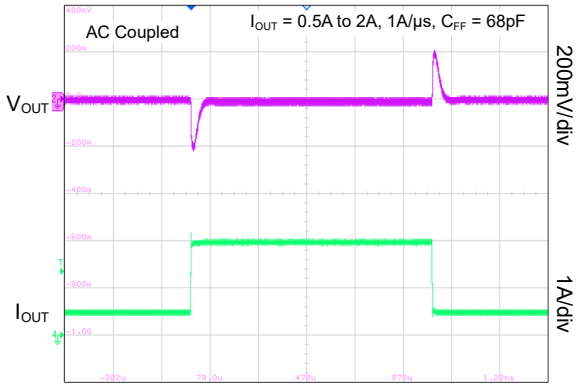


Time (50ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 24V, V_{OUT} = 5V, the corresponding BOM can be found in Table 1, unless otherwise noted.

Load Transient



Time (200μs/div)

FUNCTIONAL BLOCK DIAGRAM

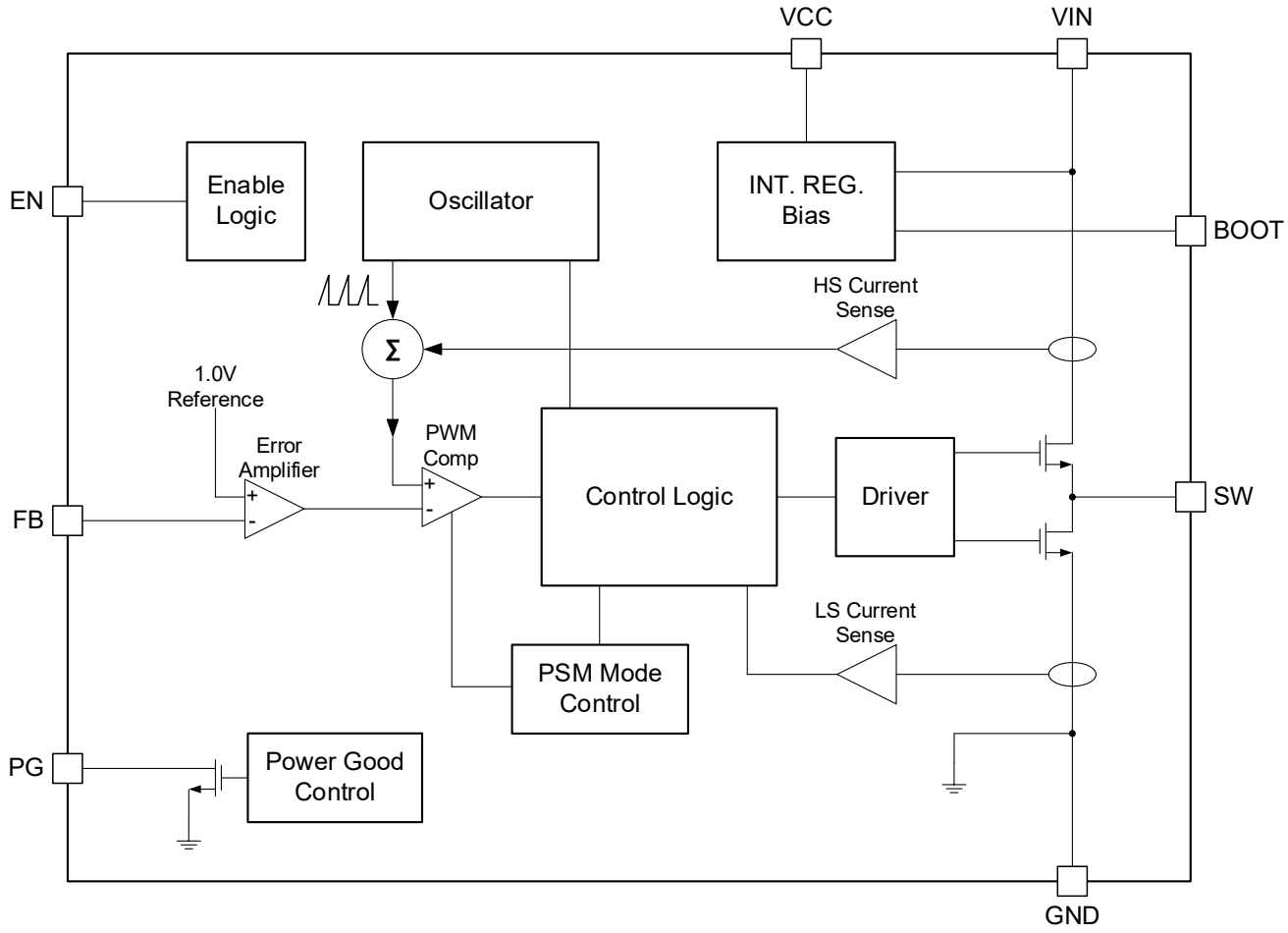


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61620 is a 60V synchronous Buck converter with two integrated N-MOSTETs and 2A continuous output current capability. Its internally compensated peak current mode control simplifies the design process and reduces the need for external components.

The minimum operating input voltage of the device is 4.2V. The output voltage can be set down to 1V (reference voltage). No switching operating current is 32μA (TYP). The shutdown current is 2μA (TYP) if the device is disabled. High efficiency is achieved through the integrated low R_{DSON} high-side switch (240mΩ) and low-side switch (160mΩ).

The bootstrap diode is integrated, and only a small capacitor (C_{BOOT}) between BOOT and SW pins is needed for the high-side MOSFET gate driving bias.

Additional features such as thermal shutdown and short-circuit protection (hiccup mode) are also provided.

Enable Input and UVLO Adjustment

The EN pin serves as an on/off control for the device. When the EN voltage is greater than $V_{EN\_VCC\_H}$ (1.14V MAX), the device enters standby mode, where it supplies power to the internal V_{CC} but does not generate an output voltage. To fully enable the device, continue to increase the EN voltage until it is above $V_{EN\_VOUT\_H}$ (1.21V TYP). If the EN voltage falls below $V_{EN\_VOUT\_H}$ - $V_{EN\_VOUT\_HYS}$, the device will stop switching and enter standby mode. When the EN voltage is below $V_{EN\_VCC\_L}$ (0.3V MIN), the device will be completely shut down.

If an application requires increasing the V_{IN} turn-on threshold and adding hysteresis to the V_{IN} UVLO, a voltage divider as shown in Figure 3 is required. Use Equations 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage. In addition, if this feature is not required, the EN input can be connected directly to VIN, but make sure it is not left floating.

$$R_{EN1} = \left(\frac{V_{START}}{V_{EN\_VOUT\_H}} - 1 \right) \times R_{EN2} \quad (1)$$

$$V_{STOP} = V_{START} \times \left(1 - \frac{V_{EN\_VOUT\_HYS}}{V_{EN\_VOUT\_H}} \right) \quad (2)$$

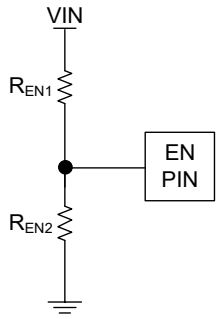


Figure 3. VIN UVLO Adjustment

Power Good

The SGM61620 features a power-good (PG) pin that indicates whether the output voltage is at the desired level. This pin is an open-drain output.

To ensure that the PG pin is low logic with no input for SGM61620, it is recommended to pull up the PG pin to the VCC of SGM61620.

Figure 4 illustrates that when the FB voltage is within the power-good range, the PG switch is turned off, and the PG pin is pulled up to high. Conversely, when the FB voltage is outside the power-good range, the PG switch is turned on, and the PG pin is pulled down to low. When EN is pulled low, the flag output will also be forced low.

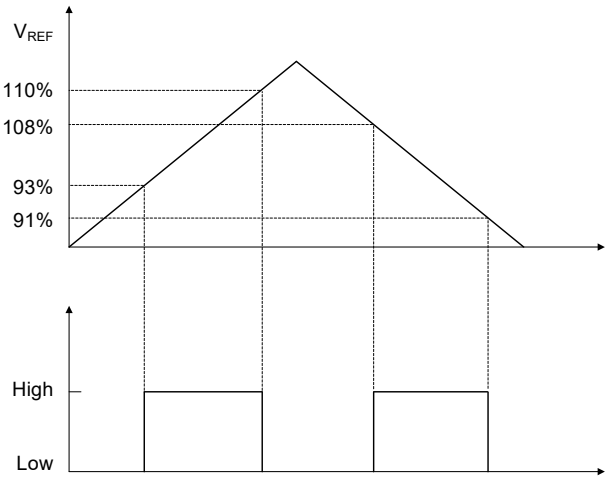


Figure 4. Power-Good Flag

DETAILED DESCRIPTION (continued)

Bootstrap Gate Driving (BOOT)

An internal voltage regulator provides bias voltage to the gate driver through an external small ceramic capacitor placed between the BOOT and SW pins. A 0.1μF ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10V or higher voltage rating. Typically, C_{BOOT} is charged during each cycle when the low-side (LS) switch is turned on and discharged to the boot regulator when the high-side (HS) switch is turned on.

Light Load Operation with PSM (SGM61620A)

At light loads, SGM61620A enters power save mode (PSM) to reduce switching loss and keep high efficiency by lowering the number of switching pulses. When the peak inductor current is below PSM current threshold, the corresponding internal COMP voltage (V_{COMP}) will be lower than the internal threshold, the device will enter PSM.

After entering PSM for a delay time, some modules are shut down to minimum input current, and the device draws only 32μA (TYP) input quiescent current. The high-side MOSFET will not switch until the output voltage falls for the internal V_{COMP} to rise above the internal threshold.

Low Dropout

As input voltage drops, the difference between input voltage and output voltage decreases, causing off-time of the high-side MOSFET to approach its minimum possible value. Dropout occurs when input voltage falls below the required minimum for the regulator to maintain output voltage. To maintain output voltage at nominal value, SGM61620 will decrease its switching frequency and increase duty cycle.

Over-Current Protection

Current mode control provides over-current protection (OCP) by HS current sensing, which compares the sensed HS switch current with the HS current-limit threshold in each cycle. When the HS current reaches that threshold, the HS switch is turned off. Then the LS switch is turned on, the conduction current is monitored by the internal circuitry. In each cycle, the sensed LS switch current is compared to the internally LS current-limit threshold only when the HS current-limit threshold is triggered. If the sensed LS switch current is higher than the LS current-limit threshold during LS conduction, the HS does not turn on and the LS stays on when the clock signal comes. When the sensed LS switch current is below the LS current-limit threshold, for SGM61620, the HS switch waits until the clock signal arrives before turning on again.

In addition, if the HS current reaches the current-limit threshold for more than 128 times and FB drops below 40% of V_{REF} at the same time, the device enters hiccup mode in which the device will turn off switching and restart cyclically until the over current fault is cleared. Hiccup mode is a protective measure designed to prevent overheating and severe damage from over-current conditions.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +165℃ (TYP), the TSD protection circuit will stop the switch from operating to protect the device from overheating. After the junction temperature drops below +150°C (TYP), the device automatically restarts and goes through the power-up procedure.

APPLICATION INFORMATION

The design method for the SGM61620 Buck converter is explained in this section. A typical application circuit for the SGM61620 is shown in Figure 5. It is used for converting a 6V to 60V supply voltage to a lower 5V output voltage with a maximum output current of 2A.

The external components are designed based on the application requirements and device stability. Some suitable parameters for different output voltages are provided in Table 1 to simplify the selection of components. The C_{OUT} values in Table 1 are rated values.

Typical Application

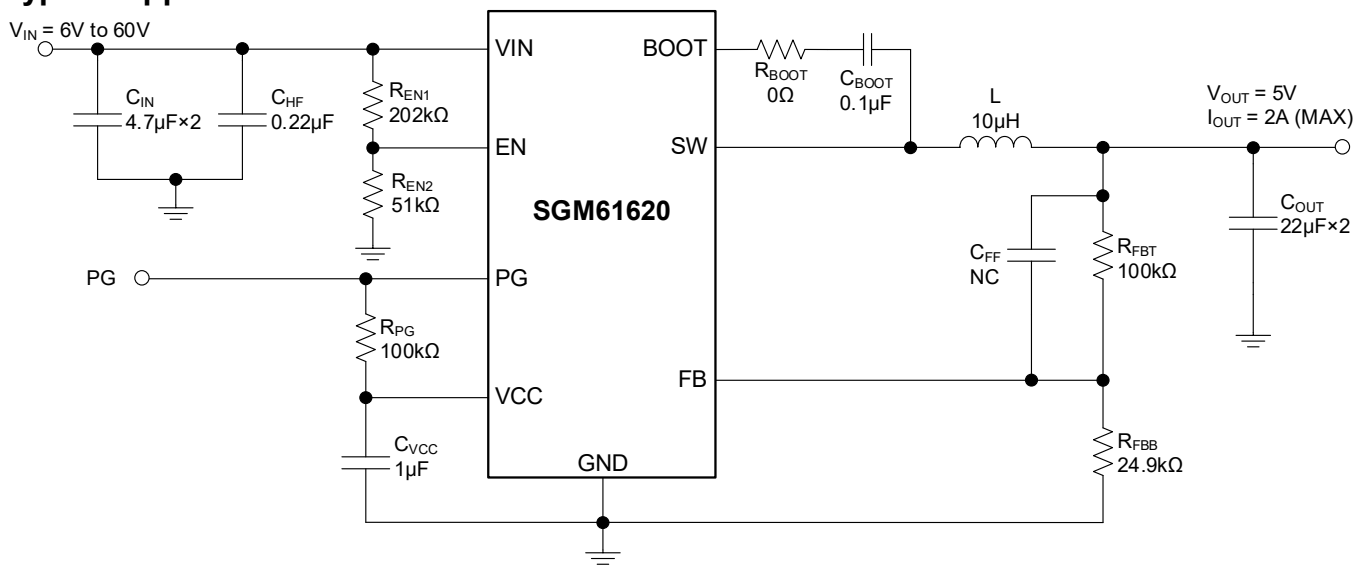


Figure 5. SGM61620 Typical Application Circuit

Table 1. Some Typical Parameters for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF} (pF)
400	3.3	6.8	3×22	100	43.2	NC
400	5	10	2×22	100	24.9	NC
400	12	33	4×10	100	9.09	NC

Requirements

The design parameters required for the design example are given in Table 2.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	24V TYP
Output Voltage	5V
Output Current Rating	2A
Operating Frequency	400kHz

Input Capacitors Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61620. At least 3μF of effective capacitance (after derating) is needed at the input. In some applications, additional bulk capacitance may also be required for the input, for example, when the SGM61620 is more than 5cm away from the input source. The input capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 3 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 2A, yields an RMS input ripple current of 1A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (3)$$

APPLICATION INFORMATION (continued)

For this design, a ceramic capacitor with at least 100V voltage rating is required to support the maximum input voltage. Therefore, two 4.7μF/100V capacitors are selected for VIN to cover all DC bias, thermal and aging derating. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

It is recommended to place an additional small size 220nF/0603 ceramic capacitor (C_{HF}) right beside VIN and GND pins for high frequency filtering.

Inductor Design

Equation 5 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor (K_{IND} = $\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions. For peak current mode converter, selecting an inductor with saturation current must be above the switch current limit. Typically, a 20% to 40% current ripple is selected (K_{IND} = 0.2 ~ 0.4).

$$L = \frac{V_{IN} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (5)$$

In this example, the calculated inductance will be 12.4μH with K_{IND} = 0.4 at V_{IN} = 24V, a 10uH inductor is selected here. The ripple, RMS and peak inductors current calculations are summarized in Equations 6, 7 and 8 respectively.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (6)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (7)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (8)$$

Output Capacitor Design

There are three main criteria that must be considered when designing the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect and respond to the output change. Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 9 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (9)$$

where:

- ΔI_{OUT} is the change in output current.
- ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1A to 2A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 1A, the minimum required capacitance will be 20μF. Note that the impact of output capacitor ESR on the transient is not considered in Equation 9. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient.

APPLICATION INFORMATION (continued)

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 10 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{\left(V_{OUT} + \Delta V_{OUT}\right)^2 - V_{OUT}^2} \quad (10)$$

where:

- I_{OUT_H} is the output current under heavy load.
- I_{OUT_L} is the output current under light load.

For example, if the acceptable transient from 2A to 1A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 11.7μF.

Equation 11 can be used for the output ripple criteria and finding the minimum output capacitance needed. V_{OUT_RIPPLE} is the maximum acceptable ripple. In this example, the allowed ripple is 50mV that results in minimum capacitance of 6.2μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (11)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 11. For a specific output capacitance value, use Equation 12 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (12)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, two 22μF/25V ceramic capacitors are used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 13 calculates the RMS current that the output capacitor must support.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (13)$$

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_{BOOT}). It is recommended to reserve a resistor R_{BOOT} in series with C_{BOOT} for improving radiated EMI performance if needed. Too high values for R_{BOOT} may cause insufficient C_{BOOT} charging in high duty-cycle applications. Slower switch switch-on speed will also increase switch losses and reduce efficiency.

UVLO Setting

The input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61620, as shown in Figure 3. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 6V (UVLO rising threshold). When the regulator is working, it will not stop switching until the input falls below 5.2V (UVLO falling threshold). Equations 1 and 2 are provided to calculate R_{EN1} and V_{STOP}, respectively.

Feedback Resistors Setting

Use a resistor divider (R_{FBT} and R_{FBB}) to set the output voltage using Equations 14 and 15.

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}} \quad (14)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FBT}}{R_{FBB}} + 1\right) \quad (15)$$

Recommended to choose R_{FBT} around 100kΩ and calculate R_{FBB} from Equation 14. Use accurate and stable resistors (1% or better) to enhance output accuracy. For this example, the selected values are R_{FBT} = 100kΩ and R_{FBB} = 24.9kΩ, resulting in a 5.016V output voltage.

APPLICATION INFORMATION (continued)

C_{FF} Selection

Even though the SGM61620 is internally compensated, with low ESR ceramic capacitors, the phase margin can be low depending on the V_{OUT} and f_{SW} values. By adding an external feed-forward capacitor (C_{FF}) in parallel with the R_{FBT}, the phase margin can be improved (phase boost around crossover frequency). Without C_{FF}, and if ESR is very small, the crossover frequency (f_X) can be estimated from Equation 16, in which C_{OUT} is the actual derated value:

$$f_X = \frac{K}{V_{OUT} \times C_{OUT}} \quad (16)$$

where K = 4.313.

Then C_{FF} value can be estimated from:

$$C_{FF} = \frac{1}{2\pi \times f_X \times R_{FBT}} \quad (17)$$

For slightly larger ESR values, choose a C_{FF} value that is less than Equation 17 estimate. For larger ESR values, C_{FF} is not needed. Table 1 gives a quick starting point.

Layout Considerations

Example of PCB layout for SGM61620 is provided in Figure 6. This layout has been shown to bring good results, although other layout designs may also obtain good performance.

- Bypass the VIN pin to GND pin with low-ESR ceramic capacitors and place them as close as possible to the device.
- Share the same GND connection point with the input and output capacitors.
- Connect the device GND to the PCB ground plane right at the GND pin.
- Minimize the length and the area of the connection route from SW pin to the inductor to reduce the noise coupling from this area.
- Consider sufficient ground plane area on the top side for proper heat dissipation. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.

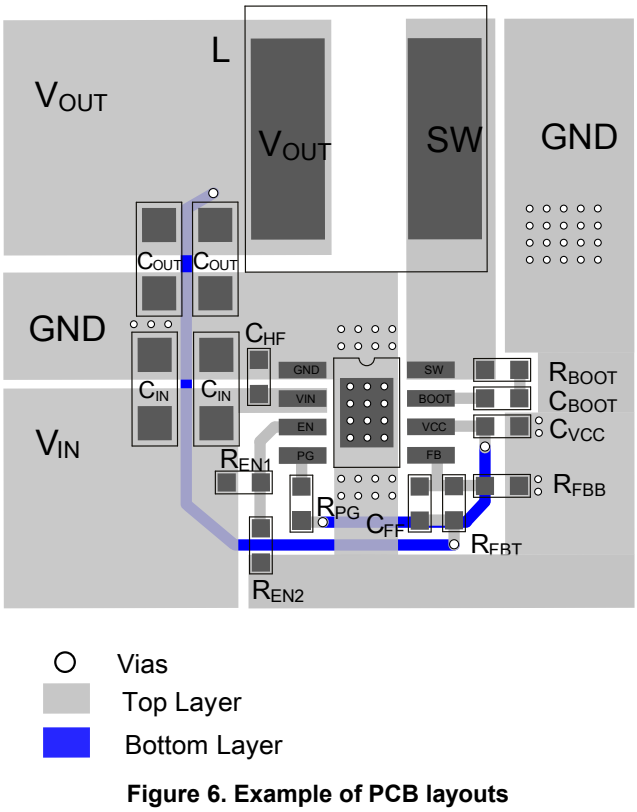


Figure 6. Example of PCB layouts

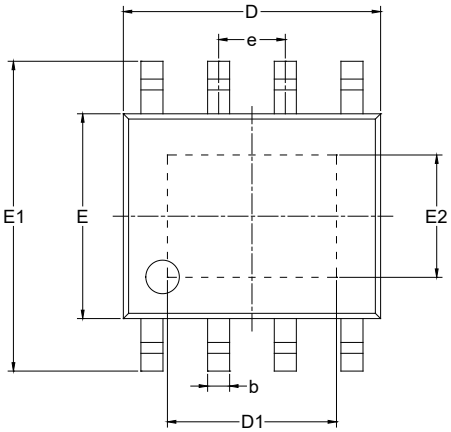
REVISION HISTORY

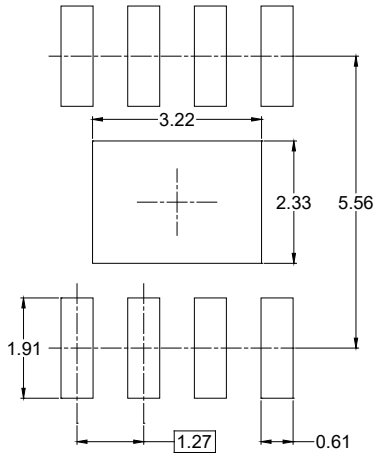
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

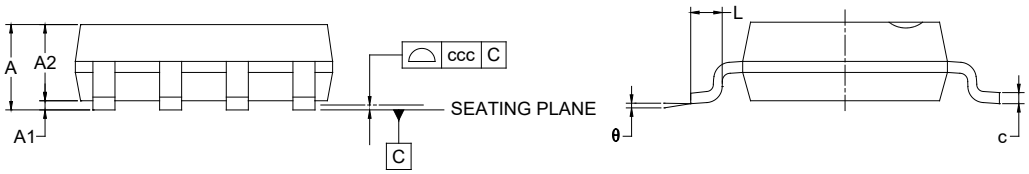
PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

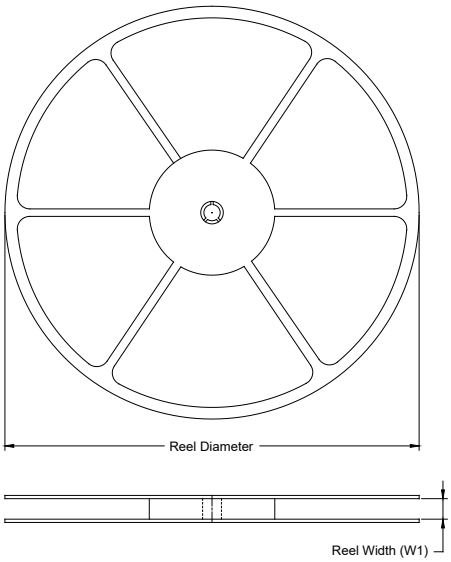


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

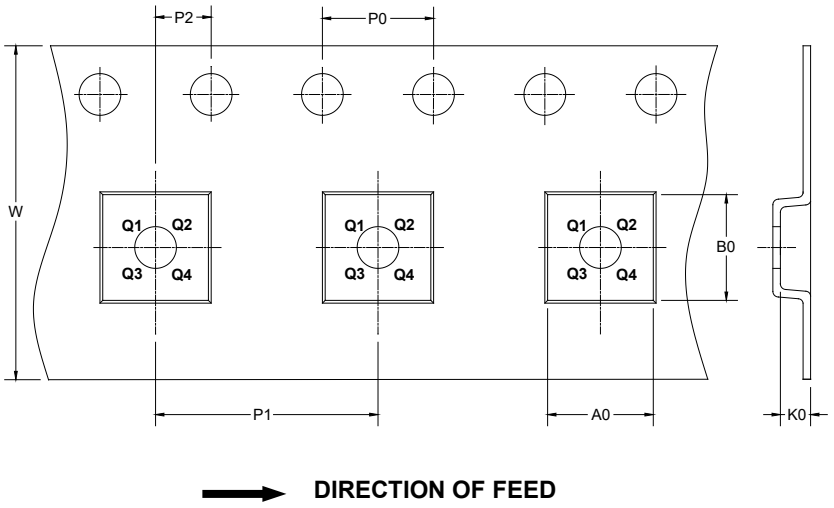
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



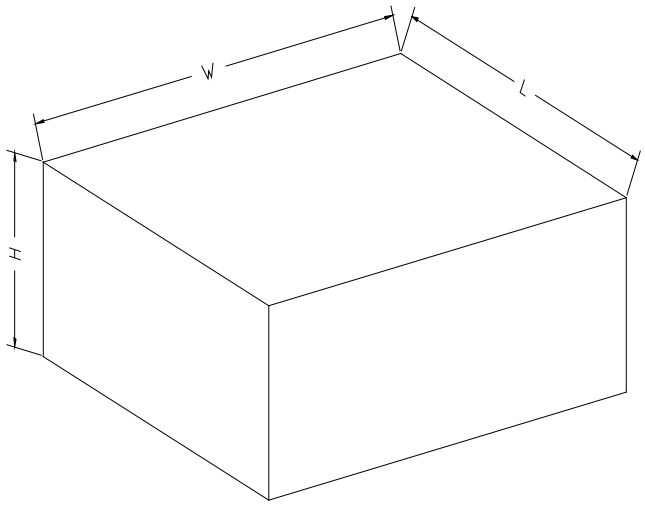
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002