SGM2547
23V, 8A Electronic Fuse with Bi-directional Power Delivery

GENERAL DESCRIPTION

The SGM2547 family is a compact electronic fuse (eFuse) with a full suite of protection functions. With very few external components, the SGM2547 can provide multiple protection modes: over-current, over-voltage, short-circuit and reverse current blocking.

The output current limit threshold and the transient over-current blanking timer can be adjusted by the user. The analog output load current is monitored by the ILIM pin. Programmable over-voltage protection is used to turn off the device if the IN rises over a threshold value and the downstream circuitry is not damaged by unintended power supply. Due to the back-to-back FETs packaged inside the chip, the SGM2547 can block reverse current from flowing through the channel when it is turned on, this function can be also disabled by pulling RCBCTRL pin (SGM2547CR only) low, which is very suitable for USB OTG. The V_{OUT} rise time can be programmed by setting an additional capacitor to the SS pin, which can minimize inrush current.

The SGM2547 is available in a Green WLCSP-2.5×1.79-12L package.

SIMPLIFIED SCHEMATIC

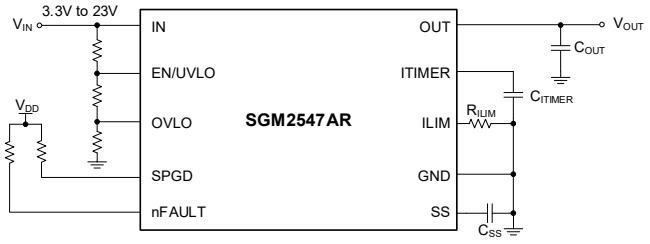


Figure 1. Simplified Schematic

FEATURES

- **Input Voltage: 3.3V to 23V, Surge up to 28V**
- **Either IN or OUT Sourcing**
- **Back-to-Back FETs with True Reverse Blocking**
- **Low On-Resistance: 13.2mΩ (TYP)**
- **Programmable Output Ramp Time**
- **Programmable Current Limit: 1A to 9A (±10% Accuracy for I_{LIM} > 3A)**
- **Load Current Monitor (±5% (TYP) Accuracy for I_{OUT} > 3A)**
- **Programmable Transient Blanking Timer (ITIMER Pin) to Allow Peak Current up to 2 × I_{LIM}**
- **Full Set of Protections**
  - **Programmable Over-Voltage Lockout (OVLO)**
  - **Short-Circuit Protection on OUT Pin**
  - **Under-Voltage Lockout**
  - **Thermal Shutdown**
- **Digital Outputs: Supply Good (SPGD) and Fault Indication (nFAULT)**
- **Available in a Green WLCSP-2.5×1.79-12L Package**

APPLICATIONS

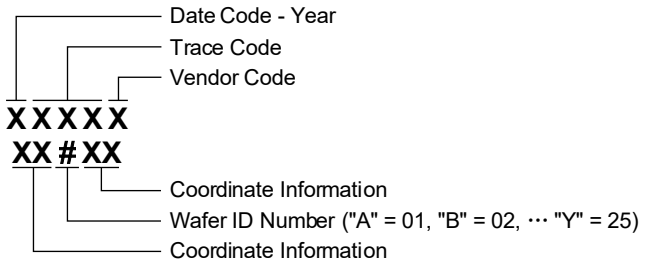
Hot-Swap and Hot-Plug
Adapter Power Devices
SSD and HDD Drives
Set-Top Boxes
Printers
White Goods
Digital TVs

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2547AR	WLCSP-2.5×1.79-12L	-40℃ to +125℃	SGM2547ARXG/TR	1H7 XXXXX XX#XX	Tape and Reel, 4500
SGM2547CR	WLCSP-2.5×1.79-12L	-40℃ to +125℃	SGM2547CRXG/TR	1H9 XXXXX XX#XX	Tape and Reel, 4500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

SELECTABLE MODEL

Model	SPGD Polarity	nFAULT or RCBCTRL	Steady-State Fast-Trip Threshold	Response to Fault
SGM2547AR	Active-High	nFAULT	Adjustable (2 × I_{LIM}) + Fixed	Auto-Retry
SGM2547CR	Active-High	RCBCTRL	Adjustable (2 × I_{LIM}) + Fixed	Auto-Retry

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN_MAX} ..... -0.3V to 28V
Output Voltage Range, V_{OUT_MAX} ..... -0.3V to 28V
Minimum Output Voltage Pulse (< 1μs), $V_{OUT_MAX_PLS}$ .....
.....> -0.8V
Enable Pin Voltage Range, $V_{EN/UVLO_MAX}$ ..... -0.3V to 6.5V
OVLO Pin Voltage Range, V_{OVLO_MAX} ..... -0.3V to 6.5V
SS Pin Voltage Range, V_{SS_MAX} ..... Internally Limited
ITIMER Pin Voltage Range, V_{ITIMER_MAX} ..... Internally Limited
RCBCTRL Pin Voltage Range, $V_{RCBCTRL_MAX}$ .... -0.3V to 6.5V
SPGD Pin Voltage Range, V_{SPGD_MAX} ..... -0.3V to 6.5V
nFAULT Pin Voltage Range, V_{nFAULT_MAX} ..... -0.3V to 6.5V
ILIM Pin Voltage Range, V_{ILIM_MAX} ..... Internally Limited
Maximum Continuous Switch Current, I_{MAX}.....
..... Internally Limited
Package Thermal Resistance
WLCSP-2.5×1.79-12L, θ_{JA} ..... 56.8℃/W
WLCSP-2.5×1.79-12L, θ_{JB} ..... 5.9℃/W
WLCSP-2.5×1.79-12L, θ_{JC} ..... 14.5℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 3.3V to 23V
Output Voltage Range, V_{OUT} ..... 23V (MAX)
Enable Pin Voltage Range, $V_{EN/UVLO}$ ..... 5V (MAX)
OVLO Pin Voltage Range, V_{OVLO} ..... 5V (MAX)
SS Capacitor Voltage Rating, V_{SS} ..... V_{IN} + 5V (1) (MIN)
RCBCTRL Pin Voltage Range, $V_{RCBCTRL}$ ..... 5V (MAX)
nFAULT Pin Voltage Range, V_{nFAULT} ..... 5V (MAX)
SPGD Pin Voltage Range, V_{SPGD} ..... 5V (MAX)
ITIMER Capacitor Voltage Rating, V_{ITIMER} ..... 4V (MIN)
ILIM Pin Resistance, R_{ILIM} .....536Ω to 4834Ω
Continuous Switch Current, T_J ≤ +125℃, I_{LOAD} ..... 8A (MAX)

NOTE: 1. The SS capacitor rating should be higher than maximum output voltage + 5V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

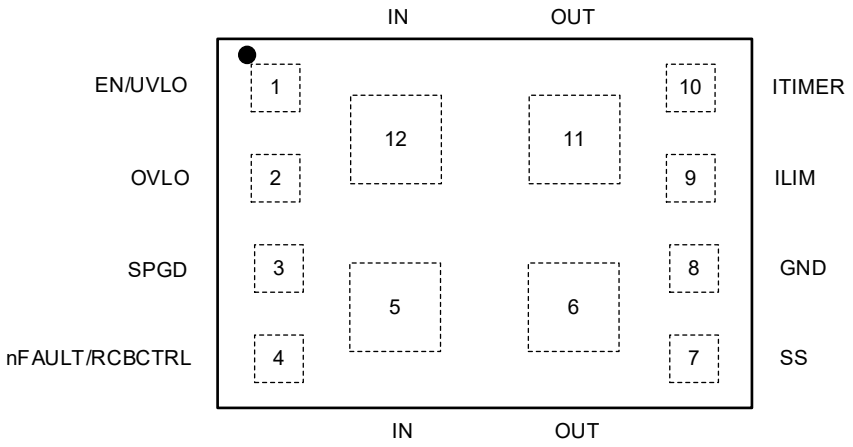
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.5×1.79-12L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	EN/UVLO	Enable and Under-Voltage Lockout Input. Asserting EN/UVLO pin high enables the device. Place a resistor divider to set programmable under-voltage lockout threshold. Do not float this pin.
2	OVLO	Over-Voltage Lockout Pin. The over-voltage lockout threshold is programmed by the resistor divider from the power supply to the OVLO terminal to GND. The device is enabled when this pin is tied to low level. This pin cannot be left floating.
3	SPGD	Supply Good Indication (Active-High). This is an open-drain pin. When the input voltage is within the valid range and the soft-start has finished, this pin goes high.
4	nFAULT	SGM2547AR: Fault Event Indicator (Active-Low). This pin is an open-drain output. When a fault occurs, it will be low.
	RCBCTRL	SGM2547CR: Reverse Current Blocking Enable Input (Active-High). Active-high or leave this pin floating enable true reverse current blocking and active-low in steady state to disable this function.
5, 12	IN	Input Supply Voltage.
6, 11	OUT	Output of the Device.
7	SS	Soft-Start Pin. The capacitor between SS and GND pins will set the slew rate according to the application requirements. When this pin is left floating, the device will start up at the fastest rate.
8	GND	GND.
9	ILIM	Programming Current Limit Pin. A resistor between this pin and GND sets the overload and short-circuit current limit levels. The analog output load current is monitored by this pin. Do not float this pin.
10	ITIMER	Place a capacitor between this pin and GND can set the over-current blanking time. At this stage, the output current value can temporarily exceed the internally set current limit value (but not exceed the fast-trip threshold). After this time, the device will take action if it is still in over-current state. Leaving this pin open will provide the fastest response to an over-current event.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT = open, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{ILIM} = 536Ω, SS = open, ITIMER = open, SPGD = open, nFAULT = open for SGM2547AR, RCBCTRL = open for SGM2547CR. Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply (IN)						
IN Supply Under-Voltage Protection Threshold	$V_{UVP_R_IN}$	Rising	2.43	2.7	2.95	V
	$V_{UVP_F_IN}$	Falling	2.07	2.2	2.40	
IN Supply On-State Quiescent Current	I_{Q_ON}	IN sourcing, $V_{EN} > V_{UVLO_R}$		200	450	μA
IN Supply Off-State Current	I_{Q_OFF}	IN sourcing, $V_{SD_F} < V_{EN} < V_{UVLO_R}$		60	150	μA
IN Supply Shutdown Current	I_{SD_IN}	IN sourcing, $V_{EN} < V_{SD_F}$		10	25	μA
OUT Supply Under-Voltage Protection	$V_{UVP_R_OUT}$	Rising	2.33	2.8	3.25	V
	$V_{UVP_F_OUT}$	Falling	2.05	2.2	2.40	V
On-Resistance (IN - OUT)						
On-Resistance	R_{ON}	V_{IN} = 12V, I_{OUT} = 3A, T_J = +25℃		13.2	17	mΩ
		V_{IN} = 3.3V to 23V, I_{OUT} = 3A, T_J = -40℃ to +125℃			23	mΩ
Enable/Under-Voltage Lockout (EN/UVLO)						
EN/UVLO Threshold	V_{UVLO_R}	Rising	1.185	1.21	1.23	V
	V_{UVLO_F}	Falling	1.08	1.11	1.13	
EN/UVLO Falling Threshold for Lowest Shutdown Current	V_{SD_F}		0.4	0.74		V
EN/UVLO Leakage Current	I_{ENLKG}		-0.6		0.6	μA
Output Supply (OUT)						
OUT Supply On-State Quiescent Current	$I_{Q_ON_OUT}$	OUT sourcing, $V_{EN} > V_{UVLO_R}$		184	450	μA
OUT Supply Off-State Current	$I_{Q_OFF_UVLO_OUT}$	OUT sourcing, $V_{SD_F} < V_{EN} < V_{UVLO_R}$		59	150	μA
OUT Supply Shutdown Current	I_{SD_OUT}	OUT sourcing, $V_{EN} < V_{SD_F}$		7	25	μA
Over-Voltage Lockout (OVLO)						
OVLO Rising Threshold	V_{OV_R}		1.185	1.21	1.23	V
OVLO Falling Threshold	V_{OV_F}		1.08	1.11	1.13	V
OVLO Leakage Current	I_{OVLKG}	V_{OVLO} = 0V to 5V	-0.1		0.1	μA
Over-Current Protection (OUT)						
Over-Current Threshold	I_{LIM}	R_{ILIM} = 2.43kΩ	1.85	2.06	2.26	A
		R_{ILIM} = 1.62kΩ	2.8	3.04	3.3	A
		R_{ILIM} = 604Ω	7.4	8	8.6	A
Circuit-Breaker Threshold	I_{nFAULT}	ILIM pin open			0.15	A
		ILIM pin shorted to GND		1.6	2	A
Adjustable Fast-Trip Comparator Threshold	I_{AFT}	ILIM ratio		200		%
Fixed Fast-Trip Comparator Threshold	I_{FFT}			25		A
V_{OUT} Threshold to Exit Current Limit Foldback	V_{FB}		1.4	1.9	2.4	V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, V_{IN} = 12V, OUT = open, $V_{EN/UVLO}$ = 2V, V_{OVLO} = 0V, R_{ILIM} = 536Ω, SS = open, ITIMER = open, SPGD = open, nFAULT = open for SGM2547AR, RCBCTRL = open for SGM2547CR. Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Over-Current Fault Timer (ITIMER)							
ITIMER Internal Pull-Up Voltage	V_{INT}			2.6	2.7	2.8	V
ITIMER Internal Pull-Up Resistance	R_{ITIMER}				16.5		kΩ
ITIMER Discharge Current, $I_{OUT} > I_{LIM}$	I_{ITIMER}			1.4	1.98	2.5	μA
ITIMER Discharge Differential Voltage Threshold	ΔV_{ITIMER}			1.45	1.6	1.75	V
Output Load Current Monitor (ILIM)							
Analog Load Current Monitor Gain	G_{IMON}	I_{MON}:I_{OUT}	I_{OUT} = 1A, $I_{OUT} < I_{LIM}$	113	127	141	μA/A
			I_{OUT} = 3A to 8A, $I_{OUT} < I_{LIM}$	123	133	143	μA/A
Reverse Current Blocking (IN - OUT)							
IN - OUT Forward Regulation Voltage	V_{FWD}	I_{OUT} = 10mA		0.4	6.5	20	mV
V_{IN} - V_{OUT} Threshold for Fast BFET Turn-Off	V_{REVTH}	Enter reverse current blocking		-50	-32	-9	mV
V_{IN} - V_{OUT} Threshold for Fast BFET Turn-On	V_{FWDTH}	Exit reverse current blocking		65	115	150	mV
Reverse Leakage Current during Reverse Current Blocking Condition	I_{REVLKG}	T_J = +25℃		-4.2	-0.1		μA
Supply Good Indication (SPGD)							
SPGD Low Voltage	V_{SPGD}	V_{IN} > 3.3V, and strong pull-up				150	mV
		V_{IN} < 3.3V, EN < V_{SD_F}, weak pull-up			525	800	mV
		V_{IN} < 3.3V, EN < V_{SD_F}, strong pull-up			650	900	mV
SPGD High Leakage Current	$I_{SPGDLKG}$			-3		3	μA
Fault Indication (nFAULT) or Reverse Current Blocking Control (RCBCTRL)							
nFAULT Leakage Current	$I_{FAULTBLKG}$			-1		1	μA
nFAULT Pin Internal Pull-Down Resistance	R_{nFAULT}				14.3		Ω
RCBCTRL Internal Pull-Up Current	$I_{RCBCTRL}$				7		μA
RCBCTRL Logic Detection Threshold	$V_{IH_RCBCTRL}$			1.1	1.15	1.2	V
	$V_{IL_RCBCTRL}$			0.9	1.01	1.1	V
Over-Temperature Protection (OTP)							
Thermal Shutdown Temperature	T_{SD}	T_J rising			155		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling			20		℃
Slew Rate Control (SS)							
SS Charging Current	I_{SS}				7.4		μA

TIMING REQUIREMENTS

(Typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Over-Voltage Lockout Response Time	t_{OVLO}	V_{OVLO} > V_{OV_R} to V_{OUT}↓		1.2		μs
Current Limit Response Time	t_{LIM}	I_{OUT} > 1.2 × I_{LIM} and ITIMER expired to I_{OUT} settling to within 5% of ILIM		200		μs
Scalable Fast-Trip Response Time (1)	t_{SC}	I_{OUT} > 3 × I_{LIM} to I_{OUT}↓		700		ns
Fixed Fast-Trip Response Time (1)	t_{FT}	I_{OUT} > I_{FFT} to I_{OUT}↓		600		ns
Auto-Retry Interval after Fault	t_{RST}			97		ms
OVLO Fast Recovery Response Time	t_{SWOV}	V_{OVLO} < V_{OV_F} to V_{OUT}↑		90		μs
Reverse Current Blocking Recovery Time	t_{SWRCB}	V_{IN} - V_{OUT} > V_{FWDTH} to V_{OUT}↑		50		μs
Reverse Current Blocking Comparator Response Time	t_{RCB}	V_{OUT} - V_{IN} > 1.3 × V_{REVTH} to BFET off		1.5		μs
Supply Good Assertion De-Glitch	t_{SPGDA}			20		μs
Supply Good De-Assertion De-Glitch	t_{SPGDD}			12.8		μs

NOTE: 1. Guaranteed by design.

SWITCHING CHARACTERISTICS

Over the entire normal operating voltage range, the output voltage's rise rate is fixed internally to ensure that the load conditions do not influence the startup sequence. Adding capacitance between the SS pin and GND can change the OUT rising slope. A larger C_{SS} value will reduce the slew rate (SR) of the output voltage. For further details on inrush current suppression (via the SS pin) and slew rate control, refer to the relevant sections.

(R_L = Open, C_{OUT1} = 1μF, C_{OUT2} = 0.1μF, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	V_{IN}	C_{SS} = Open	C_{SS} = 2.2nF	C_{SS} = 10nF	UNITS
Rise Time	t_R	5V	0.28	1.6	6.1	ms
		10V	0.38	3.2	13.6	
		20V	0.45	6.5	18.3	

FUNCTIONAL BLOCK DIAGRAM

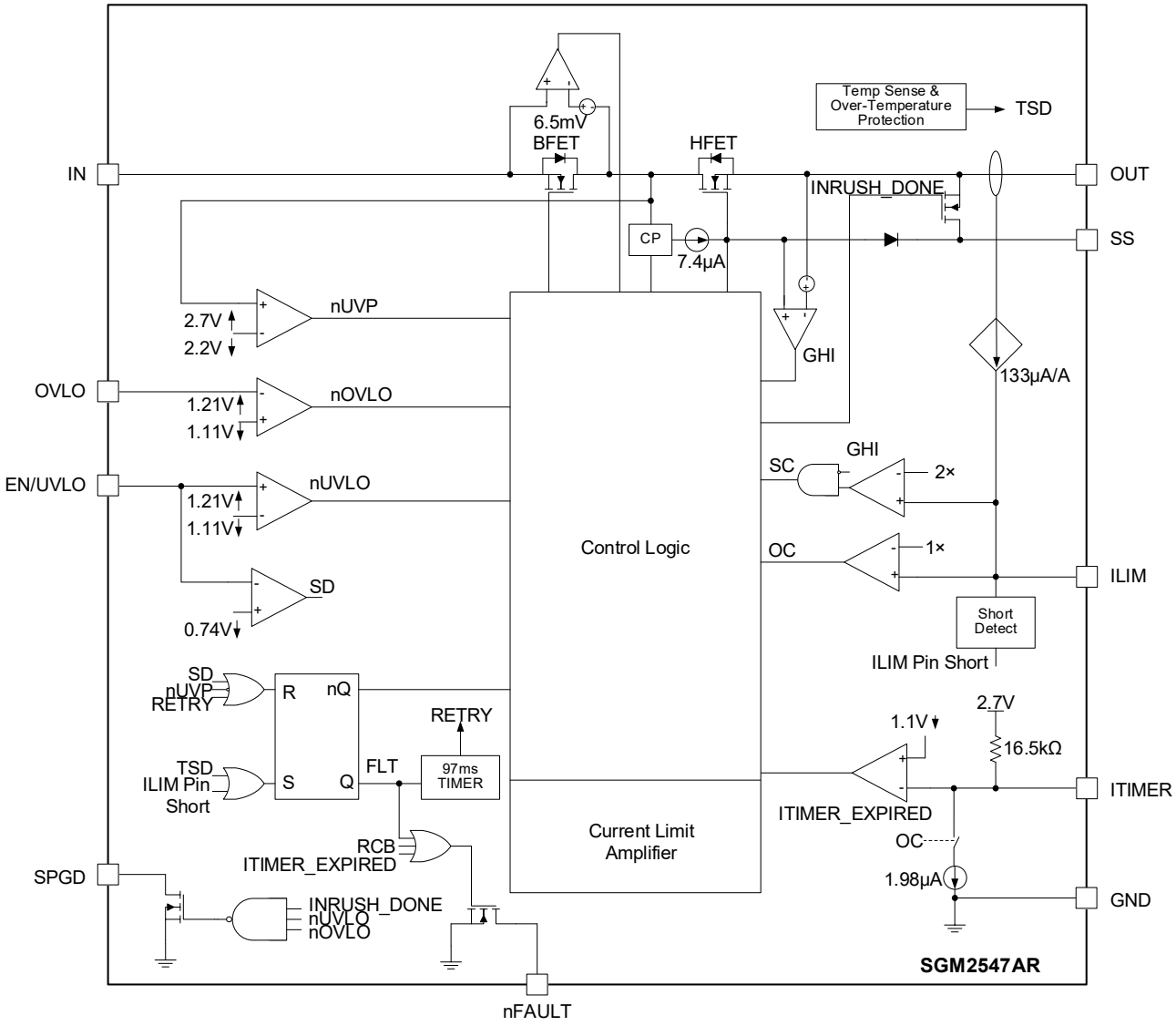


Figure 2. SGM2547AR Block Diagram

FUNCTIONAL BLOCK DIAGRAM (continued)

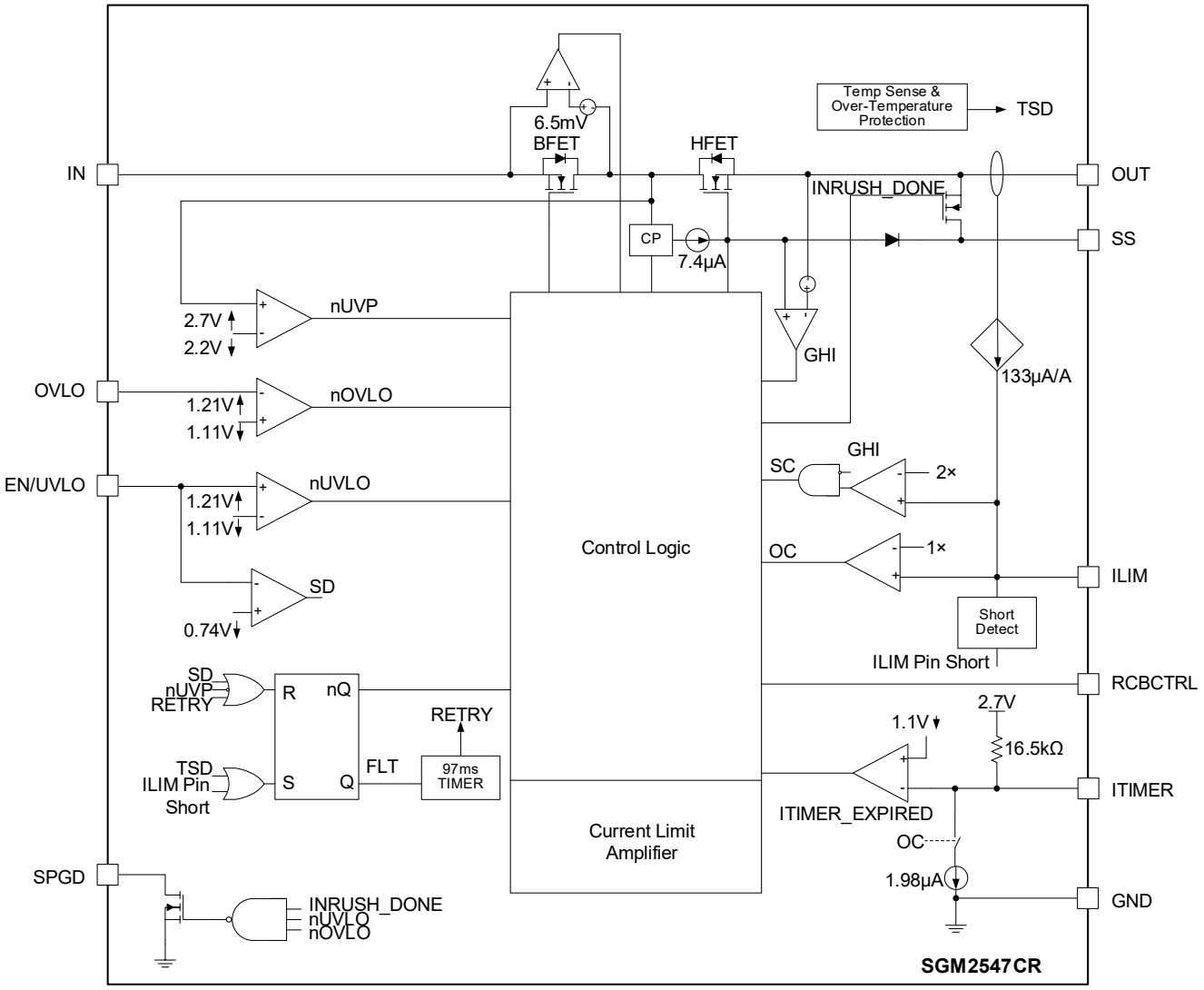
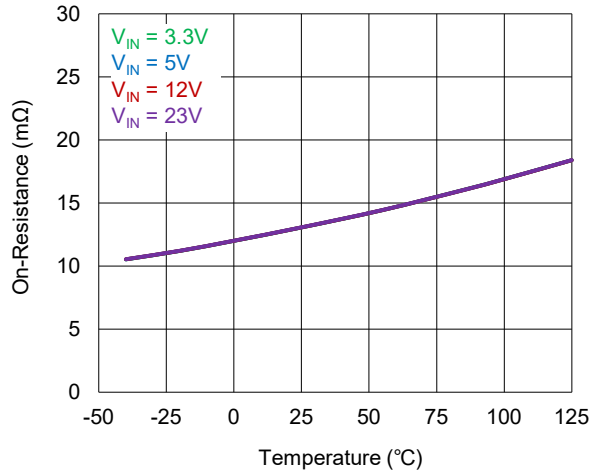


Figure 3. SGM2547CR Block Diagram

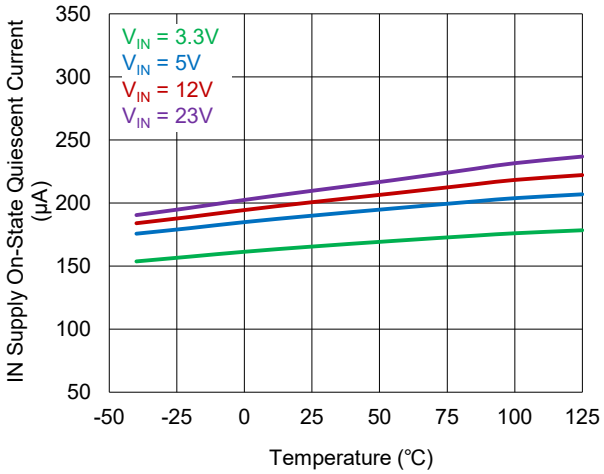
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

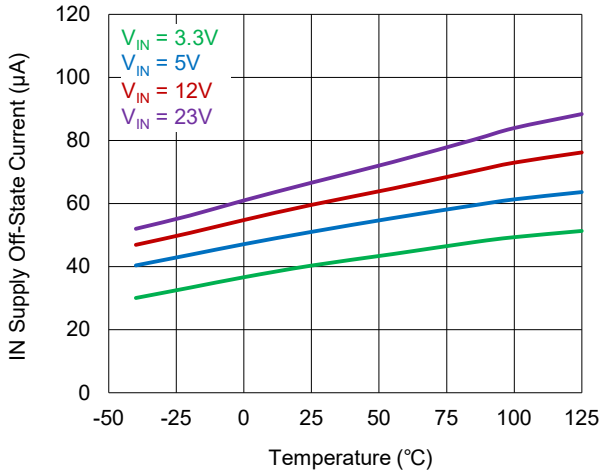
On-Resistance vs. Temperature



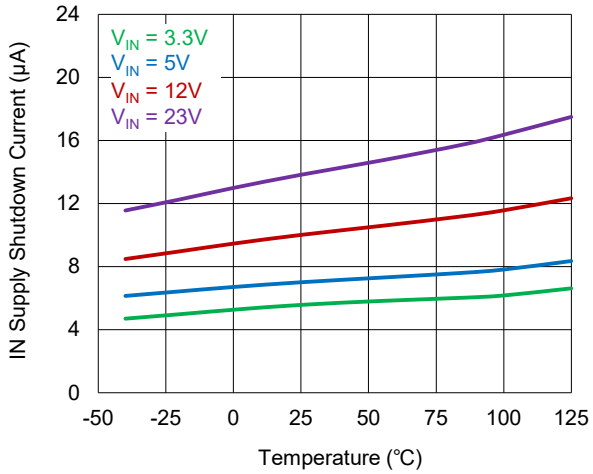
IN Supply On-State Quiescent Current vs. Temperature



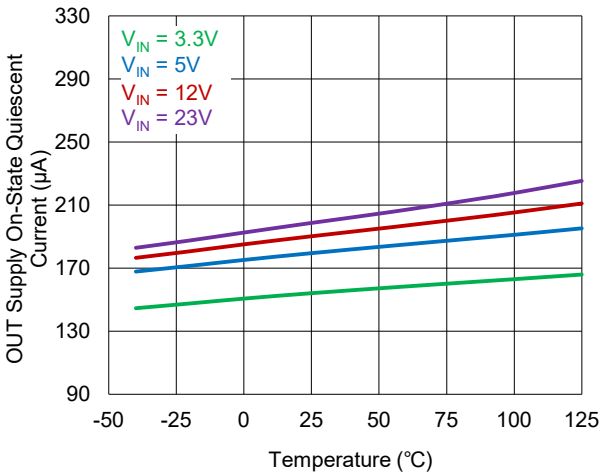
IN Supply Off-State Current vs. Temperature



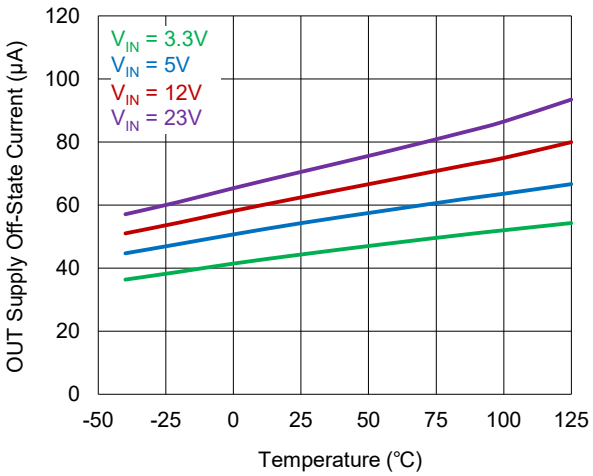
IN Supply Shutdown Current vs. Temperature



OUT Supply On-State Quiescent Current vs. Temperature



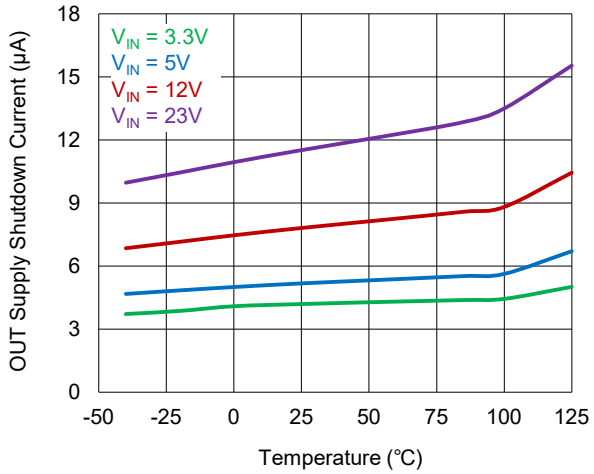
OUT Supply Off-State Current vs. Temperature



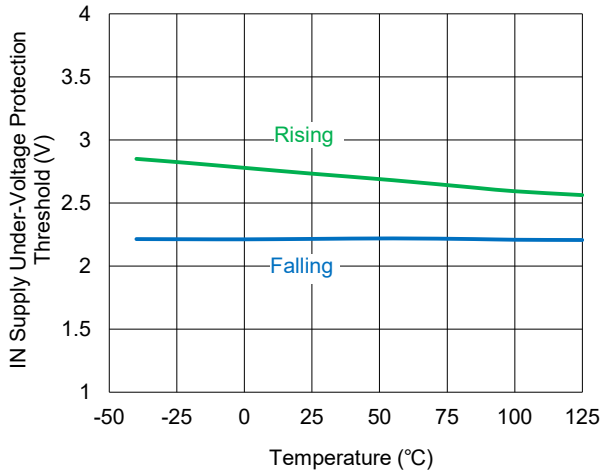
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

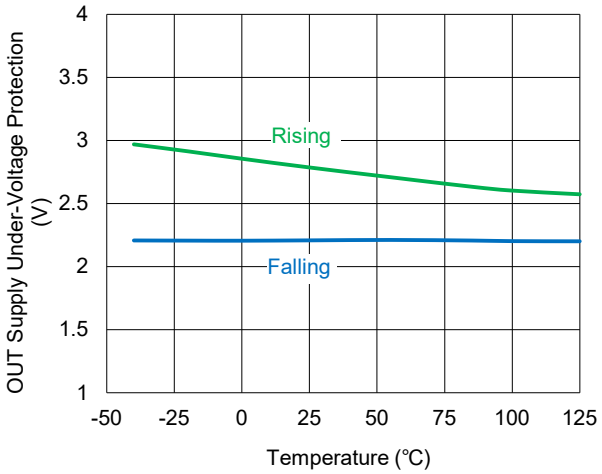
OUT Supply Shutdown Current vs. Temperature



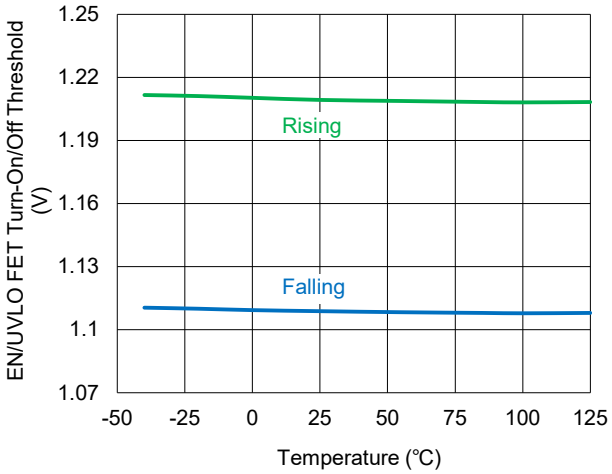
IN Supply Under-Voltage Protection Threshold vs. Temperature



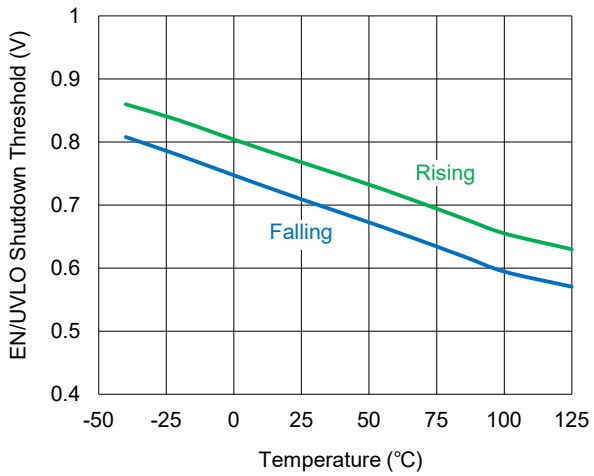
OUT Supply Under-Voltage Protection vs. Temperature



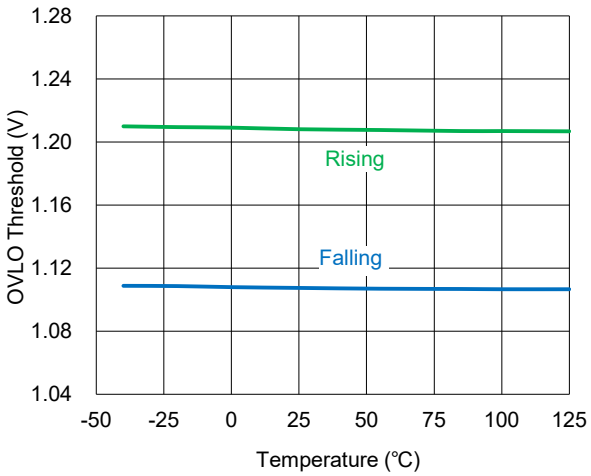
EN/UVLO FET Turn-On/Off Threshold vs. Temperature



EN/UVLO Shutdown Threshold vs. Temperature



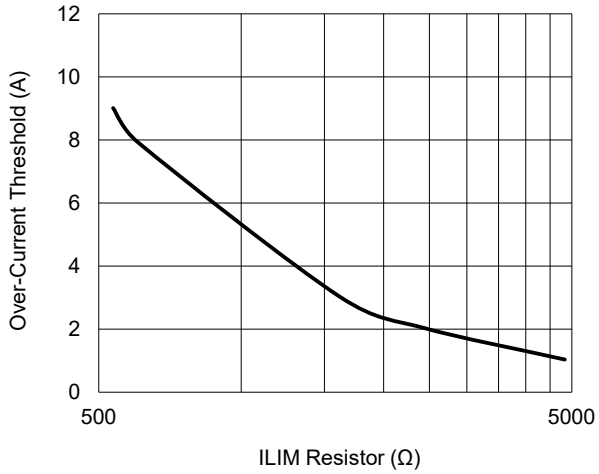
OVLO Threshold vs. Temperature



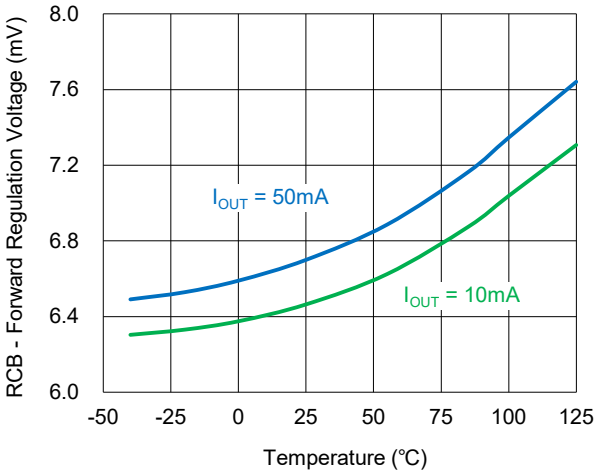
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

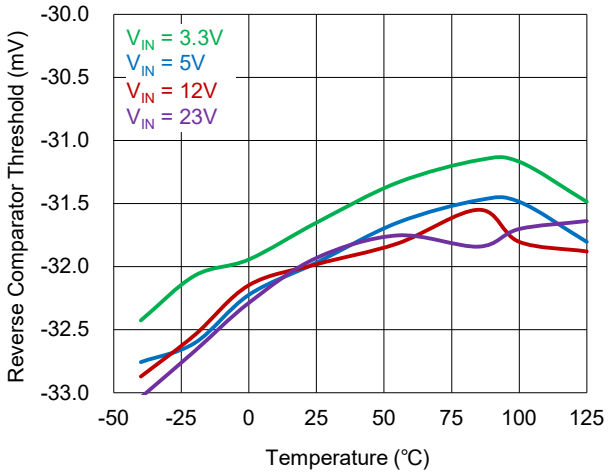
Over-Current Threshold vs. ILIM Resistor



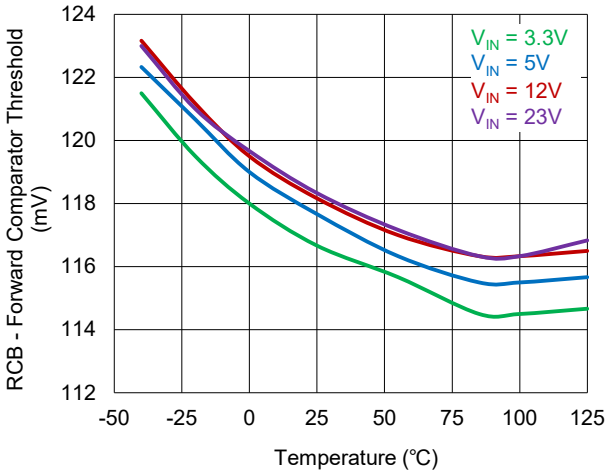
RCB - Forward Regulation Voltage vs. Temperature



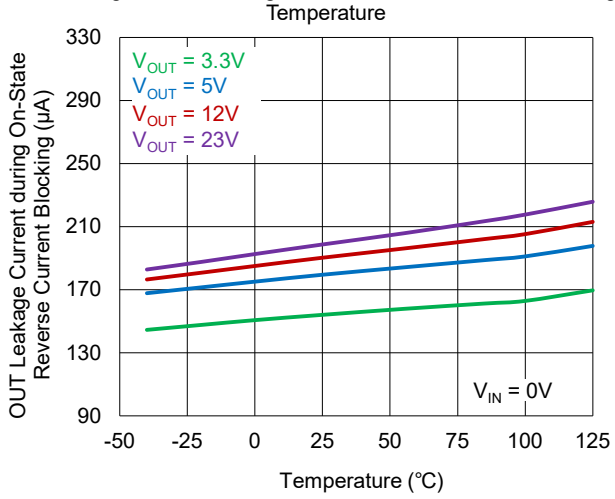
RCB - Reverse Comparator Threshold vs. Temperature



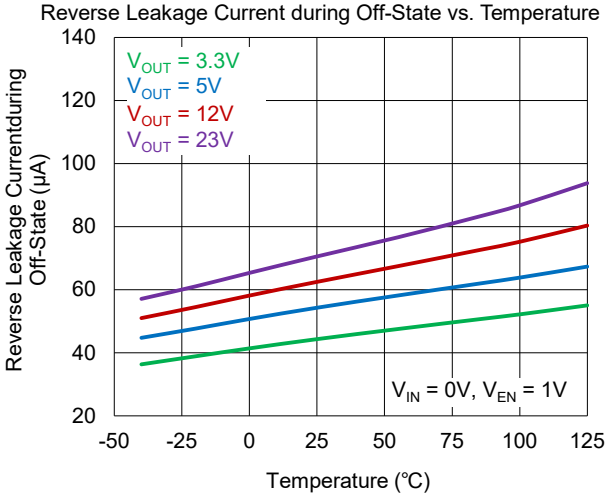
RCB - Forward Comparator Threshold vs. Temperature



OUT Leakage Current during On-State Reverse Current Blocking vs. Temperature



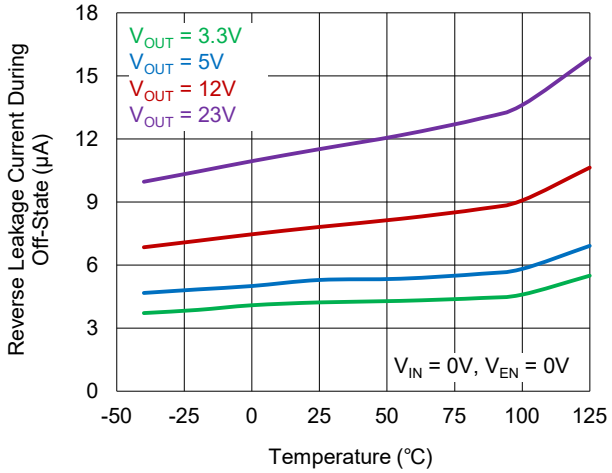
Reverse Leakage Current during Off-State vs. Temperature



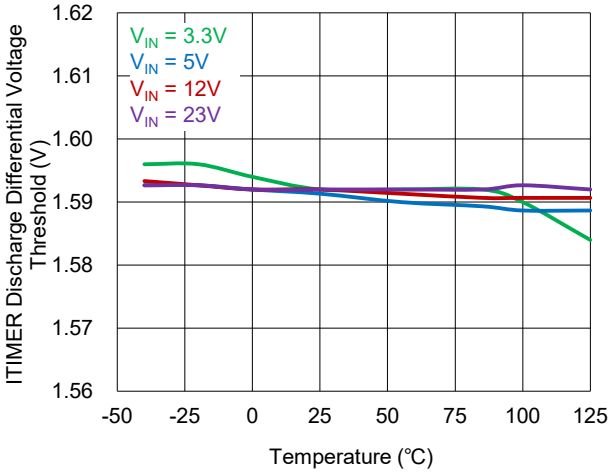
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

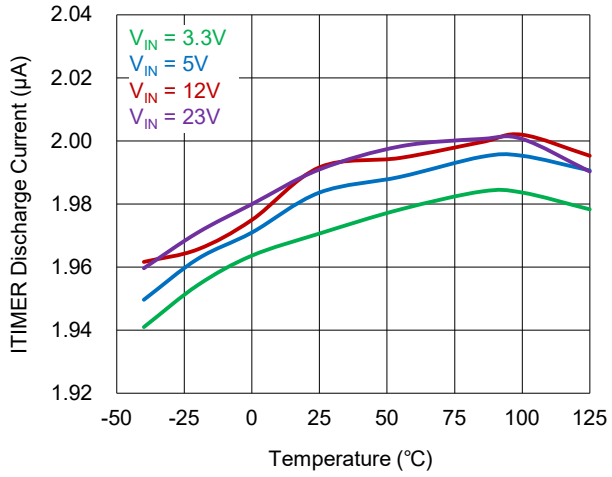
Reverse Leakage Current during Off-State vs. Temperature



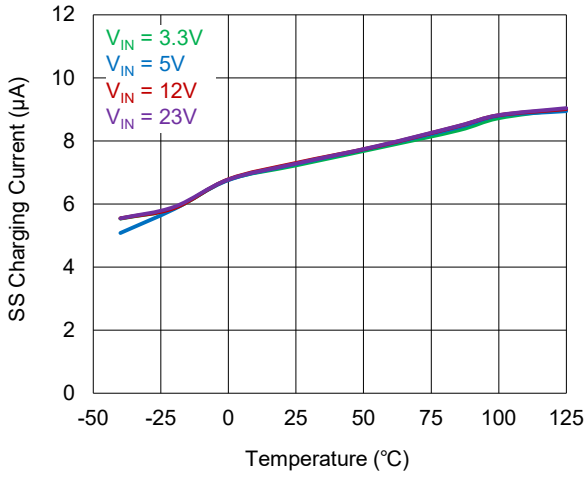
ITIMER Discharge Differential Voltage Threshold vs. Temperature



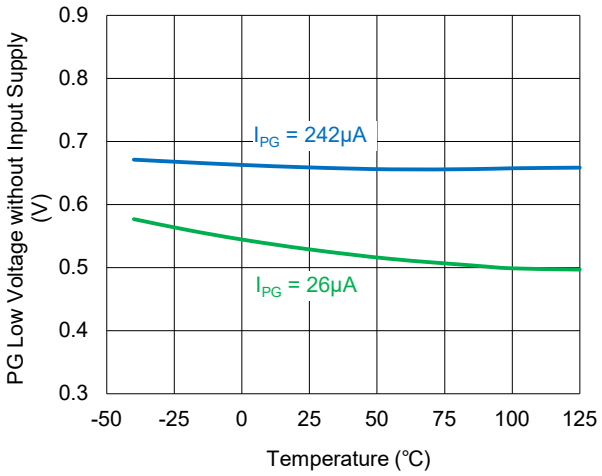
ITIMER Discharge Current vs. Temperature



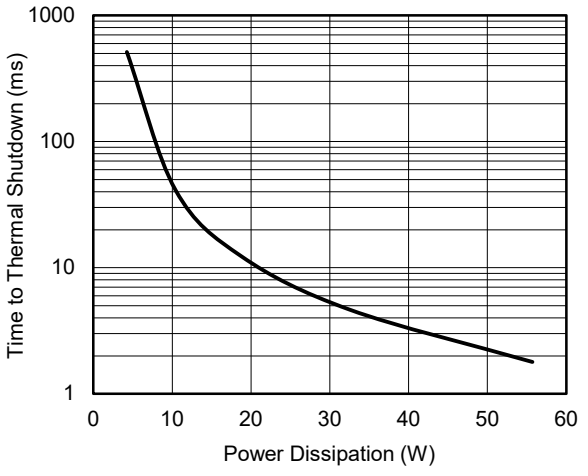
SS Charging Current vs. Temperature



PG Low Voltage without Input Supply vs. Temperature



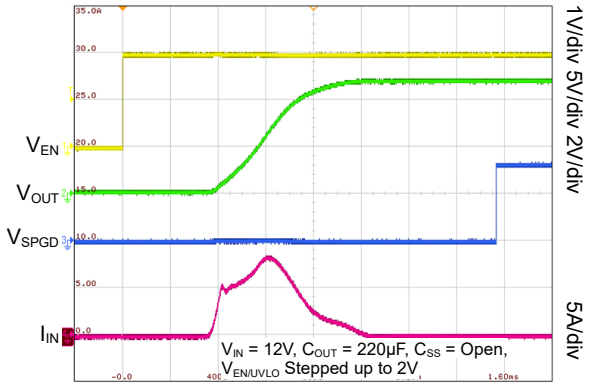
Time to Thermal Shutdown vs. Power Dissipation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

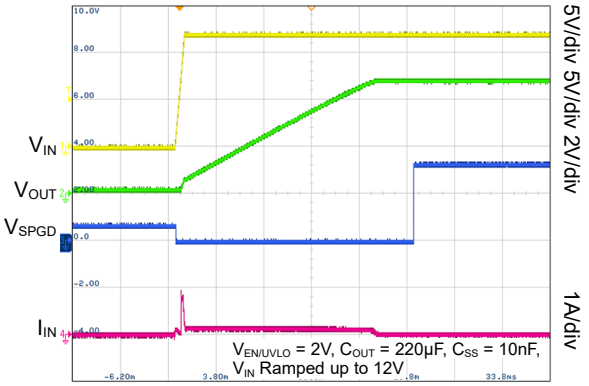
T_J = +25℃, unless otherwise noted.

Start-Up With Enable



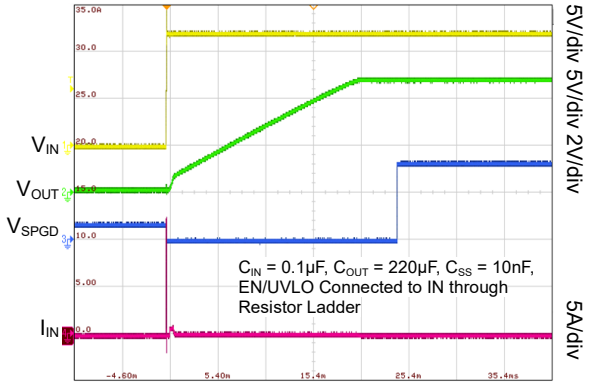
Time (200μs/div)

Start-Up With Supply



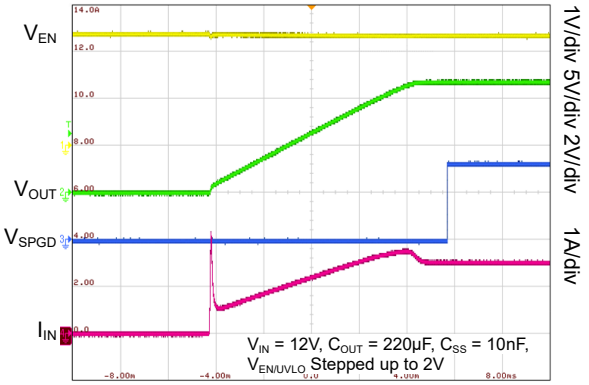
Time (5ms/div)

Input Hot-Plug



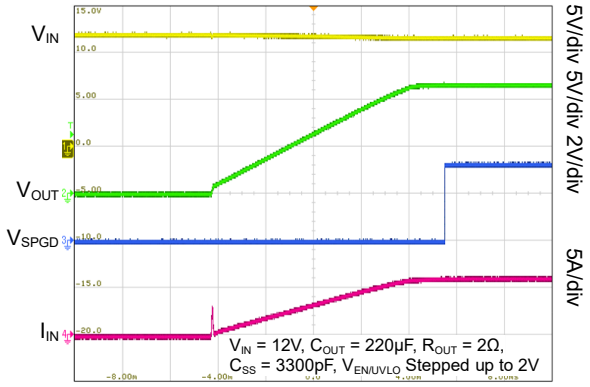
Time (5ms/div)

Inrush Current with Capacitive Load



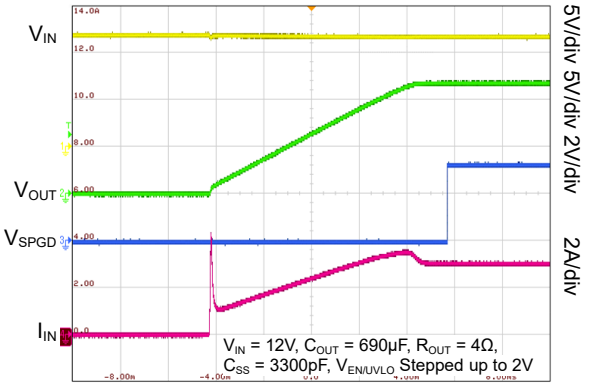
Time (5ms/div)

Inrush Current with Resistive and Capacitive Load



Time (2ms/div)

Inrush Current with Resistive and Capacitive Load

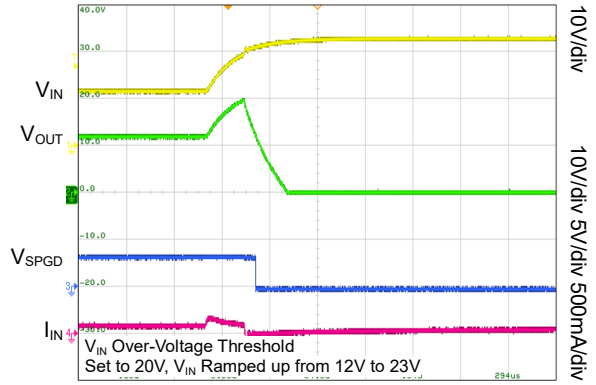


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

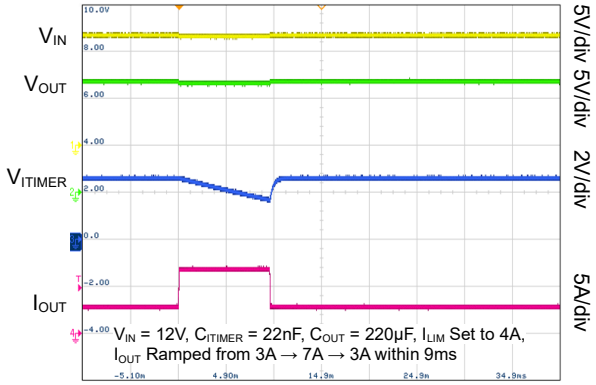
T_J = +25℃, unless otherwise noted.

Over-Voltage Lockout Response



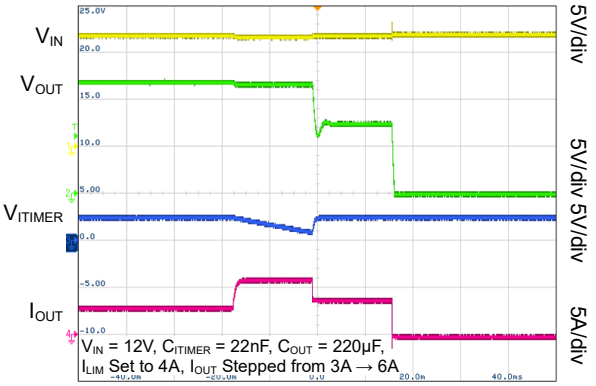
Time (50μs/div)

Transient Over-Current Blanking Timer Response



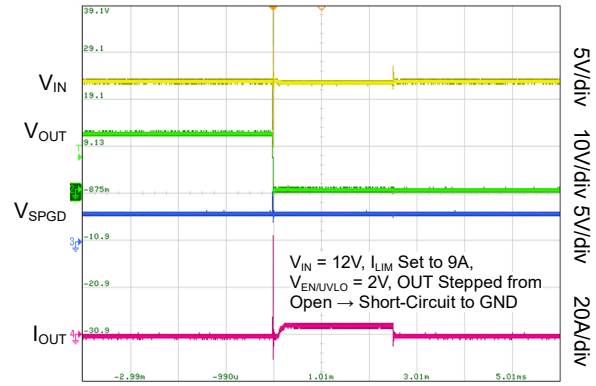
Time (5ms/div)

Active Current Limit Response Followed by TSD



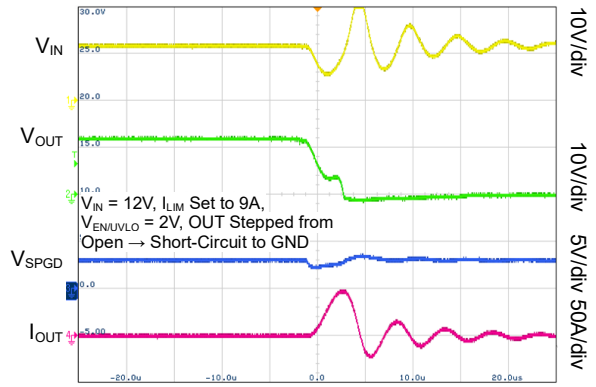
Time (10ms/div)

Output Short-Circuit during Steady State



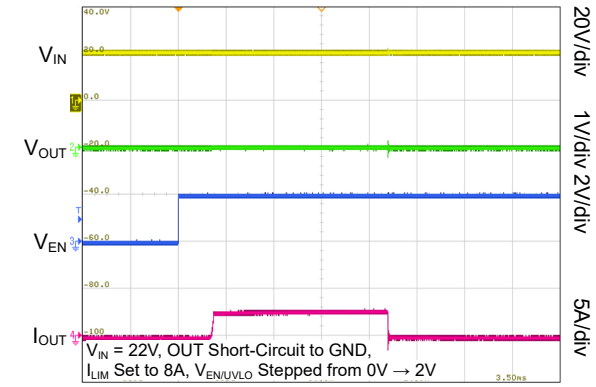
Time (1ms/div)

Output Short-Circuit during Steady State (Zoomed In)



Time (5μs/div)

Power-Up into Short-Circuit

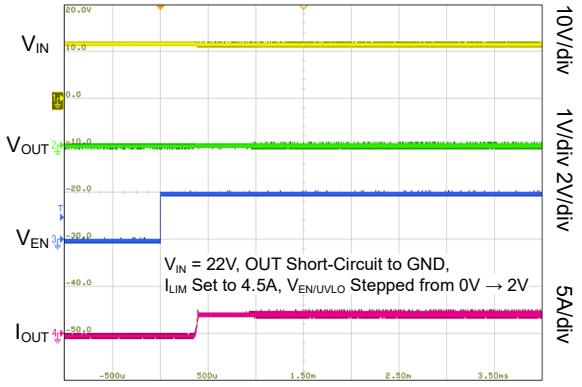


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

Power-Up into Short-Circuit



Time (500μs/div)

DETAILED DESCRIPTION

Overview

SGM2547 is an eFuse with internal integration of back-to-back FETs (BFET + HFET). It ensures the safety of the power delivery system due to its rich features. When the V_{IN} is greater than V_{UVP_R}, the device starts to sample the voltage of the EN/UVLO pin ($V_{EN/UVLO}$). If $V_{EN/UVLO}$ exceeds V_{UVLO_R}, BFET and HFET start to operate, and current can flow from the input to the output. When the V_{IN} is less than V_{UVP_F} or $V_{EN/UVLO}$ < V_{UVLO_F}, both BFET and HFET are turned off to realize the reverse current blocking.

After device start-up, the SGM2547 will monitor the V_{IN} and forward current (from IN to OUT). By controlling HFET, the load current cannot exceed the set current limit threshold (I_{LIM}), and over-voltage spikes are cut-off if they exceed the user-adjustable over-voltage lockout threshold (V_{OVLO}). The fast-trip response of the device can provide rapid protection against serious over-current during short-circuit of OUT pin, so as to prevent the system from being damaged by harmful voltage and current. In addition, the device also provides a user-adjustable over-current blanking timer to allow short-time over-current in the power path without tripping the device frequently. Therefore, SGM2547 not only provides complete protection functions, but also ensures the maximum system uptime during transient events.

The device incorporates a built-in reverse current blocking FET (BFET) that functions similarly to an ideal diode. During forward conduction, the BFET is linearly controlled to sustain a low and stable forward voltage drop (V_{FWD}). When the output voltage rises above the input voltage, the BFET is fully turned off to prevent reverse current flow. SGM2547CR is equipped with external control pin (RCBCTRL) which is used to disable the reverse current blocking function, thereby enabling bidirectional current flow. This feature is crucial for applications such as USB on-the-go (OTG) or dual-role ports (DRP), where dynamic role switching between power supply and load needs to be achieved.

There is an integrated thermal sensor to protect itself when the device temperature exceeds the T_{SD}.

Under-Voltage Lockout (UVLO and UVP)

The SGM2547 implements under-voltage protection at IN pin to prevent IN voltage from being too low for normal operation of system and equipment. A fixed locking threshold voltage (V_{UVP}) is provided inside the device for under-voltage protection. In addition, the comparator on the EN/UVLO terminal can be used to set the user-adjustable under-voltage protection threshold through the external resistor divider. Figure 4 and Equation 1 show how to set the specific value of under-voltage protection threshold using an external resistor divider.

$$V_{IN_UV} = \frac{V_{UVLO_F} \times (R_1 + R_2)}{R_2} \quad (1)$$

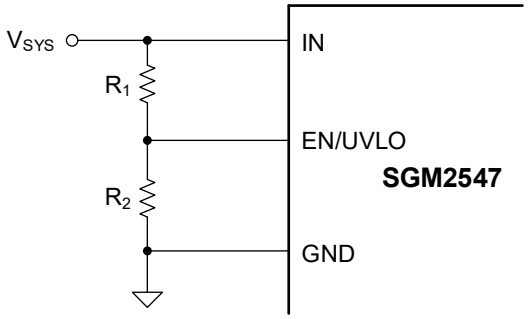


Figure 4. Adjustable Under-Voltage Lockout

Over-Voltage Lockout (OVLO)

The SGM2547 implements over-voltage lockout at OVLO pin to prevent IN voltage from being too high for normal operation of system and equipment. The comparator on the OVLO pin is used to set the user-adjustable over-voltage protection threshold through the external resistor divider. If the voltage of OVLO pin exceeds the V_{OVLO_R}, the device will shut down the power path. When the voltage of OVLO pin is lower than the V_{OVLO_F}, the power path will be reopened with inrush control. There is a hysteresis between the rising threshold and falling threshold of OVLO. The Equation 2 and Figure 5 show how to set the specific value of over-voltage protection threshold using an external resistor divider.

$$V_{IN_OV} = \frac{V_{OVLO} \times (R_1 + R_2)}{R_2} \quad (2)$$

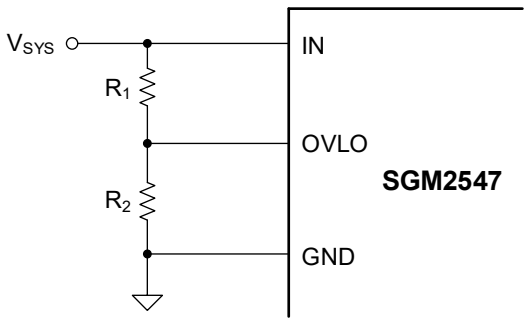


Figure 5. Adjustable Over-Voltage Lockout

DETAILED DESCRIPTION (continued)

During recovery from an OVLO (over-voltage lockout) event, the SGM2547 employs a unique startup strategy that bypasses the conventional soft-start (SS) inrush current control mechanism. This design approach enables the system to initiate operation with current limit characteristics, achieving dual benefits: significantly reduced turn-on time and effective mitigation of power supply voltage dips during transient conditions.

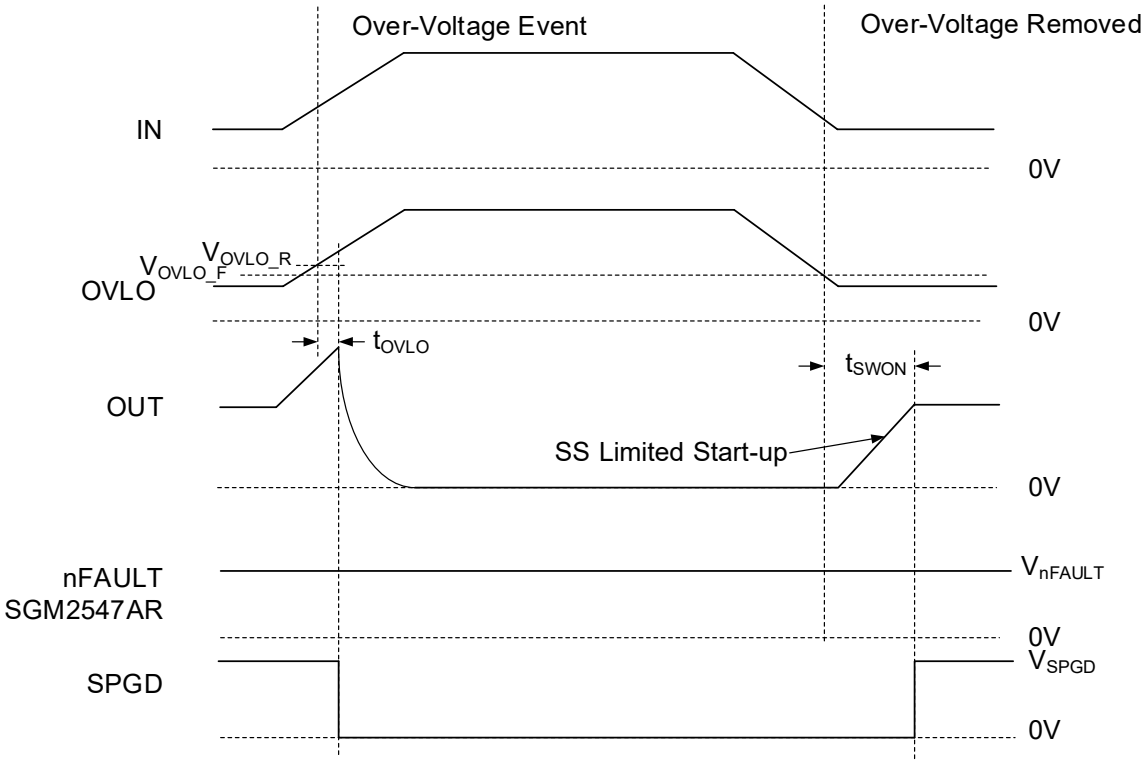


Figure 6. Over-Voltage Lockout and Recovery

Inrush Current, Over-Current, and Short-Circuit Protection

SGM2547 adopts four levels of forward over-current protection function:

- Programmable slew rate (SR) for inrush current protection.
- Programmable current limit threshold (I_{LIM}) for over-current in steady state or start-up.
- Programmable threshold (I_{SC}) for severe over-current in steady state or start-up.
- Fixed I_{FT} for fast-trip function when short-circuit of OUT occurs.

Slew Rate (SR) and Inrush Current Protection

When hot-plug or system charging large capacitive load occurs, a large inrush current is generated in the equipment power path. The input connector may be damaged or the input power rail voltage may drop, which affects the normal operation and even restarts other equipment in the system.

For a given C_{OUT}, the relationship between the slew rate (SR) and inrush current (I_{INRUSH}) is shown in Equation 3.

$$SR\ (V/ms) = \frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)} \quad (3)$$

The slew rate can be controlled by connecting a capacitor at the SS pin to reduce inrush current. For a given slew rate, the corresponding C_{SS} can be calculated by Equation 4. When the SS pin is left floating, the fastest output slew rate can be obtained.

$$C_{SS}\ (pF) = \frac{7000}{SR\ (V/ms)} \quad (4)$$

NOTE: For C_{SS} > 10nF, a 100Ω resistor is recommended to be in series with the C_{SS} on the SS pin.

DETAILED DESCRIPTION (continued)

Current Limit

When an output over-current condition occurs, the device actively limits the current after the blanking timer expires. If the load current exceeds the overcurrent threshold (I_{LIM}) but remains below the short-circuit threshold (2 × I_{LIM} or I_{FFT}), the device discharges the C_{ITIMER} voltage at the ITIMER pin using an internal 1.98μA sink current source. If the load current drops below the over-current threshold before the C_{ITIMER} voltage has decreased by ΔV_{ITIMER}, the ITIMER pin is internally pulled high to V_{INT}, and current limiting is not triggered. If the overcurrent condition persists after the C_{ITIMER} voltage has dropped by ΔV_{ITIMER}, the device regulates the HFET to clamp the current at the overcurrent threshold. Additionally, this clamping is subject to a power limitation: when the product of the input-output voltage differential (V_{IN} - V_{OUT}) and the I_{OUT} exceeds the typical 55W threshold (i.e., (V_{IN} - V_{OUT}) × I_{OUT} > 55W), the clamping IOUT is reduced to maintain the total power at 55W (TYP) ITIMER pin is then recharged to V_{INT}, resetting its state before the next overcurrent event to ensure full blanking time for subsequent occurrences. This mechanism provides overcurrent protection while allowing transient current pulses to pass through the power path. For a given over-current threshold, the value of the R_{ILIM} resistor (Equation 5) can be calculated to configure the current limit.

$$R_{ILIM}(\Omega) = \frac{3960}{I_{LIM}(A)^{0.972}} \quad (5)$$

NOTES:

1. The SGM2547 is limited by 2 × I_{LIM} for the ITIMER duration.
2. Leave the ILIM pin floating to set the over-current threshold near zero, and the device can hardly be loaded.
3. The current limit circuit implements the fold-back mechanism. In the fold-back region (0V < V_{OUT} < V_{FB}), the current limit threshold (I_{LIM}) is smaller than the current limit threshold under steady state.
4. When the ILIM is short to the GND under normal operations, it will be detected as a fault case. There is a minimum I_{nFAULT} which the device allows in this case before the pin short condition is detected.

The blanking time can be adjusted by changing the capacitance connected to the ITIMER pin. Over-current blanking time can be calculated by Equation 6.

$$t_{ITIMER}\ (ms) = \frac{\Delta V_{ITIMER}\ (V) \times C_{ITIMER}\ (nF)}{I_{ITIMER}\ (\mu A)} \quad (6)$$

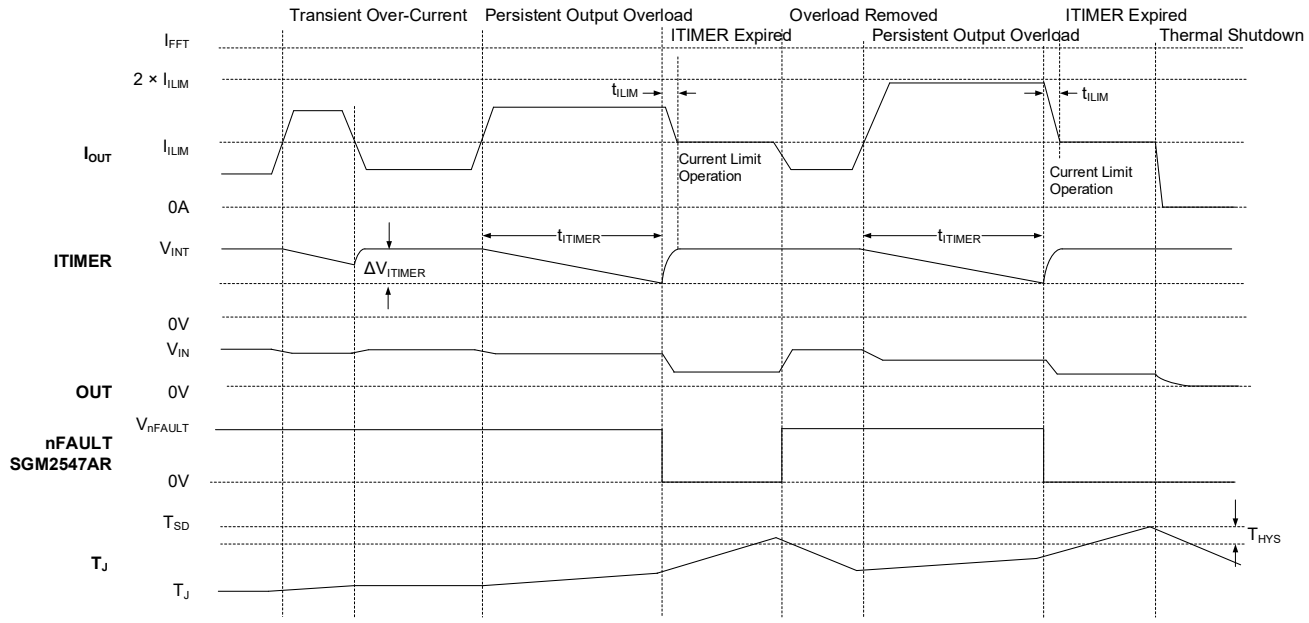


Figure 7. Current Limit Response

DETAILED DESCRIPTION (continued)

NOTES:

1. Leaving the ITIMER pin floating or short to GND sets the minimum over-current blanking time. But it is not recommended to leave ITIMER pin short to GND, because it increases the current consumption of the device.

2. The active current limit set by R_{ILIM} is still valid during start-up, which ensures that the load current does not exceed I_{LIM} during start-up. However, there is no over-current blanking time in the start-up process.

3. Increasing C_{ITIMER} can increase the over-current blanking time, but it also increases the time for C_{ITIMER} to charge to V_{INT}. If the next over-current case occurs before the C_{ITIMER} is fully charged to the V_{INT}, the current blanking time of this event will be shorter than intended.

During the activation of current limiting, the output voltage will drop. This is because the field-effect transistor (HFET) will consume more power. If the internal temperature of the device exceeds the limit temperature (T_{SD}), this field-effect transistor will be turned off. The device will automatically restart after a certain time interval.

Short-Circuit Protection

When a serious over-current event similar to a short-circuit event occurs, the SGM2547 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device.

For the SGM2547AR and SGM2547CR, the fast-trip comparator with scalable threshold (I_{SC} = 2 × I_{LIM}) is adopted inside the device, which allows users to program the fast-trip threshold in low current system. A fixed fast-trip threshold is also set inside the device for fast protection against hard short-circuit events in steady state. It is recommended that the fixed fast-trip threshold be greater than the maximum value of the scalable fast-trip threshold.

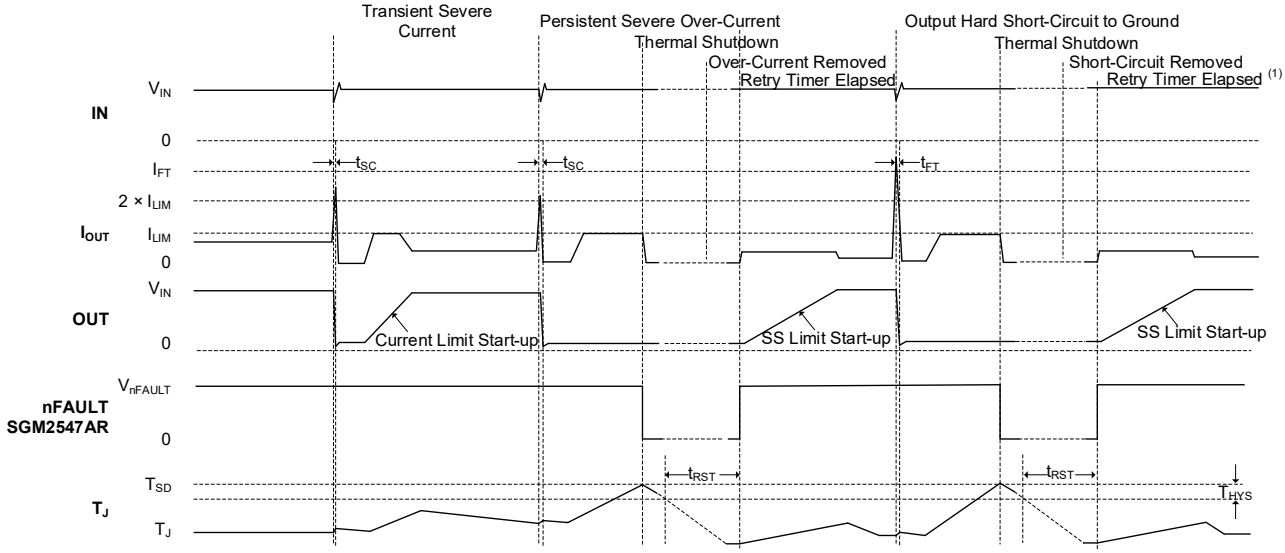


Figure 8. Short-Circuit Response

Load Current Monitor Output

The device provides an analog current sensing output proportional to the load current at the ILIM pin, which enables the device to monitor the load current (from IN to OUT). The user can calculate the load current through the voltage of the ILIM pin connected to the R_{ILIM}. The relationship between V_{ILIM} and I_{OUT} is shown in Equation 7.

$$I_{OUT}\ (A) = \frac{V_{ILIM}\ (\mu V)}{R_{ILIM}\ (\Omega) \times G_{IMON}\ (\mu A/A)} \quad (7)$$

NOTE: ILIM pin is sensitive to capacitive loads. In order to ensure the normal operation of the device, the parasitic capacitance of the ILIM pin needs to be less than 50pF.

DETAILED DESCRIPTION (continued)

Reverse Current Protection

The SGM2547 operates in ideal diode mode, preventing reverse current from flowing from the OUT to IN terminals under all operating conditions. This functionality is achieved through a common-source topology integrating back-to-back MOSFETs. By continuously monitoring the voltage drop between the IN and OUT pins, the chip dynamically adjusts the blocking FET (BFET)'s gate drive voltage, enabling precise regulation of the forward conduction voltage (V_{FWD}). The closed-loop linear ORing control scheme ensures smooth MOSFET turn-off during reverse current events while maintaining near-zero DC reverse current.

To address transient reverse currents, the device incorporates a traditional comparator-based reverse blocking mechanism (V_{REVTH}), which provides a nanosecond-level response time (t_{RCB}). Upon detecting a reverse current condition, the device holds the blocking state until the forward voltage differential (V_{IN} - V_{OUT}) exceeds the preset threshold (V_{FWDTH}), at which point it triggers a rapid recovery process (t_{SWRCB}) to restore full forward conduction. This hysteresis mechanism suppresses interference from supply noise or ripple in the reverse protection circuit.

The fast recovery capability significantly reduces supply voltage droop, making the device ideal for applications such as power multiplexing/ORing and USB fast role swap (FRS), where quick transitions and stable voltage delivery are critical.

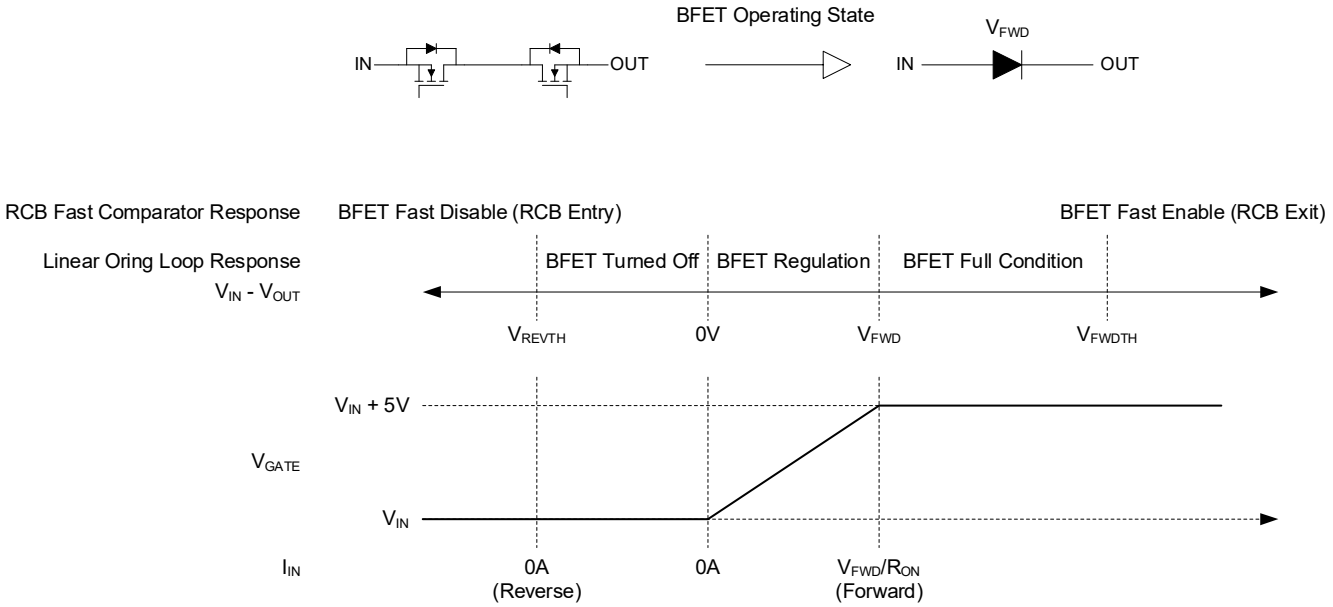


Figure 9. Reverse Current Blocking Response

The subsequent waveforms demonstrate the device's reverse current blocking capability across various operating scenarios.

During a sudden voltage transition at the output, such as during a hot-plug event, the fast-comparator-based reverse blocking mechanism suppresses voltage spikes and minimizes glitches on the input rail, maintaining stable voltage regulation.

DETAILED DESCRIPTION (continued)

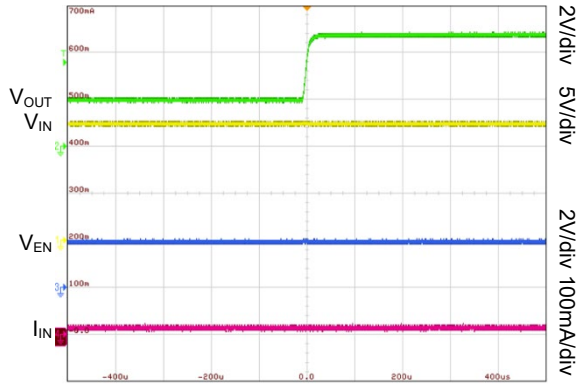


Figure 10. Reverse Current Blocking Performance during Fast Voltage Step at Output

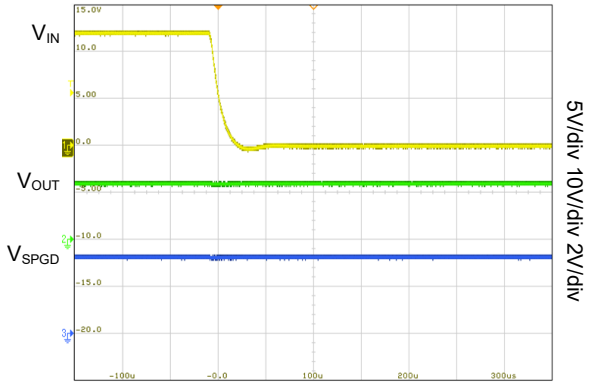


Figure 11. Reverse Current Blocking Performance during Input Supply Failure

During a gradual voltage ramp-up at the output, the linear-ORing-based reverse blocking mechanism suppresses DC current flow from output to input to near-zero levels, thereby preventing the input rail from gradually charging toward the output voltage and maintaining stable input voltage regulation.

When the input supply voltage droops or becomes disconnected while the output storage element (bulk capacitor or super capacitor) is fully charged, the linear-ORing-based scheme suppresses reverse self-discharge currents from the output (OUT) to the input (IN). This maximizes the hold-up time of the storage element in critical power-backup applications by maintaining its energy capacity. Additionally, the mechanism prevents erroneous supply presence indications in systems that rely on input voltage sensing to detect active power connections, thereby ensuring reliable system operation during backup modes.

Over-Temperature Protection (OTP)

The SGM2547 always monitors the temperature (T_J) of the internal die. Once the internal temperature exceeds the T_{SD}, the device shuts down immediately. The SGM2547 will not turn on until the internal temperature is lower than a safe threshold (T_{SD} - T_{HYS}).

When SGM2547 triggers the thermal shutdown, it remains in the shutdown state until the internal temperature of the equipment drops by T_{HYS}. After that, it will retry to turn on automatically after a t_{RST} delay time if the device is still enabled.

Table 1. Thermal Shutdown

Device	Enter T_{SD}	Exit T_{SD}
SGM2547xR	$T_J \geq T_{SD}$	$T_J < T_{SD}$ - T_{HYS}, $V_{IN} < V_{UVP_F}$, or $V_{EN} < V_{SD_F}$, or t_{RST} timer expired

Fault Response and Indication (nFAULT)

Table 2 shows the protection response of equipment under different fault conditions. The SGM2547AR provides an active-low external fault flag pin.

DETAILED DESCRIPTION (continued)

Table 2. Fault Summary

Event	Protection Response	Fault Latched Internally	nFAULT Pin Status (1)	nFAULT Assertion Delay (1)
Over-Temperature	Shutdown	Y	L	
Under-Voltage (UVP or UVLO)	Shutdown	N	H	
Over-Voltage	Shutdown	N	H	
Transient Over-Current (I_{LIM} < I_{OUT} < 2 × I_{LIM} or I_{FFT} for duration less than t_{ITIMER})	None	N	H	
Continuous Over-Current Condition	Current Limit	N	L	t_{ITIMER}
Output Port Short-Circuited to GND	Current Limit Function After Circuit Breaker Activation	N	H	
ILIM Pin Open (During Steady State)	Shutdown	N	L	I_{OUT} > 100mA Shutdown
ILIM Pin Shorted to GND	Shutdown	Y	L	
Reverse Current (V_{OUT} - V_{IN} > V_{REVTH})	Reverse Current Blocking	N	L	

NOTE: 1. SGM2547AR only.

A latched fault can be cleared by power cycling (pulling V_{IN} to 0V) or re-enable (pulling EN/UVLO pin below V_{SD}). This will also reset the t_{RST} in SGM2547. It is worth mentioning for the SGM2547AR, pulling down EN/UVLO below the UVLO threshold cannot clear the latched fault. The SGM2547 will retry automatically after the t_{RST} timer expiring when a fault has occurred.

Input Supply Good Indication (SPGD)

The SGM2547 provides an active-high open-drain output (SPGD) as a supply valid status indication to the downstream load or system supervisor. SPGD is asserted when the IN voltage is in a proper range (UVP/UVLO < V_{IN} < OVLO) and the inrush sequence of the device is completed. SPGD pin needs to be pulled up to an external power supply. For the SGM2547AR/SGM2547CR, SPGD is an active-high output.

Upon power-up, the SPGD pin is initially de-asserted, and the device initiates an inrush current control sequence by gradually turning on the high-side FET (HFET). Once the FET gate voltage reaches full overdrive, signifying completion of the inrush sequence and readiness to deliver full power, the SPGD pin is asserted. Thereafter, this pin remains asserted unless the input supply voltage falls below the UVP/UVLO threshold or exceeds the OVLO threshold; load-side events or faults have no influence on its de-assertion. The pin serves dual purposes: it controls the auxiliary channel in a priority power multiplexer (MUX) configuration when two SGM2547 devices are interconnected, and it indicates supply validity to downstream loads or system supervisors as a status signal.

DETAILED DESCRIPTION (continued)

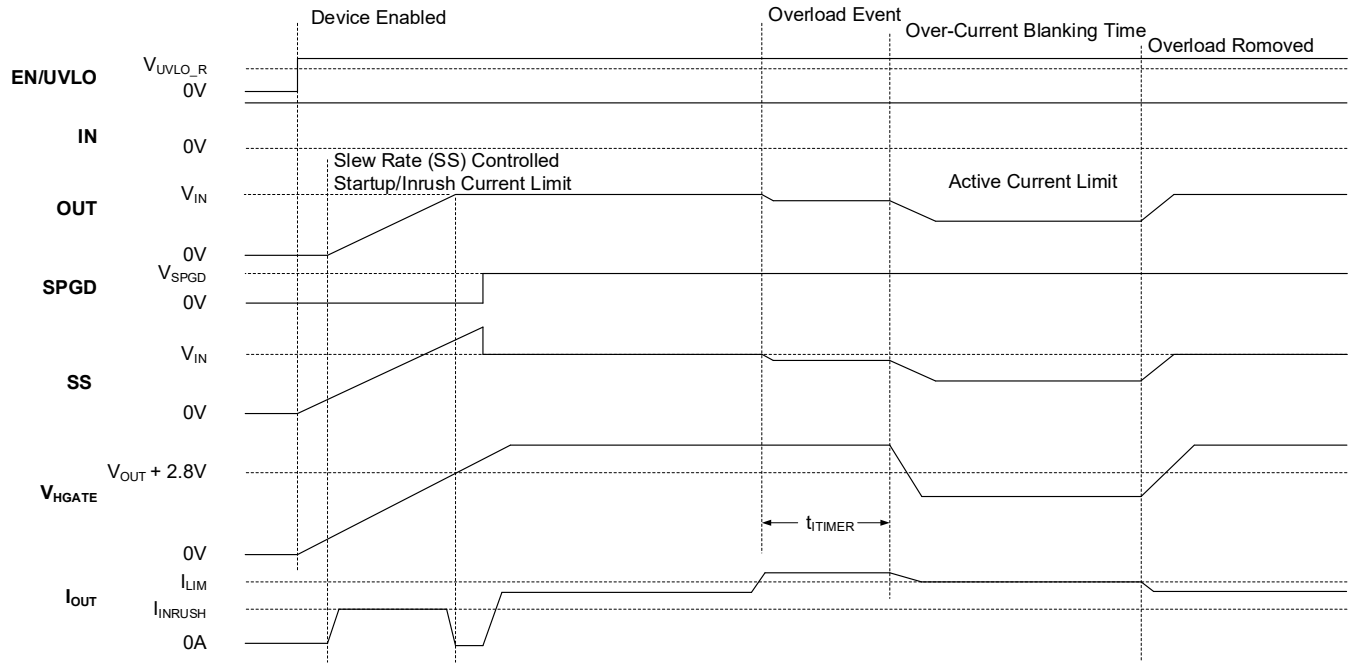


Figure 12. SPGD Timing

Table 3. SGM2547 SPGD Indication

Event/Condition	SPGD Pin
Supply Brownout (UVP)	L
Shutdown (V_{EN} < V_{SD})	L
Under-Voltage (UVLO)	L
Over-Voltage (OVLO)	L
Inrush	L
Steady State	H
Over-Current	H
Short-Circuit	H
ILIM Pin Open	H
ILIM Pin Shorted to GND	H
Reverse Current (V_{OUT} – V_{IN} > V_{REVTH})	H
Over-Temperature	H

When SGM2547 is unpowered, the SPGD pin remains in a low state but lacks an active pull-down to ensure it reaches 0V. If the pin is connected to an independent supply via a pull-up resistor even when unpowered, a small voltage may appear depending on its sink current, which is determined by the pull-up voltage and resistor values. To ensure the voltage stays below logic-high thresholds for external circuits (thus avoiding unintended shutdown of the auxiliary channel in a priority power multiplexer configuration), minimize the sink current to keep the SPGD signal undetectable as an active high in this condition.

Device Functional Modes

Table 4. SGM2547CR Reverse Current Blocking Operation

RCBCTRL Pin Connection	Reverse Current Blocking in Steady-State
Low	Disabled
Open or High	Enabled

APPLICATION INFORMATION

The SGM2547 is a 3.3V to 23V, 8A electronic fuse (eFuse) designed to protect power rails across a wide range of applications. Operating within the 3.3V to 23V voltage range, it provides programmable over-voltage and under-voltage protection while controlling inrush current. Additionally, it incorporates an ideal diode function to safeguard against reverse current conditions. This device is commonly deployed in systems such as adapter/charger input protection, USB PD protection for smartphones, tablets, PCs, notebooks, monitors, docks, servers, and motherboards, as well as enterprise storage solutions (RAID, HBA, SAN, eSSD) and power multiplexing (ORing) systems.

Single Device, Self-Controlled

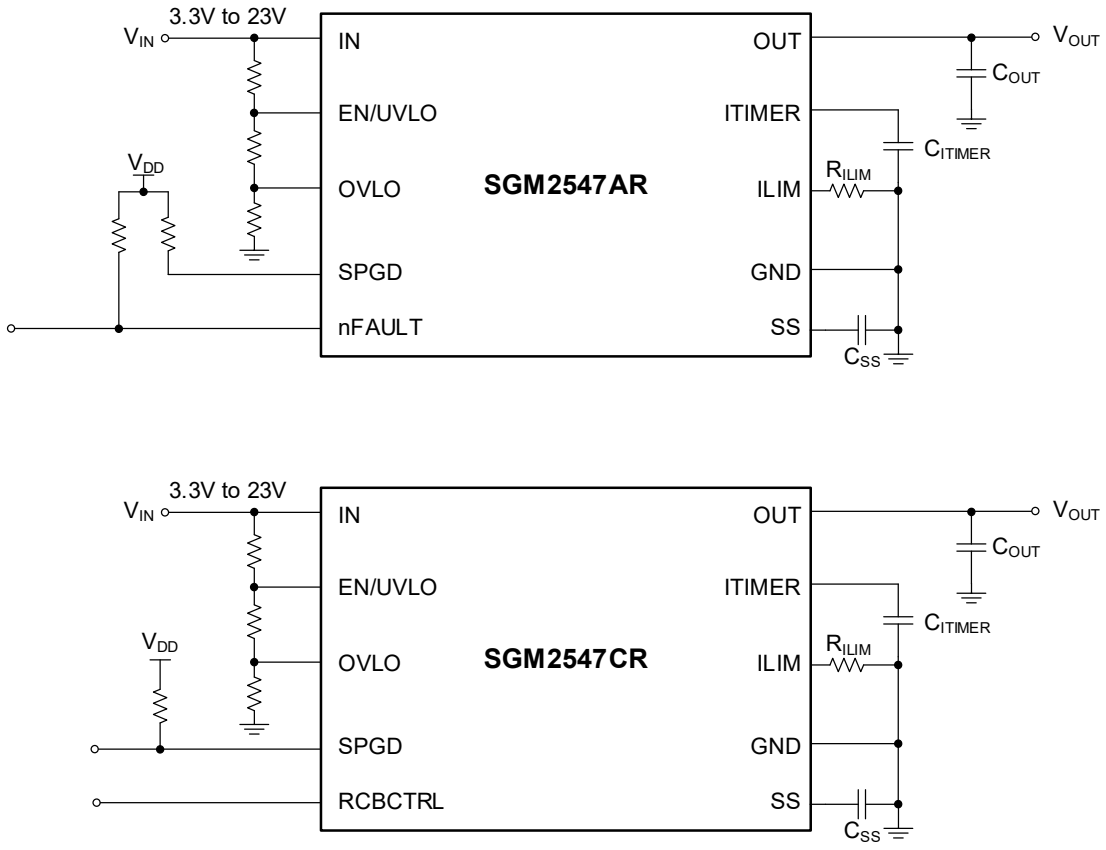


Figure 13. Single Device, Self-Controlled

Other variations:

In a system where the MCU is the host, the EN/UVLO or OVLO pin of the device can be driven by the GPIO of the host to realize the control of the device. The ILIM pin can be used as an ADC input to the MCU for current monitoring.

NOTE: To ensure stable operation, the parasitic capacitance on the ILIM pin should remain below 50pF.

APPLICATION INFORMATION (continued)

Typical Application

Modern smartphones integrate USB on-the-go (OTG) functionality, allowing their USB ports to serve dual purposes, both charging the device and enabling it to act as a USB host to power accessories such as headphones, USB drives, and other peripherals. Some smartphones also support wireless charging with power-sharing capabilities, allowing wireless power delivery to other devices. The SGM2547 can function as a bidirectional power switch in these applications, as shown in Figure 15.

When an external charger is connected to the USB port, the SGM2547C establishes a conductive path from the IN pin to the OUT pin, enabling the battery charger IC to simultaneously charge the battery and power the system load. The device further integrates overvoltage (OVP) and overcurrent (OCP) protection to safeguard the power path under fault conditions.

In another use case, when an accessory like headphones is connected to the USB port, the phone's MCU detects this and switches the battery charger to OTG boost mode. This enables power delivery from the battery to the USB port. The MCU simultaneously pulls down the RCBCTRL pin to reverse the SGM2547C's conduction path (OUT to IN), enabling a low-impedance power path capable of high-power output to the connected accessory.

Similarly, the SGM2547 facilitates controlled bidirectional power flow in wireless charging and power-sharing subsystems, ensuring reliable power distribution in both directions.

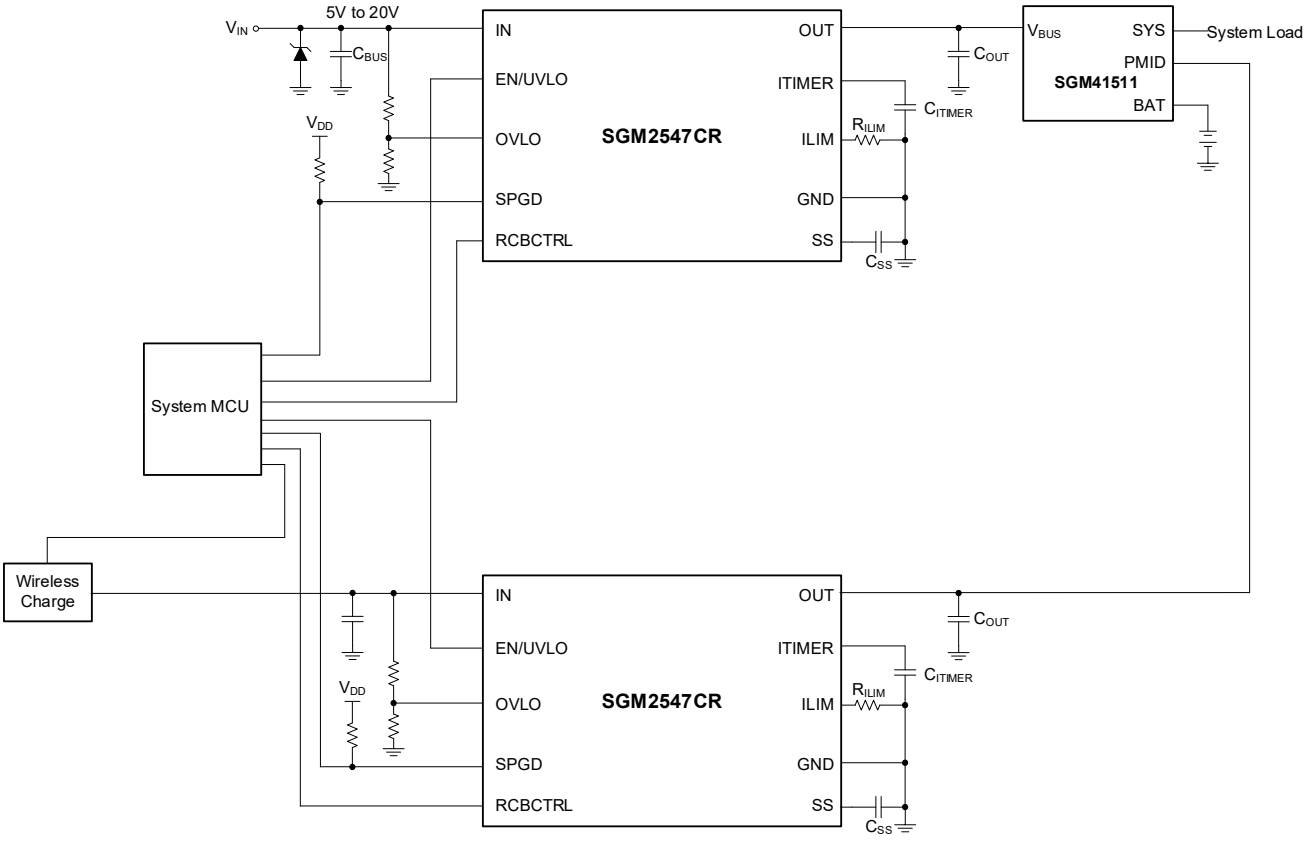
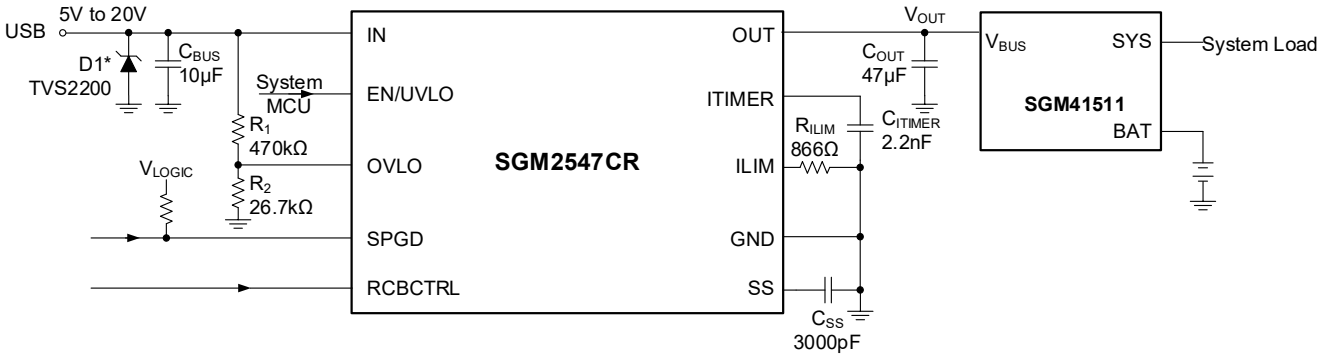


Figure 14. Smartphone Power Path Example

APPLICATION INFORMATION (continued)



*: The selection of optional transient protection components is dependent on the input/output inductance values in the circuit design. Consult the Transient Protection section for further details.

Figure 15. Design Example of USB OTG Port Protection

Design Requirements

Table 5. Design Parameters

PARAMETER	VALUE
Charging Bus Voltage (V_{IN})	20V
Over-Voltage Protection Threshold (V_{IN_OV}) during Charging	22V
Maximum Continuous Charging Current	5A
Load Transient Blanking Interval (t_{ITIMER}) during Charging	2ms
Output Capacitance (C_{OUT})	47μF
Output Rise Time (t_R)	12ms
Over-Current Threshold (I_{LIM}) during Charging	5.5A

Detailed Design Procedure

Setting Over-Voltage Threshold

The supply over-voltage threshold is determined by resistors R_1 and R_2, the resistance values of which can be calculated using the formula below:

$$V_{IN_OV} = V_{OV_R} \times \frac{R_1 + R_2}{R_2} \quad (8)$$

The OVLO rising threshold V_{OV_R} is defined by resistors R_1 and R_2. Since these resistors draw leakage current I_R = V_{IN} / (R_1 + R_2) from the input supply V_{IN}, their values must be selected based on the allowable leakage current. Leakage currents from external active components connected to the resistor divider chain can introduce calculation errors. To mitigate this issue, the I_R current should be set to at least 20 times the maximum leakage current at the OVLO pin (typically 0.1μA).

Based on the design requirements, V_{IN_OV} = 22V. According to R_1 = 470kΩ and the formula, R_2 = 27.11kΩ, Selecting the nearest available standard 1% resistor values, we get R_1 = 470kΩ, R_2 = 26.7kΩ.

Setting Output Voltage Rise Time (t_R)

To ensure a successful design, the device's junction temperature must remain below its absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses are often an order of magnitude higher than static power stresses, necessitating the determination of appropriate start-up time and inrush current limits required to accommodate the system capacitance and prevent thermal shutdown during the initial phase.

To determine the necessary slew rate (SR) for the target output rise time, use the equation below:

$$SR(V/ms) = \frac{V_{IN}(V)}{t_R(ms)} = \frac{20(V)}{12(ms)} = 1.67(V/ms) \quad (9)$$

The C_{SS} needed to meet the specified slew rate requirement can be derived from the equation below:

$$C_{SS}(pF) = \frac{7000}{SR(V/ms)} = \frac{7000}{1.67} = 4192(pF) \quad (10)$$

Select the closest standard capacitor value of 4000pF.

The inrush current corresponding to this slew rate is determined by the following equation:

$$I_{INRUSH}(mA) = SR(V/ms) \times C_{OUT}(\mu F) = 1.67V/ms \times 47\mu F = 79mA \quad (11)$$

APPLICATION INFORMATION (continued)

The average power dissipation inside the part during inrush can be calculated as:

$$P_{D_INRUSH}(W) = I_{INRUSH}(A) \times \frac{V_{IN}(V)}{2} = 0.079 \times \frac{20}{2} = 0.8(W) \quad (12)$$

Based on the calculated power dissipation, the corresponding thermal shutdown time must be higher than the output rise time. *Time to Thermal Shutdown vs. Power Dissipation* shows that for 0.8W, the device thermal shutdown time is greater than 10s, which is much larger than the output rise time (12ms). Therefore, setting the output rise time to 12ms has no negative impact on device security.

Setting Over-Current Threshold (ILIM)

The over-current protection threshold is determined by the R_{ILIM} resistor, whose value is calculated using the following equation:

$$R_{ILIM}(\Omega) = \frac{3960}{I_{ILIM}(A)} = \frac{3960}{5.5(A)} = 720(\Omega) \quad (13)$$

Choose nearest 1% standard resistor value as 724Ω.

Setting Over-Current Blanking Interval (t_{ITIMER})

The C_{ITIMER} capacitor determines the over-current blanking interval; its required value is calculated as following equation:

$$C_{ITIMER}(nF) = 1.2 \times t_{ITIMER}(ms) \quad (14)$$

Active ORing

A conventional redundant power supply arrangement is depicted in Figure 16. Schottky ORing diodes have historically been employed to parallelize multiple power inputs, such as wall adapters coupled with batteries or hold-up capacitors. A notable limitation of this approach lies in the significant voltage loss across diodes and the resultant energy dissipation. The SGM2547, incorporating integrated, ultra-low resistance back-to-back MOSFETs, delivers an optimized and low-loss solution. Figure 16 below illustrates the active ORing architecture realized with SGM2547 devices.

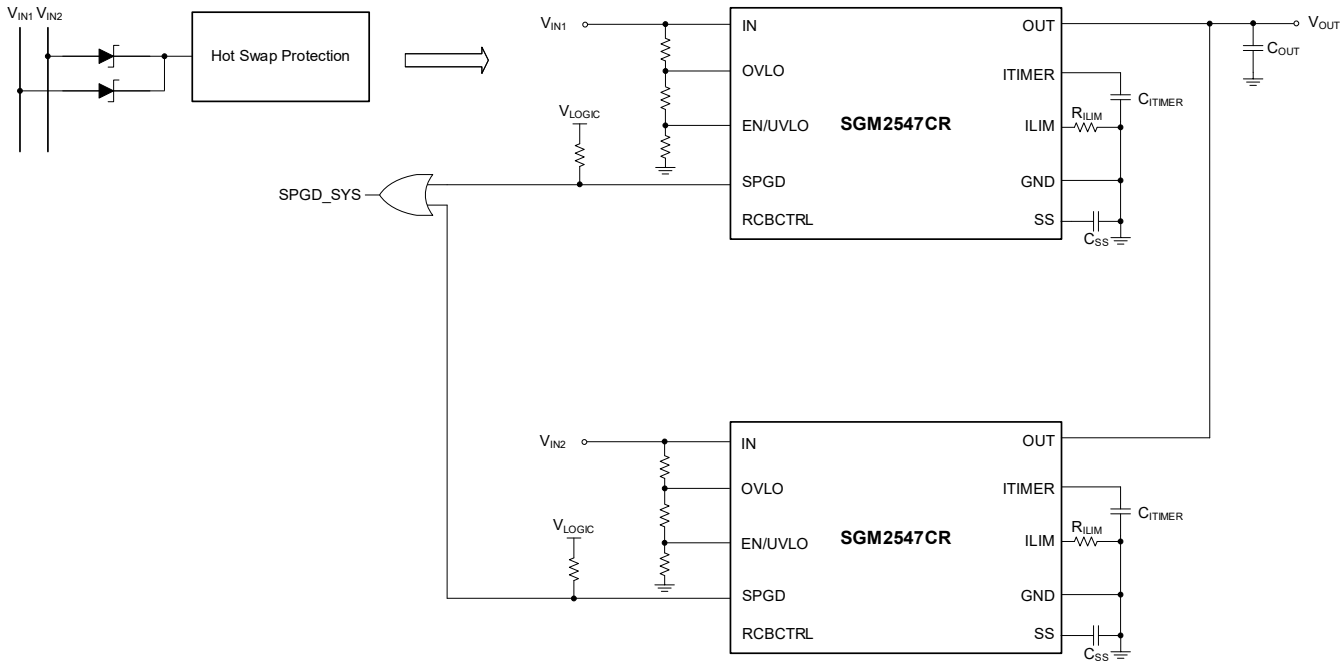


Figure 16. Two Devices, Active ORing Configuration

APPLICATION INFORMATION (continued)

The SGM2547's linear ORing mechanism prevents reverse current flow between power sources during rapid or gradual voltage transitions of either input supply.

The subsequent waveform demonstrates the active ORing behavior under sequential ramp-up of the supply rails.

When input voltages (V_{IN1} and V_{IN2}) reach equilibrium, the internal MOSFET in each channel operates in forward-conduction mode, sourcing load current. During this steady-state phase, current distribution between the two rails depends on the voltage differential across each device's conduction path.

Beyond power ORing, the device continuously guards against system-level risks, including over-voltage events, excessive inrush current, overloads, and short-circuit faults.

NOTE: ORing supports both symmetric and asymmetric voltage configurations between rails. For setups with mismatched voltages, the SS pin's capacitor value must be sized according to the higher supply voltage. Detailed guidelines can be found in the RECOMMENDED OPERATING CONDITIONS section.

Priority Power MUXing

Dual-power systems such as PCIe cards, tablets, and portable battery equipment often require prioritization of one energy source over another. For instance, mains supply (wall adapter) typically has higher priority than internal battery backup. The SGM2547 enables seamless transition to backup power exclusively when the main input voltage drops below a defined threshold, offering a streamlined solution for prioritized power selection needs.

Figure 17 illustrates a typical priority power multiplexing implementation using SGM2547 devices. Under normal operation where the primary input (V_{IN1}) remains within its valid voltage range (not in UV/OV condition), the primary path device continuously delivers power to the output bus. The auxiliary path's OVLO pin is forced to a high state via the SPGD signal from the primary device, thereby disabling the auxiliary path device regardless of the auxiliary supply voltage (V_{IN2}) relative to V_{IN1}. Once the primary supply voltage enters a UV/OV fault state, the primary device ceases asserting the SPGD signal, triggering the auxiliary path device to enable instantaneously. The auxiliary device then assumes power delivery by bypassing conventional soft-start constraints, enabling rapid output resumption within the t_{SWOV} timeframe through a fast-recovery mechanism. When the primary supply is restored, the primary path gradually resumes full operation at a predefined slew rate while reasserting the SPGD signal to high, which forces the auxiliary path into shutdown. This design ensures a smooth transition from the auxiliary supply to the primary source, minimizing output voltage droop and fully eliminating shoot-through currents during the handover process.

A critical design criterion in power multiplexing systems is the minimum voltage droop experienced by the output bus during supply transitions. This droop magnitude is determined by three key parameters: output load current (I_{LOAD}), output bus hold-up capacitance (C_{OUT}), and the switchover time (t_{SW}). The minimum achievable bus voltage when switching from the primary (V_{IN1}) to the auxiliary supply (V_{IN2}) can be calculated using Equation 15. This calculation uses the switchover time (t_{SW}), which is defined as the fast over-voltage lockout recovery time (t_{SWOV}) required for the SGM2547 to fully activate its auxiliary path and begin supplying the load.

$$V_{OUT_MIN}(V) = \min(V_{IN1}, V_{IN2}) - t_{SW}(\mu s) \times \frac{I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (15)$$

APPLICATION INFORMATION (continued)

During the transition from the auxiliary supply (V_{IN2}) to the primary supply V_{IN1}, the minimum achievable bus voltage is determined by Equation 16. In this case, the maximum switchover time (t_{SW}) corresponds to the RCB recovery time (t_{SWRCB}), which is contingent on the initial condition where V_{IN1} is equal to or lower than (V_{IN2}) prior to the switch.

$$V_{OUT_MIN}(V) = \min(V_{IN1}, V_{IN2}) - V_{FWDTH}(V) - t_{SWRCB}(\mu s) \times \frac{I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (16)$$

The SPGD pin can be configured as a digital output signal to identify the active power supply path and indicate which supply is powering the load.

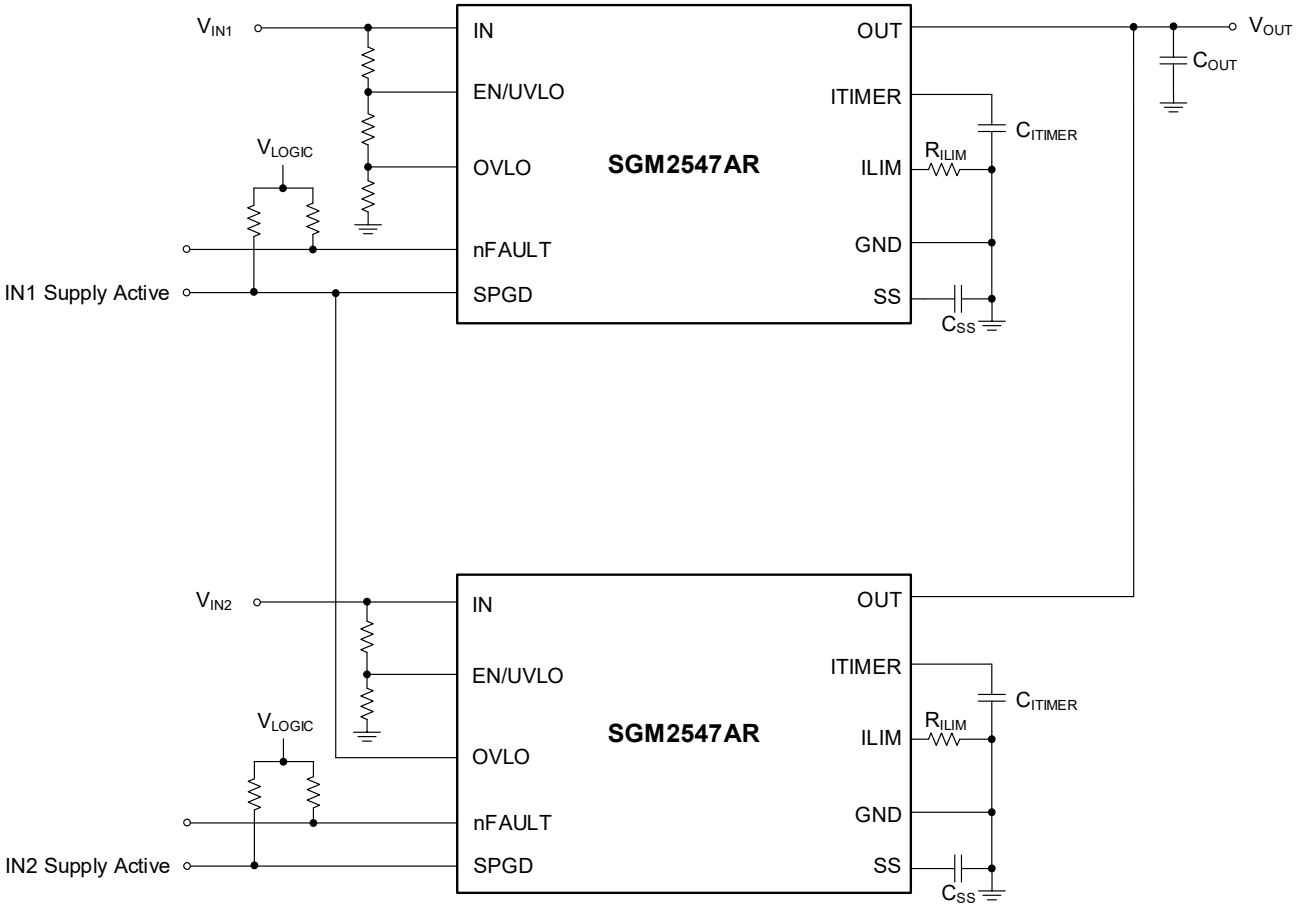


Figure 17. Priority Power MUXing with 2 × SGM2547AR (a)

APPLICATION INFORMATION (continued)

This configuration offers the most compact priority power multiplexer (MUX) architecture, incorporating dual-channel active current limit protection and over-voltage protection on the primary supply path, while delivering the fastest switchover time from primary to auxiliary supply. However, this comes at a small trade-off: the auxiliary path incurs an increased quiescent current when the primary supply is active. Additionally, the design minimizes external component count, yet sacrifices OVP on the auxiliary path, as this protection is bypassed in favor of reduced external elements.

The subsequent waveforms depict the operational characteristics of the SGM2547AR in a priority power multiplexer (MUX) configuration. To enable over-voltage protection on both supply channels, an alternative circuit topology is implemented as shown in Figure 18. This design incorporates an additional N-channel MOSFET to trigger the OVLO pin of the auxiliary path device, thereby activating its over-voltage lockout mechanism. Crucially, the switchover time remains consistent with the base configuration, ensuring reliable and rapid load transfer without compromising system performance.

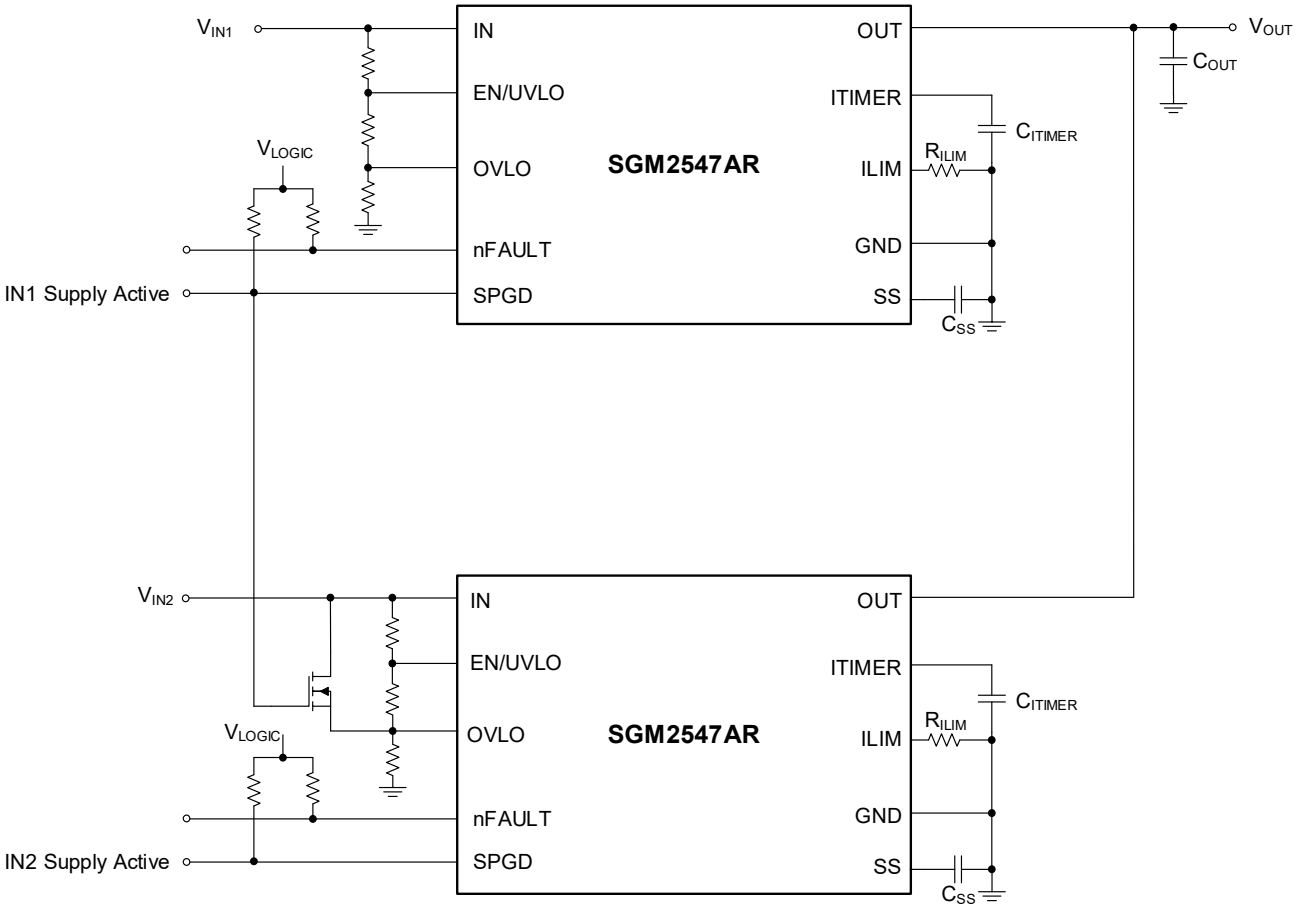


Figure 18. Priority Power MUXing with 2 × SGM2547AR (b)

APPLICATION INFORMATION (continued)

A modified configuration is proposed to minimize quiescent current on the auxiliary channel when the primary supply is active. This is achieved by incorporating an additional N-channel MOSFET to regulate the EN/UVLO pin of the auxiliary path device, as illustrated in Figure 19. However, this design introduces a trade-off: while the quiescent current is reduced, the switchover delay from primary to auxiliary supply increases compared to the baseline configuration. The delay arises from the added component's activation sequence, though it preserves system reliability during load transitions.

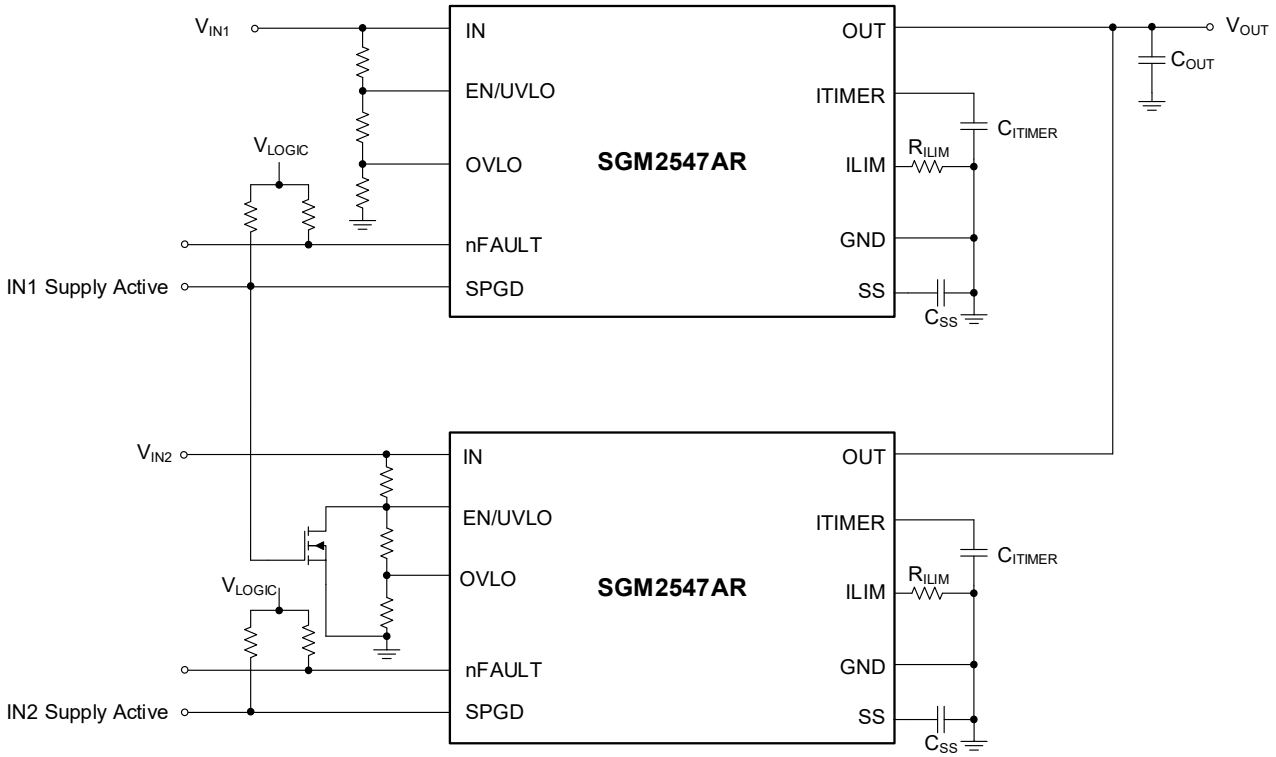


Figure 19. Priority Power MUXing with 2 × SGM2547AR (c)

The minimum acceptable bus voltage during a transition from a higher to a lower supply rail is given by Equation 17. The switchover time (t_{SWRCB}) in this equation is the duration required for the device to exit its reverse current blocking state, thereby defining the latency before the auxiliary power path becomes active.

$$V_{OUT_MIN}(V) = \min(V_{IN1}, V_{IN2}) - V_{FWDTH}(V) - t_{SWRCB}(\mu s) \times \frac{I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (17)$$

Equation 18 can be used to determine the minimum acceptable bus voltage during a transition from a lower to a higher supply rail. The switchover time (t_{SW}) in this context is defined as the total time required for the device to achieve full conduction, which is equivalent to its turn-on time (t_{ON}). This t_{ON} is the sum of the turn-on delay (t_{D_ON}) and the rise time (t_R), both of which are set by the slope compensation capacitor (C_{SS}) and the bus voltage.

$$V_{OUT_MIN}(V) = \min(V_{IN1}, V_{IN2}) - t_{SW}(\mu s) \times \frac{I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (18)$$

NOTE:

For power multiplexing scenarios with asymmetric voltage pairs (e.g., when channels operate at significantly different voltages), it is critical to design the EN/OVLO pins of lower-voltage channel devices to ensure their absolute maximum ratings are not exceeded by voltages from the opposing channel. Additionally, the SS pin's capacitor rating must be selected based on the higher supply voltage of the two rails to maintain compatibility across all operating conditions. Refer to RECOMMENDED OPERATING CONDITIONS for detailed specifications.

APPLICATION INFORMATION (continued)

Parallel Operation

For applications requiring higher steady-state currents, multiple SGM2547 devices can be connected in parallel (refer to Figure 20). In this configuration, the first device initially activates to regulate the inrush current, while the second device remains inactive by having its EN/UVLO pin held low via the SPGD signal from the first device. Once the inrush phase completes, the first device drives its SPGD pin high to enable the second device. The second device then asserts its SPGD signal once it achieves full conduction, signaling the system that the parallel setup is ready to deliver maximum steady-state current. During steady-state operation, current sharing between the devices occurs nearly equally. However, minor current imbalances may arise due to part-to-part variations in R_{ON} (on-state resistance) or mismatches in PCB trace resistance.

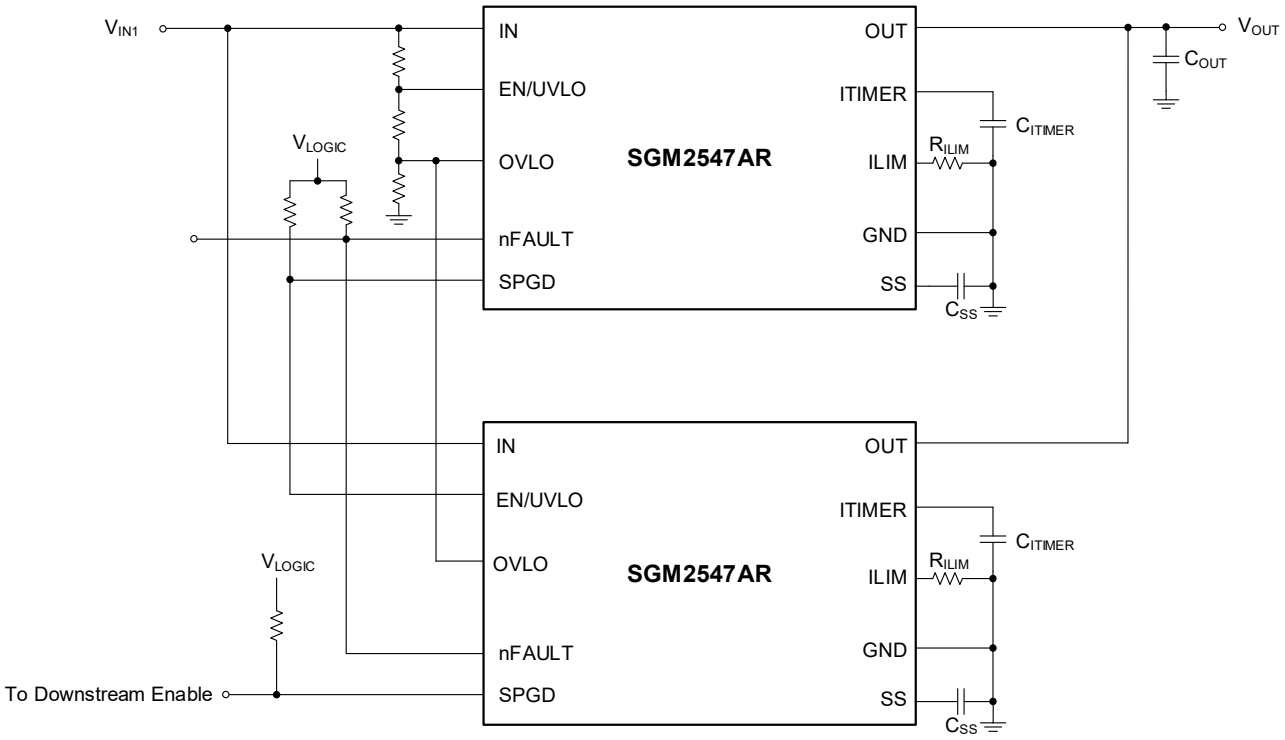
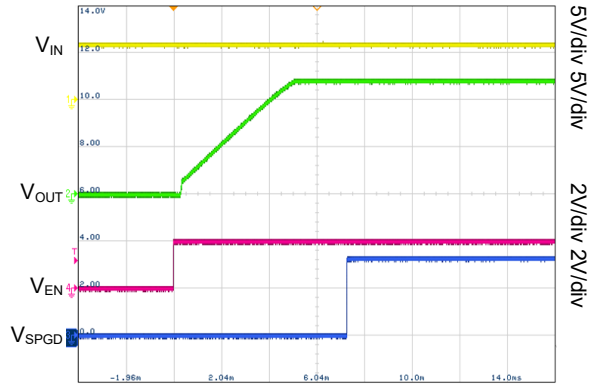


Figure 20. Enhanced Steady-State Current via Two-Device Parallel Architecture

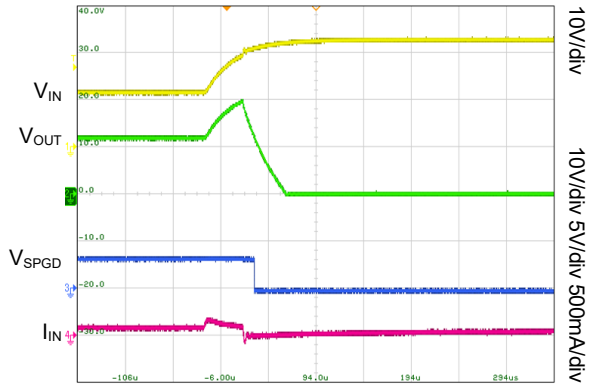
The waveforms below demonstrate the parallel configuration behavior (during start-up and steady state).

APPLICATION INFORMATION (continued)



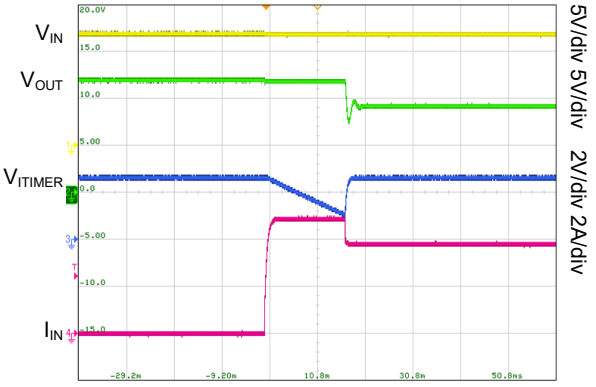
Time (2ms/div)

Figure 21. Power-Up



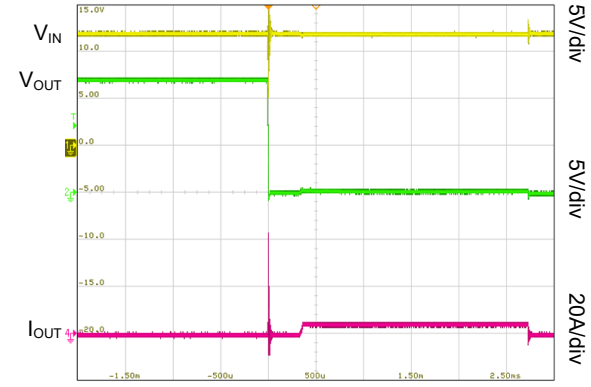
Time (50μs/div)

Figure 22. Over-Voltage Protection



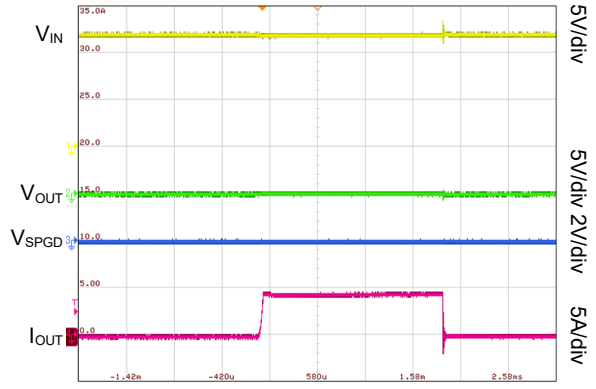
Time (10ms/div)

Figure 23. Over-Current Protection



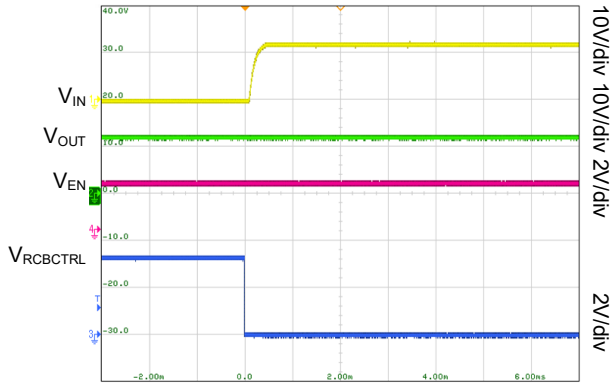
Time (500μs/div)

Figure 24. Short at Output Protection



Time (500μs/div)

Figure 25. Wake up into Short Protection



Time (1ms/div)

Figure 26. Power-Up in OTG Mode

APPLICATION INFORMATION (continued)

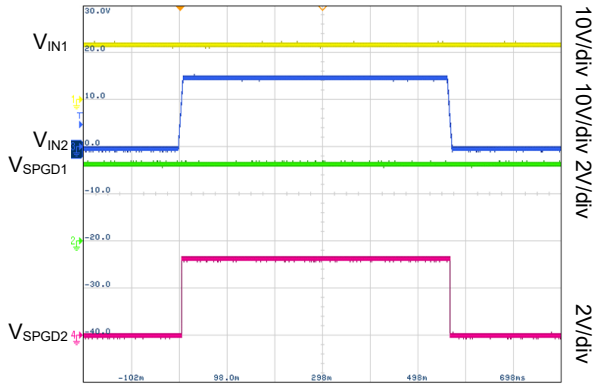


Figure 27. Active ORing Response

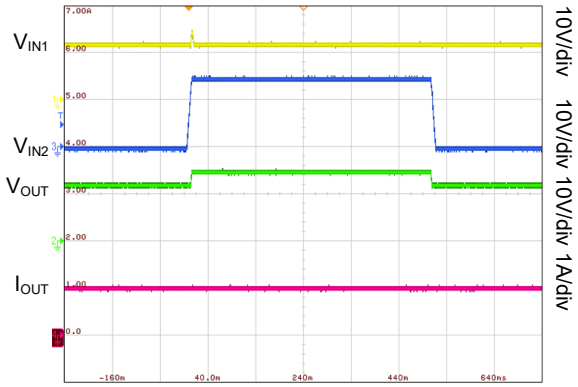


Figure 28. Active ORing Response

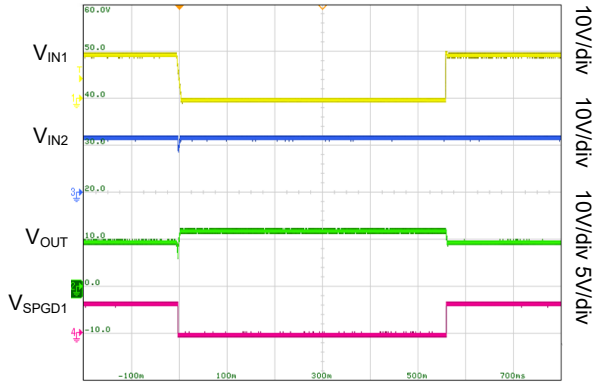


Figure 29. Power MUX - Switchover Between Primary and Auxiliary Supplies

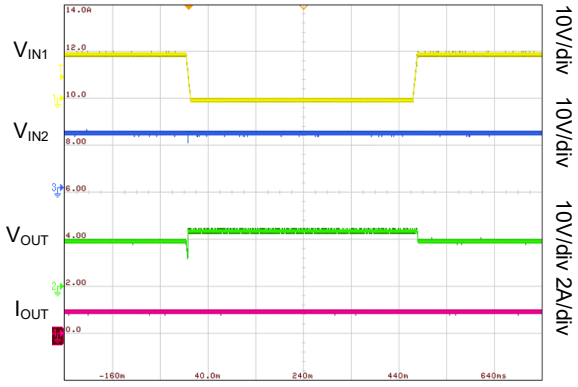


Figure 30. Power MUX - Switchover Between Primary and Auxiliary Supplies

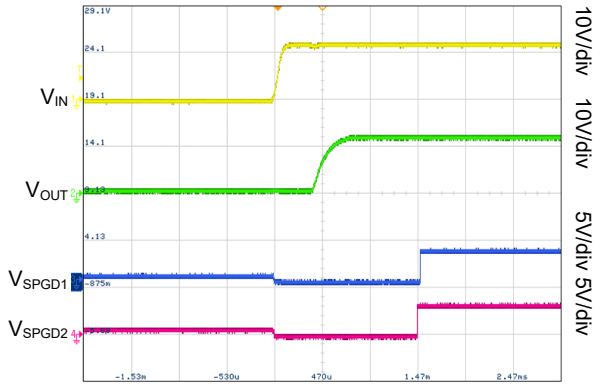


Figure 31. Parallel Devices Sequencing during Start-Up

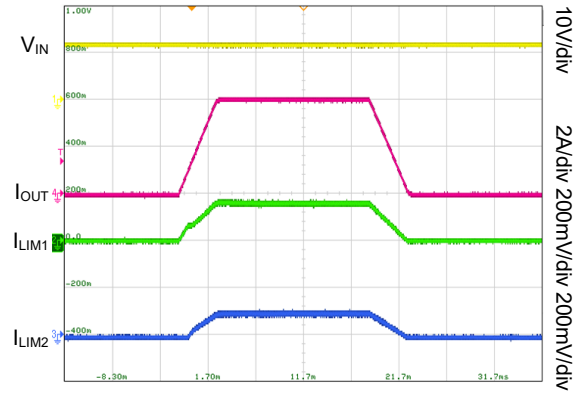


Figure 32. Parallel Devices Load Current during Steady State

APPLICATION INFORMATION (continued)

USB PD Port Protection

End devices such as PCs, notebooks, docking stations, and monitors support USB power delivery (PD) ports configurable as a DFP (Source), UFP (Sink), or DRP (Source/Sink). The SGM2547 can serve as a fully integrated power path management solution for USB PD ports, as illustrated in Figure 33.

SGM2547 integrates all essential protection features required for USB power path management, including over-voltage, over-current, and short-circuit protection, along with real-time monitoring and control circuits. The device's linear ORing mechanism ensures no reverse current flows between power sources during voltage transitions of either supply, whether rapid or gradual.

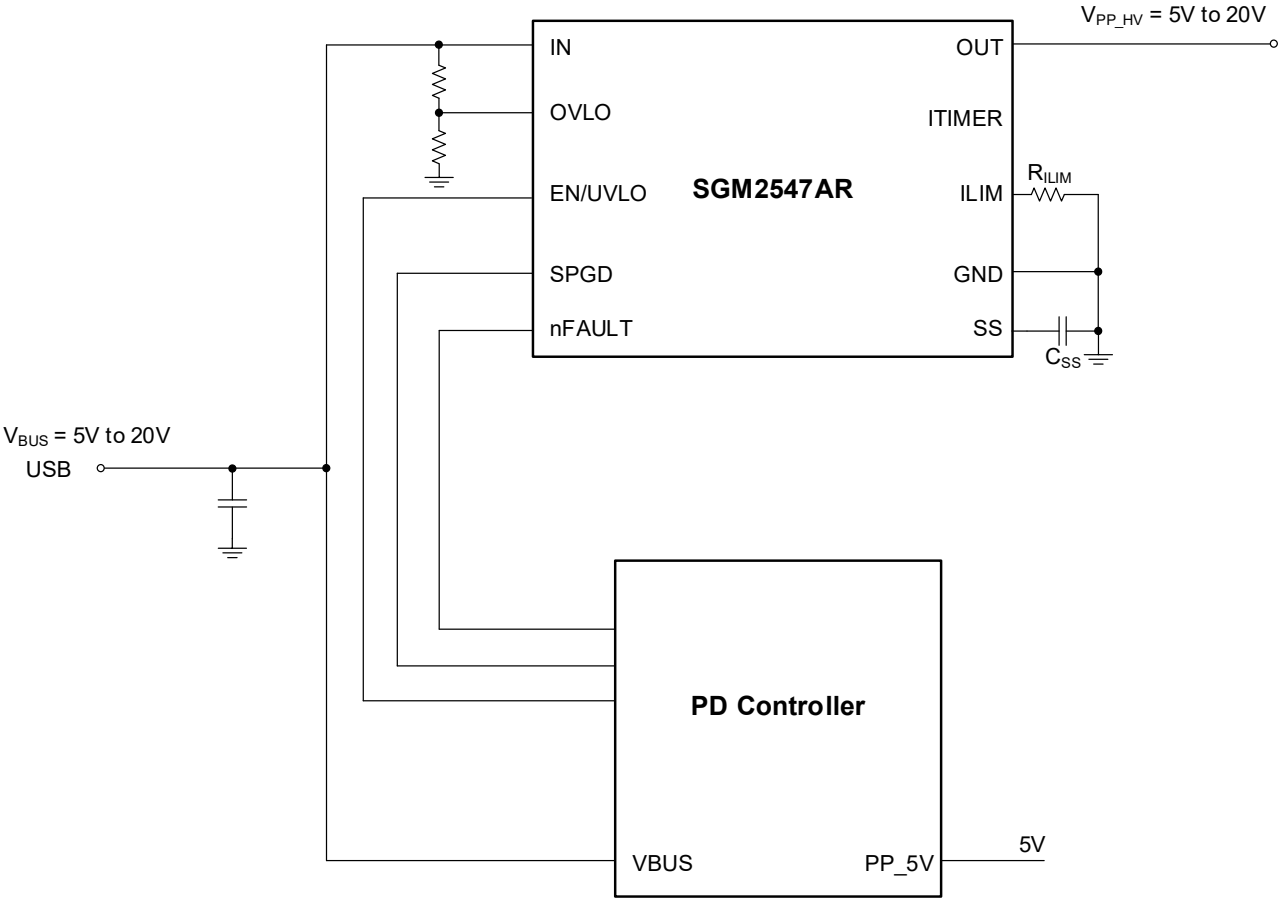


Figure 33. USB PD Port Protection

Power Supply Recommendations

The SGM2547 operates within a 3.3V to 23V supply voltage range for both input (V_{IN}) and output (V_{OUT}) rails. A ceramic bypass capacitor > 0.1μF is mandatory when the input supply is positioned more than several inches from the device. The power supply must support currents exceeding the programmed over-current limit to prevent voltage dips during short-circuit or over-current events.

Transient Protection

During short-circuit events or when the output current exceeds the programmed overload threshold, the device interrupts current flow. The input inductance generates a positive voltage spike across its terminals, while the output inductance produces a negative spike across its terminals. The peak amplitude of these voltage transients is directly proportional to the series inductance in the input/output paths. If unmitigated, such transients may exceed the device's absolute maximum ratings, risking permanent damage. Common mitigation strategies include:

APPLICATION INFORMATION (continued)

- Reducing lead lengths and inductance in both input and output paths to minimize energy storage during current interruption.
- Implementing a solid ground plane on the PCB to provide a low-impedance return path, reducing noise coupling.
- Connecting a reverse-biased Schottky diode between the OUT pin and ground to clamp negative voltage transients.
- Placing a low-ESR capacitor (> 1μF) at the output pin in close proximity to the device to dissipate energy and stabilize the output voltage.
- Adding a low-value ceramic capacitor (e.g., 1μF) on the input side to absorb transient energy and dampen inductive ringing. Ensure its voltage rating is at least twice the input supply voltage to withstand positive voltage excursions during transients.

The approximate value of input capacitance can be calculated using the following Equation 19:

$$V_{SPIKE_ABS} = V_{IN} + I_{LOAD} \times \frac{L_{IN}}{C_{IN}} \quad (19)$$

The key parameters are defined as follows:

- V_{IN}: The nominal input supply voltage
- I_{LOAD}: The steady-state or operating current drawn by the load circuit
- L_{IN}: represents the effective inductance observed at the power source side parasitic inductance in the current path
- C_{IN}: Capacitor at the input end

In certain applications, a transient voltage suppressor (TVS) may be required to ensure transient voltages do not exceed the device's absolute maximum ratings. Even when transient amplitudes remain below these ratings, a TVS can absorb excess energy to prevent rapid voltage spikes on the IC's input supply pin. Such spikes might otherwise couple into internal control circuits, leading to unintended operational anomalies.

For applications like USB-C ports with powered cables connected to the device's output, voltage stress from OUT to IN can exceed the device's absolute maximum ratings. To mitigate this risk, a TVS diode should be added between OUT and IN to clamp the voltage within safe limits. Figure 34 illustrates this protective circuit configuration, including optional components.

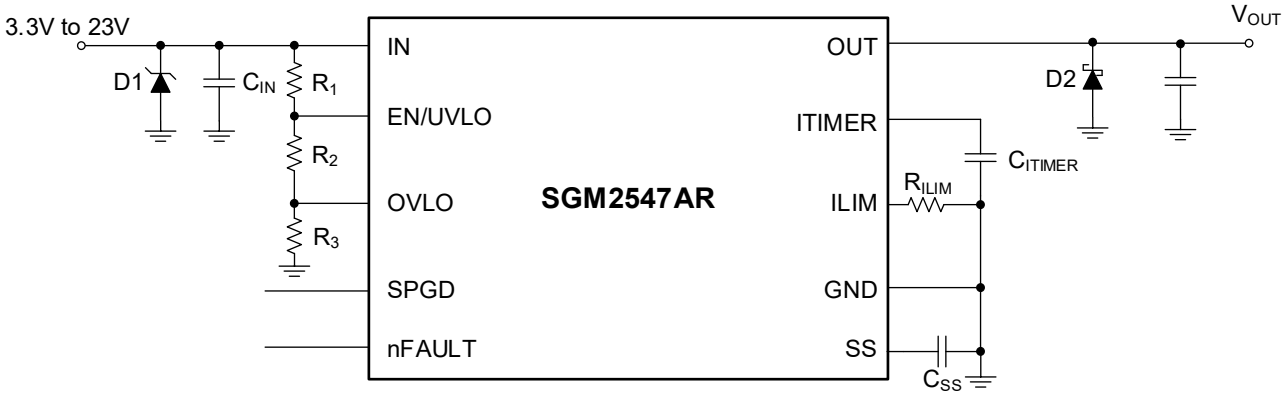


Figure 34. Modular Circuit with Optional TVS Protection Blocks

Output Short-Circuit Measurements

Short-circuit test results are inherently variable and difficult to replicate. Key influencing factors include:

- Power source routing
- Input lead characteristics
- PCB layout parasitic
- Component selection
- Short-circuit implementation method
- Short-circuit proximity to power nodes

Waveforms will not perfectly align with datasheet examples, as every test environment introduces unique parasitic effects and configuration dependencies.

APPLICATION INFORMATION (continued)

Layout

Layout Guidelines

For all applications, a ceramic decoupling capacitor of at least 0.1μF must be placed between the IN and GND terminals. High-current power paths require the shortest possible trace lengths with cross-sectional areas rated for double the full-load current. The IC's GND pin must connect directly to the PCB ground plane via the shortest trace to ensure minimal impedance. The PCB ground must form a continuous solid copper plane or localized island to maintain low impedance. A dedicated isolated ground plane is required for eFuse circuitry, which must exclude high-current paths and provide a noise-free reference solely for critical analog signals involved in eFuse operation. The device ground shall connect to the system power ground through a star-point topology to reduce interference and eliminate ground loops.

The IN and OUT pads are designed for heat dissipation. To maximize thermal performance, connect them to large-area copper regions on both the top and bottom PCB layers via thermal vias. Strategically placing vias beneath the device minimizes voltage gradients across the IN and OUT pads and ensures uniform current distribution through the component. These measures are critical to achieving optimal on-resistance and precise current-sense accuracy.

- Component Grounding: Connect the unused terminal of the component to the device's GND pin via the shortest practicable trace to minimize parasitic inductance.
- Signal Integrity for Critical Nodes: Route traces for the R_{ILIM}, C_{ITIMER}, and C_{SS} components to the device with minimal length, ensuring the shortest possible path to reduce parasitic inductance and capacitance. This maintains accuracy in current-limiting, over-current timing, and soft-start stability.
- ILIM Pin Capacitance Control: Keep parasitic capacitance on the ILIM pin below 50pF to prevent oscillations or erroneous triggering, ensuring stable over-current protection.
- Switching Signal Isolation: All traces must avoid coupling with high-frequency switching signals elsewhere on the PCB to prevent cross-talk and interference.
- ILIM Node Isolation: The ILIM pin's bias current directly determines over-current protection thresholds. Route the ILIM node away from switching noise sources (e.g., high-speed traces, inductive loads) to prevent signal interference.
- Protection components (TVS diodes, snubbers, capacitors, or diodes) must be placed physically adjacent to the device they protect to reduce parasitic inductance.
- All protection component traces must be kept as short as possible to minimize inductive effects.
- A Schottky diode is required to clamp negative voltage transients caused by inductive load switching, and must be directly connected to the OUT pin.
- A ceramic decoupling capacitor (≥ 1μF) must be placed between the OUT pin and GND. This capacitor must be positioned within 2mm of the OUT pin to optimize decoupling performance.
- The loop area formed by the Schottky diode, bypass capacitor, OUT pin, and IC's GND terminal must be minimized to reduce electromagnetic interference (EMI).

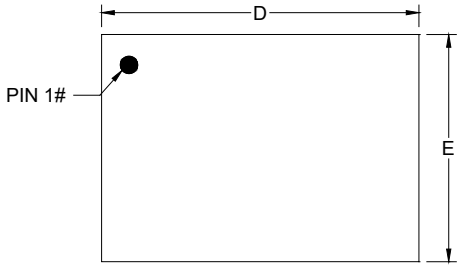
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

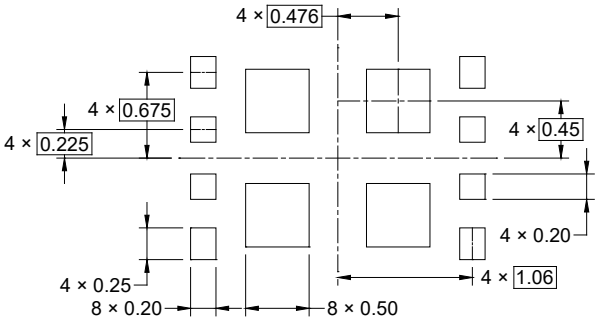
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

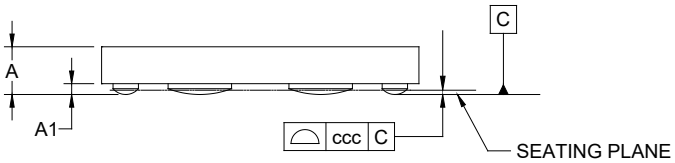
WLCSP-2.5×1.79-12L



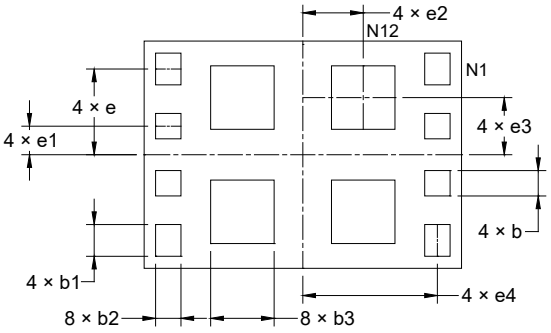
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



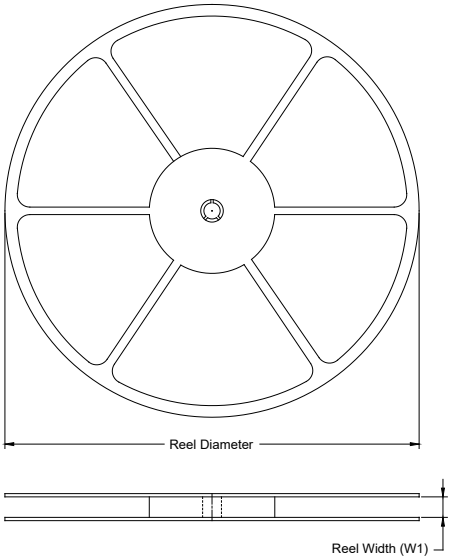
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.376
A1	0.070	-	0.100
D	2.470	-	2.530
E	1.760	-	1.820
b	0.185	-	0.215
b1	0.235	-	0.265
b2	0.185	-	0.215
b3	0.485	-	0.515
e	0.675 BSC		
e1	0.225 BSC		
e2	0.476 BSC		
e3	0.450 BSC		
e4	1.060 BSC		
ccc	0.050		

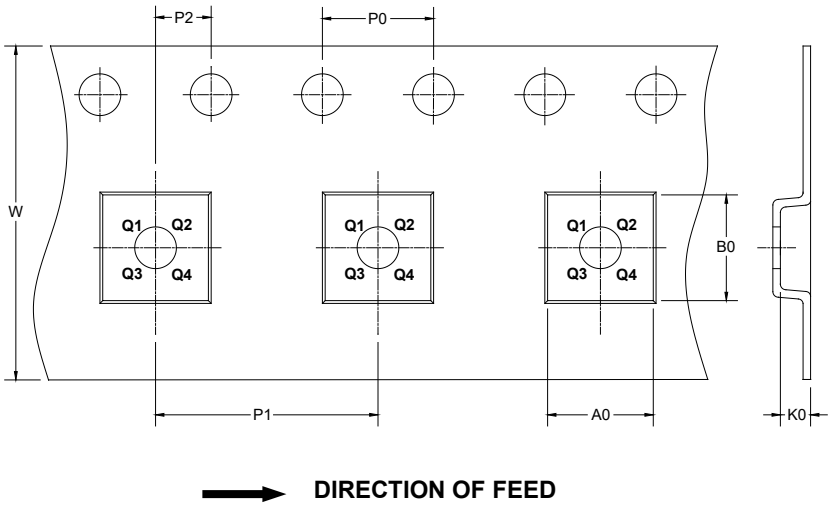
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



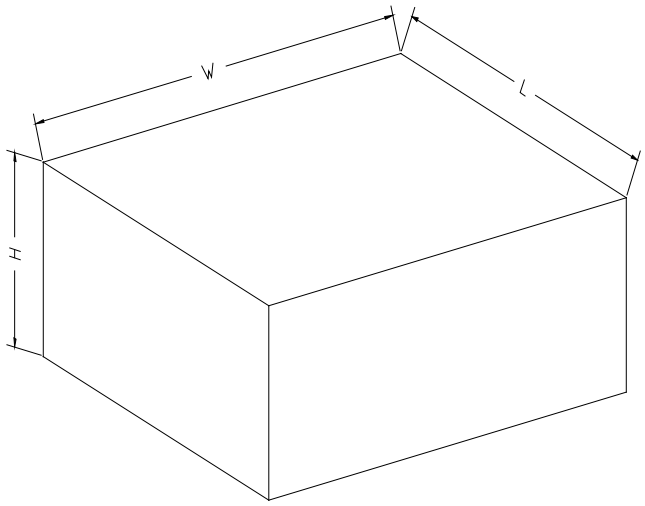
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.5×1.79-12L	7"	9.5	1.97	2.72	0.47	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002