

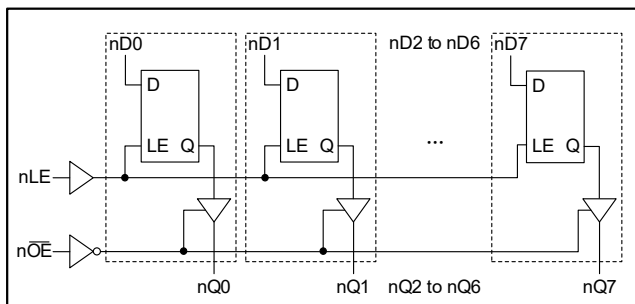
### GENERAL DESCRIPTION

The 74LVTH16373 is a 16-bit high-performance D-type transparent latch with non-inverting 3-state outputs designed for 3.3V  $V_{CC}$  operation. The device can be used for driving loads with high capacitance or relatively low-impedance, making it suitable for applications in buffer registers, I/O ports, bidirectional bus drivers and working registers.

The device can be operated as two 8-bit latches or one 16-bit latch. When latch enable input  $nLE$  is set high, the outputs  $nQn$  will indicate the data of inputs  $nDn$ . When  $nLE$  is set low, the  $nQn$  outputs will be latched at the levels of the inputs  $nDn$  one setup time before the High-to-Low transition.

The output enable  $\overline{nOE}$  input can make all outputs in high/low logic levels or high-impedance state. The bus hold on data inputs eliminates the need for external pull-up/pull-down resistors to hold unused inputs.

### LOGIC DIAGRAM



### FEATURES

- Wide Operating Voltage Range: 2.7V to 3.6V
- Input and Output Interface Capability to 5V System Environment
- +64mA/-32mA Output Current
- 16-Bit Transparent Latch
- 3-State Buffers
- Input and Output Switching Levels of TTL
- Power-Up Reset
- Power-Up 3-State
- No Bus Current Load when Output is Connected to 5V Bus
- Bus Hold on Data Inputs with No Need for External Pull-Up/Pull-Down Resistors
- Support Live Insertion and Extraction
- -40°C to +125°C Operating Temperature Range
- Available in a Green TSSOP-48 Package

### FUNCTION TABLE

CONTROL INPUT			INTERNAL LATCHES	OUTPUT $nQn$
$\overline{nOE}$	$nLE$	$nDn$		
L	H	L	L	L
L	H	H	H	H
L	L	I	L	L
L	L	h	H	H
H	L	I	L	Z
H	L	h	H	Z

H = High Voltage Level

h = High Voltage Level One Setup Time before the High-to-Low Transition of  $nLE$

L = Low Voltage Level

I = Low Voltage Level One Setup Time before the High-to-Low Transition of  $nLE$

Z = High-Impedance State

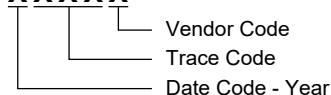
## PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVTH16373	TSSOP-48	-40°C to +125°C	74LVTH16373XTS48G/TR	74LVTH16373 XTS48 XXXXX	Tape and Reel, 2500

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply Voltage Range, $V_{CC}$	-0.5V to 4.6V
Input Voltage Range, $V_I$ <sup>(2)</sup>	-0.5V to 7.0V
Output Voltage Range, $V_O$ <sup>(2)</sup>	
3-State or High-State	-0.5V to 7.0V
Input Clamping Current, $I_{IK}$ ( $V_I < 0V$ )	-50mA
Output Clamping Current, $I_{OK}$ ( $V_O < 0V$ )	-50mA
Output Current, $I_O$	
High-State	-64mA
Low-State	128mA
Supply Current, $I_{CC}$	128mA
Ground Current, $I_{GND}$	-256mA
Junction Temperature <sup>(3)</sup>	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	7000V
CDM	1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, $V_{CC}$	2.7V to 3.6V
Input Voltage Range, $V_I$	0V to 5.5V
High-Level Output Current, $I_{OH}$	-32mA
Low-Level Output Current, $I_{OL}$	64mA
Input Transition Rise or Fall Rate, $\Delta t/\Delta V$	10ns/V (MAX)
Operating Temperature Range	-40°C to +125°C

## OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

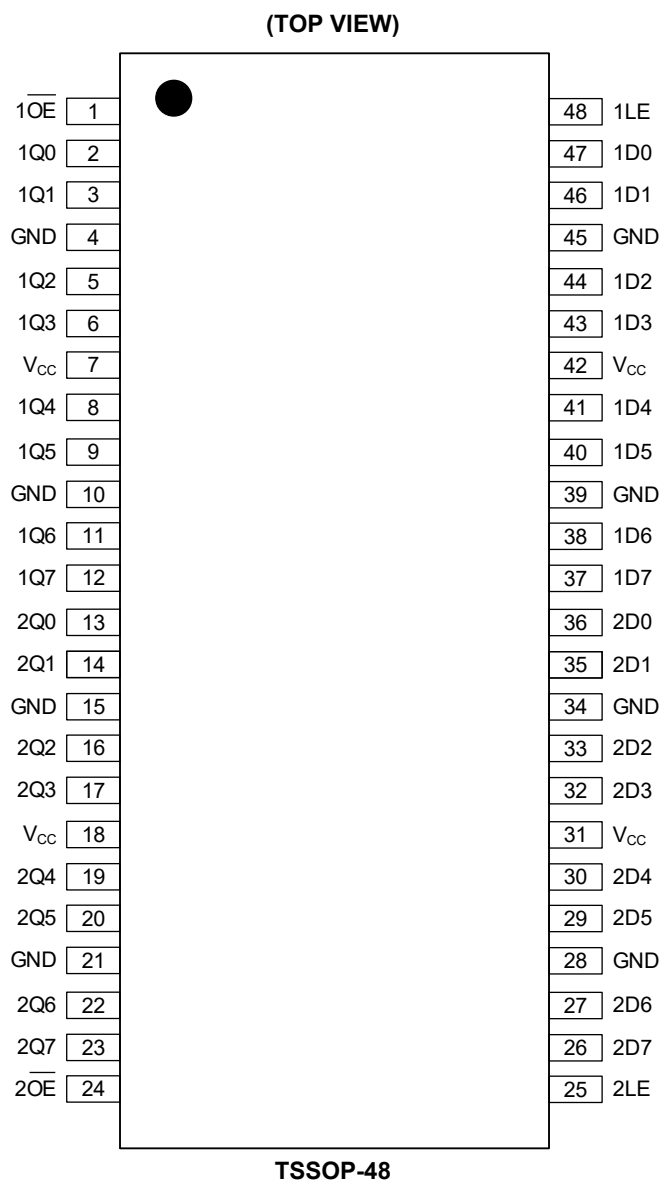
## ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN	NAME	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37	1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	Data Inputs.
36, 35, 33, 32, 30, 29, 27, 26	2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	Data Inputs.
1, 24	1OE, 2OE	Output Enable Inputs (Active-Low).
48, 25	1LE, 2LE	Latch Enable Inputs (Active-High).
2, 3, 5, 6, 8, 9, 11, 12	1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	Data Outputs.
13, 14, 16, 17, 19, 20, 22, 23	2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	Data Outputs.
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground.
7, 18, 31, 42	V <sub>CC</sub>	Supply Voltage.

## ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at  $V_{CC} = 3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Clamping Voltage	$V_{IK}$	$V_{CC} = 2.7V$ , $I_{IK} = -18mA$	Full	-1.2	-0.78		V
High-Level Input Voltage	$V_{IH}$	$V_{CC} = 2.7V$ to $3.6V$	Full	2.0			V
Low-Level Input Voltage	$V_{IL}$	$V_{CC} = 2.7V$ to $3.6V$	Full			0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{CC} = 2.7V$ to $3.6V$ , $I_{OH} = -100\mu A$	Full	$V_{CC} - 0.05$	$V_{CC} - 0.001$		V
		$V_{CC} = 2.7V$ , $I_{OH} = -8mA$	Full	2.45	2.60		
		$V_{CC} = 3.0V$ , $I_{OH} = -32mA$	Full	2.10	2.65		
Low-Level Output Voltage	$V_{OL}$	$V_{CC} = 2.7V$ , $I_{OL} = 100\mu A$	Full		0.001	0.05	V
		$V_{CC} = 2.7V$ , $I_{OL} = 24mA$	Full		0.15	0.28	
		$V_{CC} = 3.0V$ , $I_{OL} = 16mA$	Full		0.1	0.18	
		$V_{CC} = 3.0V$ , $I_{OL} = 32mA$	Full		0.2	0.36	
		$V_{CC} = 3.0V$ , $I_{OL} = 64mA$	Full		0.4	0.55	
Power-Up Low-Level Output Voltage <sup>(1)</sup>	$V_{OL\_PU}$	$V_{CC} = 3.6V$ , $I_{OL} = 1mA$ , $V_I = V_{CC}$ or GND	Full		5	50	mV
Input Leakage Current	$I_I$	Control pins, $V_{CC} = 3.6V$ , $V_I = V_{CC}$ or GND	Full		$\pm 0.01$	$\pm 1$	$\mu A$
		Control pins, $V_{CC} = 0V$ or $3.6V$ , $V_I = 5.5V$	Full		0.01	5	
		Input data pins <sup>(2)</sup> , $V_{CC} = 0V$ or $3.6V$ , $V_I = 5.5V$	Full		0.4	5	
		Input data pins <sup>(2)</sup> , $V_{CC} = 3.6V$ , $V_I = V_{CC}$	Full		0.3	2	
		Input data pins <sup>(2)</sup> , $V_{CC} = 3.6V$ , $V_I = GND$	Full	-2	-0.01		
Off-State Output Current	$I_{OZ}$	$V_{CC} = 3.6V$ , $V_O = 3.0V$	Full		0.01	2	$\mu A$
		$V_{CC} = 3.6V$ , $V_O = 0.5V$	Full	-2	-0.01		
Output Leakage Current	$I_{LO}$	Outputs in high-state when $V_O > V_{CC}$ , $V_{CC} = 3.0V$ , $V_O = 5.5V$	Full		1	30	$\mu A$
Power-Up/Down Output Current	$I_{O\_PU/PD}$	$V_{CC} \leq 1.2V$ , $V_O = 0.5V$ to $V_{CC}$ , $V_I = GND$ or $V_{CC}$ , $n\overline{OE} = \text{don't care}$	+25°C		0.01	10	$\mu A$
Power-Off Leakage Current	$I_{OFF}$	$V_{CC} = 0V$ , $V_I$ or $V_O = 0V$ to $5.5V$	Full		0.01	10	$\mu A$
Supply Current	$I_{CC}$	$V_{CC} = 3.6V$ , $V_I = GND$ or $V_{CC}$ , $I_O = 0A$	Outputs high	Full	12	80	$\mu A$
			Outputs low	Full	12	80	
			Outputs disabled <sup>(3)</sup>	Full	12	80	
Additional Supply Current <sup>(4)</sup>	$\Delta I_{CC}$	Per input pin, $V_{CC} = 3.0V$ to $3.6V$ , one input at $V_{CC} - 0.6V$ , other inputs at $V_{CC}$ or GND	Full		0.2	200	$\mu A$
Input Capacitance	$C_I$	Input pins, $V_I = 0V$ or $3.0V$	+25°C		6		pF
Output Capacitance	$C_O$	Output pins nQn, outputs disabled, $V_O = 0V$ or $V_{CC}$	+25°C		9		pF
Bus Hold Low Current	$I_{BHL}$	$V_{CC} = 3.0V$ , $V_I = 0.8V$	Full	50	100		$\mu A$
Bus Hold High Current	$I_{BHH}$	$V_{CC} = 3.0V$ , $V_I = 2.0V$	Full		-130	-75	$\mu A$
Bus Hold Low Overdrive Current <sup>(5)</sup>	$I_{BHLO}$	Input data pins, $V_I = 0V$ to $3.6V$ , $V_{CC} = 3.6V$	Full	500	200		$\mu A$
Bus Hold High Overdrive Current <sup>(5)</sup>	$I_{BHHO}$	Input data pins, $V_I = 0V$ to $3.6V$ , $V_{CC} = 3.6V$	Full		-280	-500	$\mu A$

## NOTES:

- When power is applied, data cannot be loaded into the latches to get the valuable test results.
- Other pins must be tied to  $V_{CC}$  or GND and should not be floating.
- $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.
- It is the increase in supply current for per input at the specified voltage level except  $V_{CC}$  or GND.
- It is the minimum overdrive current required to switch the input from one state to another.

**DYNAMIC CHARACTERISTICS**

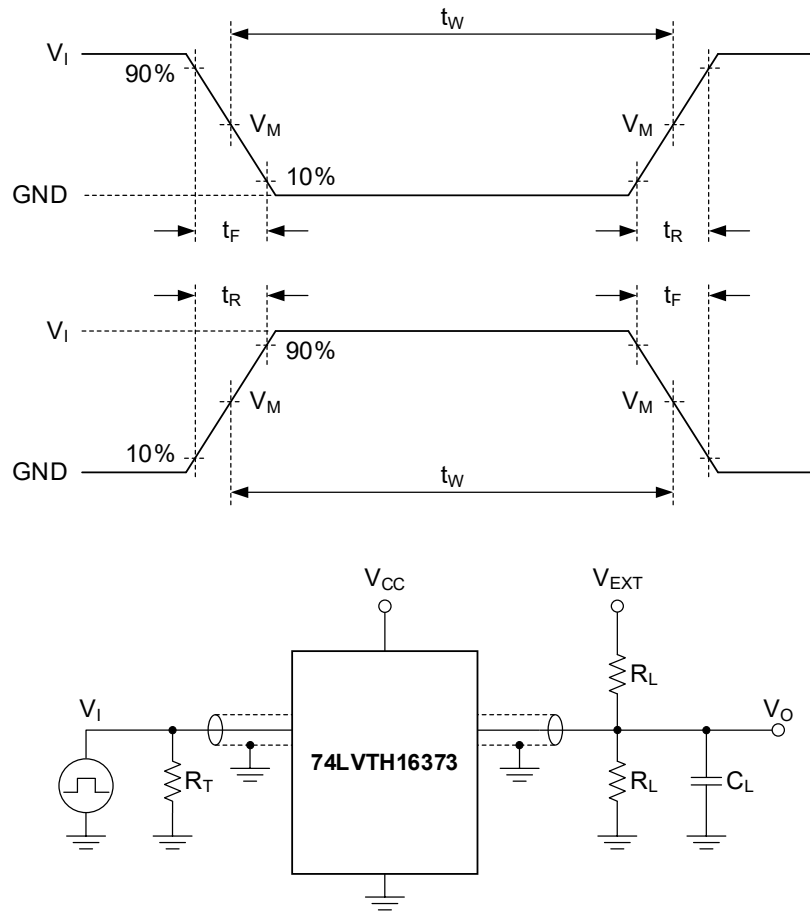
(See Figure 1 for test circuit. Full = -40°C to +125°C, all typical values are measured at  $V_{CC} = 3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN <sup>(1)</sup>	TYP	MAX <sup>(1)</sup>	UNITS
Low-to-High Propagation Delay	$t_{PLH}$	nDn to nQn, see Figure 2	$V_{CC} = 2.7V$	Full	3.6	8.5	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	3.4	
High-to-Low Propagation Delay	$t_{PHL}$	nDn to nQn, see Figure 2	$V_{CC} = 2.7V$	Full	3.2	6.2	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	3.0	
Low-to-High Propagation Delay	$t_{PLH}$	nLE to nQn, see Figure 3	$V_{CC} = 2.7V$	Full	3.8	8.8	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	3.6	
High-to-Low Propagation Delay	$t_{PHL}$	nLE to nQn, see Figure 3	$V_{CC} = 2.7V$	Full	3.4	6.0	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	3.2	
Off-to-High Propagation Delay	$t_{PZH}$	$\overline{nOE}$ to nQn, see Figure 4	$V_{CC} = 2.7V$	Full	4.2	9.4	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	4.0	
Off-to-Low Propagation Delay	$t_{PZL}$	$\overline{nOE}$ to nQn, see Figure 4	$V_{CC} = 2.7V$	Full	4.0	6.5	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	3.8	
High-to-Off Propagation Delay	$t_{PHZ}$	$\overline{nOE}$ to nQn, see Figure 4	$V_{CC} = 2.7V$	Full	4.4	7.6	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	4.0	
Low-to-Off Propagation Delay	$t_{PLZ}$	$\overline{nOE}$ to nQn, see Figure 4	$V_{CC} = 2.7V$	Full	4.2	6.8	ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	0.5	4.0	
High Setup Time	$t_{SUH}$	nDn to nLE, see Figure 5	$V_{CC} = 2.7V$	Full	2.0		ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	2.0		
Low Setup Time	$t_{SUL}$	nDn to nLE, see Figure 5	$V_{CC} = 2.7V$	Full	2.0		ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	2.0		
High Hold Time	$t_{HH}$	nDn to nLE, see Figure 5	$V_{CC} = 2.7V$	Full	1.2		ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	1.2		
Low Hold Time	$t_{HL}$	nDn to nLE, see Figure 5	$V_{CC} = 2.7V$	Full	1.2		ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	1.2		
High Pulse Width	$t_{WH}$	nLE, see Figure 3	$V_{CC} = 2.7V$	Full	3.3		ns
			$V_{CC} = 3.0V$ to $3.6V$	Full	3.3		

**NOTE:**

1. Specified by design and characterization, not production tested.

## TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

$R_L$ : Load resistance.

$C_L$ : Load capacitance (includes jig and probe).

$R_T$ : Termination resistance (equals to output impedance  $Z_O$  of the pulse generator).

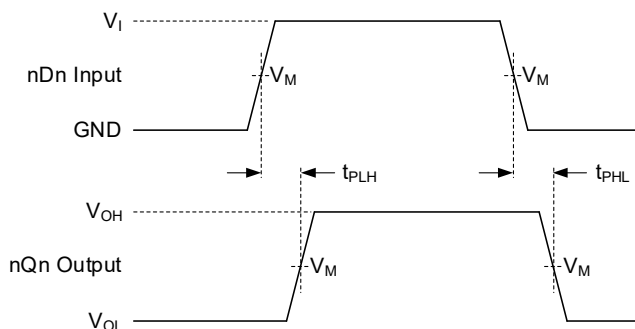
$V_{EXT}$ : External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT				LOAD		$V_{EXT}$		
$V_{CC}$	$V_I$	$f_i$	$t_W$	$t_R, t_F$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7V to 3.6V	2.7V	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	50pF	500 $\Omega$	GND	6V	Open

## WAVEFORMS

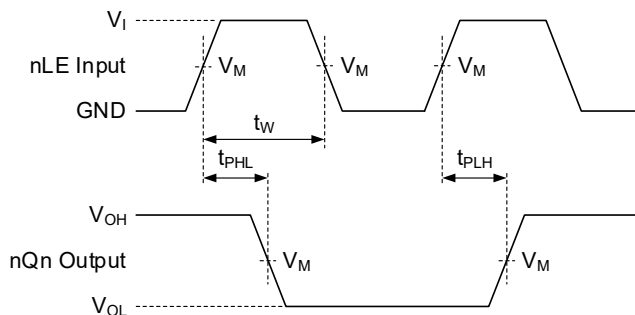


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Figure 2. Input nDn to Output nQn Propagation Delays**

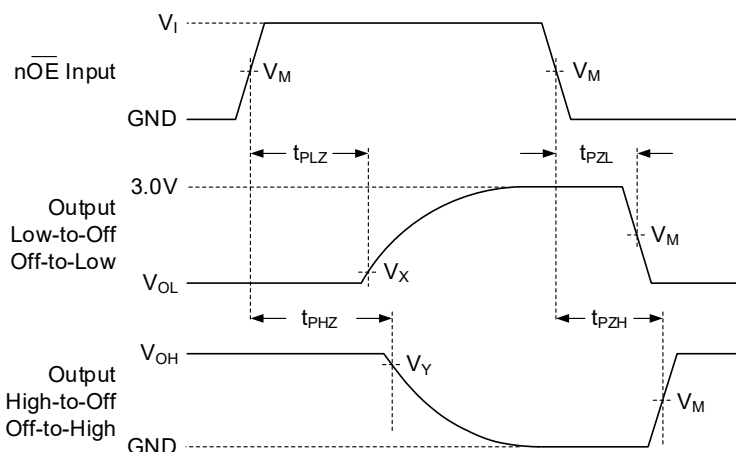


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Figure 3. The Latch Enable Input to Output Propagation Delays and Pulse Width**



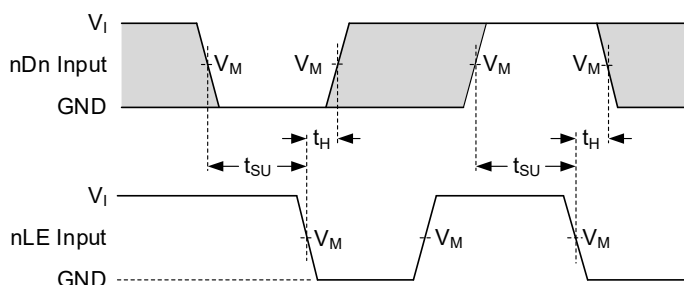
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Figure 4. Enable and Disable Times**

## WAVEFORMS (continued)



Test conditions are given in Table 1.

Measurement points are given in Table 2.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Data Setup and Hold Times for nDn Input to nLE Input

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
$V_{CC}$	$V_I$	$V_M^{(1)}$	$V_M$	$V_X$	$V_Y$
2.7V to 3.6V	2.7V	1.5V	1.5V	$V_{OL} + 0.3V$	$V_{OH} - 0.3V$

NOTE:

1. The measurement points should be  $V_{IH}$  or  $V_{IL}$  when the input rising or falling time exceeds 2.5ns.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## JANUARY 2024 – REV.A.1 to REV.A.2

Page

Updated Dynamic Characteristics section.....5

## NOVEMBER 2021 – REV.A to REV.A.1

Page

Updated HBM value in Absolute Maximum Ratings section.....2

## Changes from Original (MARCH 2021) to REV.A

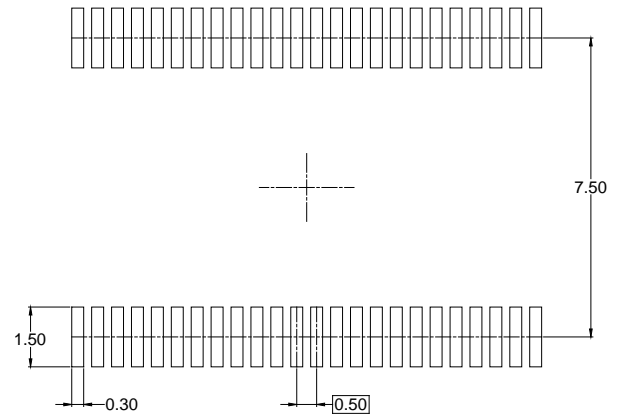
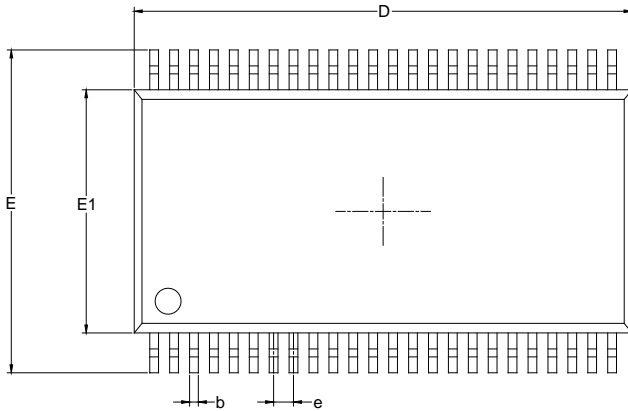
Page

Changed from product preview to production data.....All

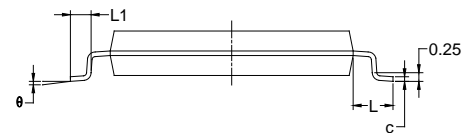
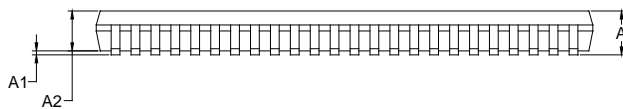


## PACKAGE OUTLINE DIMENSIONS

### TSSOP-48



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.18		0.26
c	0.15		0.19
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0°		8°

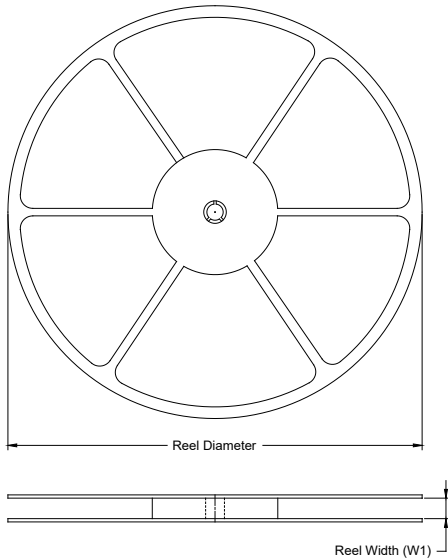
#### NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

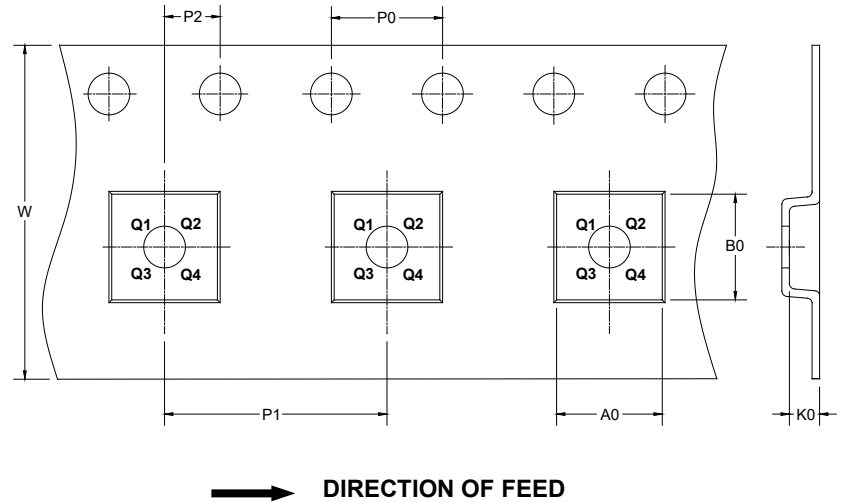
## PACKAGE INFORMATION

### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS



#### TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

#### KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-48	13"	24.4	8.60	13.00	1.80	4.0	12.0	2.0	24.0	Q1

DD00001

## PACKAGE INFORMATION

### CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

### KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002