# 74LVTN16245
# 3.3V, 16-Bit Transceiver with Direction Pin and 3-State Outputs

## GENERAL DESCRIPTION

The 74LVTN16245 is a 16-bit high-performance transceiver for 3.3V $V_{CC}$ operation, but with the capability to provide an interface to 5V system environment. The non-inverting 3-state bus compatible outputs are available in both sending and receiving directions.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. The direction control (nDIR) input determines the direction of the data flow. nDIR (active-high) enables data from nAn port to nBn port. nDIR (active-low) enables data from nBn port to nAn port. The output enable ($n\overline{OE}$) input, when high, disables both nAn and nBn ports by placing them in a high-impedance state.

## FEATURES

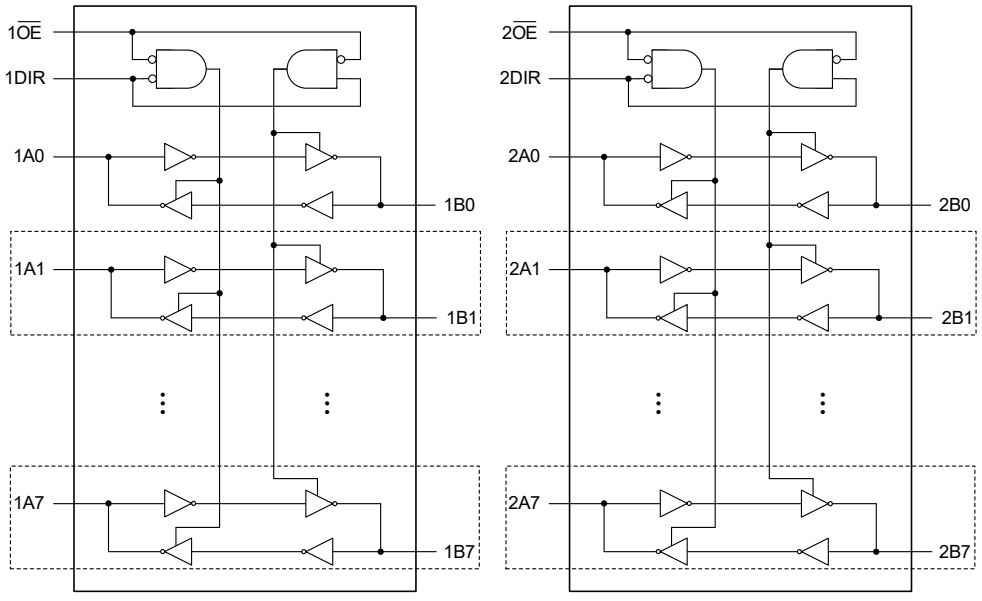
- **Wide Operating Voltage Range: 2.7V to 3.6V**
- **Input and Output Interface Capability to 5V System Environment**
- **+64mA/-32mA Output Current**
- **3-State Outputs Drive Bus Lines Directly**
- **Power-Up and $I_{OFF}$ 3-State**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-48 Package**

## FUNCTION TABLE

| CONTROL INPUT | | INPUT/OUTPUT | |
|---|---|---|---|
| **$n\overline{OE}$** | **nDIR** | **nAn** | **nBn** |
| L | L | nAn = nBn | Inputs |
| L | H | Inputs | nBn = nAn |
| H | *X* | Z | Z |

H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance State
*X* = Don't Care

## LOGIC DIAGRAM

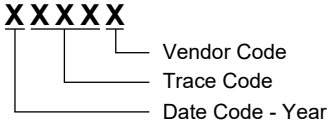


# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| 74LVTN16245 | TSSOP-48 | -40℃ to +125℃ | 74LVTN16245XTS48G/TR | 74LVTN16245<br>XTS48<br>XXXXX | Tape and Reel, 2500 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, $V_{CC}$ ..... -0.5V to 4.6V
Input Voltage Range, $V_I$ (2) ..... -0.5V to 7.0V
Output Voltage Range, $V_O$ (2)
3-State or High-State ..... -0.5V to 7.0V
Input Clamping Current, $I_{IK}$ ($V_I$ < 0V) ..... -50mA
Output Clamping Current, $I_{OK}$ ($V_O$ < 0V) ..... -50mA
Output Current, $I_O$
High-State ..... -64mA
Low-State ..... 128mA
Supply Current, $I_{CC}$ ..... 128mA
Ground Current, $I_{GND}$ ..... -256mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 8000V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, $V_{CC}$ ..... 2.7V to 3.6V
Input Voltage Range, $V_I$ ..... 0V to 5.5V
High-Level Output Current, $I_{OH}$ ..... -32mA
Low-Level Output Current, $I_{OL}$ ..... 64mA
Input Transition Rise or Fall Rate, Δt/ΔV ..... 10ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## ESD SENSITIVITY CAUTION

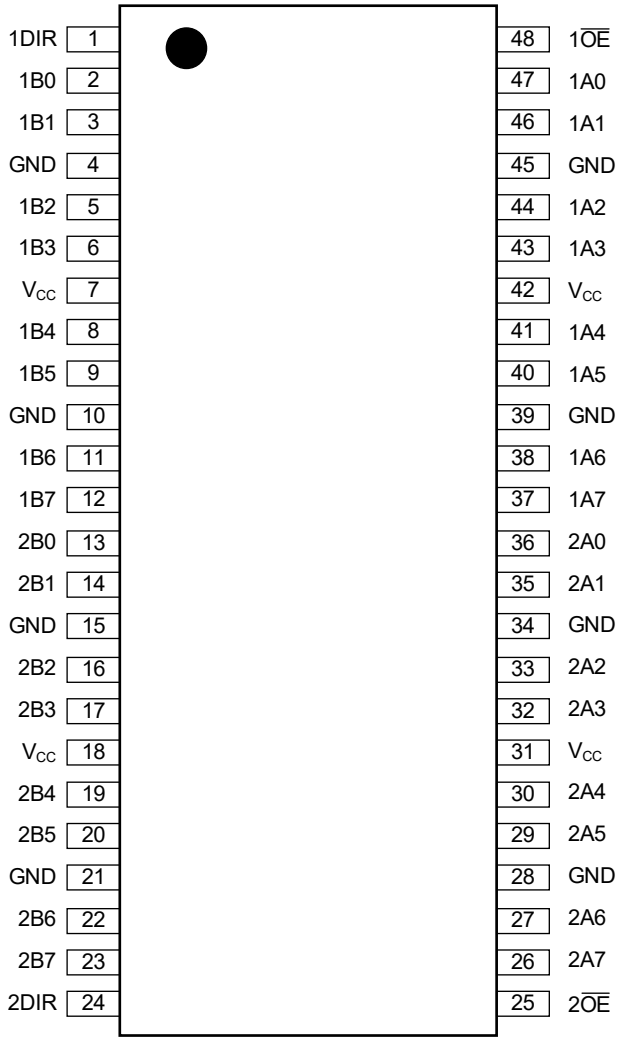
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




TSSOP-48

## PIN DESCRIPTION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 24 | 1DIR, 2DIR | Direction Control Inputs. |
| 2, 3, 5, 6, 8, 9, 11, 12 | 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | Data Inputs/Outputs. |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | Data Inputs/Outputs. |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground. |
| 7, 18, 31, 42 | $V_{CC}$ | Supply Voltage. |
| 48, 25 | $1\overline{OE}$, $2\overline{OE}$ | Output Enable Inputs (Active-Low). |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | Data Inputs/Outputs. |
| 47, 46, 44, 43, 41, 40, 38, 37 | 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | Data Inputs/Outputs. |

## ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at $V_{CC}$ = 3.3V and $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Input Clamping Voltage | $V_{IK}$ | $V_{CC}$ = 2.7V, $I_{IK}$ = -18mA | | Full | -1.2 | -0.78 | | V |
| High-Level Input Voltage | $V_{IH}$ | $V_{CC}$ = 2.7V to 3.6V | | Full | 2.0 | | | V |
| Low-Level Input Voltage | $V_{IL}$ | $V_{CC}$ = 2.7V to 3.6V | | Full | | | 0.8 | V |
| High-Level Output Voltage | $V_{OH}$ | $V_{CC}$ = 2.7V to 3.6V, $I_{OH}$ = -100μA | | Full | $V_{CC}$ - 0.05 | $V_{CC}$ - 0.001 | | V |
| | | $V_{CC}$ = 2.7V, $I_{OH}$ = -8mA | | Full | 2.45 | 2.60 | | |
| | | $V_{CC}$ = 3.0V, $I_{OH}$ = -32mA | | Full | 2.10 | 2.65 | | |
| Low-Level Output Voltage | $V_{OL}$ | $V_{CC}$ = 2.7V, $I_{OL}$ = 100μA | | Full | | 0.001 | 0.05 | V |
| | | $V_{CC}$ = 2.7V, $I_{OL}$ = 24mA | | Full | | 0.15 | 0.28 | |
| | | $V_{CC}$ = 3.0V, $I_{OL}$ = 16mA | | Full | | 0.1 | 0.18 | |
| | | $V_{CC}$ = 3.0V, $I_{OL}$ = 32mA | | Full | | 0.2 | 0.36 | |
| | | $V_{CC}$ = 3.0V, $I_{OL}$ = 64mA | | Full | | 0.4 | 0.55 | |
| Input Leakage Current | $I_I$ | Control pins, $V_{CC}$ = 3.6V, $V_I$ = $V_{CC}$ or GND | | Full | | ±0.01 | ±1 | μA |
| | | Control pins, $V_{CC}$ = 0V or 3.6V, $V_I$ = 5.5V | | Full | | 0.01 | 5 | |
| | | Input/output data pins (1), $V_{CC}$ = 3.6V, $V_I$ = 5.5V | | Full | | 1 | 5 | |
| | | Input/output data pins (1), $V_{CC}$ = 3.6V, $V_I$ = $V_{CC}$ | | Full | | 0.01 | 1 | |
| | | Input/output data pins (1), $V_{CC}$ = 3.6V, $V_I$ = 0V | | Full | -2 | -0.01 | | |
| Output Leakage Current | $I_{LO}$ | Outputs in high-state when $V_O$ > $V_{CC}$, $V_{CC}$ = 3.0V, $V_O$ = 5.5V | | Full | | 1 | 30 | μA |
| Power-Up/Down Output Current | $I_{O\_PU/PD}$ | $V_{CC}$ ≤ 1.2V, $V_O$ = 0.5V to $V_{CC}$, $V_I$ = GND or $V_{CC}$, $n\overline{OE}$ = don't care | | +25℃ | | 0.01 | 10 | μA |
| Power-Off Leakage Current | $I_{OFF}$ | $V_{CC}$ = 0V, $V_I$ or $V_O$ = 0V to 5.5V | | Full | | 0.01 | 10 | μA |
| Supply Current | $I_{CC}$ | $V_{CC}$ = 3.6V, $V_I$ = GND or $V_{CC}$, $I_O$ = 0A | Outputs high | Full | | 16 | 90 | μA |
| | | | Outputs low | Full | | 16 | 90 | |
| | | | Outputs disabled (2) | Full | | 16 | 85 | |
| Additional Supply Current | $\Delta I_{CC}$ | Per input pin, $V_{CC}$ = 3.0V to 3.6V, one input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | Full | | 0.2 | 80 | μA |
| Input Capacitance | $C_I$ | nDIR and $n\overline{OE}$ inputs, $V_I$ = 0Vor 3.0V | | +25℃ | | 6 | | pF |
| Input/Output Capacitance | $C_{I/O}$ | At input/output data pins, outputs disabled, $V_{I/O}$ = 0V or 3.0V | | +25℃ | | 9 | | pF |

NOTES:

1. Other pins must be tied to $V_{CC}$ or GND and should not be floating.
2. $I_{CC}$ is measured with outputs pulled to $V_{CC}$ or GND.

## DYNAMIC CHARACTERISTICS

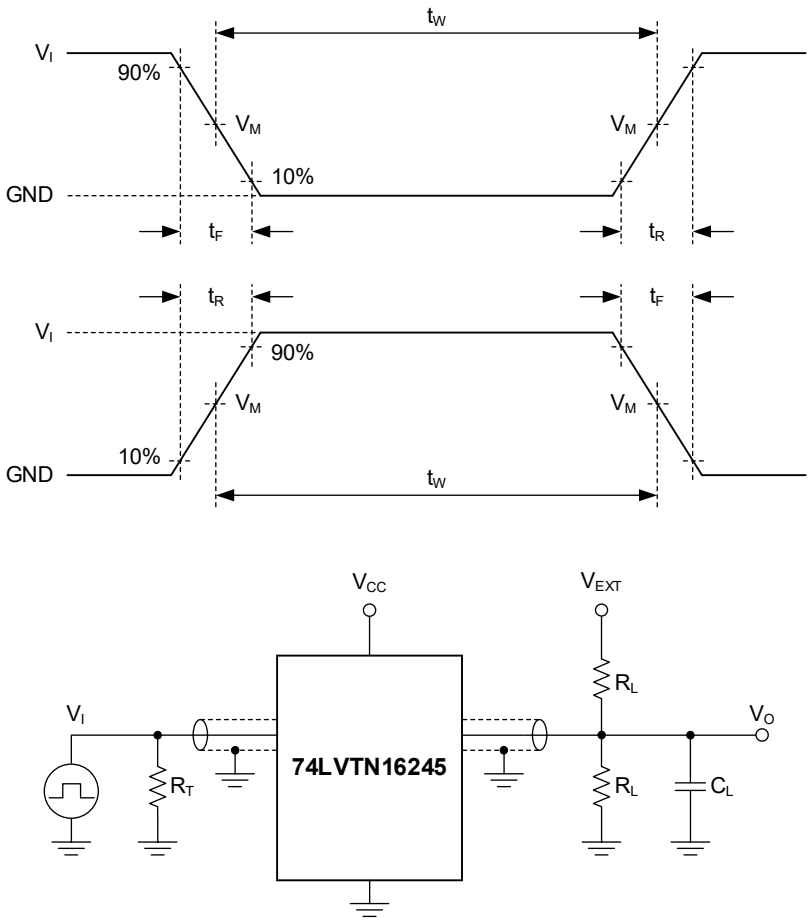
(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at $V_{CC}$ = 3.3V and $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | TEMP | MIN (1) | TYP | MAX (1) | UNITS |
|---|---|---|---|---|---|---|---|---|
| Low-to-High Propagation Delay | $t_{PLH}$ | nAn to nBn or nBn to nAn, see Figure 2 | $V_{CC}$ = 2.7V | Full | | 3.6 | 8.5 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 3.4 | 7.2 | |
| High-to-Low Propagation Delay | $t_{PHL}$ | nAn to nBn or nBn to nAn, see Figure 2 | $V_{CC}$ = 2.7V | Full | | 3.2 | 6.2 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 3.0 | 5.6 | |
| Off-to-High Propagation Delay | $t_{PZH}$ | $n\overline{OE}$ to nAn or nBn, see Figure 3 | $V_{CC}$ = 2.7V | Full | | 4.2 | 9.4 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 4.0 | 7.8 | |
| Off-to-Low Propagation Delay | $t_{PZL}$ | $n\overline{OE}$ to nAn or nBn, see Figure 3 | $V_{CC}$ = 2.7V | Full | | 4.0 | 6.5 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 3.8 | 6.2 | |
| High-to-Off Propagation Delay | $t_{PHZ}$ | $n\overline{OE}$ to nAn or nBn, see Figure 3 | $V_{CC}$ = 2.7V | Full | | 4.4 | 7.6 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 4.0 | 7.0 | |
| Low-to-Off Propagation Delay | $t_{PLZ}$ | $n\overline{OE}$ to nAn or nBn, see Figure 3 | $V_{CC}$ = 2.7V | Full | | 4.2 | 6.8 | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | Full | 0.5 | 4.0 | 6.5 | |

NOTE:

1. Specified by design and characterization, not production tested.

## TEST CIRCUIT




Test conditions are given in Table 1.

Definitions for test circuit:

$R_L$: Load resistance.

$C_L$: Load capacitance (includes jig and probe).

$R_T$: Termination resistance (equals to output impedance $Z_O$ of the pulse generator).

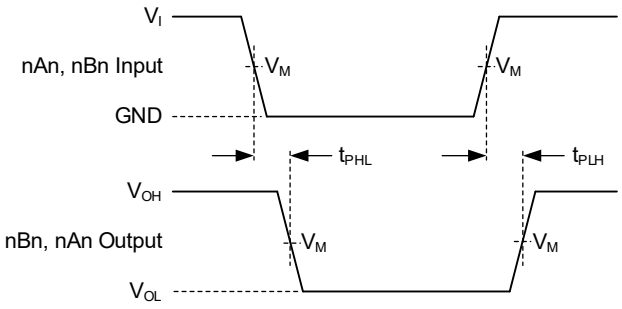
$V_{EXT}$: External voltage is used to measure switching time.

**Figure 1. Test Circuit for Measuring Switching Times**

**Table 1. Test Conditions**

| SUPPLY VOLTAGE | INPUT | | LOAD | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_R$, $t_F$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 2.7V to 3.6V | 2.7V | ≤ 2.5ns | 50pF | 500Ω | GND | 6V | Open |

## WAVEFORMS

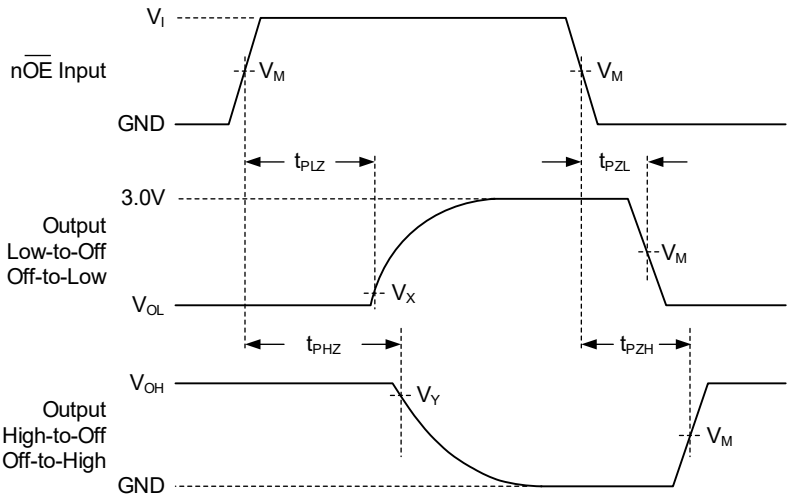



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Figure 2. Input (nAn, nBn) to Output (nBn, nAn) Propagation Delays**




Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Figure 3. Enable and Disable Times**

**Table 2. Measurement Points**

| SUPPLY VOLTAGE | INPUT | | OUTPUT | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ (1) | $V_M$ | $V_X$ | $V_Y$ |
| 2.7V to 3.6V | 2.7V | 1.5V | 1.5V | $V_{OL}$ + 0.3V | $V_{OH}$ - 0.3V |

NOTE:

1. The measurement points should be $V_{IH}$ or $V_{IL}$ when the input rising or falling time exceeds 2.5ns.

# REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

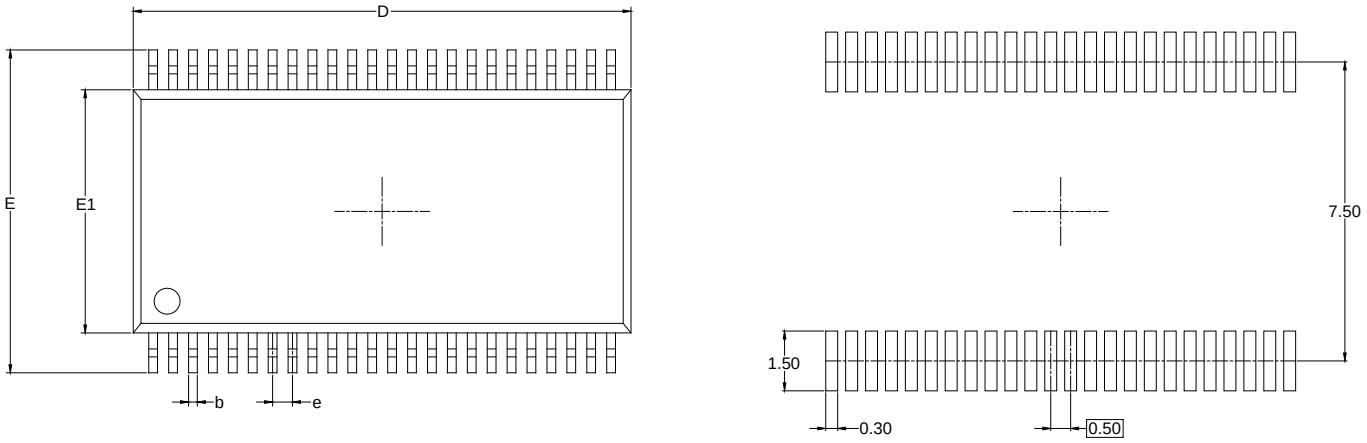
| JANUARY 2024 – REV.A.1 to REV.A.2 | Page |
|---|---|
| Updated Dynamic Characteristics section | 5 |

| JANUARY 2022 – REV.A to REV.A.1 | Page |
|---|---|
| Updated $I_I$ and $I_{CC}$ values in Electrical Characteristics section | 4 |

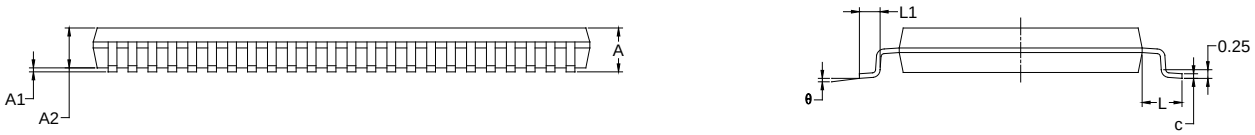
| Changes from Original (MARCH 2021) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

## TSSOP-48




**RECOMMENDED LAND PATTERN** (Unit: mm)

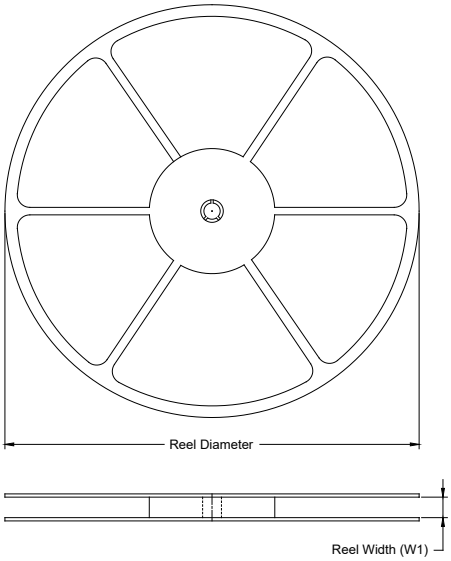



| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | | | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.95 | 1.05 |
| b | 0.18 | | 0.26 |
| c | 0.15 | | 0.19 |
| D | 12.40 | 12.50 | 12.60 |
| E | 7.90 | 8.10 | 8.30 |
| E1 | 6.00 | 6.10 | 6.20 |
| e | 0.50 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.45 | | 0.75 |
| θ | 0° | | 8° |

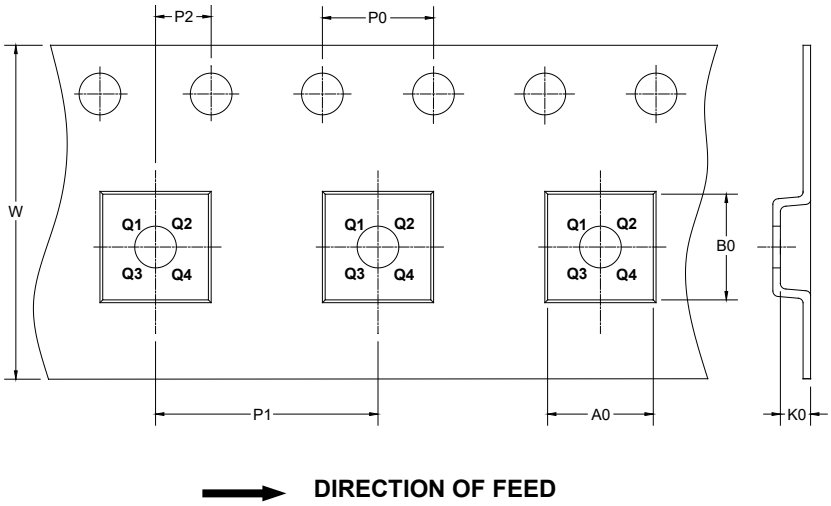
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



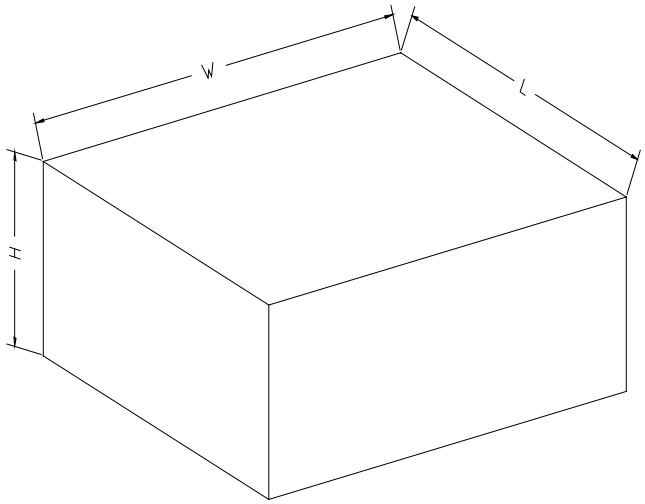

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP-48 | 13” | 24.4 | 8.60 | 13.00 | 1.80 | 4.0 | 12.0 | 2.0 | 24.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002