74AHC541
Octal Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The 74AHC541 is an octal buffer/line driver with 3-state outputs, which can accept supply voltage range from 2.0V to 5.5V.

The 3-state control gate is a two-input AND gate with active low inputs. $\overline{OE}1$ and $\overline{OE}2$ are two output enable inputs. When $\overline{OE}1$ and $\overline{OE}2$ are low, data transmits from An inputs to the Yn outputs. When $\overline{OE}1$ or $\overline{OE}2$ is high, all outputs are in high-impedance state.

$\overline{OE}1$ and $\overline{OE}2$ should be connected to V_{CC} by using a pull-up resistor to ensure the high-impedance state in the period of power-up or power-down, and the minimum of the resistor depends on the current-sinking capability of the driver.

FEATURES

- **Wide Supply Voltage Range: 2.0V to 5.5V**
- **+8mA/-8mA Output Current**
- **3-State Buffers**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-20 and TSSOP-20 Packages**

APPLICATIONS

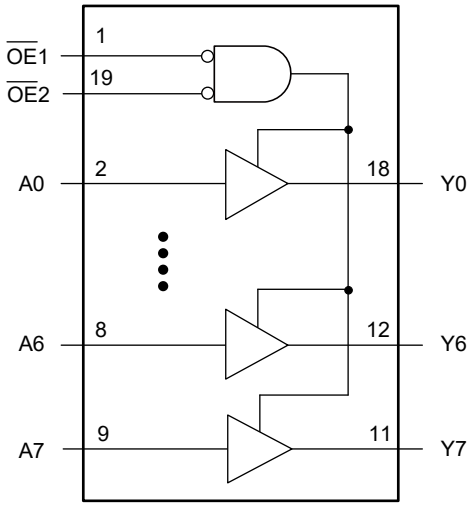
Mother Board for Server, PC and Notebook Pad
Telecom Equipment
LED Display
Industrial/Medical Equipment

FUNCTION TABLE

INPUT			OUTPUT
$\overline{OE}1$	$\overline{OE}2$	An	Yn
L	L	L	L
L	L	H	H
H	*X*	*X*	Z
X	H	*X*	Z

H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance State
X = Don't Care

LOGIC DIAGRAM

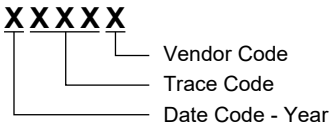


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC541	SOIC-20	-40℃ to +125℃	74AHC541XS20G/TR	74AHC541XS20 XXXXX	Tape and Reel, 1500
	TSSOP-20	-40℃ to +125℃	74AHC541XTS20G/TR	05RXTS20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 7.0V
Input Voltage, V_I (2) ..... -0.5V to 7.0V
Output Voltage, V_O (2) ..... -0.5V to MIN (7.0V, V_{CC} + 0.5V)
Input Clamping Current, I_{IK} (V_I < 0V) ..... -20mA
Output Clamping Current, I_{OK} (V_O < 0V or V_O > V_{CC}) ... ±20mA
Output Current, I_O (V_O < 0V to V_{CC}) ..... ±25mA
Supply Current, I_{CC} 75mA
Ground Current, I_{GND} ..... -75mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 2.0V to 5.5V
Input Voltage, V_I ..... 0V to 5.5V
Output Voltage, V_O ..... 0V to V_{CC}
Output Current, I_O ..... ±8mA
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 3.3V ± 0.3V ..... 100ns/V (MAX)
V_{CC} = 5.0V ± 0.5V ..... 20ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

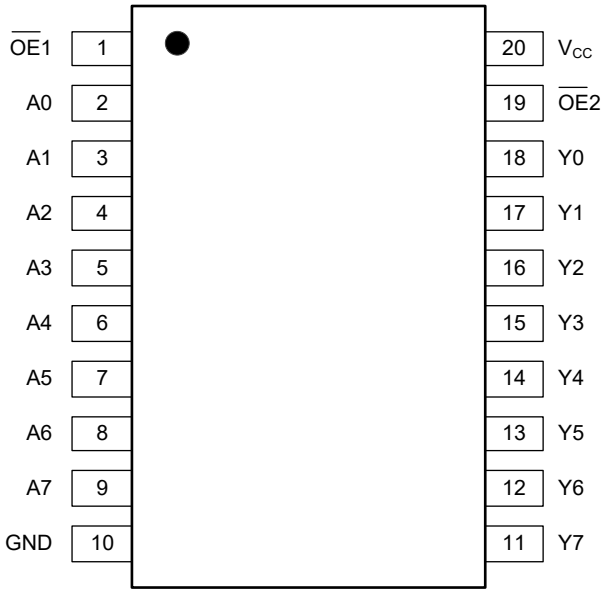
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOIC-20/TSSOP-20

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 19	$\overline{OE}$1, $\overline{OE}$2	Output Enable Inputs (Active Low).
2, 3, 4, 5, 6, 7, 8, 9	A0, A1, A2, A3, A4, A5, A6, A7	Data Inputs.
18, 17, 16, 15, 14, 13, 12, 11	Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7	Data Outputs.
10	GND	Ground.
20	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		Full	1.5			V
		V_{CC} = 3.0V		Full	2.1			
		V_{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V		Full			0.5	V
		V_{CC} = 3.0V		Full			0.9	
		V_{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V_{OH}	I_{OH} = -50μA	V_{CC} = 2.0V	Full	1.9	1.99		V
			V_{CC} = 3.0V	Full	2.9	2.99		
			V_{CC} = 4.5V	Full	4.4	4.49		
		I_{OH} = -4.0mA	V_{CC} = 3.0V	Full	2.48	2.8		
		I_{OH} = -8.0mA	V_{CC} = 4.5V	Full	3.8	4.25		
Low-Level Output Voltage	V_{OL}	I_{OL} = 50μA	V_{CC} = 2.0V	Full		0.01	0.1	V
			V_{CC} = 3.0V	Full		0.01	0.1	
			V_{CC} = 4.5V	Full		0.01	0.1	
		I_{OL} = 4.0mA	V_{CC} = 3.0V	Full		0.15	0.5	
		I_{OH} = 8.0mA	V_{CC} = 4.5V	Full		0.25	0.5	
Input Leakage Current	I_I	V_I = 5.5V or GND, V_{CC} = 0V to 5.5V		Full		±0.02	±1	μA
Off-State Output Current (1)	I_{OZ}	V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND, V_{CC} = 5.5V		Full		±0.02	±2	μA
Supply Current	I_{CC}	V_I = V_{CC} or GND, I_O = 0A, V_{CC} = 5.5V		Full		±0.02	±2	μA
Input Capacitance	C_I			+25℃		7		pF
Output Capacitance	C_O			+25℃		7		pF

NOTE:

1. For I/O ports, the parameter I_{OZ} includes the input leakage current.

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	An to Yn, V_{CC} = 3.3V ± 0.3V	C_L = 15pF	Full	1.0	4.5	8.5	ns
			C_L = 50pF	Full	1.0	5.5	13.5	
		An to Yn, V_{CC} = 5.0V ± 0.5V	C_L = 15pF	Full	1.0	3.5	6.0	
			C_L = 50pF	Full	1.0	4.5	8.5	
Enable Time (2)	t_{EN}	$\overline{OE}$n to Yn V_{CC} = 3.3V ± 0.3V	C_L = 15pF	Full	1.0	8.0	13.0	ns
			C_L = 50pF	Full	1.0	9.5	18.0	
		$\overline{OE}$n to Yn V_{CC} = 5.0V ± 0.5V	C_L = 15pF	Full	1.0	6.0	8.5	
			C_L = 50pF	Full	1.0	6.5	11.5	
Disable Time (2)	t_{DIS}	$\overline{OE}$n to Yn V_{CC} = 3.3V ± 0.3V	C_L = 15pF	Full	1.0	11.5	14.0	ns
			C_L = 50pF	Full	1.0	12.5	16.0	
		$\overline{OE}$n to Yn V_{CC} = 5.0V ± 0.5V	C_L = 15pF	Full	1.0	6.0	8.0	
			C_L = 50pF	Full	1.0	6.5	10.5	
Channel-to-Channel Skew	t_{SKO}	V_{CC} = 3.3V ± 0.3V	C_L = 50pF	+25℃		0.5		ns
		V_{CC} = 5.0V ± 0.5V	C_L = 50pF	+25℃		0.5		
Power Dissipation Capacitance (3)	C_{PD}	No load, f = 1MHz, V_{CC} = 5.0V		+25℃		14.0		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

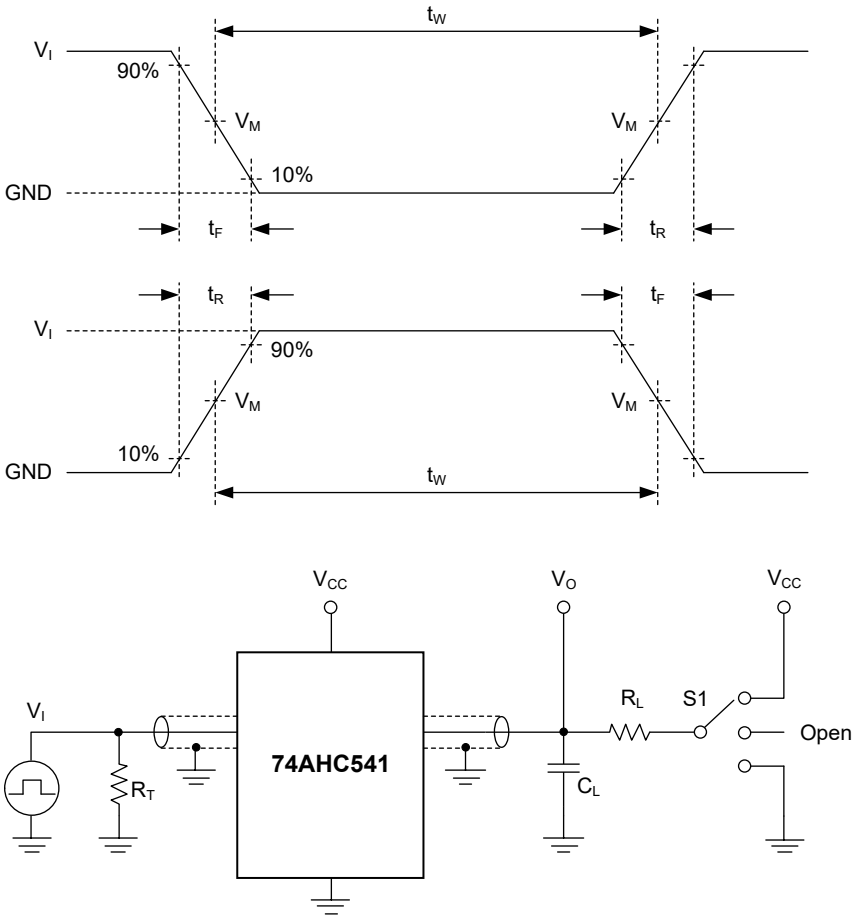
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

NOISE CHARACTERISTICS

(All typical values are measured at V_{CC} = 5.0V and T_A = +25℃, C_L = 50pF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Maximum Dynamic Low-Level Output Voltage	V_{OLDMAX}	Quiet Output	+25℃		0.3		V
Minimum Dynamic Low-Level Output Voltage	V_{OLDMIN}	Quiet Output	+25℃		-0.3		V
Minimum Dynamic High-Level Output Voltage	V_{OHDMIN}	Quiet Output	+25℃		4.75		V
Dynamic High-Level Input Voltage	V_{IHD}		Full	3.5			V
Dynamic Low-Level Input Voltage	V_{ILD}		Full			1.5	V

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

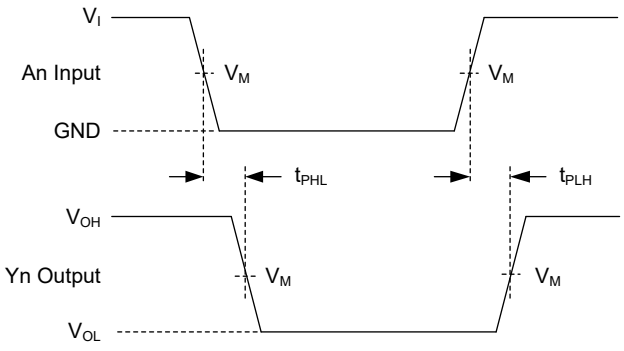
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

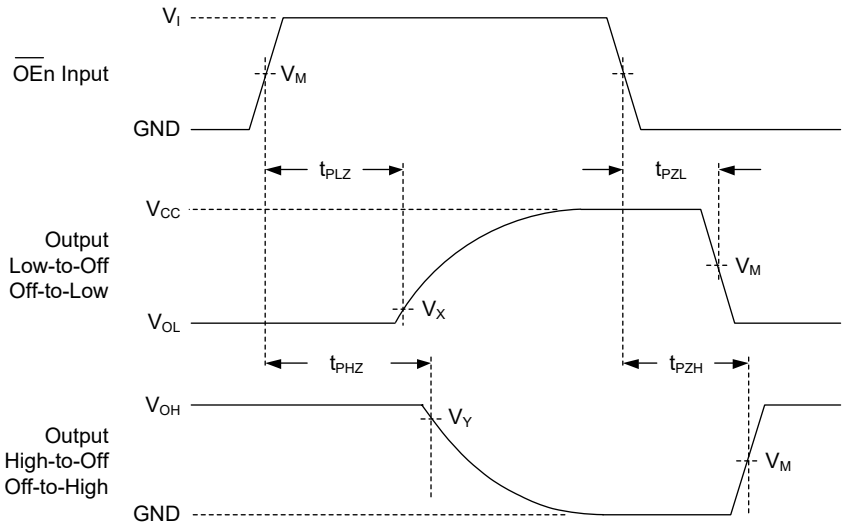
SUPPLY VOLTAGE	INPUT		LOAD		S1		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.0V to 5.5V	GND to V_{CC}	≤ 3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (An) to Output (Yn) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
2.0V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

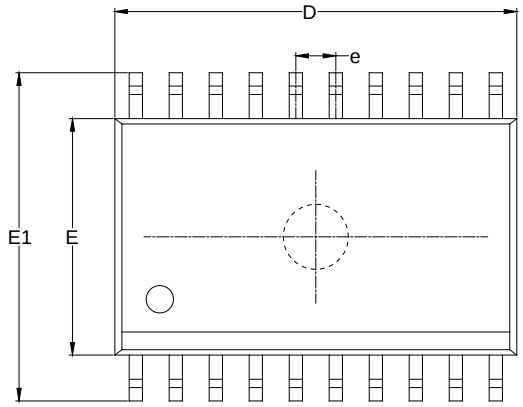
REVISION HISTORY

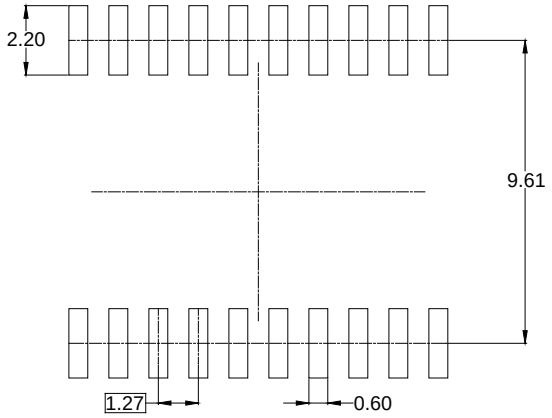
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MARCH 2023) to REV.A	Page
Changed from product preview to production data	All

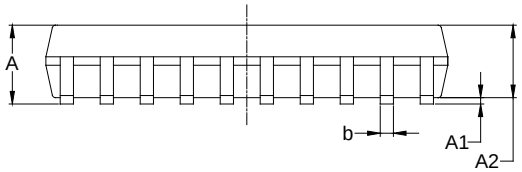
PACKAGE OUTLINE DIMENSIONS

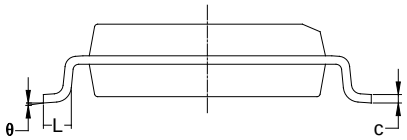
SOIC-20





RECOMMENDED LAND PATTERN (Unit: mm)



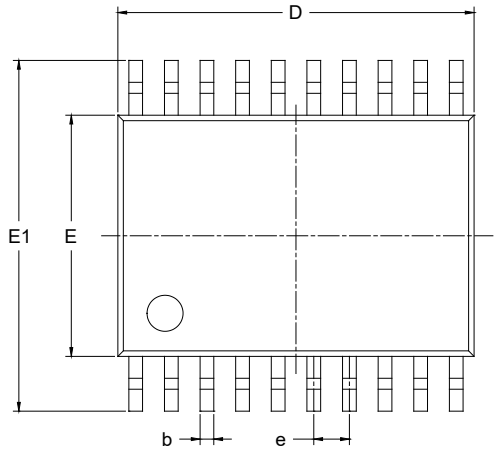


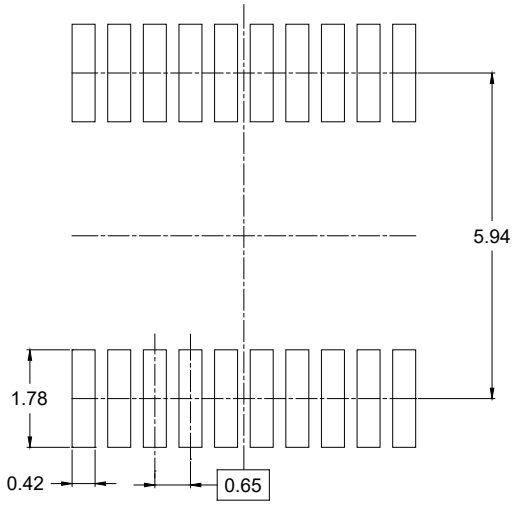
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

TSSOP-20





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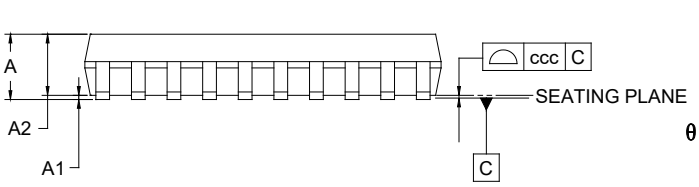
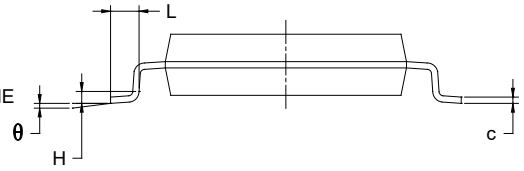


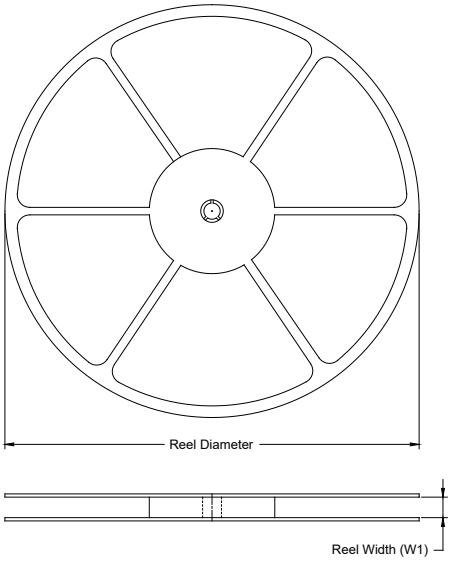


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

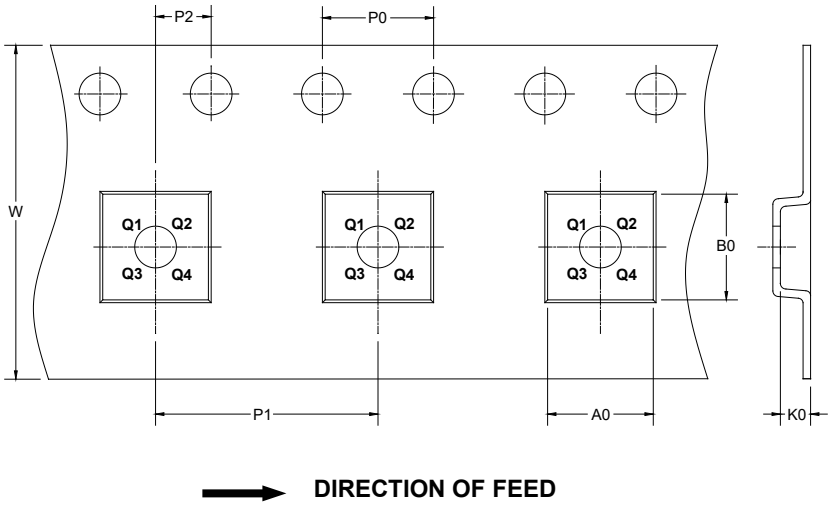
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



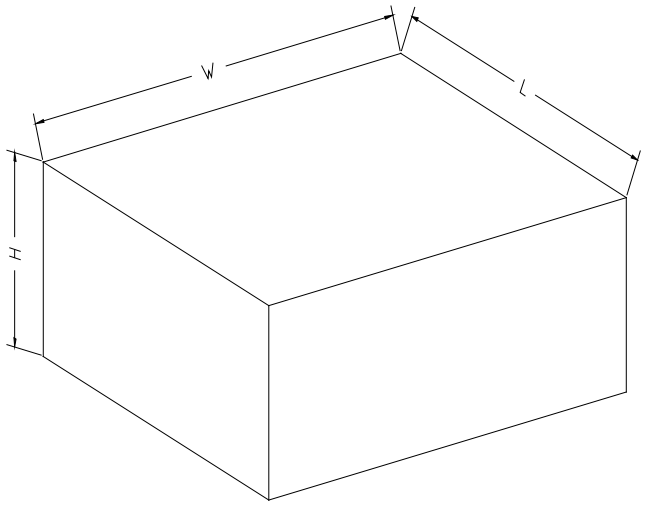
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-20	13″	24.4	10.90	13.30	3.00	4.0	12.0	2.0	24.0	Q1
TSSOP-20	13″	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002