

GENERAL DESCRIPTION

The 74HC165 is an 8-bit parallel-load shift register with a wide operating voltage range of 2.0V to 5.5V. When the shift/load input is low, eight parallel data inputs (A to H) are enabled and allowed to enter each stage. Data is shifted to a serial output when the device is clocked. The device also provides a complementary serial output.

When the shift/load input is high and the clock inhibit input is low, the clock transition can be completed by a low-to-high transition of the clock input. Due to the interchangeable function of the clock input and the clock inhibit input, the clock transition also can be completed by a low level of the clock input and a low-to-high transition of the clock inhibit input. When the shift/load input remains high, parallel load is inhibited. When the shift/load input remains low, parallel inputs enter the register, independent of other inputs.

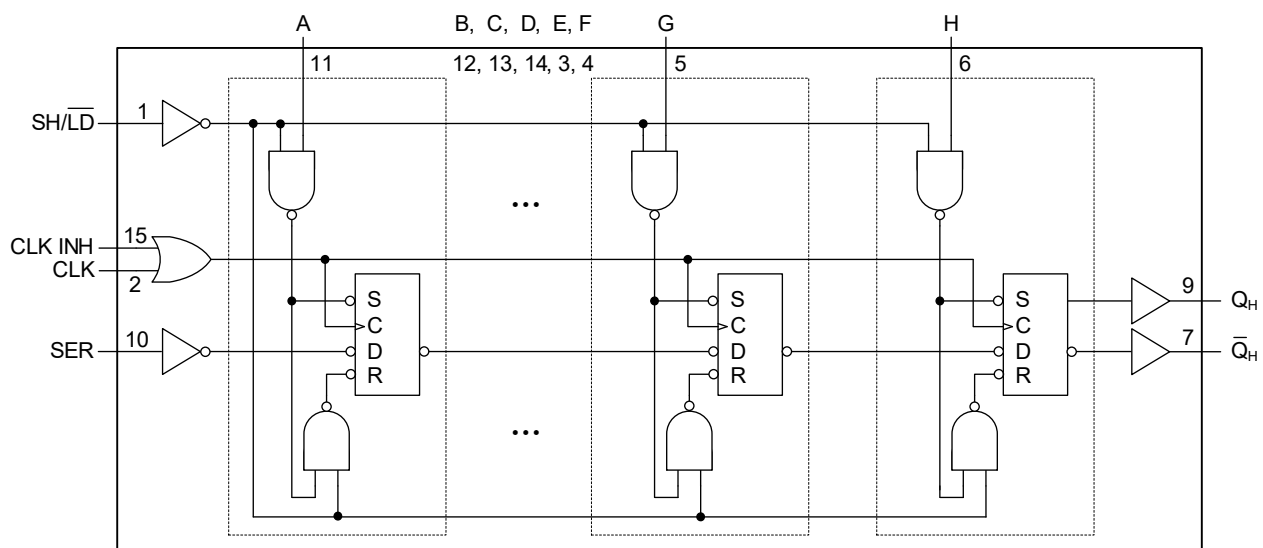
FEATURES

- **Wide Supply Voltage Range: 2.0V to 5.5V**
- **+5.2mA/-5.2mA Output Current**
- **Synchronous Serial Input**
- **CMOS Low Power Dissipation**
- **Data Transformation of Parallel-to-Serial**
- **-40°C to +125°C Operating Temperature Range**
- **Available in Green SOIC-16 and TSSOP-16 Packages**

APPLICATIONS

Programmable Logic Controller
System of Video Display
Output Expander and Keyboard
Appliance

LOGIC DIAGRAM



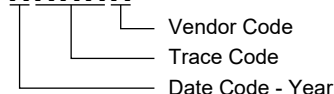
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HC165	SOIC-16	-40°C to +125°C	74HC165XS16G/TR	74HC165XS16 XXXXX	Tape and Reel, 2500
	TSSOP-16	-40°C to +125°C	74HC165XTS16G/TR	74HC165 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage Range, V_{CC}	-0.5V to 7.0V
Input Voltage Range, V_I ⁽²⁾	-0.5V to MIN(7.0V, $V_{CC} + 0.5V$)
Output Voltage Range, V_O ⁽²⁾	-0.5V to MIN(7.0V, $V_{CC} + 0.5V$)
Input Clamp Current, I_{IK} ($V_I < 0V$ or $V_I > V_{CC}$)	 $\pm 20mA$ (MAX)
Output Clamp Current, I_{OK} ($V_O < 0V$ or $V_O > V_{CC}$)	 $\pm 20mA$ (MAX)
Continuous Output Current, I_O ($V_O = 0V$ to V_{CC})	 $\pm 25mA$ (MAX)
Continuous Current through V_{CC} or GND	 $\pm 50mA$ (MAX)
Junction Temperature ⁽³⁾	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	6000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}	2.0V to 5.5V
Input Voltage Range, V_I	0V to V_{CC}
Output Voltage Range, V_O	0V to V_{CC}
Output Current, I_O	 $\pm 5.2mA$
Input Transition Rise or Fall Rate, $\Delta t/\Delta V$	
$V_{CC} = 2.0V$	1000ns/V (MAX)
$V_{CC} = 4.5V$	500ns/V (MAX)
$V_{CC} = 5.5V$	400ns/V (MAX)
Operating Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

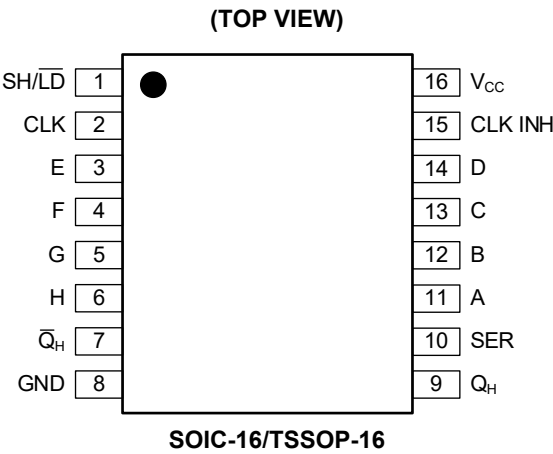
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	SH/LD	Shift/Load Input. Data is shifted at high level and data is loaded from parallel inputs at low level.
2	CLK	Clock Input (Low-to-High Clock Transition, Edge-Triggered).
3, 4, 5, 6	E, F, G, H	Parallel Inputs.
7	Q _H	Complementary Serial Output.
8	GND	Ground.
9	Q _H	Serial Output.
10	SER	Serial Input.
11, 12, 13, 14	A, B, C, D	Parallel Inputs.
15	CLK INH	Clock Inhibit Input (Active-Low). There is no change in output at high level.
16	V _{CC}	Supply Voltage.

FUNCTION TABLE

OPERATING MODES	INPUT					Q _A to Q _G REGISTERS		OUTPUT	
	SH/LD	CLK INH	CLK	SER	A to H	Q _A	Q _B to Q _G	Q _H	$\bar{Q}_H$
Parallel Load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
Serial Shift	H	L	↑	l	X	L	q _A to q _F	q _G	$\bar{q}_G$
	H	L	↑	h	X	H	q _A to q _F	q _G	$\bar{q}_G$
	H	↑	L	l	X	L	q _A to q _F	q _G	$\bar{q}_G$
	H	↑	L	h	X	H	q _A to q _F	q _G	$\bar{q}_G$
No Change	H	H	X	X	X	q _A	q _B to q _G	q _H	$\bar{q}_H$
	H	X	H	X	X	q _A	q _B to q _G	q _H	$\bar{q}_H$

H = High voltage level.

h = High voltage level one setup time before clock rising edge ↑.

L = Low voltage level.

l = Low voltage level one setup time before clock rising edge ↑.

q = The state of the referenced output one setup time before clock rising edge ↑.

↑ = Low-to-high clock transition.

X = Don't care.

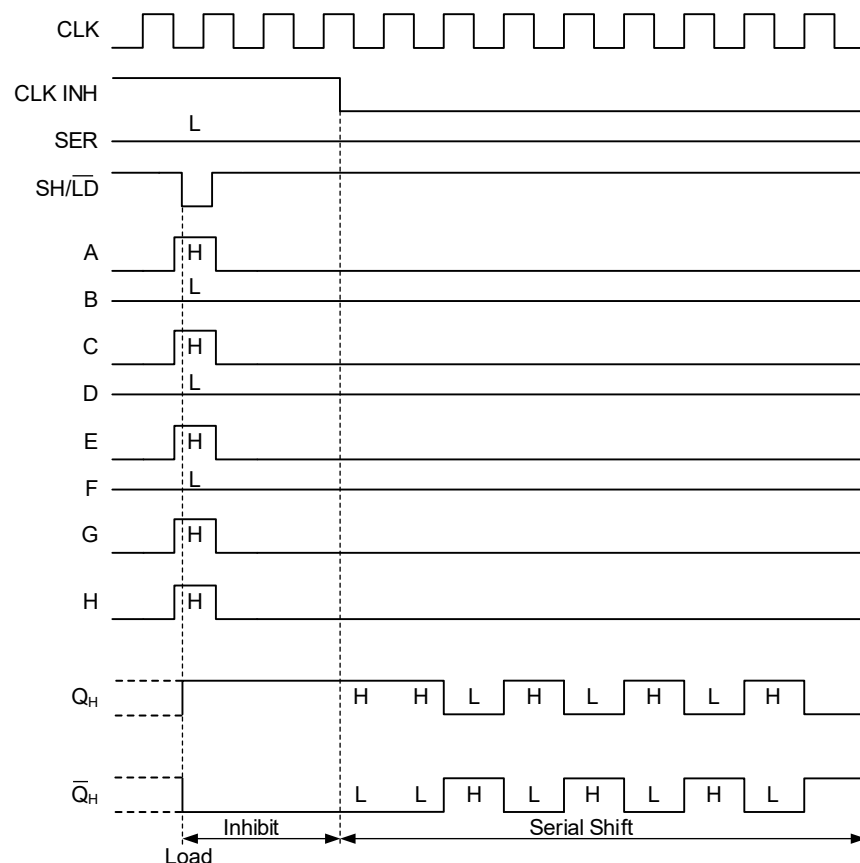


Figure 1. Timing Diagram

ELECTRICAL CHARACTERISTICS(Full = -40°C to +125°C, all typical values are measured at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V _{IH}	V _{CC} = 2.0V	Full	1.50			V
		V _{CC} = 4.5V	Full	3.15			
		V _{CC} = 5.5V	Full	3.85			
Low-Level Input Voltage	V _{IL}	V _{CC} = 2.0V	Full			0.50	V
		V _{CC} = 4.5V	Full			1.35	
		V _{CC} = 5.5V	Full			1.65	
High-Level Output Voltage	V _{OH}	V _{CC} = 2.0V, I _{OH} = -20μA	Full	1.95	1.995		V
		V _{CC} = 4.5V, I _{OH} = -20μA	Full	4.45	4.495		
		V _{CC} = 5.5V, I _{OH} = -20μA	Full	5.45	5.495		
		V _{CC} = 4.5V, I _{OH} = -4.0mA	Full	3.84	4.390		
		V _{CC} = 5.5V, I _{OH} = -5.2mA	Full	4.84	5.380		
Low-Level Output Voltage	V _{OL}	V _{CC} = 2.0V, I _{OL} = 20μA	Full		0.005	0.05	V
		V _{CC} = 4.5V, I _{OL} = 20μA	Full		0.005	0.05	
		V _{CC} = 5.5V, I _{OL} = 20μA	Full		0.005	0.05	
		V _{CC} = 4.5V, I _{OL} = 4.0mA	Full		0.10	0.33	
		V _{CC} = 5.5V, I _{OL} = 5.2mA	Full		0.12	0.33	
Input Leakage Current	I _I	V _{CC} = 5.5V, V _I = V _{CC} or 0V	Full			±1	μA
Supply Current	I _{CC}	V _{CC} = 5.5V, V _I = V _{CC} or 0V, I _O = 0A	Full			10	μA
Input Capacitance	C _I	V _{CC} = 2.0V to 5.5V	+25°C		4		pF

DYNAMIC CHARACTERISTICS

(See Figure 2 for test circuit. Full = -40°C to +125°C, all typical values are measured at $C_L = 50\text{pF}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Propagation Delay ⁽²⁾	t _{PD}	SH/ $\overline{\text{LD}}$ to Q _H or $\overline{\text{Q}}_{\text{H}}$	V _{CC} = 2.0V	Full	4	31	100	ns
			V _{CC} = 4.5V	Full	2	12	35	
			V _{CC} = 5.5V	Full	2	10	30	
		CLK to Q _H or $\overline{\text{Q}}_{\text{H}}$	V _{CC} = 2.0V	Full	3	34	100	
			V _{CC} = 4.5V	Full	2	13	35	
			V _{CC} = 5.5V	Full	2	11	33	
		H to Q _H or $\overline{\text{Q}}_{\text{H}}$	V _{CC} = 2.0V	Full	4	31	100	
			V _{CC} = 4.5V	Full	2	12	35	
			V _{CC} = 5.5V	Full	2	10	30	
Transition Time ⁽²⁾	t _T	Any	V _{CC} = 2.0V	Full	1.5	13	60	ns
			V _{CC} = 4.5V	Full	0.3	4	18	
			V _{CC} = 5.5V	Full	0.3	3	15	
Pulse Width	t _W	SH/ $\overline{\text{LD}}$ low	V _{CC} = 2.0V	Full	50			ns
			V _{CC} = 4.5V	Full	22			
			V _{CC} = 5.5V	Full	20			
		CLK high or low	V _{CC} = 2.0V	Full	50			
			V _{CC} = 4.5V	Full	22			
			V _{CC} = 5.5V	Full	20			
Setup Time	t _{SU}	SH/ $\overline{\text{LD}}$ high before CLK	V _{CC} = 2.0V	Full	50			ns
			V _{CC} = 4.5V	Full	22			
			V _{CC} = 5.5V	Full	20			
		SER before CLK	V _{CC} = 2.0V	Full	30			
			V _{CC} = 4.5V	Full	10			
			V _{CC} = 5.5V	Full	8			
		CLK INH before CLK	V _{CC} = 2.0V	Full	50			
			V _{CC} = 4.5V	Full	25			
			V _{CC} = 5.5V	Full	20			
		Data before SH/ $\overline{\text{LD}}$	V _{CC} = 2.0V	Full	80			
			V _{CC} = 4.5V	Full	25			
			V _{CC} = 5.5V	Full	20			
Hold Time	t _H	SER data after CLK	V _{CC} = 2.0V	Full	5			ns
			V _{CC} = 4.5V	Full	5			
			V _{CC} = 5.5V	Full	5			
		PAR data after SH/ $\overline{\text{LD}}$	V _{CC} = 2.0V	Full	15			
			V _{CC} = 4.5V	Full	8			
			V _{CC} = 5.5V	Full	8			

DYNAMIC CHARACTERISTICS (continued)

(See Figure 2 for test circuit. Full = -40°C to +125°C, all typical values are measured at $C_L = 50\text{pF}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Maximum Frequency	f_{max}	$V_{\text{CC}} = 2.0\text{V}$	Full	4.2			MHz
		$V_{\text{CC}} = 2.7\text{V}$	Full	12			
		$V_{\text{CC}} = 3.3\text{V}$	Full	18			
		$V_{\text{CC}} = 4.5\text{V}$	Full	21			
		$V_{\text{CC}} = 5.5\text{V}$	Full	25			
Power Dissipation Capacitance ⁽³⁾	C_{PD}	No load	+25°C		13		pF

NOTES:

- Specified by design and characterization, not production tested.
- t_{PD} is the same as t_{PLH} and t_{PHL} . t_{T} is the same as t_{THL} and t_{TLH} .
- C_{PD} is used to determine the dynamic power dissipation (P_{D} in μW).

$$P_{\text{D}} = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_{\text{i}} \times N + \Sigma(C_{\text{L}} \times V_{\text{CC}}^2 \times f_{\text{o}})$$

where:

f_{i} = Input frequency in MHz.

f_{o} = Output frequency in MHz.

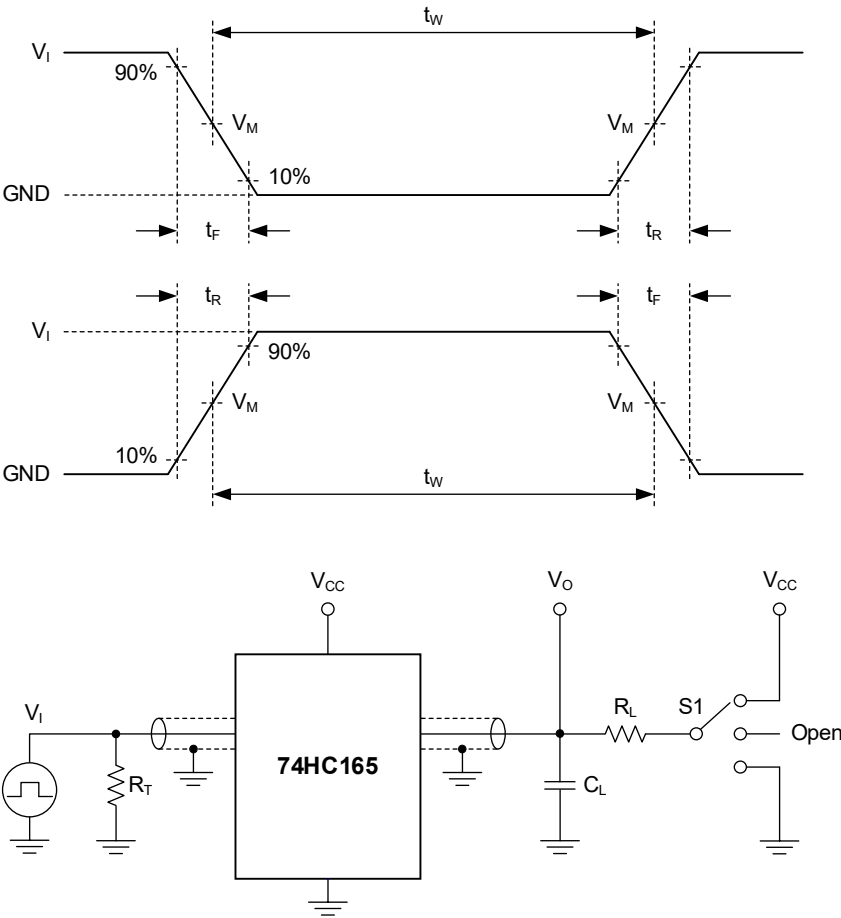
C_{L} = Output load capacitance in pF.

V_{CC} = Supply voltage in Volts.

N = Number of inputs switching.

$\Sigma(C_{\text{L}} \times V_{\text{CC}}^2 \times f_{\text{o}})$ = Sum of the outputs.

TEST CIRCUIT



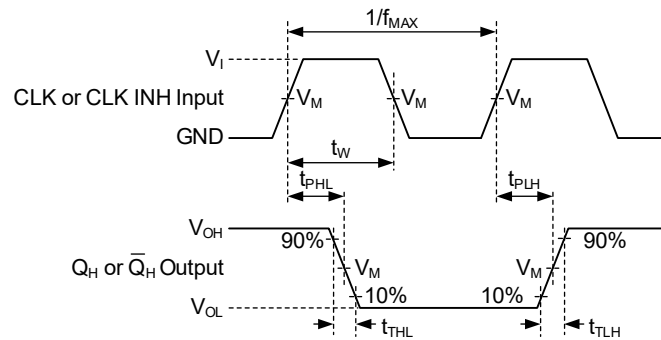
Test conditions are given in Table 1.
Definitions for test circuit:
 R_L : Load resistance.
 C_L : Load capacitance (includes jig and probe).
 R_T : Termination resistance (equals to output impedance Z_O of the pulse generator).
 $S1$: Test selection switch.

Figure 2. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}
2.0V to 5.5V	V_{CC}	$\leq 6.0ns$	50pF	1k Ω	Open

WAVEFORMS

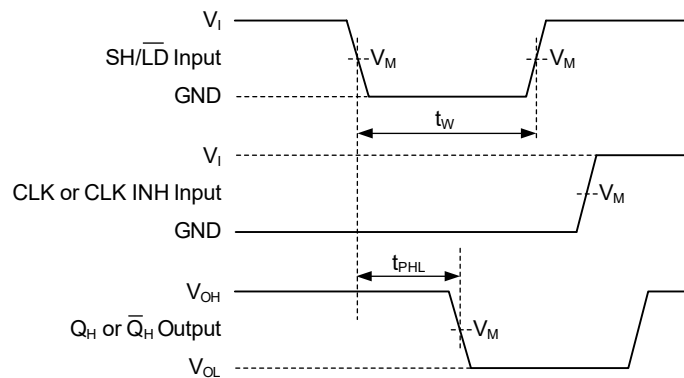


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Clock Pulse Width, Transition Times, Maximum Frequency and Clock Input/Clock Inhibit to Output Propagation Delays

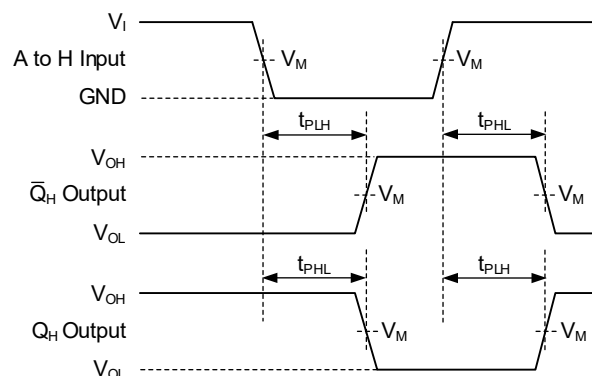


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Shift/Load Input to Output Propagation Delays and Pulse Width



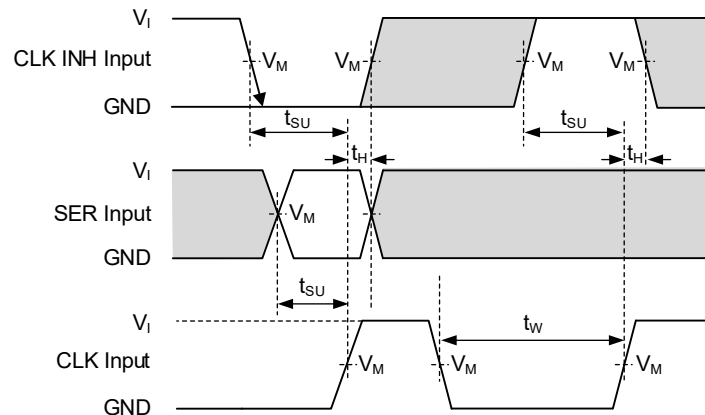
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. Parallel Input to Output Propagation Delays at Shift/Load Input Low

WAVEFORMS (continued)



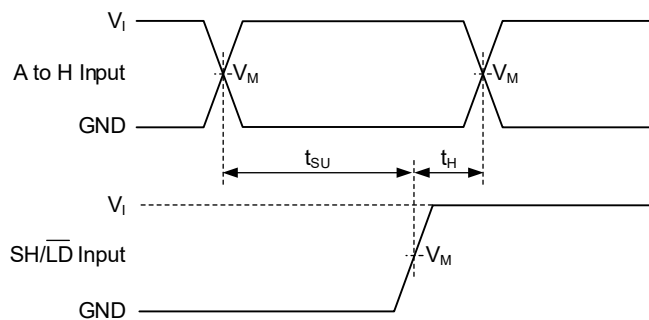
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 6. Serial Input to Clock Input/Clock Inhibit, Clock Input to Clock Inhibit and Clock Inhibit to Clock Input Setup and Hold Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Parallel Input to Shift/Load Input Setup and Hold Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	$V_M^{(1)}$	V_M
2.0V to 5.5V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 6.0ns.

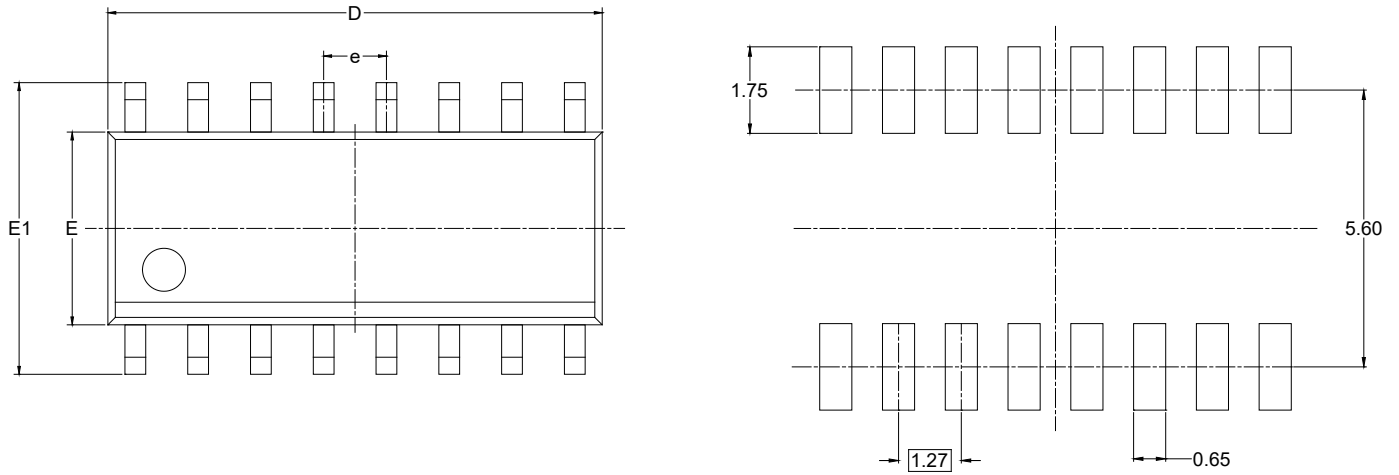
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

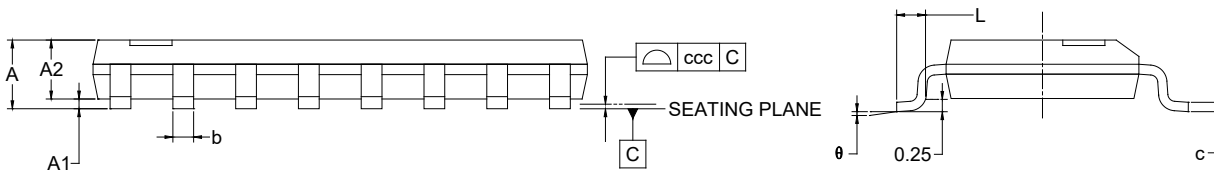
OCTOBER 2024 – REV.A.1 to REV.A.2	Page
Updated Dynamic Characteristics section	7
Updated Package Outline Dimensions section	12
AUGUST 2023 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	5
Added TSSOP-16 package.....	All
Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS SOIC-16



RECOMMENDED LAND PATTERN (Unit: mm)



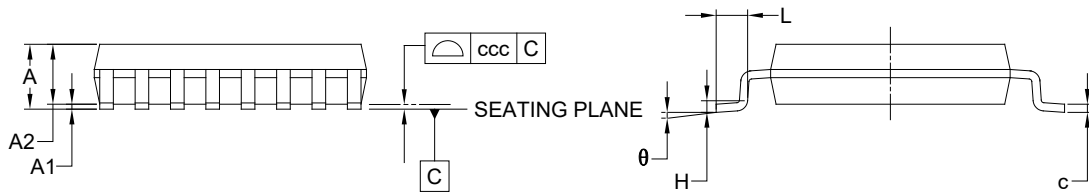
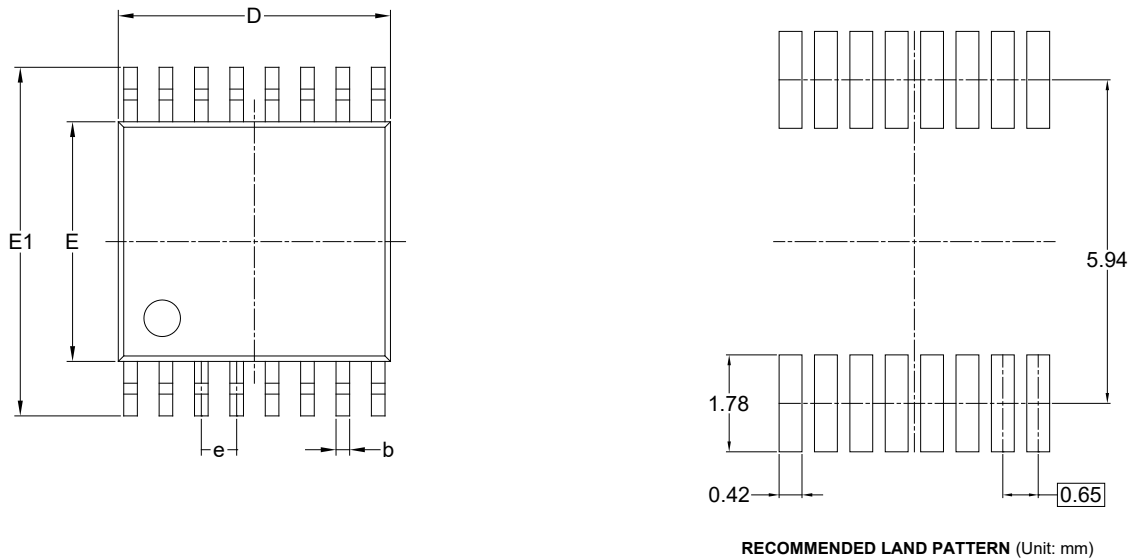
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

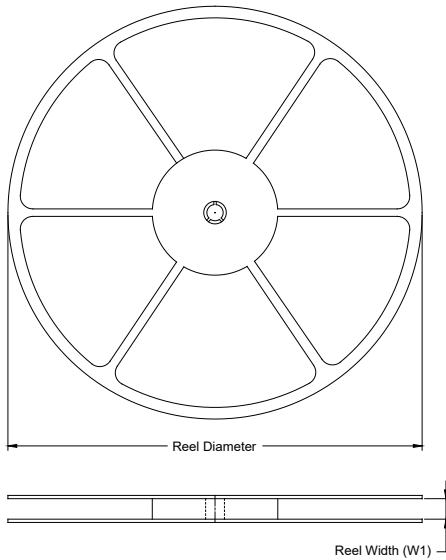
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

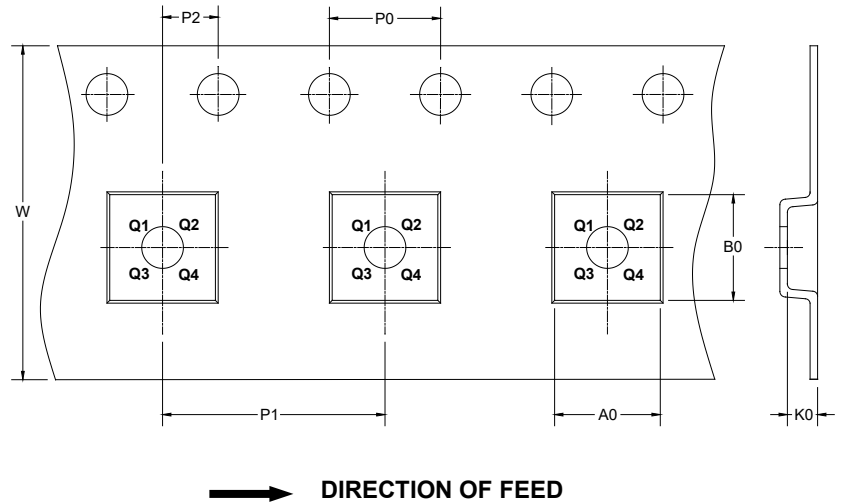
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

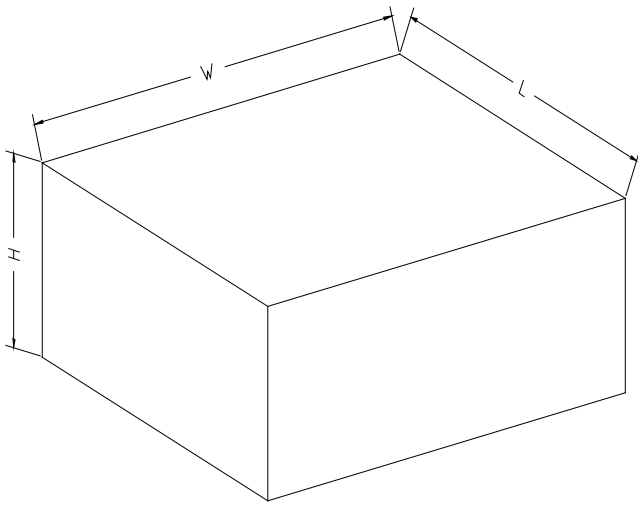
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002