74LVC1G74
Single D-Type Positive Edge-Triggered Flip-Flop with Clear and Preset

GENERAL DESCRIPTION

The 74LVC1G74 is a single D-Type positive edge-triggered flip-flop with clear and preset functions. This device can operate in the supply voltage range from 1.65V to 5.5V. No matter what the levels of the other inputs are, the preset ($\overline{PRE}$) input or clear ($\overline{CLR}$) input can be pulled low to set or reset the outputs. When the preset input and clear input are held high, data at the D input that suffices for setup time purposes is moved to the Q output on the low-to-high clock transition. After the hold time interval, data at the D input can be changed without any influence on output levels. Clock triggering appears at a voltage level which is uncorrelated with the rise time of the clock pulse.

This device is highly suitable for partial power-down applications by using power-off leakage current (I_{OFF}) circuit.

APPLICATIONS

Telecommunication Facilities

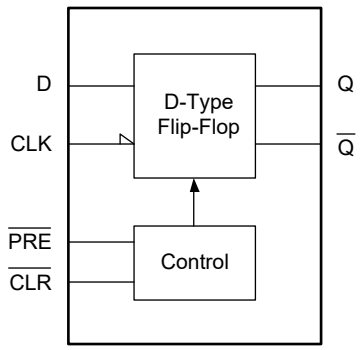
Servers and I/O Expanders

Network Switches

Motor Drivers

LED Displays

LOGIC DIAGRAM



FEATURES

- **Wide Supply Voltage Range: 1.65V to 5.5V**
- **Inputs Accept Voltages Higher than the Supply Voltage**
- **+32mA/-32mA Output Current**
- **Outputs in High-Impedance State when V_{CC} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green VSSOP-8, XTDFN-1.4×1-8L and MSOP-8(S) Packages**

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	*X*	*X*	H	L
H	L	*X*	*X*	L	H
L	L	*X*	*X*	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	*X*	Q_0	$\overline{Q}_0$

H = High Voltage Level

L = Low Voltage Level

Z = High-Impedance State

↑ = Low-to-High Clock Transition

X = Don't Care

NOTE:

1. The configuration is unstable that it cannot continue to exist when $\overline{PRE}$ or $\overline{CLR}$ returns to inactive (high) level.

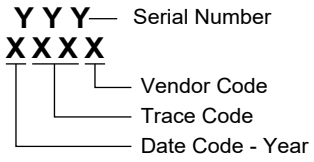
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC1G74	VSSOP-8	-40℃ to +125℃	74LVC1G74XVS8G/TR	084 XXXX	Tape and Reel, 3000
	XTDFN-1.4×1-8L	-40℃ to +125℃	74LVC1G74XXDO8G/TR	00X	Tape and Reel, 5000
	MSOP-8(S)	-40℃ to +125℃	74LVC1G74XSMS8G/TR	0GB XSMS8 XXXXX	Tape and Reel, 4000

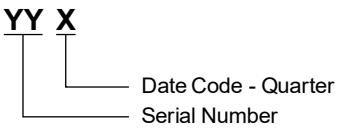
MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code. X = Date Code.

VSSOP-8

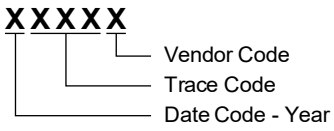


XTDFN-1.4×1-8L



NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

MSOP-8(S)



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 6.5V
Input Voltage Range, V_I (2) ..... -0.5V to 6.5V
Output Voltage Range, V_O (2)
High-State or Low-State..... -0.5V to MIN(6.5V, V_{CC} + 0.5V)
High-Impedance or Power-Off State ..... -0.5V to 6.5V
Input Clamp Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamp Current, I_{OK} (V_O < 0V) .....-50mA
Continuous Output Current, I_O .....±50mA
Continuous Current through V_{CC} or GND.....±100mA
Junction Temperature (3).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} ..... 1.65V to 5.5V
Input Voltage Range, V_I (4) ..... 0V to 5.5V
Output Voltage Range, V_O
High-State or Low-State .....0V to V_{CC}
High-Impedance or Power-Off State..... 0V to 5.5V
Output Current, I_O..... ±32mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V ..... 20ns/V (MAX)
V_{CC} = 3.3V ± 0.3V..... 10ns/V (MAX)
V_{CC} = 5.0V ± 0.5V..... 5ns/V (MAX)
Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

4. Unused input pins must be held at V_{CC} or GND to guarantee the device in normal operation.

ESD SENSITIVITY CAUTION

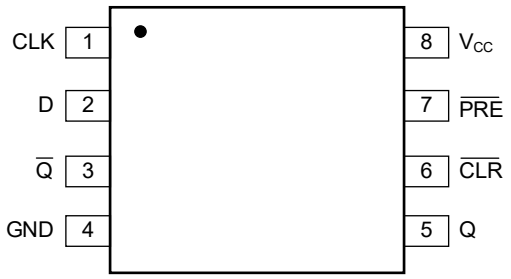
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

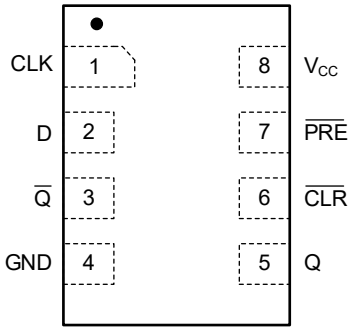
PIN CONFIGURATIONS

(TOP VIEW)



VSSOP-8/MSOP-8(S)

(TOP VIEW)



XTDFN-1.4×1-8L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	CLK	Clock Input (Low-to-High Clock Transition, Edge-Triggered).
2	D	Data Input.
3	$\overline{Q}$	Complementary Output.
4	GND	Ground.
5	Q	Output.
6	$\overline{CLR}$	Clear Input (Active-Low).
7	$\overline{PRE}$	Preset Input (Active-Low).
8	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	Full	0.65 × V_{CC}			V
		V_{CC} = 2.3V to 2.7V	Full	1.7			
		V_{CC} = 3.0V to 3.6V	Full	2.0			
		V_{CC} = 4.5V to 5.5V	Full	0.7 × V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V	Full			0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V	Full			0.7	
		V_{CC} = 3.0V to 3.6V	Full			0.8	
		V_{CC} = 4.5V to 5.5V	Full			0.3 × V_{CC}	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 5.5V, I_{OH} = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.005		V
		V_{CC} = 1.65V, I_{OH} = -4mA	Full	1.35	1.55		
		V_{CC} = 2.3V, I_{OH} = -8mA	Full	1.95	2.18		
		V_{CC} = 3.0V, I_{OH} = -16mA	Full	2.60	2.81		
		V_{CC} = 3.0V, I_{OH} = -24mA	Full	2.40	2.71		
		V_{CC} = 4.5V, I_{OH} = -32mA	Full	3.90	4.23		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65 to 5.5V, I_{OL} = 100μA	Full		0.005	0.05	V
		V_{CC} = 1.65V, I_{OL} = 4mA	Full		0.07	0.20	
		V_{CC} = 2.3V, I_{OL} = 8mA	Full		0.10	0.30	
		V_{CC} = 3.0V, I_{OL} = 16mA	Full		0.16	0.40	
		V_{CC} = 3.0V, I_{OL} = 24mA	Full		0.25	0.50	
		V_{CC} = 4.5V, I_{OL} = 32mA	Full		0.27	0.55	
Input Leakage Current	I_I	Data or control inputs, V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	Full		±0.1	±1	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 5.5V	Full		±0.1	±2	μA
Supply Current	I_{CC}	V_{CC} = 1.65V to 5.5V, V_I = 5.5V or GND, I_O = 0A	Full		0.1	4	μA
Additional Supply Current	ΔI_{CC}	V_{CC} = 3.0V to 5.5V, one input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	Full		0.1	10	μA
Input Capacitance	C_I	V_I = V_{CC} or GND	+25℃		5		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Clock Frequency	f_{CLOCK}	V_{CC} = 1.8V		Full			75	MHz
		V_{CC} = 2.5V		Full			165	
		V_{CC} = 3.3V		Full			175	
		V_{CC} = 5.0V		Full			185	
Maximum Frequency	f_{MAX}	V_{CC} = 1.8V		Full	75			MHz
		V_{CC} = 2.5V		Full	165			
		V_{CC} = 3.3V		Full	175			
		V_{CC} = 5.0V		Full	185			
Hold Time	t_H	V_{CC} = 1.8V		Full	2			ns
		V_{CC} = 2.5V		Full	1.5			
		V_{CC} = 3.3V		Full	1			
		V_{CC} = 5.0V		Full	1			
Pulse Width	t_W	CLK	V_{CC} = 1.8V	Full	5.5			ns
			V_{CC} = 2.5V	Full	3.5			
			V_{CC} = 3.3V	Full	4			
			V_{CC} = 5.0V	Full	3.5			
		$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 1.8V	Full	7			
			V_{CC} = 2.5V	Full	5.5			
			V_{CC} = 3.3V	Full	5			
			V_{CC} = 5.0V	Full	4			
Setup Time	t_{SU}	Data	V_{CC} = 1.8V	Full	4			ns
			V_{CC} = 2.5V	Full	3			
			V_{CC} = 3.3V	Full	2			
			V_{CC} = 5.0V	Full	2			
Recovery Time	t_{REC}	$\overline{PRE}$ or $\overline{CLR}$	V_{CC} = 1.8V	+25℃		2.6		ns
			V_{CC} = 2.5V	+25℃		1		
			V_{CC} = 3.3V	+25℃		0.6		
			V_{CC} = 5.0V	+25℃		0.6		
Propagation Delay (2)	t_{PD}	CLK to Q	V_{CC} = 1.8V	Full	1	10	16	ns
			V_{CC} = 2.5V	Full	1	5	9	
			V_{CC} = 3.3V	Full	1	4	7	
			V_{CC} = 5.0V	Full	1	3.5	6	
		CLK to $\overline{Q}$	V_{CC} = 1.8V	Full	1	13	21	
			V_{CC} = 2.5V	Full	1	6.5	11	
			V_{CC} = 3.3V	Full	1	5	8	
			V_{CC} = 5.0V	Full	1	4	6.5	
		$\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$	V_{CC} = 1.8V	Full	1	13.5	22	
			V_{CC} = 2.5V	Full	1	7	12	
			V_{CC} = 3.3V	Full	1	5.5	9	
			V_{CC} = 5.0V	Full	1	4	6.5	

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Power Dissipation Capacitance (3)	C_{PD}	f = 10MHz	V_{CC} = 1.8V	+25℃		23		pF
			V_{CC} = 2.5V	+25℃		25		
			V_{CC} = 3.3V	+25℃		28		
			V_{CC} = 5.0V	+25℃		29		

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

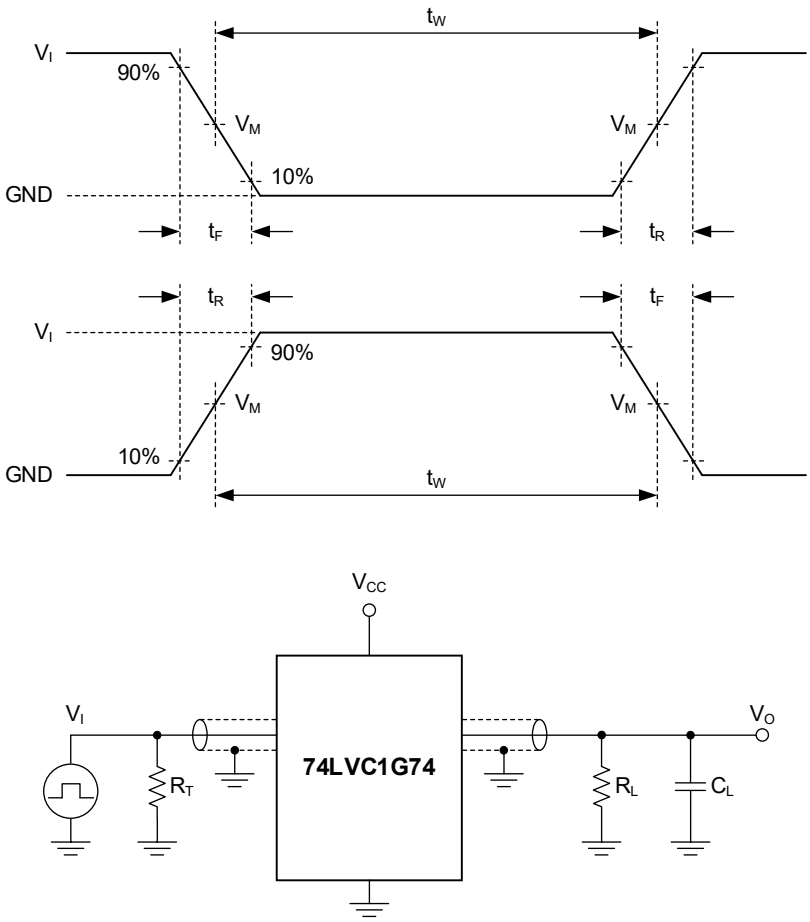
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

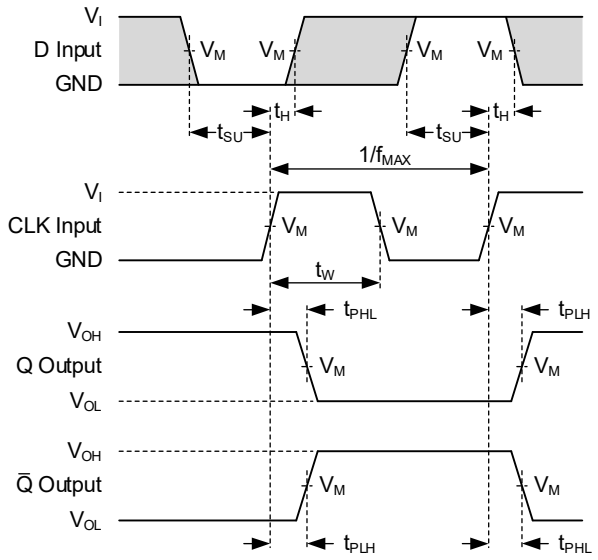
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_R, t_F	C_L	R_L
1.8V ± 0.15V	V_{CC}	≤ 2.0ns	30pF	1kΩ
2.5V ± 0.2V	V_{CC}	≤ 2.0ns	30pF	500Ω
3.3V ± 0.3V	3V	≤ 2.5ns	50pF	500Ω
5.0V ± 0.5V	V_{CC}	≤ 2.5ns	50pF	500Ω

WAVEFORMS



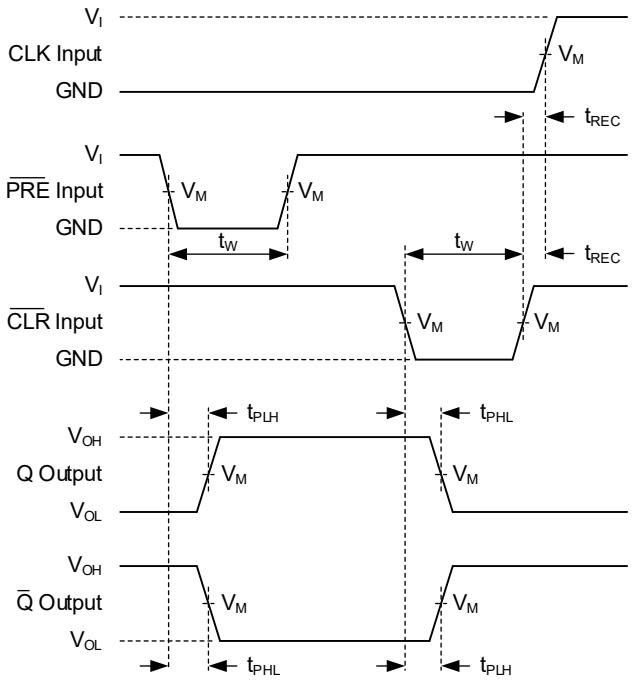
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 2. The Clock Input to Output Propagation Delays, Clock Pulse Width, the D to CLK Setup, the CLK to D Hold Times and the Maximum Frequency



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The $\overline{PRE}$ and $\overline{CLR}$ Input to Output Propagation Delays, Pulse Width and the $\overline{CLR}$ to CLK Recovery Time

WAVEFORMS (continued)

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.8V ± 0.15V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.5V ± 0.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
3.3V ± 0.3V	3V	1.5V	1.5V
5.0V ± 0.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2024 – REV.A.1 to REV.A.2 **Page**

Added MSOP-8(S) package ..... All
Updated Electrical Characteristics section 5
Updated Dynamic Characteristics section 6

NOVEMBER 2023 – REV.A to REV.A.1 **Page**

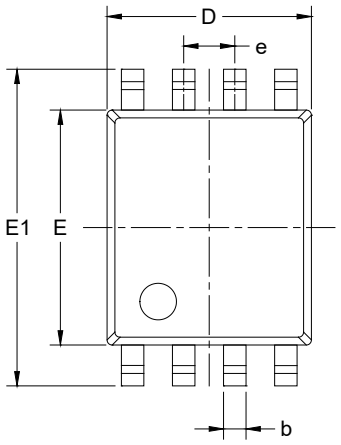
Added XTDFN-1.4×1-8L package ..... All

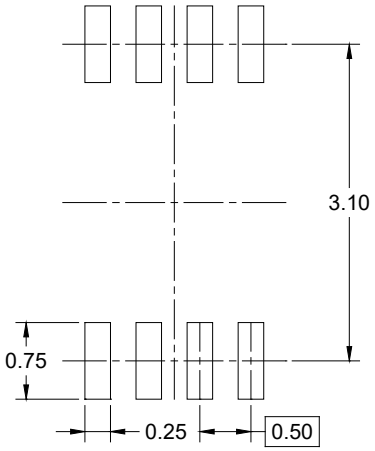
Changes from Original (JUNE 2023) to REV.A **Page**

Changed from product preview to production data ..... All

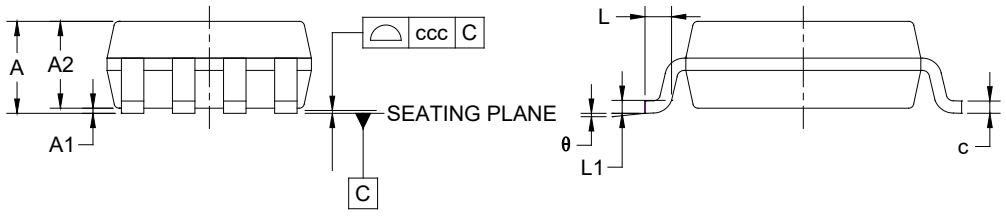
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

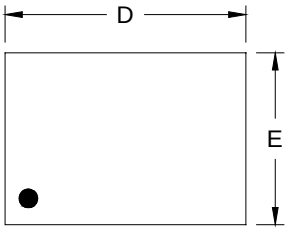


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

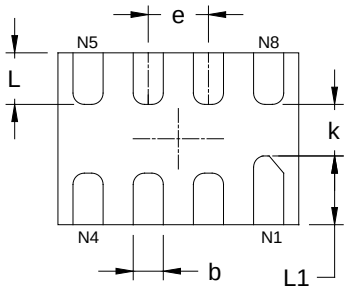
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

PACKAGE OUTLINE DIMENSIONS

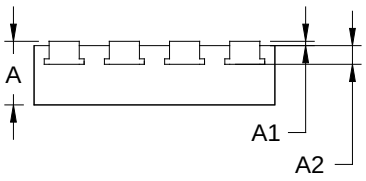
XTDFN-1.4×1-8L



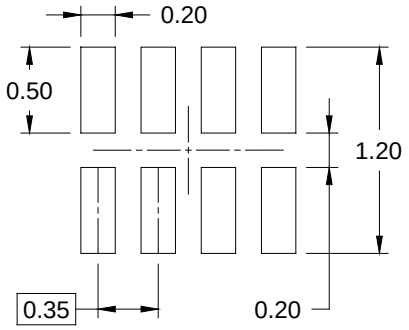
TOP VIEW



BOTTOM VIEW



SIDE VIEW



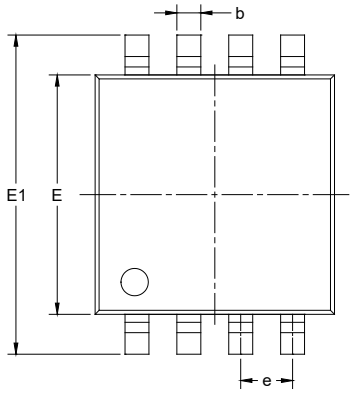
RECOMMENDED LAND PATTERN (Unit: mm)

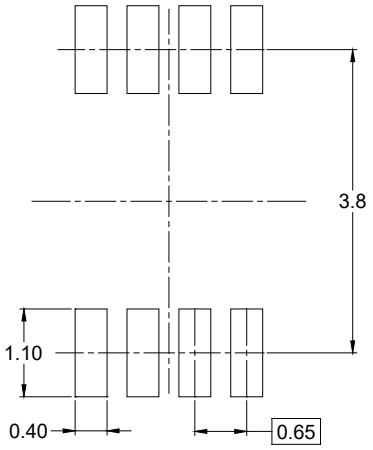
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.340	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.110 REF		0.004 REF	
D	1.350	1.450	0.053	0.057
E	0.950	1.050	0.037	0.041
k	0.200 MIN		0.008 MIN	
b	0.150	0.200	0.006	0.008
e	0.350 TYP		0.014 TYP	
L	0.250	0.350	0.010	0.014
L1	0.350	0.450	0.014	0.018

NOTE: This drawing is subject to change without notice.

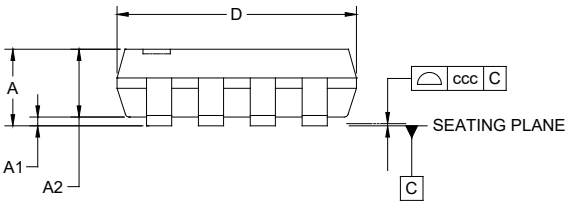
PACKAGE OUTLINE DIMENSIONS

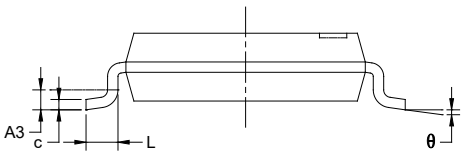
MSOP-8(S)





RECOMMENDED LAND PATTERN (Unit: mm)



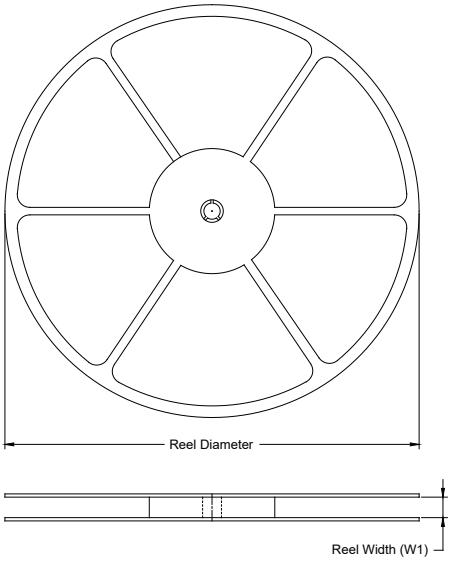


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.350
A1	0.000	-	0.150
A2	0.850 REF		
A3	0.250 REF		
b	0.150	-	0.380
c	0.080	-	0.180
D	2.750	-	3.150
E	2.600	-	3.100
E1	3.750	-	4.250
e	0.650 BSC		
L	0.200	-	0.600
θ	0°	-	8°
ccc	0.100		

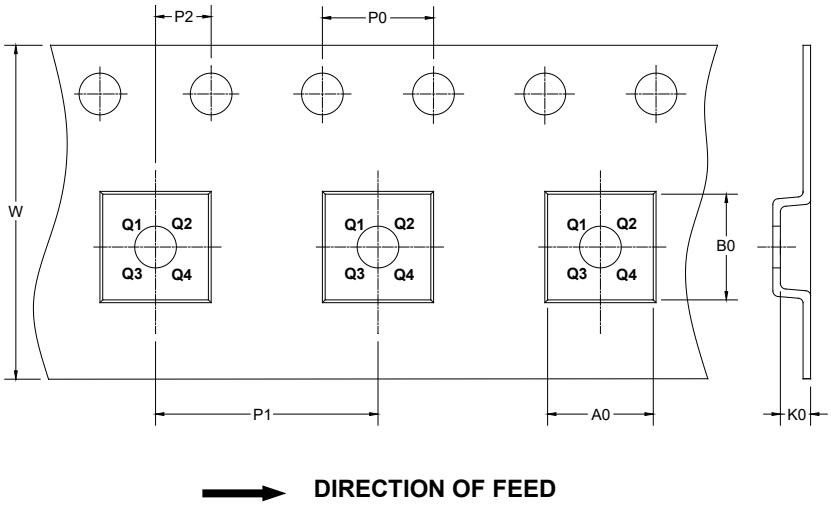
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



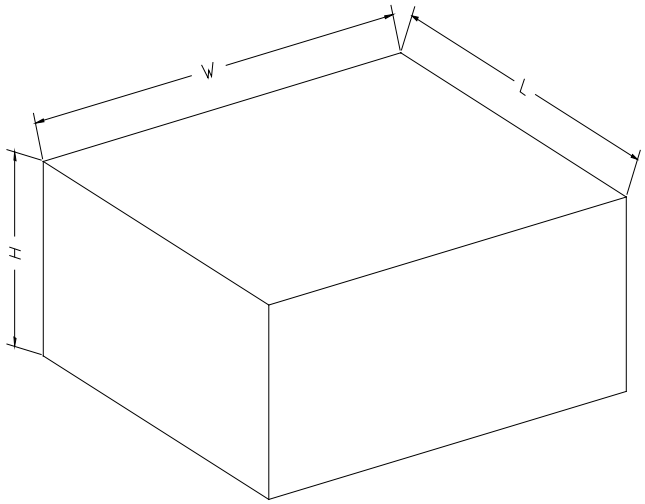
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7″	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3
XTDFN-1.4×1-8L	7"	9.5	1.15	1.60	0.50	4.0	4.0	2.0	8.0	Q1
MSOP-8(S)	13"	12.4	3.25	4.30	1.50	4.0	4.0	2.0	12.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002