SGM25811
High-Voltage MOSFET Drivers for Buck Converter Applications

GENERAL DESCRIPTION

The SGM25811 is a specialized dual, high-voltage MOSFET driver to efficiently drive two N-MOSFETs in a synchronous-rectified Buck converter. When combined with a multi-phase Buck PWM controller, it forms the core of voltage regulator for advanced micro-processors.

Its features also include anti-shoot-through protection, ensuring there's no cross-conduction in external MOSFETs while optimizing efficiency with minimal dead time. Additionally, it integrates a bootstrap switch, which eliminates the need for other external components. Controlling both gate drives is simple: pulling the EN pin low or putting the PWM pin to a high-impedance condition deactivates both, preventing the output capacitor from rapidly discharging while the system is shut down. Notably, the SGM25811 also has input under-voltage lockout function.

The SGM25811A and SGM25811B are available in a Green TDFN-2×2-8L package. The SGM25811C is available in a Green TDFN-3×3-8BL package. The SGM25811D is available in a Green SOIC-8 (Exposed Pad) package.

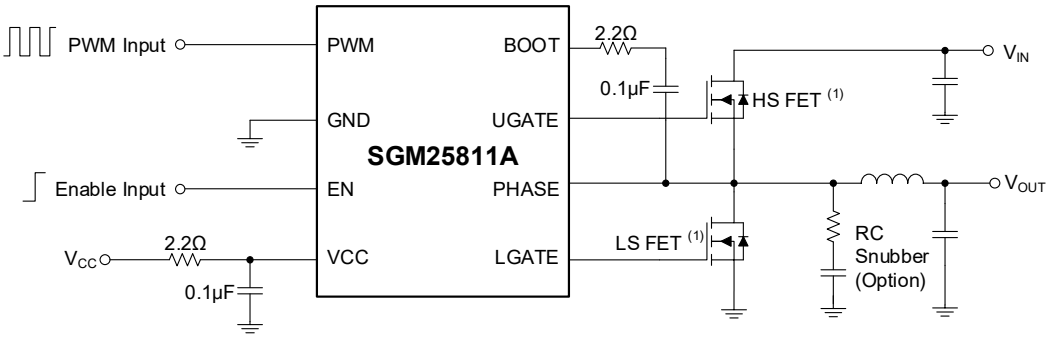
FEATURES

- **Suitable for HVMOS Driving (V_{GS} = V_{IN} = 12V)**
- **Single PWM Signal Controls Dual Drivers**
- **Integrated Synchronous Buck Driver Solution**
- **Anti-Shoot-Through Protection Circuitry**
- **Bridge Shutdown by Using Tri-State Input**
- **Built-in Bootstrap Switch Integration**
- **Turn Off both MOSFETs by Using EN Control**
- **Utilize PWM Pin for Multi-Functional Settings**
- **Supply Input Under-Voltage Lockout**
- **SGM25811A and SGM25811B are Available in a Green TDFN-2×2-8L Package**
  SGM25811C is Available in a Green TDFN-3×3-8BL Package
  SGM25811D is Available in a Green SOIC-8 (Exposed Pad) Package

APPLICATIONS

Voltage Regulators for Desktop CPU Cores
Low Profile DC/DC Converters Operating at High Frequencies
DC/DC Converters for Low Voltage at High Currents

TYPICAL APPLICATION



NOTE: 1. Suggested total solution: HS FET = SGMNQ40430, LS FET = SGMNQ28430.

Figure 1. Typical Application Circuit

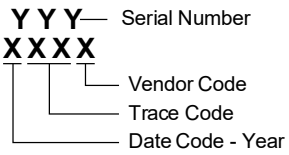
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25811A	TDFN-2×2-8L	-40℃ to +105℃	SGM25811AGTDE8G/TR	0MK XXXX	Tape and Reel, 3000
SGM25811B	TDFN-2×2-8L	-40℃ to +105℃	SGM25811BGTDE8G/TR	0ML XXXX	Tape and Reel, 3000
SGM25811C	TDFN-3×3-8BL	-40℃ to +105℃	SGM25811CGTDD8G/TR	SGM 0MNDD XXXXX	Tape and Reel, 4000
SGM25811D	SOIC-8 (Exposed Pad)	-40℃ to +105℃	SGM25811DGPS8G/TR	SGM 0MOGPS8 XXXXX	Tape and Reel, 4000

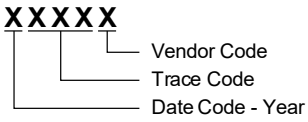
MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code. XXXXX = Date Code, Trace Code and Vendor Code.

TDFN-2×2-8L



TDFN-3×3-8BL/SOIC-8 (Exposed Pad)



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage, V_{CC} ..... -0.3V to 15V
BOOT to PHASE ..... -0.3V to 15V
PHASE to GND
DC ..... -0.7V to 15V
< 200ns ..... -8V to 30V
BOOT to GND
DC ..... -0.3V to (V_{CC} + 15V)
< 200ns ..... -0.3V to 42V
UGATE to PHASE
DC ..... -0.3V to (BOOT - PHASE + 0.3V)
< 200ns ..... -5V to (BOOT - PHASE + 0.3V)
LGATE to GND
DC ..... -0.3V to (V_{CC} + 0.3V)
< 200ns ..... -5V to (V_{CC} + 0.3V)
PWM ..... -0.3V to 6V
EN ..... -0.3V to (V_{CC} + 0.3V)
Package Thermal Resistance
TDFN-2×2-8L, θ_{JA} ..... 111.5℃/W
TDFN-2×2-8L, θ_{JB} ..... 71.5℃/W
TDFN-2×2-8L, $\theta_{JC\ (TOP)}$ ..... 97.5℃/W
TDFN-2×2-8L, $\theta_{JC\ (BOT)}$ ..... 51℃/W
TDFN-3×3-8BL, θ_{JA} ..... 86.2℃/W
TDFN-3×3-8BL, θ_{JB} ..... 57.7℃/W
TDFN-3×3-8BL, $\theta_{JC\ (TOP)}$ ..... 72.7℃/W
TDFN-3×3-8BL, $\theta_{JC\ (BOT)}$ ..... 50.6℃/W
SOIC-8 (Exposed Pad), θ_{JA} ..... 43.6℃/W
SOIC-8 (Exposed Pad), θ_{JB} ..... 20.4℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 59.2℃/W
SOIC-8 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 10.4℃/W
Power Dissipation, P_D @ T_A = +25℃
TDFN-2×2-8L 0.89W
TDFN-3×3-8BL 1.16W
SOIC-8 (Exposed Pad) 2.29W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage, V_{CC} ..... 10.8V to 13.2V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

DISCLAIMER

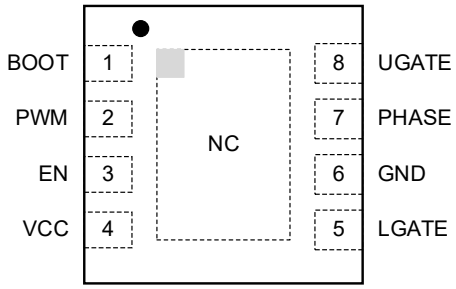
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

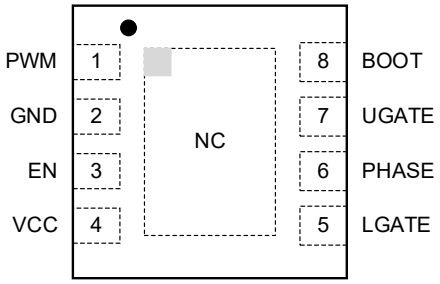
PIN CONFIGURATIONS

SGM25811A (TOP VIEW)



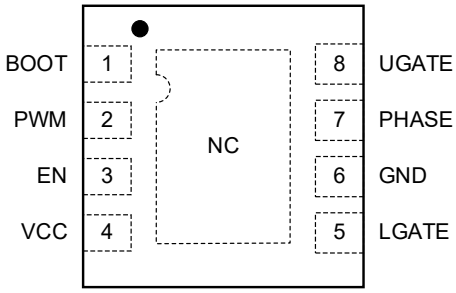
TDFN-2×2-8L

SGM25811B (TOP VIEW)



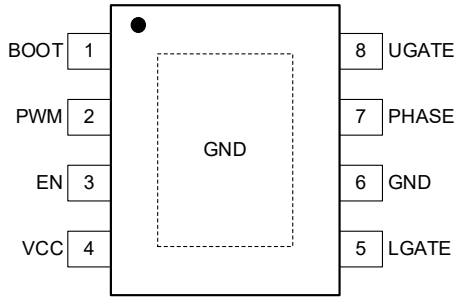
TDFN-2×2-8L

SGM25811C (TOP VIEW)



TDFN-3×3-8BL

SGM25811D (TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN		NAME	FUNCTION
SGM25811A/ SGM25811C/ SGM25811D	SGM25811B		
1	8	BOOT	Bootstrap Pin. Supply upper gate driver. A 0.1μF ceramic capacitor and a 2.2Ω R_{BOOT} are connected between this pin and PHASE pin. Ensure the 0.1μF ceramic capacitor is placed near the IC.
2	1	PWM	PWM Input. The PWM input pin receives logic-level signals, and directly controls the driver outputs. If the EN input is low, the PWM pin operates in a high-impedance state. Conversely, when the EN input is high, the internal circuit pulls the PWM pin voltage to a tri-state configuration. To ensure proper functionality of the PWM controller, the resistor connected from the PWM pin to GND should have a value greater than 15kΩ.
3	3	EN	Enable Control. When pulled low, this pin disables normal operation, causing both UGATE and LGATE to be off. Additionally, it controls the state of the PWM pin. When the EN pin is low, the PWM pin operates in a high-impedance state. It's essential to note that there are no internal mechanisms for pulling the EN pin high or low.
4	4	VCC	Power Supply for the IC. Please give a 12V voltage source to this pin and bypass it with an R/C filter.
5	5	LGATE	Output for Low-side Gate Driver. Establish a connection between this pin and the low-side MOSFET gate. The shoot-through protection circuitry monitors this pin to detect the off-state of the lower MOSFET.
7	6	PHASE	Switch Node. Connect the source of the high-side MOSFET, and the drain of the low-side MOSFET to this pin. This pin serves as the return path for the UGATE driver and is monitored by the shoot-through protection circuit to detect the state of the upper MOSFET.
8	7	UGATE	Output for High-side Gate Driver. Establish a connection between this pin and the high-side MOSFET gate. The shoot-through protection circuitry monitors this pin to detect the off-state of the high-side MOSFET.
6	2	GND	The IC's Reference Ground Pin.
Exposed Pad (SGM25811A/ SGM25811C)	Exposed Pad (SGM25811B)	NC	Not Internally Connected. While the exposed pad of the SGM25811A isn't electrically connected to GND, it's strongly advised to connect it to the GND plane to optimize heat dissipation capabilities.
Exposed Pad (SGM25811D)	-	GND	The IC's Reference Ground Pin.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Input (VCC)						
Supply Current	I_{CC}	V_{EN} = 0V		1		mA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} Rising		4.2		V
VCC POR Hysteresis	V_{CCHYS}			240		mV
PWM Input (PWM)						
High-Level Input Voltage	V_{PWMH}		2.9			V
Low-Level Input Voltage	V_{PWML}				0.4	V
PWM Floating Voltage	V_{PWM_FLT}			1.6		V
PWM Input Current	I_{PWM}	PWM = 0V	-760	-490	-200	μA
		PWM = 3.3V	0.5	1.0	1.5	mA
		PWM = 5V	1.5	2.0	2.6	mA
Enable Control (EN)						
High-Level Input Voltage	V_{ENH}		2.0			V
Low-Level Input Voltage	V_{ENL}				0.6	V
Propagation Delay Time	t_{DHEN}			2		μs
	t_{DLEN}			114		ns
Bootstrap Switch						
On-Resistance	R_{DSON}	Forward bias current = 1mA		22		Ω
High-side Driver						
Output Resistance,	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = 80mA		2.5	4	Ω
	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = -80mA		1.4	2	Ω
Output Rising Time	t_{RUG}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3.3nF		65		ns
Output Falling Time	t_{FUG}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3.3nF		62		ns
Propagation Delay Time	t_{PDHUG}	V_{BOOT} - V_{PHASE} = 12V		23		ns
	t_{PDLUG}	V_{BOOT} - V_{PHASE} = 12V		60		ns
Low-side Driver						
Output Resistance,	R_{L_SRC}	V_{CC} = 12V, I_{LGATE} = 80mA		2.7	4	Ω
	R_{L_SNK}	V_{CC} = 12V, I_{LGATE} = -80mA		1.3	2	Ω
Output Rising Time	t_{RLG}	V_{CC} = 12V, C_{LOAD} = 3.3nF		73		ns
Output Falling Time	t_{FLG}	V_{CC} = 12V, C_{LOAD} = 3.3nF		45		ns
Propagation Delay Time	t_{PDHLG}	V_{CC} = 12V		25		ns
	t_{PDLLG}	V_{CC} = 12V		34		ns

PARAMETER MEASUREMENT INFORMATION

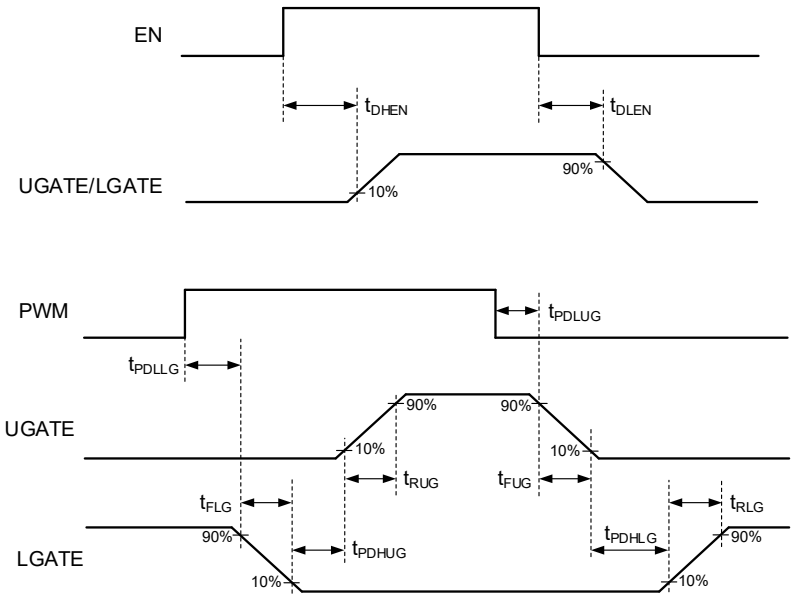


Figure 2. Timing Diagram

FUNCTIONAL BLOCK DIAGRAM

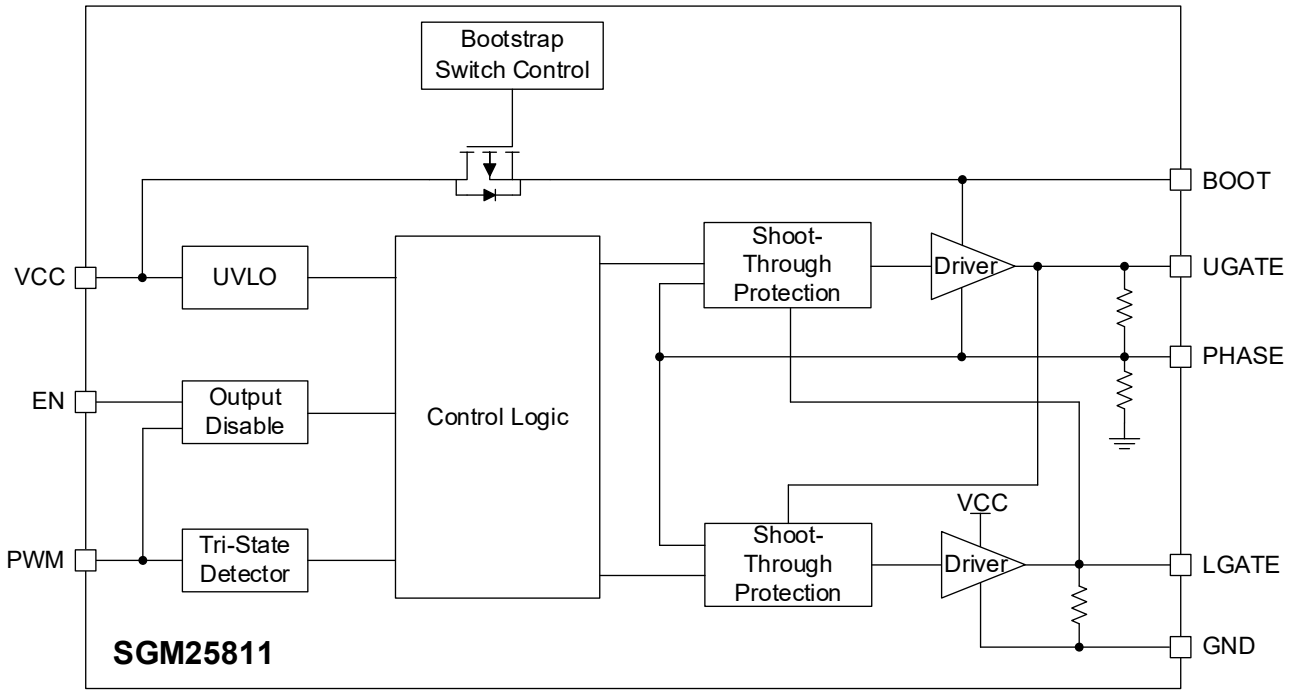
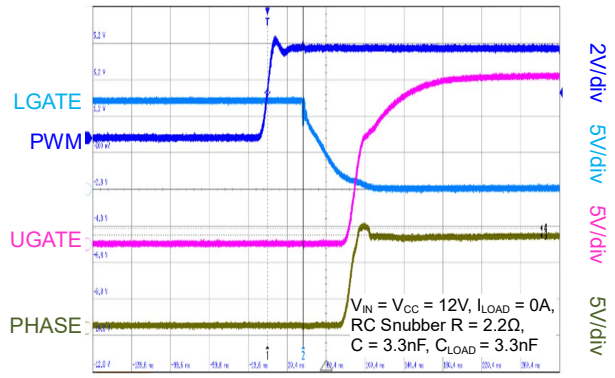


Figure 3. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

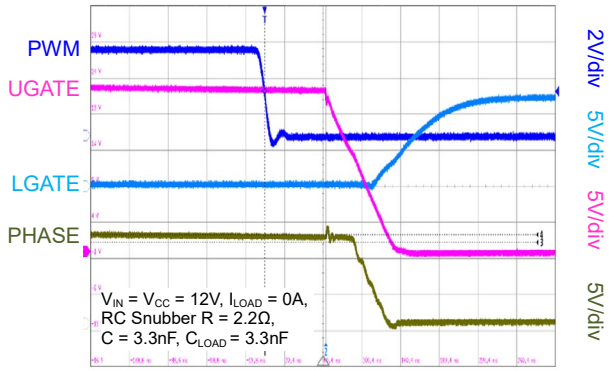
LG Falling to UG Rising Dead Time



HS FET: SGMNQ40430, LS FET: SGMNQ28430

Time (40ns/div)

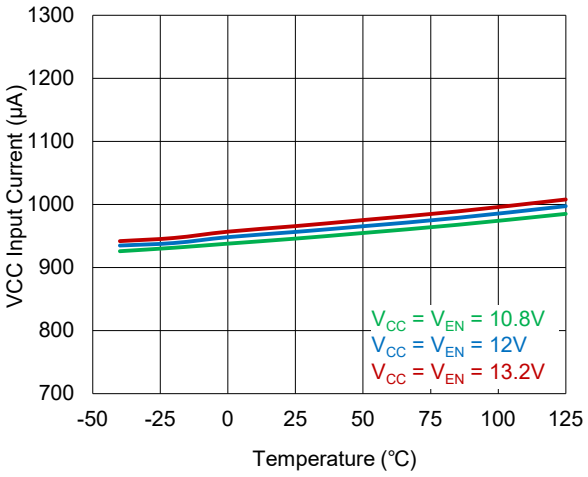
UG Falling to LG Rising Dead Time



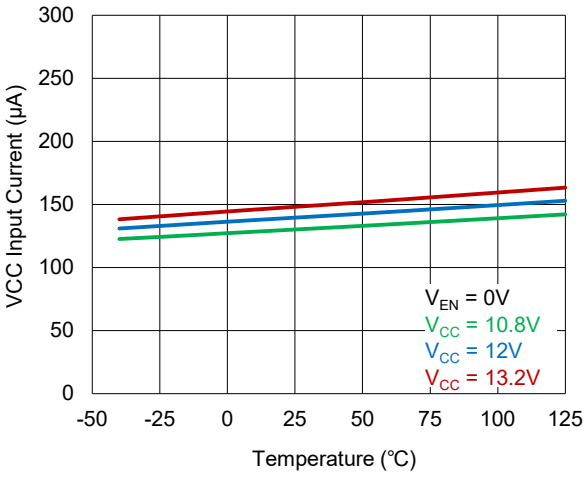
HS FET: SGMNQ40430, LS FET: SGMNQ28430

Time (40ns/div)

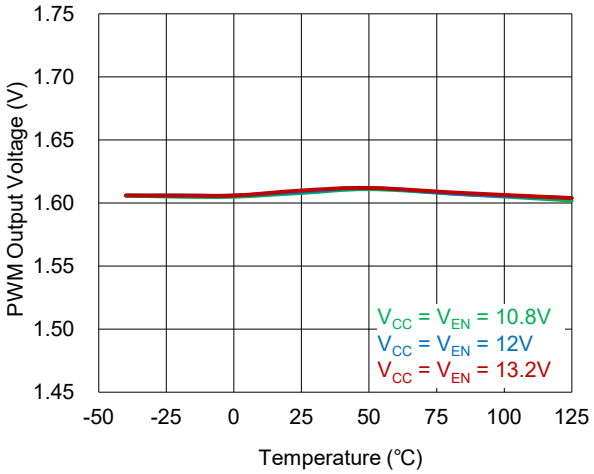
VCC Input Current vs. Temperature



VCC Input Current vs. Temperature



PWM Output Voltage vs. Temperature



DETAILED DESCRIPTION

Enable Control

The enable (EN) pin controls both the state of the PWM pin and the output of the MOSFET gate drivers. When a logic low signal is applied to EN, it disables the gate drivers, keeping both UGATE and LGATE low, while the PWM pin will be in a high-impedance state. On the other hand, a logic high input to EN enables gate driver activation after delay time (t_{DHEN}) illustrated in Figure 4. During this delay time, the PWM pin remains in a high-impedance state, with UGATE and LGATE outputs held low. Moreover, the internal control circuit can't respond to the PWM input voltage. Once t_{DHEN} finishes, both UGATE and LGATE start responding to the PWM input. This design is specifically for SGM's PWM controller, utilizing its PWM pin for multi-functional pin.

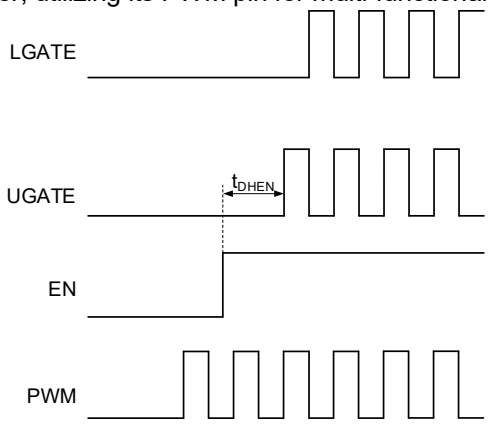


Figure 4. Enable Control

PWM Input

The PWM is a tri-state input pin. A logic high activates the high-side gate driver and deactivates the low-side gate driver once V_{CC} power-on reset (POR) is established and EN keeps high. Conversely, a logic low deactivates the high-side gate driver and activates the low-side gate driver. When the PWM pin is in high-impedance state, high-side and low-side gate drivers maintain in the low-state, turning off both MOSFETs.

In a floating state, an internal bias circuit keeps the PWM pin voltage at 1.6V. During t_{DHEN} (refer to Figure 4), both UGATE and LGATE remain low. The PWM pin stays in a high-impedance state, so any input to the PWM is disregarded.

Low-side Driver

The low-side driver is used to control an N-MOSFET referenced to ground. Its internal bias is connected to both the V_{CC} supply and ground. The low-side driver output is opposite to the PWM input: it is low when the PWM input is high, and it is high when the PWM input is low.

However, if a logic low signal is applied to EN pin or the PWM pin is set to a high-impedance state, the output of the low-side driver will remain at a low level.

High-side Driver

The high-side driver is used to control a floating N-MOSFET, and the bias voltage comes from the internally connected BOOT and PHASE pins. It utilizes an integrated bootstrap switch between the BOOT and VCC pins to provide bias current for the high-side gate driver.

The bootstrap capacitor C_{BOOT} charges to VCC when the PHASE pin is grounded, a result of turning on the low-side MOSFET. Subsequently, when the high-side MOSFET activates, PHASE pin voltage rises to V_{IN}, letting the BOOT pin voltage rise to V_{IN} + V_{CC}. It is crucial for maintaining voltage to keep the high-side MOSFET on.

If a logic low signal is applied to EN pin or the PWM pin is set to a high-impedance state, the output of the high-side driver will remain at a low level.

Shoot-Through Protection

The shoot-through protection circuit can stop the high-side and low-side MOSFETs conduct simultaneously. It accomplishes this by ensuring one MOSFET is activated only after the other has been completely turned off with a proper delay time.

During the high-side MOSFET is shutdown, the anti-shoot-through mechanism monitors UGATE and PHASE voltages. The low-side driver will be at high-state until (V_{UGATE} - V_{PHASE}) voltage drops below 1.2V, confirming the completely turning off the high-side MOSFET.

Similarly, while the low-side MOSFET is shutdown, the high-side driver checks the LGATE voltage. It remains in the off-state until V_{LGATE} drops below 1.2V, ensuring the complete turn-off of the low-side MOSFET.

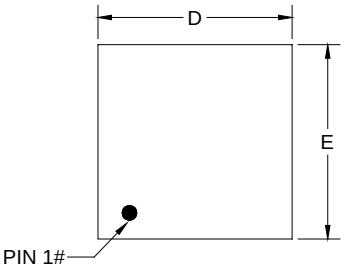
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

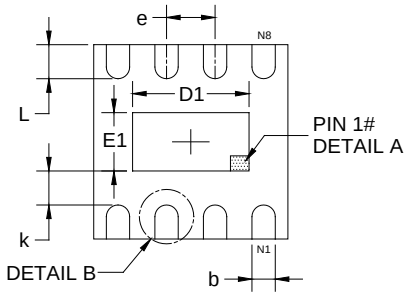
Changes from Original (JUNE 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

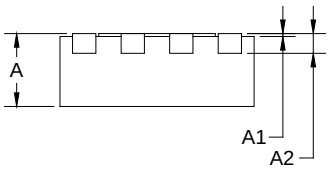
TDFN-2×2-8L



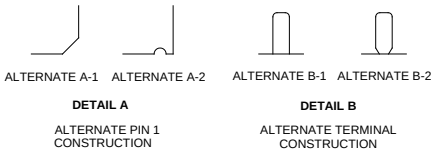
TOP VIEW

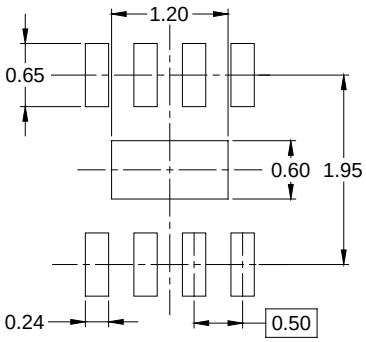


BOTTOM VIEW



SIDE VIEW





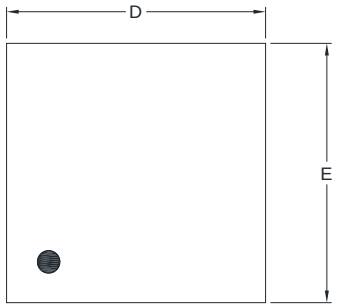
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
D	1.900	2.000	2.100
E	1.900	2.000	2.100
D1	1.100	1.200	1.300
E1	0.500	0.600	0.700
b	0.180	-	0.300
e	0.500 TYP		
k	0.200 MIN		
L	0.250	0.350	0.450

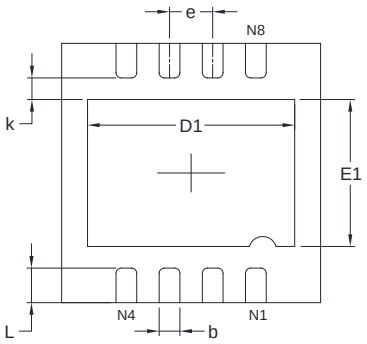
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

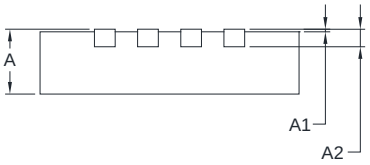
TDFN-3×3-8BL



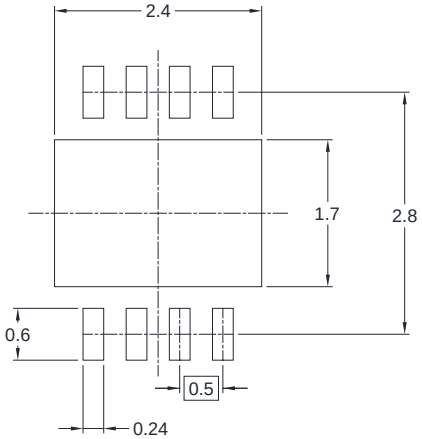
TOP VIEW



BOTTOM VIEW



SIDE VIEW



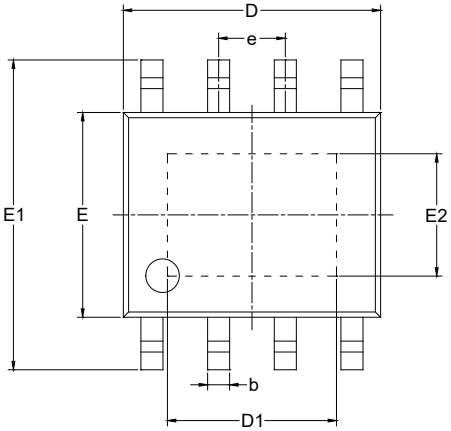
RECOMMENDED LAND PATTERN (Unit: mm)

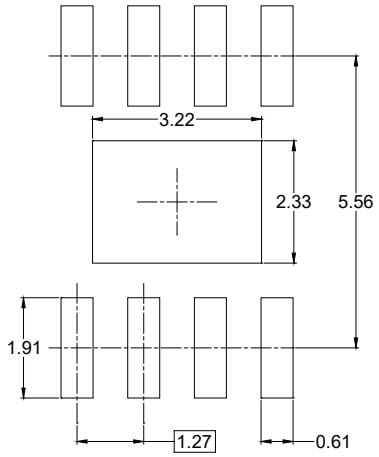
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.500	0.091	0.098
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

NOTE: This drawing is subject to change without notice.

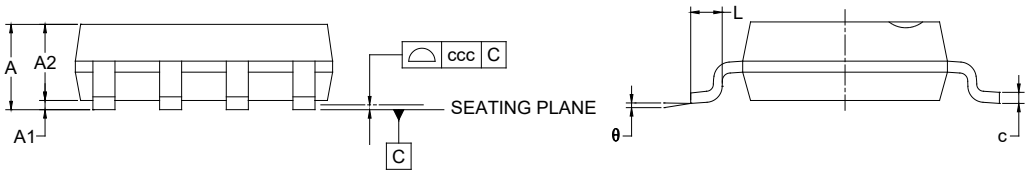
PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

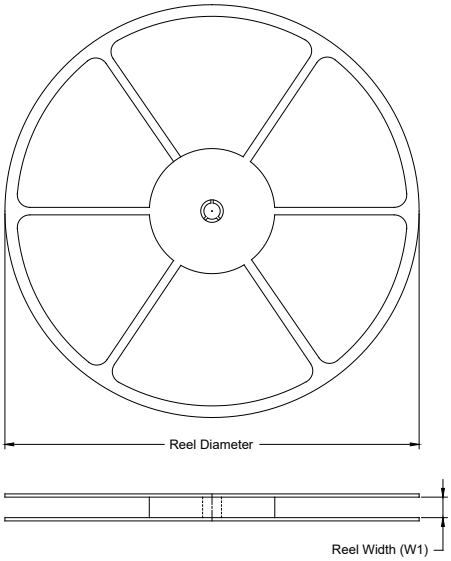


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

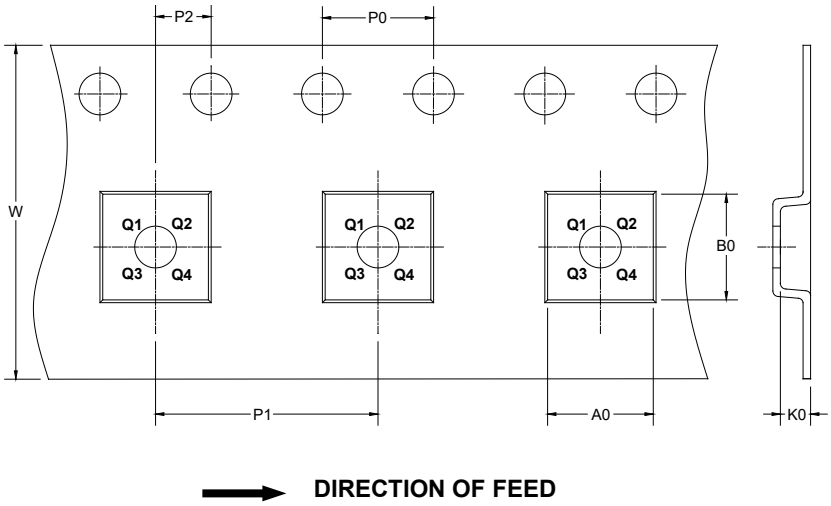
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



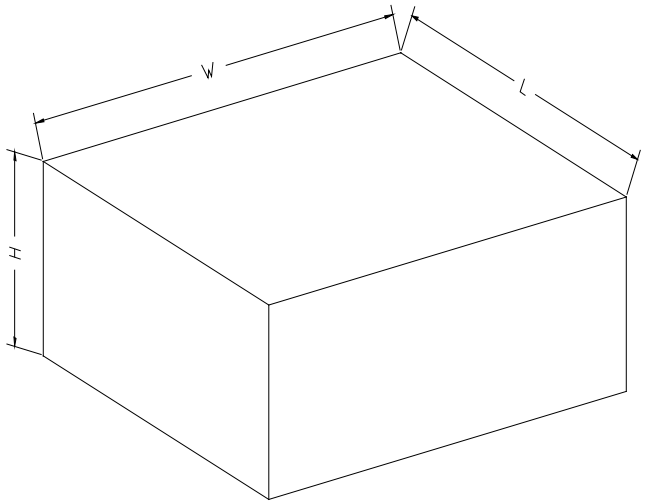
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8L	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1
TDFN-3×3-8BL	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002