SGM6030
0.6A/1A Synchronous Buck Converter with I²C/VSEL Interface

GENERAL DESCRIPTION

The SGM6030 is an efficient and miniature synchronous Buck converter with I²C/VSEL interface. The device implements auto PFM mode operation to maximize the efficiency at light load condition. At moderate to heavy load, the device automatically switches to continuous conduction mode (CCM) operation. Forced PWM operation is also available for better output ripple performance and stable switching frequency. COT-control architecture is implemented to incorporate the benefits of fast load and line transient responses and low output voltage ripple, which is beneficial for RF and noise sensitive applications.

The SGM6030 family offers VSEL option for dynamic voltage scaling (DVS) via the I²C interface, which can adjust the output voltage rapidly to adapt for any changes on the load side.

The SGM6030 is available in a Green WLCSP-0.76×1.42-8B package.

FEATURES

- **1.75V to 5.5V Input Voltage Range**
- **2.5μA (TYP) Operating Quiescent Current**
- **Up to 3.3MHz (TYP) Switching Frequency**
- **VSEL Pin Option for Changing Output Voltage**
- **Output Current**
  - **SGM6030A/B/C/D: 0.6A**
  - **SGM6030E: 1A**
- **Up to 1Mbps I²C Compatible Interface to Set:**
  - **Output Voltage from 0.4V to 1.9875V with 12.5mV Steps**
  - **Output Voltage Ramp Speed**
- **Available in a Green WLCSP-0.76×1.42-8B Package**

APPLICATIONS

Mobile Phones
Wearable and Portable Electronics
Medical Sensor Patches and Patient Monitors

TYPICAL APPLICATION

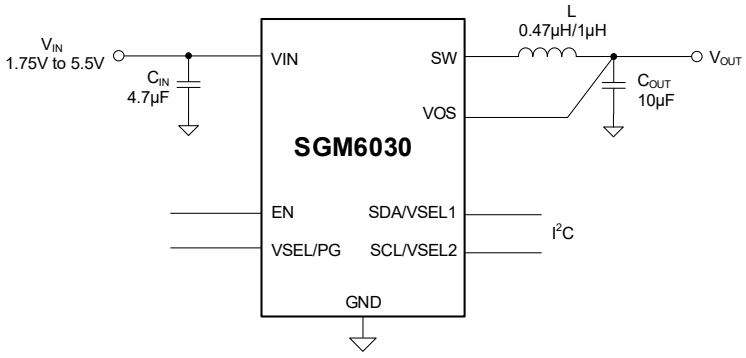


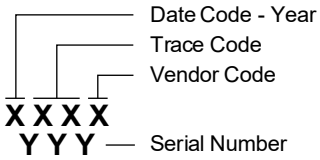
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6030A	WLCSP-0.76×1.42-8B	-40℃ to +125℃	SGM6030AXG/TR	XXXX 1GR	Tape and Reel, 5000
SGM6030B	WLCSP-0.76×1.42-8B	-40℃ to +125℃	SGM6030BXG/TR	XXXX 1TO	Tape and Reel, 5000
SGM6030C	WLCSP-0.76×1.42-8B	-40℃ to +125℃	SGM6030CXG/TR	XXXX 246	Tape and Reel, 5000
SGM6030D	WLCSP-0.76×1.42-8B	-40℃ to +125℃	SGM6030DXG/TR	XXXX 247	Tape and Reel, 5000
SGM6030E	WLCSP-0.76×1.42-8B	-40℃ to +125℃	SGM6030EXG/TR	XXXX 1TP	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE OPTIONS

Device	Output Current	Default Output Voltage Setting	f_{SW_FCCM}	User Interfaces
SGM6030A	0.6A	0.6V, 1.1V	1.4MHz	EN, I²C, VSEL
SGM6030B	0.6A	0.6V, 0.7V, 0.8V, 1.0V	1.4MHz	2 × VSEL, EN, PG
SGM6030C	0.6A	1.05V, 0.65V	1.4MHz	EN, I²C, VSEL
SGM6030D	0.6A	0.85V, 1.1V	1.4MHz	EN, I²C, VSEL
SGM6030E	1.0A	0.6V, 1.1V	3.3MHz	EN, I²C, VSEL

ABSOLUTE MAXIMUM RATINGS

VIN ..... -0.3V to 6V
SW ..... -0.3V to V_{IN} + 0.3V
SW Transient < 10ns, While Switching ..... -2.5V to 9V
EN, VSEL/PG, SDA/VSEL1, SCL/VSEL2 ..... -0.3V to 6V
VOS ..... -0.3V to 5V
Package Thermal Resistance
WLCSP-0.76×1.42-8B, θ_{JA} ..... 170.2℃/W
WLCSP-0.76×1.42-8B, θ_{JB} ..... 53.9℃/W
WLCSP-0.76×1.42-8B, θ_{JC} ..... 54.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage, V_{IN} ..... 1.75V to 5.5V
Output Voltage, V_{OUT} ..... 0.4V to 1.9875V
SW Voltage ..... 0V to 5.5V
EN, VSEL/PG, SDA/VSEL1, SCL/VSEL2 ..... 0V to 5.5V
Output Current Range, I_{OUT}
SGM6030E, V_{IN} > 2.3V ..... 1A (MAX)
SGM6030E, V_{IN} ≤ 2.3V ..... 0.7A (MAX)
SGM6030A/B/C/D ..... 0.6A (MAX)
Power Good Input Current Capability, I_{PG} ..... 1mA (MAX)
Effective Input Capacitance, C_{IN} ..... 2μF (MIN), 4.7μF (TYP)
SGM6030E
Effective Inductance, L ..... 0.33μH to 0.82μH, 0.47μH (TYP)
Effective Output Capacitance, C_{OUT} ..... 2μF to 26μF
SGM6030A/B/C/D
Effective Inductance, L ..... 0.7μH to 1.2μH, 1.0μH (TYP)
Effective Output Capacitance, C_{OUT} ..... 3μF to 26μF
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

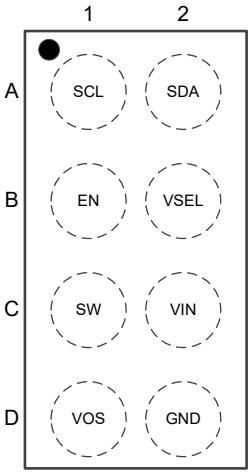
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

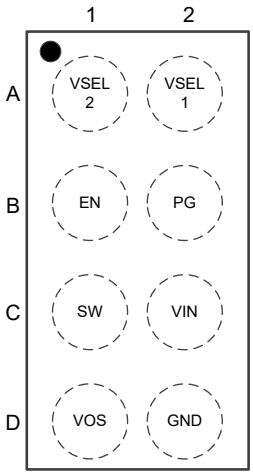
PIN CONFIGURATIONS

SGM6030A/C/D/E (TOP VIEW)



WLCSP-0.76×1.42-8B

SGM6030B (TOP VIEW)



WLCSP-0.76×1.42-8B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	SCL	I	I^2C Bus Clock Signal. Do not leave it floating. Connect it to AGND if not used.
	VSEL2	I	Voltage Selection Pin. Can be toggled during operation.
A2	SDA	I	I^2C Bus Data Signal. Do not leave it floating. Connect it to AGND if not used.
	VSEL1	I	Voltage Selection Pin. Can be toggled during operation.
B1	EN	I	Device Enable Pin. Logic high on this pin enables the device, and logic low on this pin disables the device. Do not leave it floating. The pin is connected with an internal pull-down resistor, which becomes inactive once the device is powered on.
B2	VSEL	I	Voltage Selection Pin. Can be toggled during operation. Low = 0.6V (SGM6030A/E), 1.05V (SGM6030C), 0.85V (SGM6030D). High = 1.1V (SGM6030A/D/E), 0.65V (SGM6030C).
	PG	O	Power Good Output. This is an open-drain signal. A pull-up resistor (connected to a DC voltage) is required to indicate high if the output voltage is within the regulation.
C1	SW	P	Switching Node Output. Connect it to the filter inductor.
C2	VIN	P	Power Supply Input. Connect a ceramic capacitor (C_{IN}) close to this pin and GND.
D1	VOS	I	Output Voltage Sense Input. This pin is internally connected to the feedback loop and a MOSFET to discharge the output voltage (V_{OUT}) when the device is disabled. Connect it to the output capacitor with a short trace.
D2	GND	G	Ground Pin. Connect the C_{IN} and C_{OUT} ground terminals close to this pin.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply								
VIN Quiescent Current	I_Q	EN = VIN, I_{OUT} = 0μA, V_{OUT} = 1.2V, device not switching, T_J = -40℃ to +85℃				2.5	5	μA
		EN = VIN, I_{OUT} = 0μA, V_{OUT} = 1.2V, device switching				2.5		
VIN Shutdown Supply Current	I_{SD}	EN = GND, shutdown current into VIN, VSEL = GND		T_J = +25℃		100	150	nA
				T_J = -40℃ to +85℃			800	
UVLO								
VIN UVLO Rising Threshold	V_{UVLO_R}	V_{IN} rising				1.69	1.75	V
VIN UVLO Falling Threshold	V_{UVLO_F}	V_{IN} falling				1.58	1.65	V
VIN UVLO Hysteresis	V_{UVLO_H}					110		mV
Logic Pins								
High-Level Input Voltage Threshold	V_{IH}				0.8			V
Low-Level Input Voltage Threshold	V_{IL}						0.4	V
Input Leakage Current into SDA, SCL, VSEL	I_{LKG}	Pin connected to VIN, T_J = -40℃ to +85℃				10		nA
EN Internal Pull-Down Resistance		EN Pin to GND				0.5		MΩ
Input Leakage into EN	I_{LKG}	Pin connected to VIN, T_J = -40℃ to +85℃				10		nA
VOUT Voltage								
Output Voltage Accuracy	V_{OUT}	PWM mode, no load	1V < V_{OUT} ≤ 1.9875V	T_J = +25℃	-1.5		+1.5	%
				T_J = +25℃ to +125℃	-2		+2	
			0.5V < V_{OUT} ≤ 1V	T_J = +25℃	-2		+2	
				T_J = +25℃ to +125℃	-2.5		+2.5	
			0.4V < V_{OUT} ≤ 0.5V	T_J = +25℃	-2		+2	
				T_J = -40℃ to +125℃	-3		+3	
VOS Input Leakage Current	I_{VOS_LKG}	EN = VIN, V_{OUT} = 1.2V (internal 3.2MΩ resistor divider), T_J = -40℃ to +85℃				400	1000	nA
Switching Frequency								
Switching Frequency, FCCM Operation	f_{SW_FCCM}	V_{IN} = 3.6V, V_{OUT} = 1.2V, PWM operation		SGM6030E		3.3		MHz
				SGM6030A/B/C/D		1.4		
Start-up								
Internal Fixed Soft-Start Time	t_{SS}	from V_{OUT} = 0V to 95% of V_{OUT} nominal				0.12	0.25	ms
EN High to Start of Switching Delay						500	1100	μs
Power Stage								
High-side MOSFET On-Resistance	R_{DSON_H}	I_{OUT} = 500mA				115	180	mΩ
Low-side MOSFET On-Resistance	R_{DSON_L}	I_{OUT} = 500mA				90	165	mΩ
Over-Current Protection								
High-side Peak Current Limit	I_{HS_OC}	SGM6030E			1.20	1.70	2.10	A
Low-side Valley Current Limit	I_{LS_OC}	SGM6030E			0.75	1.05	1.30	A
High-side Peak Current Limit	I_{HS_OC}	SGM6030A/B/C/D			0.95	1.20	1.45	A
Low-side Valley Current Limit	I_{LS_OC}	SGM6030A/B/C/D			0.65	0.85	1.05	A
Low-side Negative Current Limit	I_{LS_NOC}	Sinking current limit on low-side FET				0.65		A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, all typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Good						
Power Good Threshold	V_{PGTH}	PGOOD low, V_{OS} falling		93		%
		PGOOD high, V_{OS} rising		96		
Power Good Deglitch Delay	t_{PG_DLY}	PG rising edge		50		μs
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		10		nA
PG Pin Output Low-Level Voltage		I_{PG} = 1mA			400	mV
Output Discharge						
Output Discharge Resistor on VOS Pin		EN = GND, I_{VOS} = -10mA into VOS pin, T_J = -40℃ to +85℃		7	11	Ω
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	Temperature rising, PWM mode		160		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

I²C INTERFACE TIMING CHARACTERISTICS

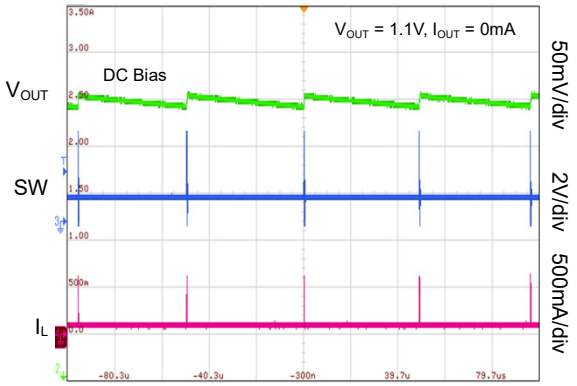
PARAMETER (1)	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode			100	kHz
		Fast Mode			400	kHz
		Fast Mode Plus			1	MHz
Bus Free Time Between a Stop and Start Condition	t_{BUF}	Standard Mode	4.7			μs
		Fast Mode	1.3			
		Fast Mode Plus	0.5			
Hold Time (Repeated) Start Condition	t_{HD}, t_{STA}	Standard Mode	4			μs
		Fast Mode	0.6			
		Fast Mode Plus	0.26			
Low Period of the SCL Clock	t_{LOW}	Standard Mode	4.7			μs
		Fast Mode	1.3			
		Fast Mode Plus	0.5			
High Period of the SCL Clock	t_{HIGH}	Standard Mode	4			μs
		Fast Mode	0.6			
		Fast Mode Plus	0.26			
Setup Time for a Repeated Start Condition	t_{SU}, t_{STA}	Standard Mode	4.7			μs
		Fast Mode	0.6			
		Fast Mode Plus	0.26			
Data Setup Time	t_{SU}, t_{DAT}	Standard Mode	250			ns
		Fast Mode	100			
		Fast Mode Plus	50			
Data Hold Time	t_{HD}, t_{DAT}	Standard Mode	0		3.45	μs
		Fast Mode	0		0.9	
		Fast Mode Plus	0			
Rise Time of SCL Signal	t_{RCL}	Standard Mode			1000	ns
		Fast Mode	$20 + 0.1C_B$		300	
		Fast Mode Plus			120	
Rise Time of SCL Signal after a Repeated Start Condition and after an Acknowledge Bit	t_{RCL1}	Standard Mode	$20 + 0.1C_B$		1000	ns
		Fast Mode	$20 + 0.1C_B$		300	
		Fast Mode Plus			120	
Fall Time of SCL Signal	t_{FCL}	Standard Mode	$20 + 0.1C_B$		300	ns
		Fast Mode			300	
		Fast Mode Plus			120	
Rise Time of SDA Signal	t_{RDA}	Standard Mode			1000	ns
		Fast Mode	$20 + 0.1C_B$		300	
		Fast Mode Plus			120	
Fall Time of SDA Signal	t_{FDA}	Standard Mode			300	ns
		Fast Mode	$20 + 0.1C_B$		300	
		Fast Mode Plus			120	
Setup Time of Stop Condition	t_{SU}, t_{STO}	Standard Mode	4			μs
		Fast Mode	0.6			
		Fast Mode Plus	0.26			
Capacitive Load for SDA and SCL	C_B	Standard Mode			400	pF
		Fast Mode			400	
		Fast Mode Plus			550	

NOTE:
1. All values refer to V_{IL} (MAX) and V_{IH} (MIN) levels.

TYPICAL PERFORMANCE CHARACTERISTICS

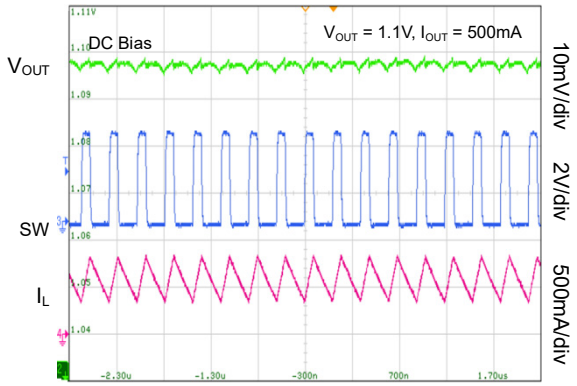
T_A = +25℃, V_{IN} = 3.8V, unless otherwise noted.

PFM Mode Operation



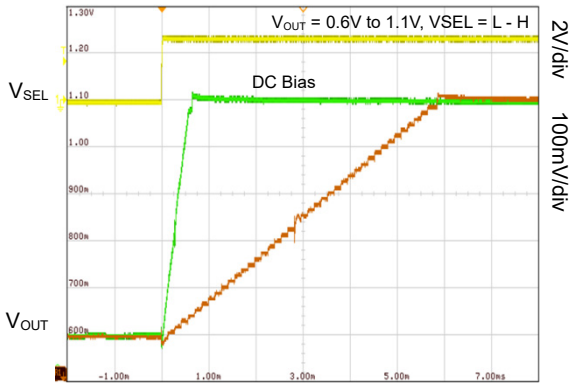
Time (20μs/div)

Forced PWM Mode Operation



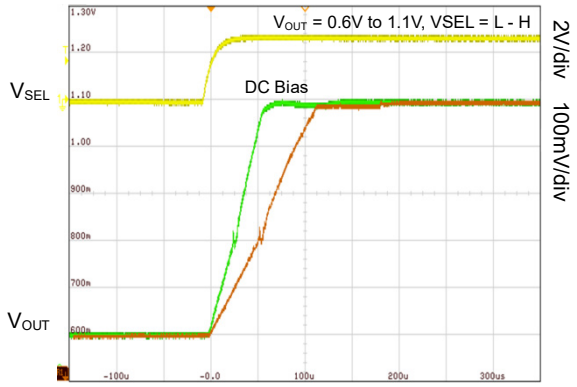
Time (500ns/div)

DVS with 0.1mV/μs, 1mV/μs Slew Rate



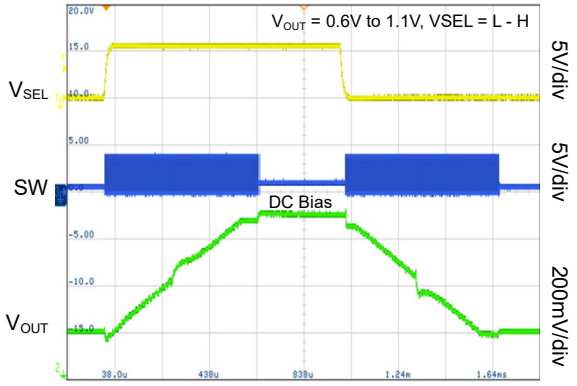
Time (1ms/div)

DVS with 5mV/μs, 10mV/μs Slew Rate



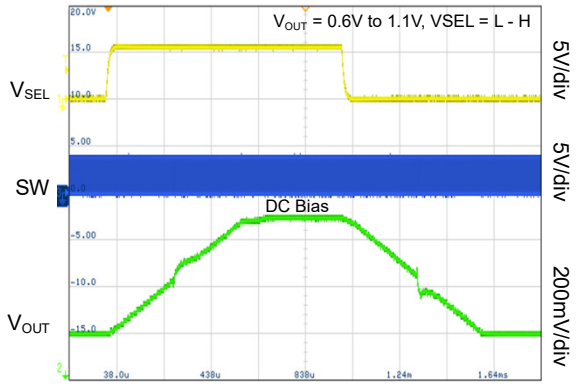
Time (50μs/div)

DVS with 1mV/μs in PFM Mode



Time (200μs/div)

DVS with 1mV/μs in FCCM Mode

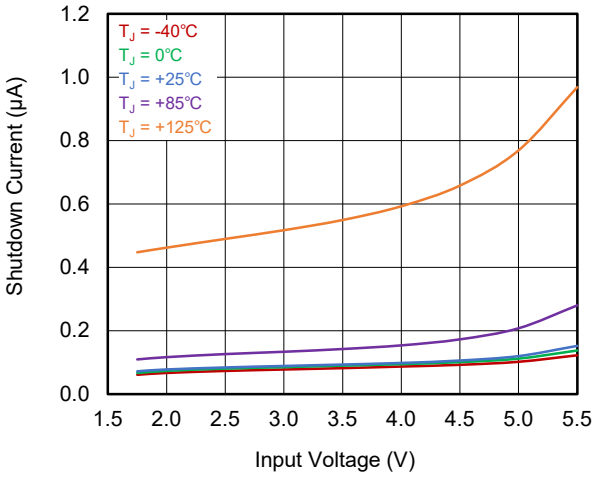


Time (200μs/div)

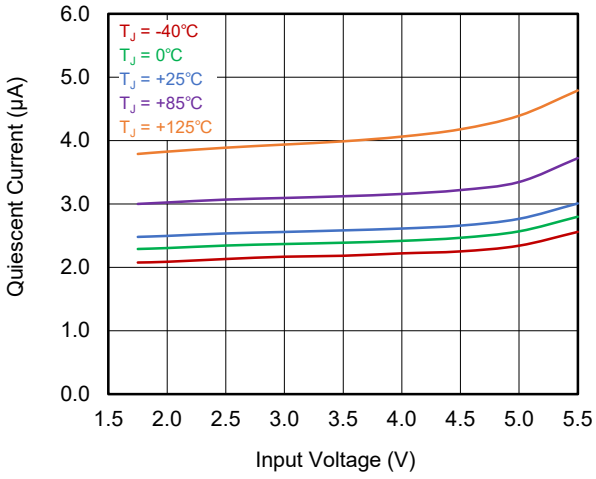
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.8V, unless otherwise noted.

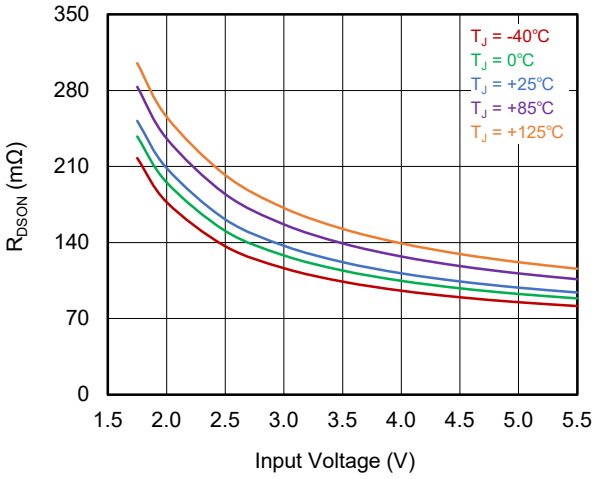
Shutdown Current vs. Input Voltage



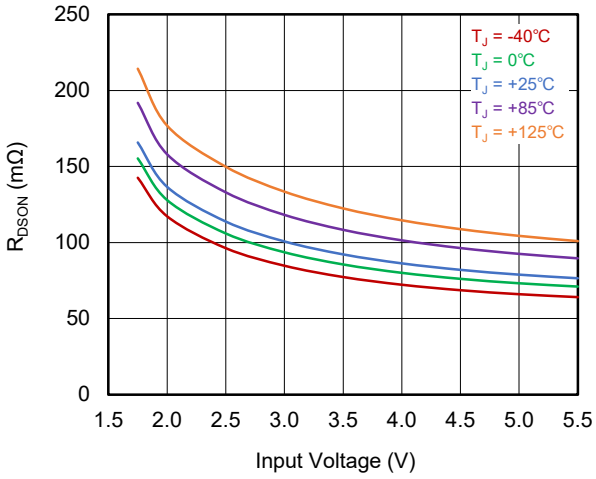
Quiescent Current vs. Input Voltage



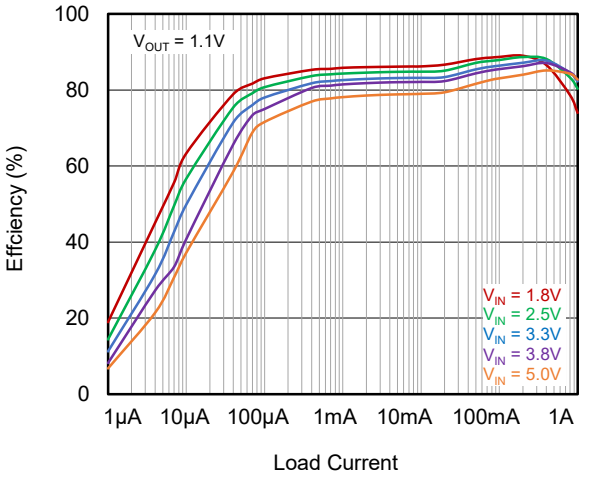
High-side Switch Drain Source Resistance vs. Input Voltage



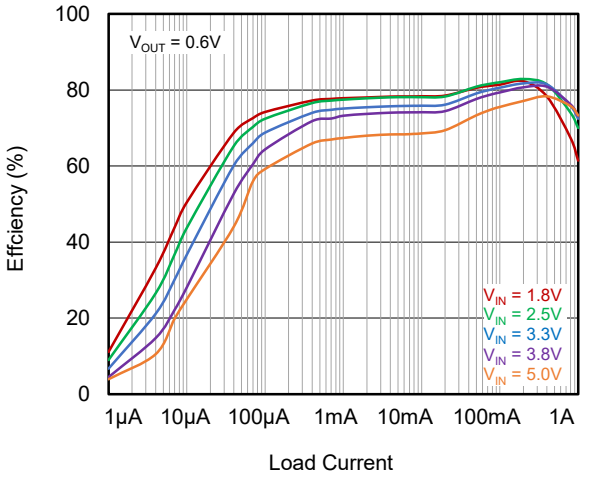
Low-side Switch Drain Source Resistance vs. Input Voltage



Efficiency vs. Load Current in Power Save Mode (SGM6030E)



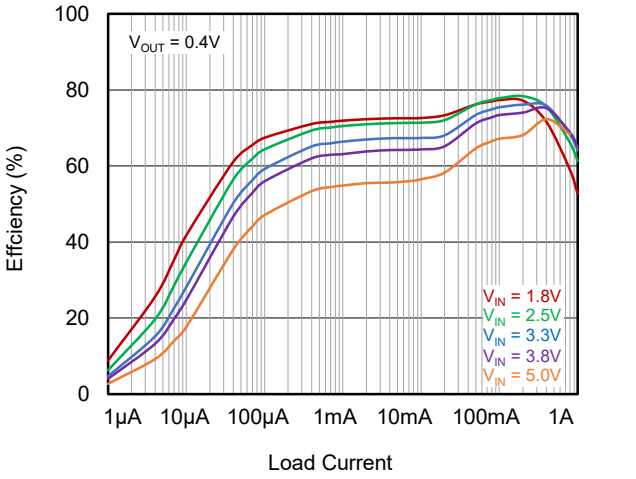
Efficiency vs. Load Current in Power Save Mode (SGM6030E)



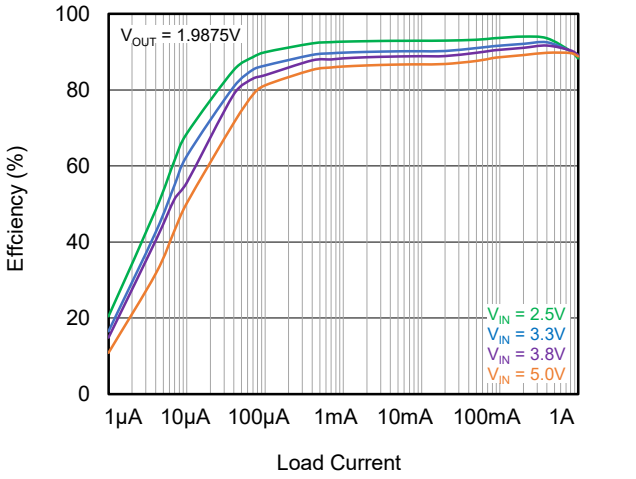
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.8V, unless otherwise noted.

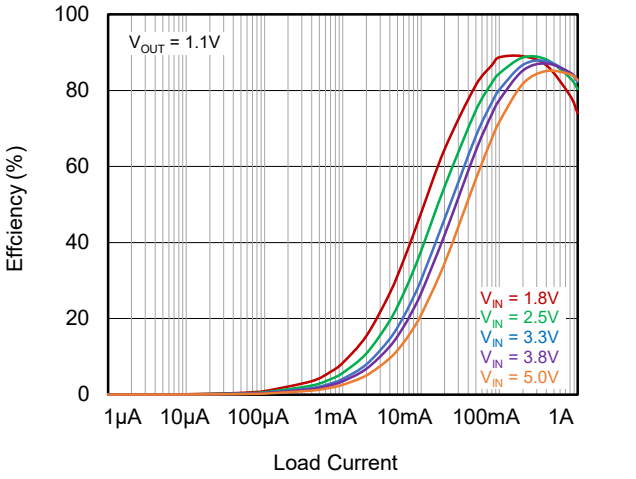
Efficiency vs. Load Current in Power Save Mode (SGM6030E)



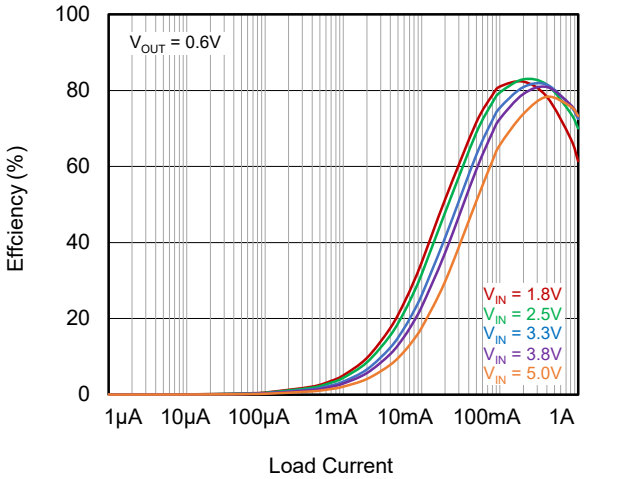
Efficiency vs. Load Current in Power Save Mode (SGM6030E)



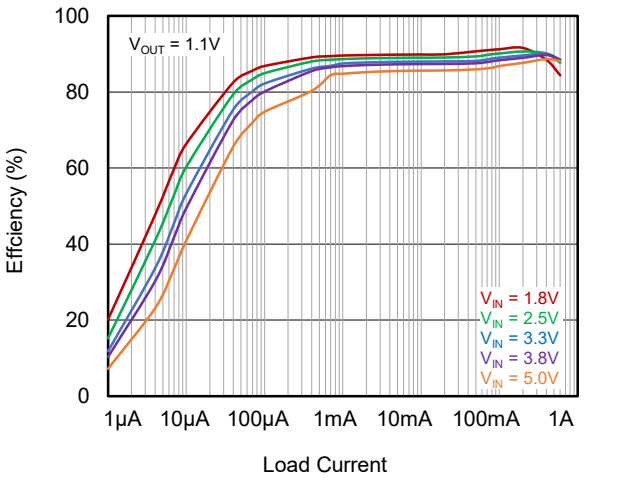
Efficiency vs. Load Current in Forced PWM Mode (SGM6030E)



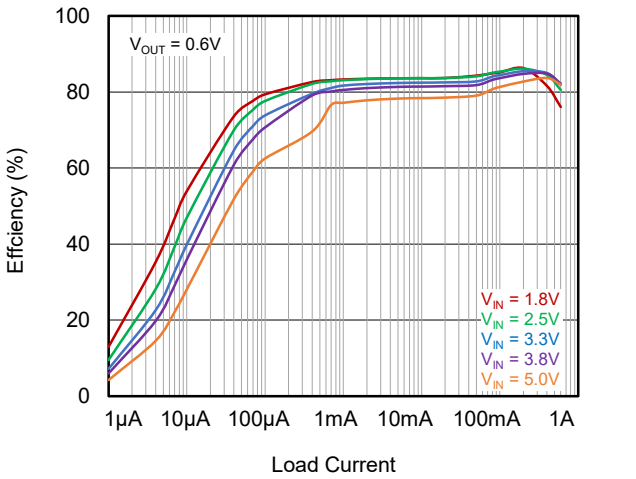
Efficiency vs. Load Current in Forced PWM Mode(SGM6030E)



Efficiency vs. Load Current in Power Save Mode (SGM6030A)



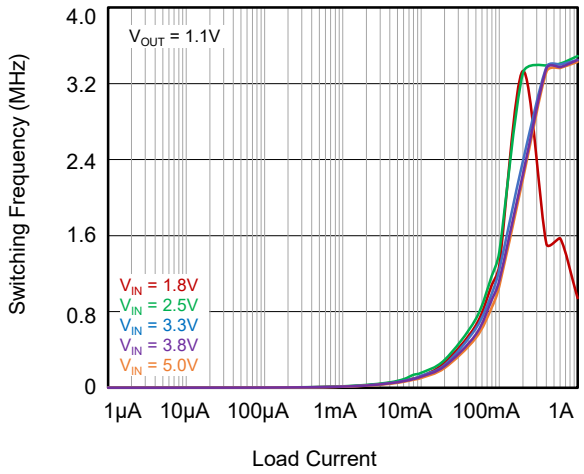
Efficiency vs. Load Current in Power Save Mode (SGM6030A)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.8V, unless otherwise noted.

Switching Frequency vs. Load Current in Power Save Mode (SGM6030E)



FUNCTIONAL BLOCK DIAGRAM

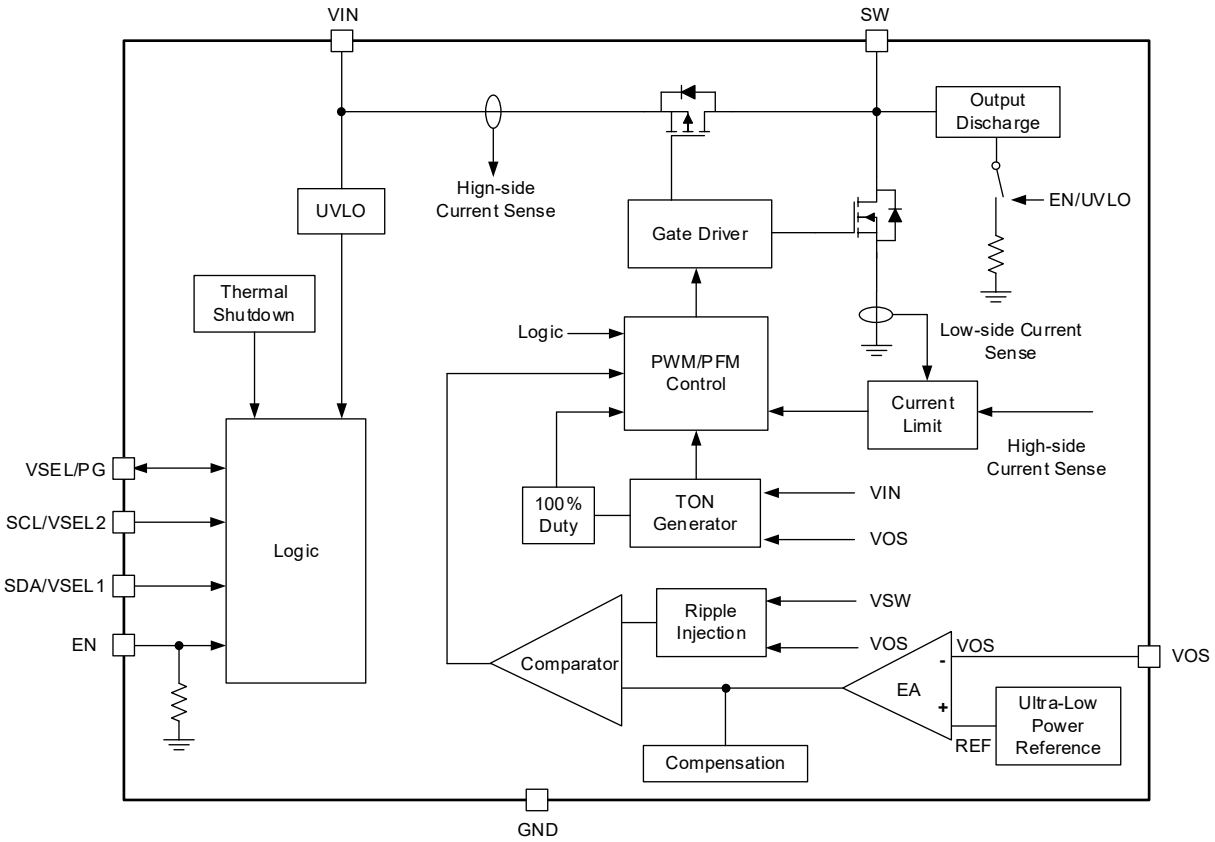


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6030 is a 2.5μA (TYP) quiescent current synchronous Buck converter that adopts the constant on-time (COT) control architecture to achieve excellent load/line transient performance. The family of SGM6030 devices offers easy programmable output voltages via I²C settings with 12.5mV adjustment steps, or the SGM6030B offers 4 different fixed output voltages via programming the VSEL1 and VSEL2 pins. The COT architecture is not limited by traditional fixed frequency architecture where switching pulses are confined by the edge switching frequency clock, a main voltage comparator is implemented to signal the changes occurring at the output. In addition, by sensing the actual output voltage, the COT architecture can quickly adapt to any load transient event and quickly adjust the switching frequency to replenish the energy delivered to the load. An internally compensated voltage error amplifier is also implemented in the SGM6030 to provide accurate DC load regulation. The SGM6030 just needs 4 external components to realize the design, which significantly reduces the solution size.

Feature Description

Power-Save Mode

As the load current decreases, the inductor current reaches around 0A in a switching cycle, the operation mode becomes discontinuous. The SGM6030 automatically enters power-save mode (PSM) in discontinuous mode. Adding more output capacitors will minimize the output voltage rise in PSM.

Forced PWM Operation

The SGM6030 is able to operate in forced PWM mode to achieve fixed switching frequency and output ripple across the entire operating load range. Forced PWM is configurable in **REG0x03** control register via I²C.

Enable and Shutdown (EN)

I²C interface is live when the EN pin is toggled logic high after the enable delay time. When the EN pin is toggled to logic low, power FETs are off as well as the internal control circuits, register settings are reset except the EN_DIS bit. Device enters shutdown mode when EN pin is logic low, I²C communication is terminated in this mode.

The device also supports a software enable/disable via EN_DEVICE bit in **REG0x03** register while EN pin is toggled to logic high. When the device is enabled by this bit, the device starts up with soft-start time. No EN high to start the switching delay is required. When the device is disabled by this bit, the device stops switching, but I²C communication remains active.

Soft-Start

When the input voltage is above the UVLO rising threshold of 1.69V (TYP), toggling the enable pin to logic high to start up the device. Before the output voltage starts ramping up, the device has an enable delay of 500μs (TYP). During the enable delay, the device establishes the internal reference determined by the VSEL pin or VSEL1/2 pin. The internal registers can be programmed via I²C after the enable delay.

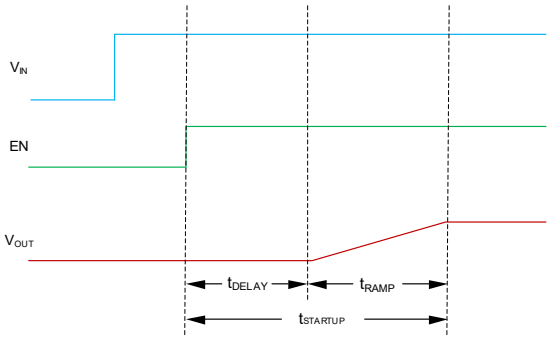


Figure 3. Start-up Sequence

The device initiates an internal soft-start when the enable delay finishes. The internal soft-start time is fixed to 0.12ms (TYP) to ramp up the output voltage from 0V to the programmed output voltage (95%). The soft-start mechanism effectively reduces the inrush current drawn from the input source, as well as providing a controlled output voltage rising ramp. For pre-biased output voltage start-up, the device starts up from the pre-biased voltage to the programmed output voltage.

Output Voltage Selection (VSEL) for SGM6030B

SGM6030B uses 2 VSEL interfaces to set the output voltage. The programmable output voltages are shown in Table 1.

Table 1. Target Output Voltages Setting by VSEL Interface

VSEL1	VSEL2	SGM6030B	Operation Mode
0	0	0.6V	PFM
1	0	0.7V	PFM
0	1	0.8V	PFM
1	1	1.0V	PFM

DETAILED DESCRIPTION (continued)

Output Voltage Selection (VSEL and I²C)

The device offers 2 selectable output voltage registers. Dynamic voltage scaling (DVS) is supported via these 2 registers. VSEL is utilized to select the active register between VO1_SET bits and VO2_SET bits.

Output voltage adjustment can be made via either I²C programming or toggling the VSEL pin, and the output voltage ramp-up/down speed is also configurable via the VOL_RAMP bits in **REG0x03** register.

Forced PWM Mode during V_{OUT} Change

During normal operation, the device does not enter forced PWM mode when receives a VSEL toggle or an I²C command to adjust V_{OUT}. Forced PWM mode during DVS allows a controlled downward ramp of V_{OUT} independent of load condition.

Power Good (PG) for SGM6030B

The SGM6030B (do not have VSEL) offers power good function. The device starts to compare the actual output voltage with the VSEL1/2 programmed output voltage after the enable delay time. When the voltage reaches 96% (TYP) of programmed output voltage, after 50μs (TYP) delay, the PG enters high-impedance status. When VIN starts up for the first time, the PG remains high until the device is enabled for the first time.

By default, the PG is pulled low immediately during the DVS stage without any blanking period or delay. Once the output voltage (V_{OUT}) reaches the new target level, the PG signal becomes high again.

Table 2. Power Good Indicator Function Table

Logic Signals				DVS Transition Active	PG Status
V_{IN}	EN	Thermal Shutdown	V_{OUT}		
V_{IN} > UVLO	H	NO	V_{OUT} on Target	NO	Z
	H	NO		YES	L
	H	NO	V_{OUT} < Target	*X*	L
	H	YES	*X*	*X*	L
	L	*X*	*X*	*X*	L
V_{IN} < UVLO	*X*	*X*	*X*	*X*	Undefined

H = High Voltage Level, L = Low Voltage Level,

Z = High-Impedance State, *X* = Don't Care

Under-Voltage Lockout (UVLO)

The SGM6030 offers input under-voltage lockout to prevent false triggering with unstable input source. The device's UVLO rising voltage is 1.69V (TYP) and falling threshold is 1.58V (TYP). Device stops operation as soon as the input voltage drops below the falling threshold. The output voltage discharge is active when UVLO falling threshold is reached. The output voltage discharge function is programmable via **REG0x03** register.

Switch Current Limit/Short-Circuit Protection

The device implements over-current protection when the load exceeds the maximum allowed 1A (SGM6030E) or 0.6A (SGM6030A/B/C/D) to prevent excessive current drawn from battery type inputs. During an output short scenario or a saturated inductor, the inductor current will reach the current limit threshold. When the current limit threshold is reached, the device turns off the high-side switch to terminate the inductor current from further increase, and the low-side switch turns on to ramp down the inductor current to the low-side switch current limit.

During the short-circuit event, as the output voltage drops below 150mV, the current limit threshold is foldback to 0.66A for SGM6030A/B/C/D/E version to prevent the device from excessive temperature rise.

Output Voltage Discharge

The device implements I²C programmable output voltage discharge function for application requiring sequencing control. The internal discharge path discharges the output voltage through the SW pin to ground. There are four scenarios to discharge the output voltage: EN pin is toggled to logic low. EN_DEVICE bit in **REG0x03** register is set to 0, input voltage UVLO and device thermal shutdown.

Output voltage discharge function is disabled when the EN_DIS bit is set to 0. The output discharge function remains active as long as the input voltage is higher than 1V (TYP) and the EN_DIS bit is retained. When a rising edge of the EN pin is applied, the EN_DIS bit is reset.

Thermal Shutdown

As the junction temperature exceeds the T_{SD} (160℃, TYP), the device stops switching, enabling active discharge to discharge the output voltage and disable both MOSFETs. The device has a 20℃ thermal shutdown hysteresis to allow the device to resume operation automatically with an internal soft-start. The register settings are not changed during thermal shutdown. This function is disabled when the device is under PFM mode.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM6030 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM6030 operates as a slave device that address is 0x40 (40H). It has four 8-bit registers, numbered from REG0x01 to REG0x03 and REG0x05. A register read besides these REGs returns 0xFF.

Physical Layer

The standard I²C interface of SGM6030 supports standard mode and fast mode plus communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode plus is up to 1Mbits/s. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 6. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

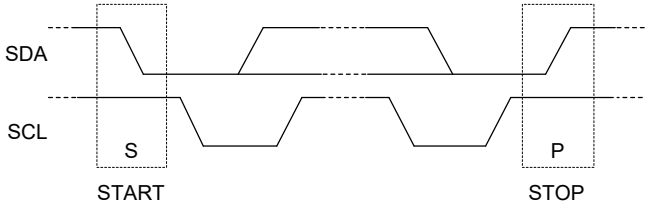


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

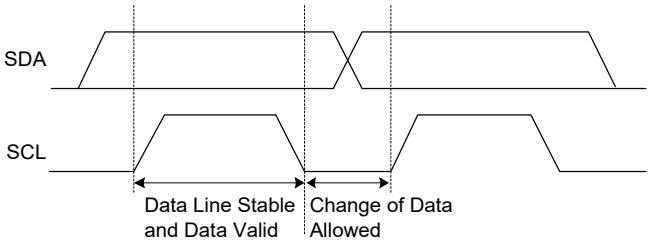


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 6 shows the byte transfer process with I²C interface.

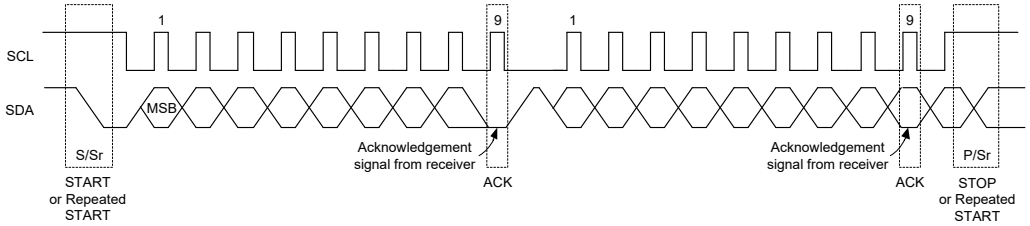


Figure 6. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 10 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 11), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

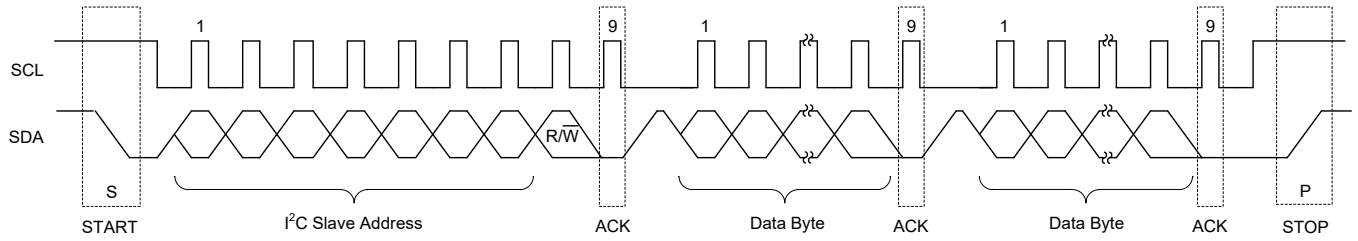


Figure 7. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

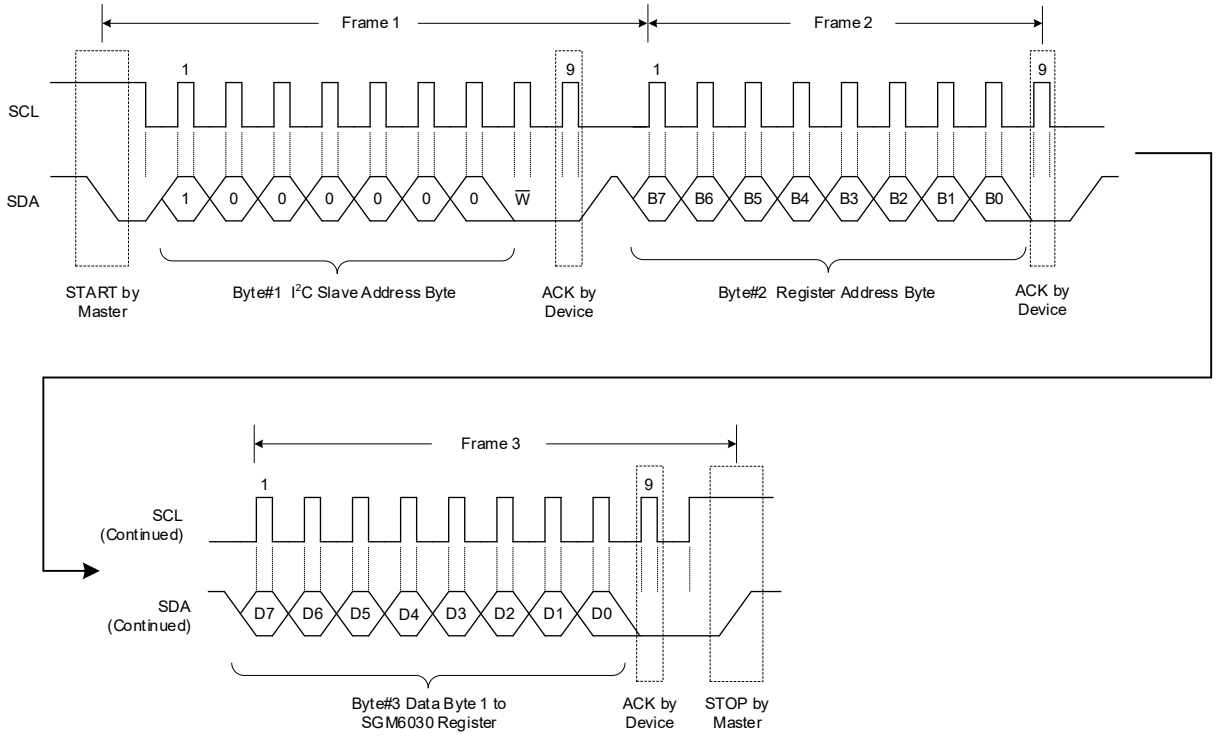


Figure 8. A Single Write Transaction

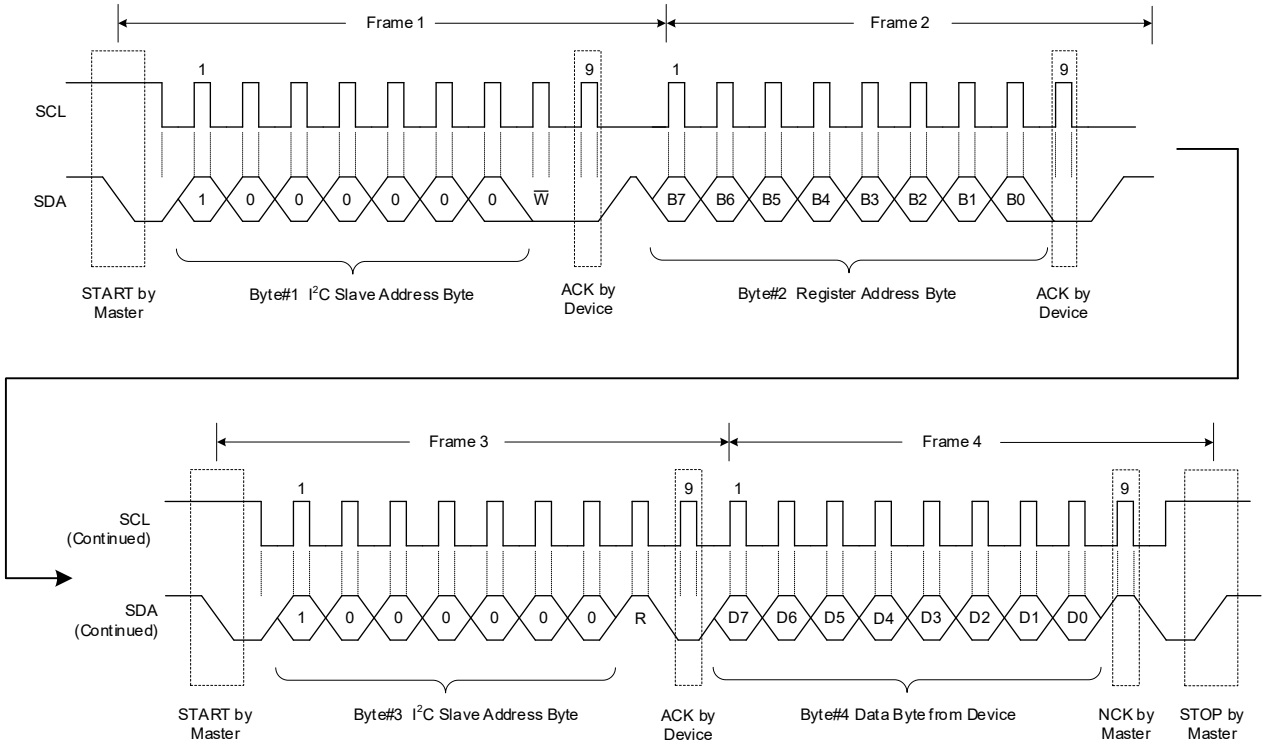


Figure 9. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM6030 for REG0x01 through REG0x05 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

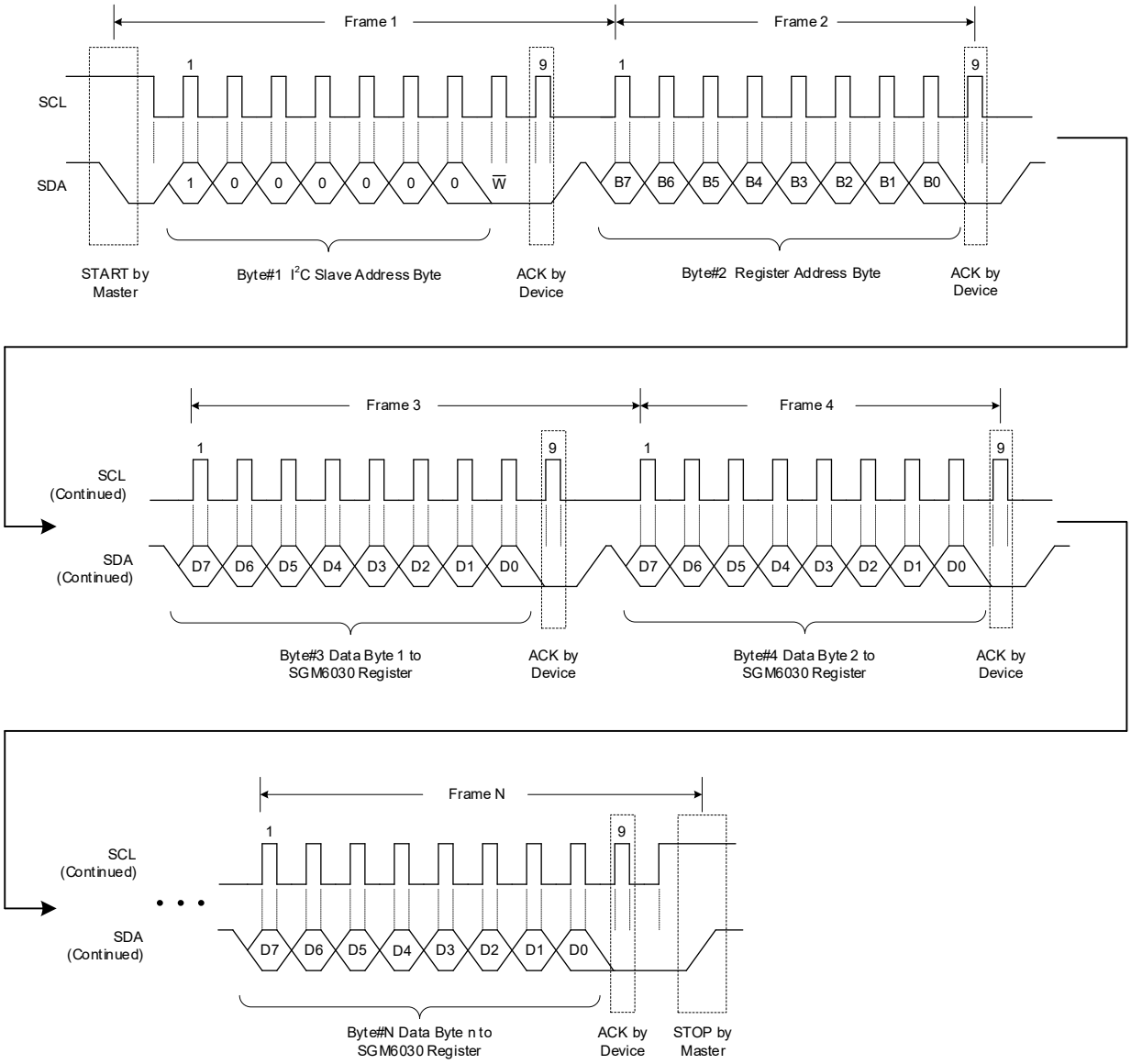


Figure 10. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

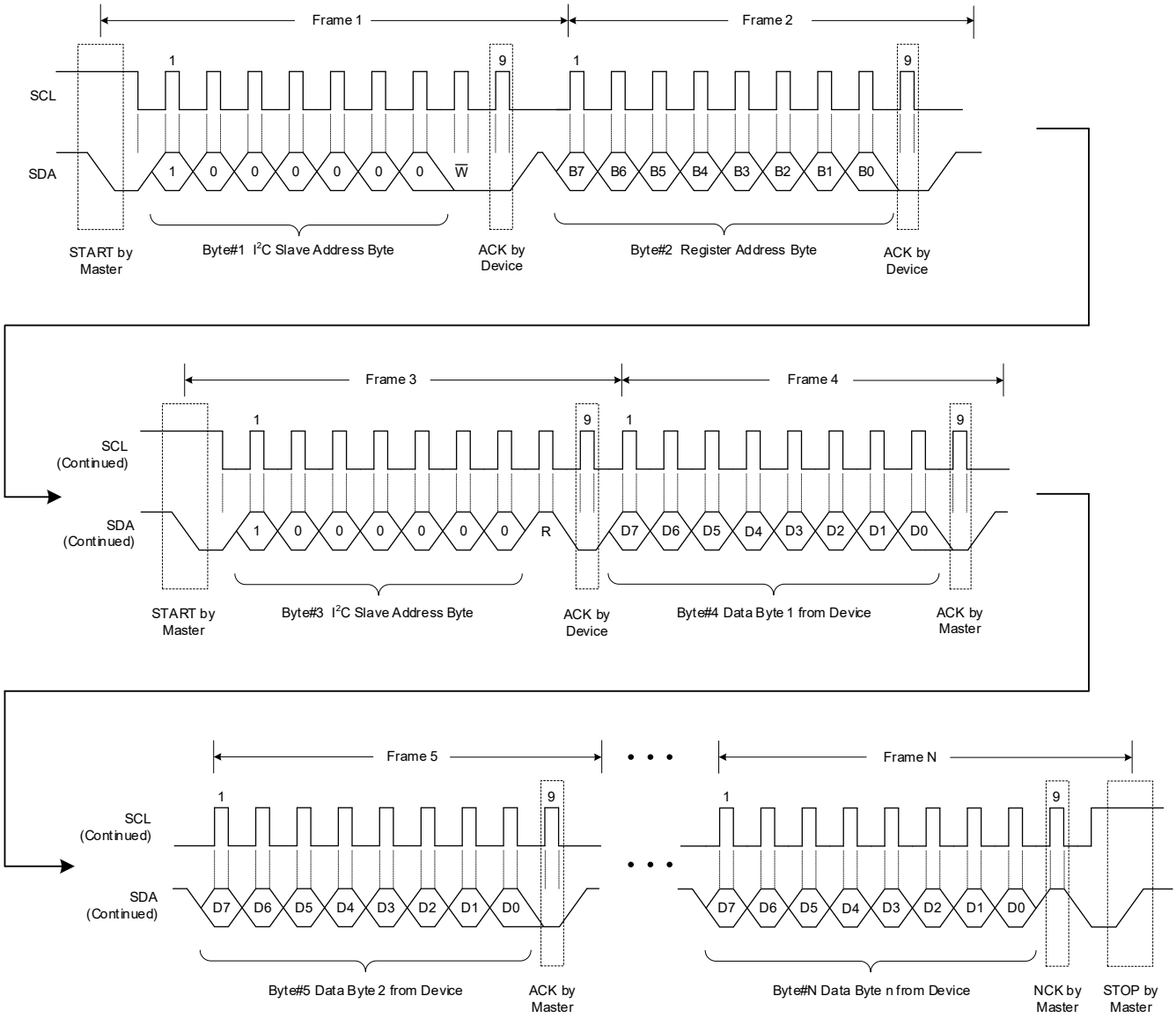


Figure 11. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x01	VO1_SET	Reserved	VO1_SET[6:0]						
0x02	VO2_SET	OPE_MODE	VO2_SET[6:0]						
0x03	CONTROL	RST	EN_FPWM_CHG	EN_DEVICE	EN_FPWM	EN_DIS	Reserved	VOL_RAMP[1:0]	
0x05	STATUS	Reserved			TSD_STAT	Reserved	POWER_BAD_STAT	Reserved	

I²C Slave Address of SGM6030: 0x40 (0b1000000 + R/W)

Bit Types:

R: Read only

R/W: Read/Write

REG0x01: Output Voltage Register 1 [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	N/A
D[6:0]	VO1_SET[6:0]	001 0000	R/W	Target Output Voltage Setting V_{OUT1} = VO1_SET[6:0] × 0.0125V + 0.4V Offset = 0.4V Default = 0.6V (001 0000), SGM6030A/E Default = 0.85V (010 0100), SGM6030D Default = 1.05V (011 0100), SGM6030C Range = 0.4V (000 0000) ~ 1.9875V (111 1111)	REG_RST

REG0x02: Output Voltage Register 2 [Reset = 0x38]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	OPE_MODE	0	R/W	Operation Mode 0 = Keep PFM/PWM selection as in control register. (default) 1 = Set the device in PWM operation for this voltage selection.	REG_RST
D[6:0]	VO2_SET[6:0]	011 1000	R/W	Target Output Voltage Setting V_{OUT2} = VO2_SET[6:0] × 0.0125V + 0.4V Offset = 0.4V Default = 0.65V (001 0100), SGM6030C Default = 1.10V (011 1000), SGM6030A/D/E Range = 0.4V (000 0000) ~ 1.9875V (111 1111)	REG_RST

REGISTER MAPS (continued)

REG0x03: Control Register [Reset = 0x68 for SGM6030C or 0x6B for SGM6030A/D/E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	RST	0	W	Reset 1 = Reset all registers to default. This bit triggers a shutdown followed by a re-reading of the internal OTP settings and a new soft-start.	N/A
D[6]	EN_FPWM_CHG	1	R/W	Enable Forced PWM mode during output voltage change. 0 = Keep the current mode status during output voltage change. 1 = Force the device in FPWM during output voltage change. (default)	REG_RST
D[5]	EN_DEVICE	1	R/W	Software Enable Device 0 = Disable. All registers values are still kept. 1 = Re-enable the device with a new start-up without the t_{DELAY} period. (default)	REG_RST
D[4]	EN_FPWM	0	R/W	Enable FPWM Mode 0 = Device works in power-save mode at light loads. (default) 1 = Device works in forced PWM mode at light loads.	REG_RST
D[3]	EN_DIS	1	R/W	Enable Output Discharge 0 = Disable. 1 = Enable. (default) Set it for the next disable cycle (Software or Hardware).	REG_RST
D[2]	Reserved	0	R/W	Reserved	N/A
D[1:0]	VOL_RAMP[1:0]	00/11	R/W	Voltage Ramp Speed 00 = 10mV/μs (default) for SGM6030C 01 = 5mV/μs 10 = 1mV/μs 11 = 0.1mV/μs (default) for SGM6030A/D/E	REG_RST

REG0x05: Status Register (1) [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000	R	Reserved	N/A
D[4]	TSD_STAT	0	R	Thermal Shutdown Tripped 0 = No thermal shutdown event occurred during the last reading. (default) 1 = Thermal shutdown has been tripped since the last reading.	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2]	POWER_BAD_STAT	0	R	Power Bad 0 = No power bad event occurred since last reading. (default) 1 = Output voltage is or was below 0.95 × V_{OUT}.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

NOTE:

1. All bit values will not change until the device receives the reset or read instruction. Then, the status register is reset to its default values.

APPLICATION INFORMATION

Figure 12 and Figure 13 below show the typical schematics with different external components.

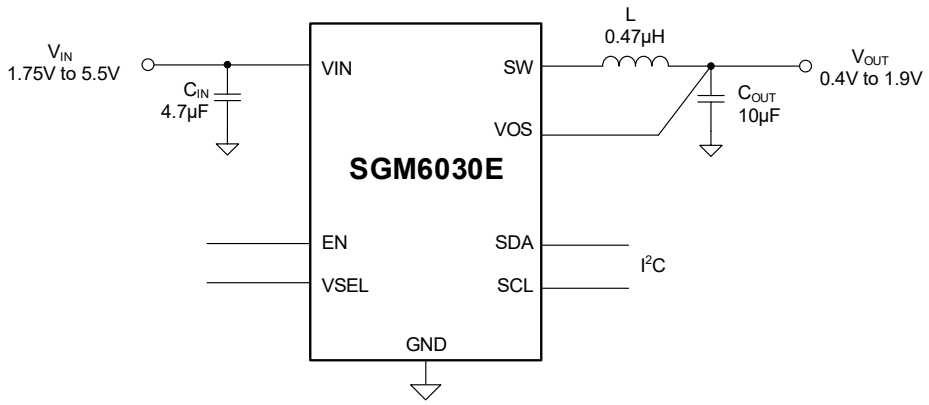


Figure 12. Typical Application for SGM6030E

Table 3. Components for Application Characteristic Curves

Reference	Description	Value	Size (L × W × T, mm³)	Manufacturer
SGM6030E	Buck Converter, 1A		1.4 × 0.70 × 0.4	SGMICRO
C_{IN}	Ceramic Capacitor, GRM155R60J475ME47D	4.7μF	0402 (1 × 0.5 × 0.6)	Murata
C_{OUT}	Ceramic Capacitor, GRM155R60J106ME15D	10μF	0402 (1 × 0.5 × 0.65)	Murata
L	Inductor DFE18SANR47MG0L	0.47μH	0603 (1.6 × 0.8 × 1.0)	Murata

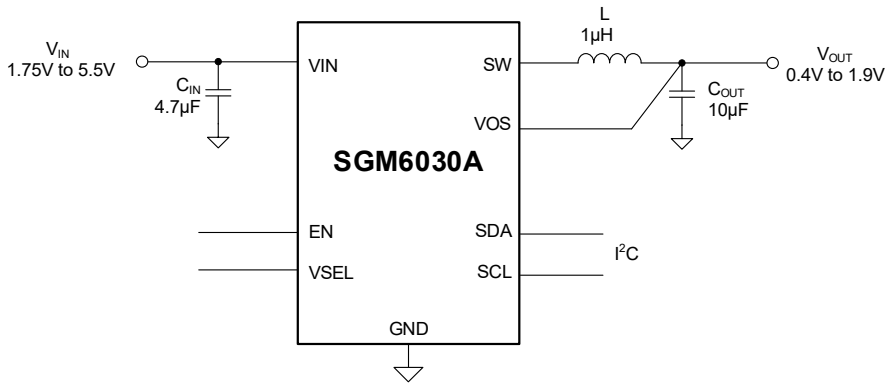


Figure 13. Typical Application for SGM6030A

Table 4. Components for Application Characteristic Curves

Reference	Description	Value	Size (L × W × T, mm³)	Manufacturer
SGM6030A	Buck Converter, 0.6A		1.4 × 0.70 × 0.4	SGMICRO
C_{IN}	Ceramic Capacitor, GRM155R60J475ME47D	4.7μF	0402 (1 × 0.5 × 0.6)	Murata
C_{OUT}	Ceramic Capacitor, GRM155R60J106ME15D	10μF	0402 (1 × 0.5 × 0.65)	Murata
L	Inductor DFE201610E	1μH	0805 (2.0 × 1.6 × 1.0)	Murata

APPLICATION INFORMATION (continued)

Layout Guidelines

It is easy to optimize PCB layout due to the SGM6030 pinout.

It is important to place low-impedance traces for main current loop.

Designer must reduce CIN-VIN-GND loop. In this way, put the C_{IN} close to VIN-GND of SGM6030.

VOS pin is internally connected to the feedback loop. Therefore, the VOS trace must be placed far away from SW node.

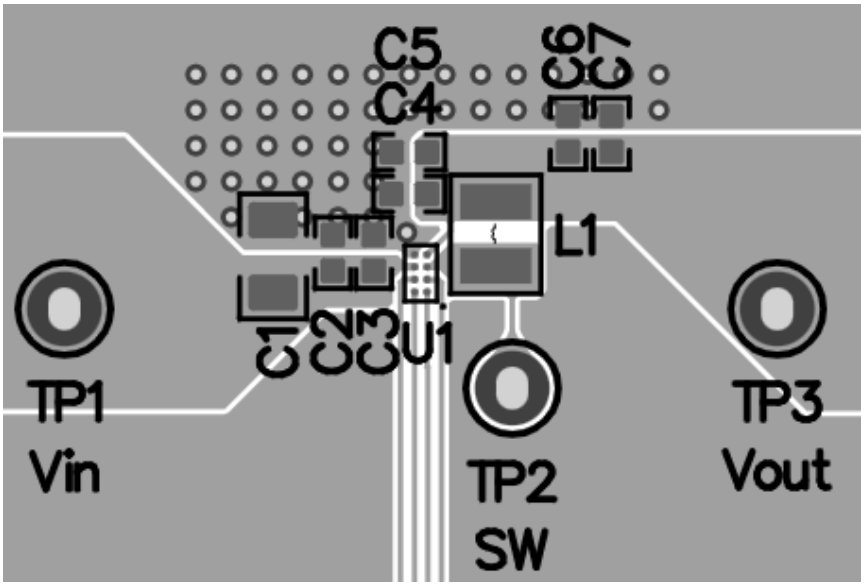


Figure 14. PCB Layout

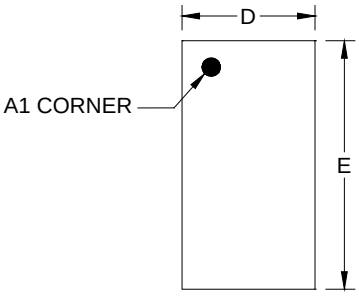
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

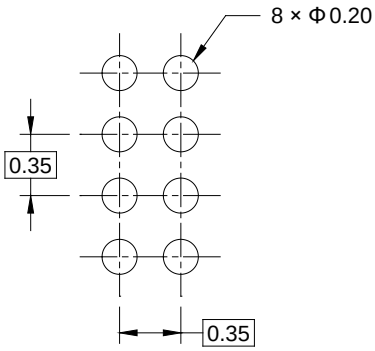
Changes from Original to REV.A (JUNE 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

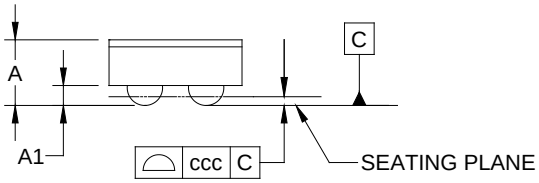
WLCSP-0.76×1.42-8B



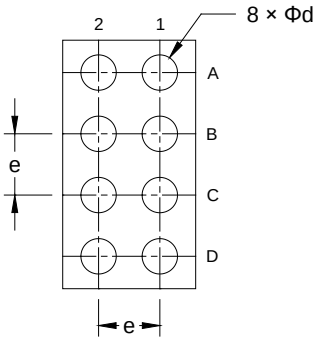
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



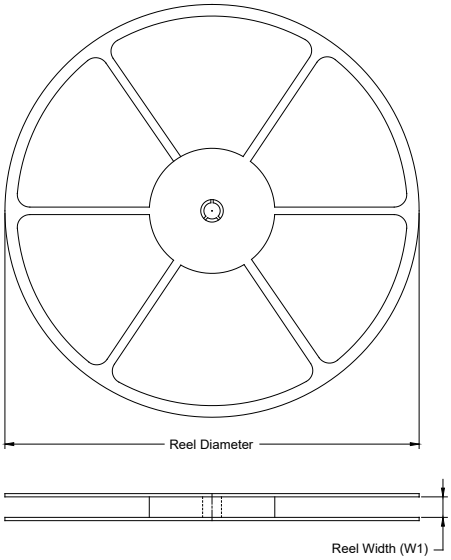
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.413
A1	0.094	-	0.134
D	0.726	-	0.786
E	1.385	-	1.445
d	0.172	-	0.232
e	0.350 BSC		
ccc	0.050		

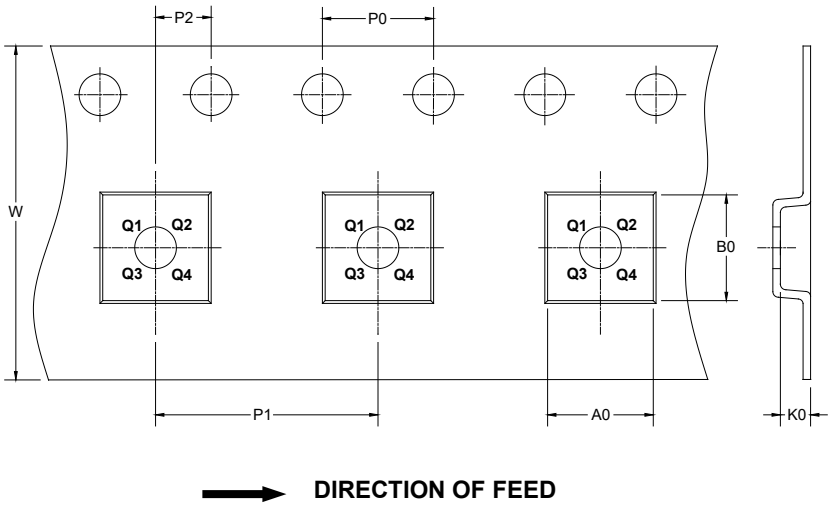
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



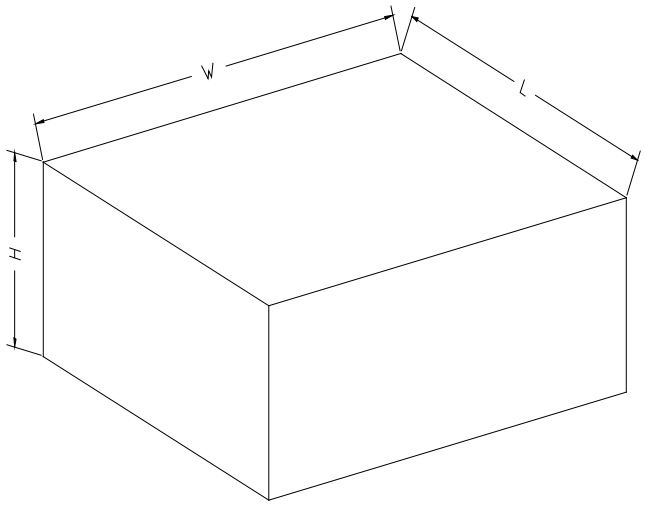
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.76×1.42-8B	7"	9.5	0.84	1.57	0.47	4.0	2.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002