SGM41543/SGM41543D
High Input Voltage, 3.78A Single-Cell Battery Charger with NVDC Power Path Management

FEATURES

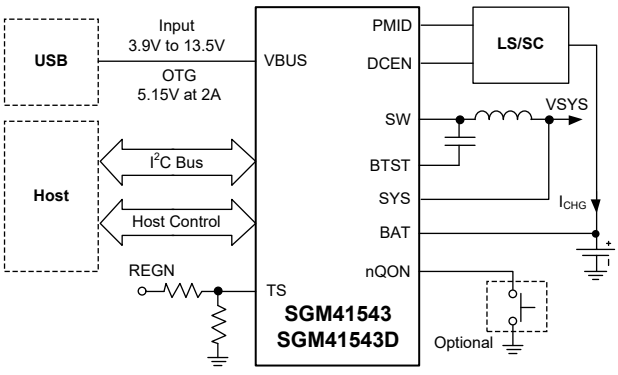
- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 94% Charge Efficiency at 1A from 5V Input
  - 91% Charge Efficiency at 2A from 9V Input
  - Optimized for USB Voltage Input (5V)
  - Selectable PFM Mode for Light Load Efficiency
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 2A Output
  - Boost Efficiency of 94.8% at 0.5A and 94.5% at 1A
  - Accurate Hiccup Mode Over-Current Protection
  - Output Short Circuit Protection
  - Selectable PFM Mode for Light Load Operations
- Single Input for USB or High Voltage Adaptors
  - 3.9V to 13.5V Operating Input Voltage Range
  - 22V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit and Dynamic Power Management (IINDPM, 100mA to 3.1A with 100mA Resolution & 3.8A) to Support USB 2.0 and USB 3.0 Standards and High Voltage Adaptors
  - Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM) with Selectable Offset
  - VINDPM Tracking of Battery Voltage
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- High Battery Discharge Efficiency with 16mΩ Switch
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
- Flexible Autonomous and I^2C Operation Modes for Optimal System Performance
- Fully Integrated Switches, Current Sense and Compensation
- External Direct Charging Path Enable Output
- 8μA Ship Mode Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation (8mV/Step)
  - ±5% Charge Current Regulation at 1.5A
  - ±10% Input Current Regulation at 0.9A
- Safety
  - Battery Temperature Sensing (Charge/Boost Modes)
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

APPLICATIONS

Smart Phones, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41543/SGM41543D are battery chargers and system power path management devices with integrated converter and power switches for using with single-cell Li-Ion or Li-polymer batteries. This highly integrated 3.78A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. I^2C programming makes it a very flexible powering and charger design solution.

The devices include four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for Buck or Boost mode (HSFET, Q2), low-side switching FET for Buck or Boost mode (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

A wide range of input sources are supported, including standard USB hosts, charging ports and USB compliant high voltage adaptors. The default input current limit is automatically selected based on the built-in USB interface. This limit is determined by the detection circuit in the system (e.g. USB PHY). SGM41543/SGM41543D are USB 2.0 and USB 3.0 power specifications compliant with input current and voltage regulation. It also meets USB On-The-Go (OTG) power rating specification and is capable of boosting the battery voltage to supply 5.15V on VBUS with 2A (or 1.2A) current limit.

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.5V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the three phases of charging cycle: pre-conditioning, constant current or constant voltage. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger begins another charging cycle.

Several safety features are provided in the SGM41543/ SGM41543D such as over-voltage and over-current protections, battery temperature monitoring, charging safety timing, thermal shutdown and input UVLO. TS pin is connected to an NTC thermistor for battery temperature monitoring and protection in both charge and Boost modes according to JEITA profile. This device also features thermal regulation in which the charge current is reduced, if the junction temperature exceeds 80℃ or 120℃ (selectable).

Charging status is reported by the STAT output and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

The devices supply a DCEN signal to control an external P-MOSFET or load switch as a direct charging path for low voltage PMID, or to control a 2:1 switching capacitor divider for high voltage PMID.

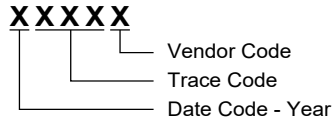
The SGM41543/SGM41543D are available in a Green TQFN-4×4-24L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41543	TQFN-4×4-24L	-40℃ to +85℃	SGM41543YTQF24G/TR	SGM41543 YTQF24 XXXXX	Tape and Reel, 3000
SGM41543D	TQFN-4×4-24L	-40℃ to +85℃	SGM41543DYTQF24G/TR	SGMMCC YTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VAC, VBUS (Converter Not Switching) ..... -2V to 22V (1)
- BTST, PMID (Converter Not Switching) ..... -0.3V to 22V
- SW ..... -2V to 16V
- SW (Peak for 10ns Duration) ..... -3V to 16V
- BTST to SW ..... -0.3V to 6V
- D+, D- ..... -0.3V to 6V
- REGN, TS, nCE, BAT, SYS (Converter Not Switching) ..... -0.3V to 6V
- SDA, SCL, nINT, nQON, STAT, DCEN ..... -0.3V to 6V

Output Sink Current
- STAT 6mA
- nINT 6mA

Package Thermal Resistance
- TQFN-4×4-24L, θ_{JA} ..... 35℃/W
- TQFN-4×4-24L, θ_{JB} ..... 10℃/W
- TQFN-4×4-24L, θ_{JC} ..... 16℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

NOTE: 1. Maximum 28V for 10 seconds.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 13.5V
Input Current (VBUS), I_{IN} ..... 3.8A (MAX)
Output DC Current (SW), I_{SWOP} ..... 5A (MAX)
Battery Voltage, V_{BATOP} ..... 4.624V (MAX)
Fast Charging Current, I_{CHGOP} ..... 3.78A (MAX)
Discharging Current (Continuous), I_{BATOP} ..... 6A (MAX)
Ambient Temperature Range ..... -40℃ to +85℃
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

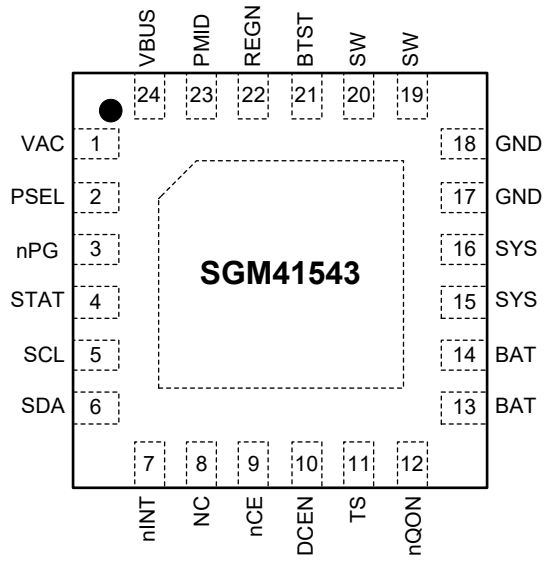
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

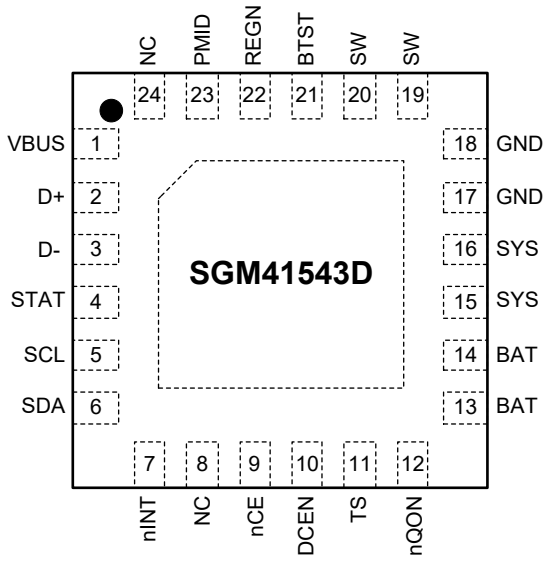
PIN CONFIGURATIONS

SGM41543 (TOP VIEW)



TQFN-4×4-24L

SGM41543D (TOP VIEW)



TQFN-4×4-24L

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
SGM 41543	SGM 41543D			
1	—	VAC	AI	Sense Input for DC Input Voltage (Typically from an AC/DC Adaptor). It must be connected to VBUS pin. (SGM41543 only)
2	—	PSEL	DI	Power Source Selection Input. If PSEL is pulled high, the input current limit is set to 500mA (USB 2.0) and if it is pulled low, the limit is set to 2.4A (adaptor). When the I^2C link to the host is established, the host can program a different input current limit value by writing to the IINDPM[4:0] register. (SGM41543 only)
—	2	D+	AIO	Positive USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DP_VSET[1:0]. (SGM41543D only)
3	—	nPG	DO	Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input (V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, V_{VBUS} is above sleep mode threshold, and V_{VBUS} > $V_{VBUSMIN}$ when I_{BAD_SRC} = 25mA). (SGM41543 only)
—	3	D-	AIO	Negative USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DM_VSET[1:0]. (SGM41543D only)
4	4	STAT	DO	Open-Drain Charge Status Output. Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charger in sleep mode: high (LED OFF). Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS). The function can be disabled via EN_ICHG_MON[1:0] register.
5	5	SCL	DI	I^2C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
6	6	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail.
7	7	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
8	8, 24	NC	—	Do Not Connect and Leave This Pin Floating.

PIN DESCRIPTION (continued)

PIN		NAME	TYPE (1)	FUNCTION
SGM 41543	SGM 41543D			
9	9	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low.
10	10	DCEN	—	External Direct Charge Enable Pin. This pin can be set high to enable an external direct charging device.
11	11	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC or TS pin function is not needed, use a 10kΩ/10kΩ pair for the resistor divider.
12	12	nQON	DI	BATFET On/Off Control Input. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn BATFET on, a logic low pulse with a duration of $t_{SHIPMODE}$ (1s TYP) can be applied to nQON. When VBUS source is not connected, a logic low pulse with a duration of t_{QON_RST} (10s TYP) resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (320ms TYP) and then goes back to provide a full power reset for system.
13, 14	13, 14	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
15, 16	15, 16	SYS	P	Connection Point to Converter Output. SYS is connected to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect a 20μF capacitor between SYS pin and GND close to the device.
17, 18	17, 18	GND	—	Ground Pin of the Device.
19, 20	19, 20	SW	P	Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
21	21	BTST	P	High-side Driver Positive Supply. It is internally connected to the boost-strap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
22	22	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Place a 4.7μF (10V rating) ceramic capacitor between REGN pin and GND. It is recommended to place the capacitor close to the REGN pin.
23	23	PMID	P	PMID Pin. PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 22μF ceramic capacitor from PMID pin to GND. It is the proper point for decoupling of high frequency switching currents.
24	1	VBUS	P	Charger Input (V_{IN}). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device. For SGM41543, this pin senses the input voltage.
Exposed Pad	Exposed Pad	—	P	Thermal Pad and Ground Reference. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie it externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE:
1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Currents						
Battery Discharge Current (BAT, SW, SYS) in Buck Mode	I_{BQ_VBUS}	V_{BAT} = 4.5V, V_{VBUS} < V_{VBUS_UVLOZ}, leakage between BAT and VBUS, BATFET off		0.1	1	μA
Battery Discharge Current (BAT) in Buck Mode	$I_{BQ\_HIZ\_BOFF}$	V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 1 or no VBUS, I^2C disabled, BATFET disabled		8	20	μA
Battery Discharge Current (BAT, SW, SYS)	$I_{BQ\_HIZ\_BON}$	V_{BAT} = 4.5V, HIZ mode and BATFET_DIS = 0 or no VBUS, I^2C disabled, BATFET enabled		15	30	μA
Input Supply Current (VBUS) in Buck Mode	I_{VBUS_HIZ}	V_{VBUS} = 5V, HIZ mode and BATFET_DIS = 1, no battery		25	40	μA
		V_{VBUS} = 12V, HIZ mode and BATFET_DIS = 1, no battery		50	75	
	I_{VBUS}	V_{VBUS} = 12V, V_{VBUS} > V_{BAT}, converter not switching		2.8	3.5	mA
		V_{BAT} = 3.8V, I_{SYS} = 0A, V_{VBUS} > V_{BAT}, V_{VBUS} > V_{VBUS_UVLOZ}, converter switching, BATFET off		4		
Battery Discharge Current in Boost Mode	I_{BOOST}	V_{BAT} = 4.2V, I_{VBUS} = 0A, converter switching		3		mA
BAT Pin, VAC Pin and VBUS Pin Power-Up						
VBUS Operating Range	V_{VBUS_OP}	V_{VBUS} rising	3.9		13.5	V
VBUS UVLO to Have Active I^2C (with No Battery) Seen by Sense VAC Pin	V_{VBUS_UVLOZ}	V_{VBUS} rising, T_J = +25℃		3.2	3.5	V
I^2C Active Hysteresis	$V_{VBUS\_UVLOZ\_HYS}$	V_{VBUS} falling from above V_{VBUS_UVLOZ}		430		mV
V_{VBUS} Minimum (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT}$	V_{VBUS} rising, T_J = +25℃		3.5	3.75	V
V_{VBUS} Hysteresis (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT\_HYS}$	V_{VBUS} falling from above $V_{VBUS\_PRESENT}$		400		mV
Sleep Mode Falling Threshold	V_{SLEEP}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VBUS} falling, T_J = +25℃	20	80	225	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VBUS} rising, T_J = +25℃	150	250	430	mV
VBUS Over-Voltage Rising Threshold — 6.5V Setting	$V_{VBUS\_OV\_RISE}$	V_{VBUS} rising, OVP[1:0] = 01	6.25	6.5	6.75	V
VBUS Over-Voltage Rising Threshold — 10.5V Setting		OVP[1:0] = 10	10.2	10.5	10.8	
VBUS Over-Voltage Rising Threshold — 14V Setting		OVP[1:0] = 11	13.6	14	14.4	
VBUS Over-Voltage Hysteresis — 6.5V Setting	$V_{VBUS\_OV\_HYS}$	V_{VBUS} falling, OVP[1:0] = 01		110		mV
VBUS Over-Voltage Hysteresis — 10.5V Setting		OVP[1:0] = 10		250		
VBUS Over-Voltage Hysteresis — 14V Setting		OVP[1:0] = 11		300		
BAT Voltage to Have Active I^2C (No Source on VBUS)	V_{BAT_UVLOZ}	V_{BAT} rising	2.7			V
BAT Depletion Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	2.18	2.35	2.55	V
	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	2.43	2.65	2.84	
BAT Depletion Rising Hysteresis	$V_{BAT\_DPL\_HYS}$			300		mV
Bad Adaptor Detection Current (Internal Current Sink)	I_{BAD_SRC}	Sink current from VBUS to GND		25		mA
Bad Adaptor Detection (VBUS Voltage Drop) Falling Threshold	$V_{VBUSMIN\_FALL}$	V_{VBUS} falling	3.67	3.77	3.87	V
Bad Adaptor Detection (VBUS Voltage Drop) Hysteresis	$V_{VBUSMIN\_HYS}$			250		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Path Management							
System Regulation Voltage	V_{SYS}	V_{BAT} = 4.4V, V_{BAT} > V_{SYS_MIN}, BATFET_DIS = 1			V_{BAT} + 50mV		V
Minimum DC System Voltage Output	V_{SYS_MIN}	V_{BAT} < SYS_MIN[2:0] = 101 (3.5V), BATFET_DIS = 1		3.57	3.65		V
Maximum DC System Voltage Output	V_{SYS_MAX}	V_{BAT} ≤ 4.4V, V_{BAT} > V_{SYS_MIN} = 3.5V, BATFET_DIS = 1		4.4	4.45	4.5	V
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_RBFET}				24		mΩ
Top Switching MOSFET On-Resistance between PMID and SW - Q2	R_{ON_HSFET}	V_{REGN} = 5V			22		mΩ
Bottom Switching MOSFET On-Resistance between SW and GND - Q3	R_{ON_LSFET}	V_{REGN} = 5V			27		mΩ
BATFET Forward Voltage in Supplement Mode	V_{FWD}				30		mV
Battery Charger							
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$			3.856		4.624	V
Charge Voltage Step	$V_{BAT\_REG\_STEP}$				32		mV
Charge Voltage Setting	V_{BAT_REG}	VREG[4:0] = 01011 (4.208V)	T_J = +25℃	4.192	4.208	4.224	V
			T_J = -40℃ to +85℃	4.186		4.23	
		VREG[4:0] = 01111 (4.352V)	T_J = +25℃	4.333	4.350	4.367	
			T_J = -40℃ to +85℃	4.325		4.375	
		VREG[4:0] = 10001 (4.400V)	T_J = +25℃	4.381	4.398	4.415	
			T_J = -40℃ to +85℃	4.372		4.424	
Charge Voltage Setting Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.208V or V_{BAT_REG} = 4.352V or V_{BAT_REG} = 4.400V	T_J = +25℃	-0.4		0.4	%
			T_J = -40℃ to +85℃	-0.6		0.6	
Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$			0		3780	mA
Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$				60		mA
Charge Current Regulation Setting	I_{CHG_REG}	V_{BAT} =3.1V, T_J = +25℃	I_{CHG} = 60mA	0.05	0.065	0.08	A
			I_{CHG} = 240mA	0.21	0.24	0.27	
			I_{CHG} = 720mA	0.67	0.72	0.77	
			I_{CHG} = 1.38A	1.32	1.38	1.44	
			I_{CHG} = 2.04A	1.97	2.04	2.11	
		V_{BAT} = 3.8V, T_J = +25℃	I_{CHG} = 60mA	0.05	0.06	0.07	
			I_{CHG} = 240mA	0.225	0.24	0.255	
			I_{CHG} = 720mA	0.69	0.72	0.75	
			I_{CHG} = 1.38A	1.33	1.38	1.43	
			I_{CHG} = 2.04A	1.97	2.04	2.11	
Pre-Charge Current Regulation Setting	I_{PRECHG}	IPRECHG[3:0] = 0010 (180mA), T_J = +25℃		155	180	205	mA
Battery LOW Falling Threshold	V_{BATLOW_FALL}	I_{CHG} = 480mA		2.67	2.84	3	V
Battery LOW Rising Threshold	V_{BATLOW_RISE}	Change from pre-charge to fast charging		3.06	3.14	3.22	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
Termination Current Regulation Setting	I_{TERM}	V_{BAT_REG} = 4.208V, ITERM[3:0] = 0010 (180mA), T_J = +25℃	I_{CHG} > 1.26A	150	180	210	mA
			I_{CHG} ≤ 1.26A	165	180	195	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling, T_J = +25℃		1.75	1.9	2.05	V
	V_{SHORTZ}	V_{BAT} rising, T_J = +25℃		2.1	2.2	2.3	
Battery Short Current	I_{SHORT}	V_{BAT} < V_{SHORTZ}			100		mA
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling	VRECHG = 0 (100mV)	80	110	145	mV
			VRECHG = 1 (200mV)	185	220	260	
System Discharge Load Current	I_{SYS_LOAD}	V_{SYS} = 4.2V			27		mA
BATFET MOSFET On-Resistance	R_{ON_BATFET}	V_{BAT} = 4.2V, measured from BAT pin to SYS pin, T_J = +25℃			16	22	mΩ
Input Voltage and Current Regulation (DPM: Dynamic Power Management)							
Input Voltage Regulation Limit	V_{INDPM}	VINDPM[3:0] = 0101	VINDPM_OS[1:0] = 00 (4.4V)	4.35	4.4	4.45	V
			VINDPM_OS[1:0] = 01 (6.4V)	6.32	6.4	6.48	
			VINDPM_OS[1:0] = 10 (8V)	7.9	8	8.1	
			VINDPM_OS[1:0] = 11 (11V)	10.83	11	11.13	
Input Voltage Regulation Accuracy	V_{INDPM_ACC}			-2.0		2.0	%
Input Voltage Regulation Limit Tracking VBAT	V_{DPM_VBAT}	V_{BAT} = 4V, V_{INDPM} = 3.9V, T_J = +25℃, VDPM_BAT_TRACK[1:0] = 11 (300mV)		4.22	4.33	4.44	V
Input Voltage Regulation Accuracy Tracking VBAT	$V_{DPM\_VBAT\_ACC}$	T_J = +25℃		-3		3	%
USB Input Current Regulation Limit	I_{INDPM}	V_{VBUS} = 5V, T_J = +25℃, current pulled from SW	IINDPM[4:0] = 00100 (500mA)	410		530	mA
			IINDPM[4:0] = 01000 (900mA)	790		910	
			IINDPM[4:0] = 01110 (1.5A)	1360		1480	
			IINDPM[4:0] = 10011 (2A)	1830		1970	
Input Current Limit during System Start-Up Sequence	I_{IN_START}				200		mA
BAT Pin Over-Voltage Protection							
Battery Over-Voltage Threshold	V_{BATOVP_RISE}	As percentage of V_{BAT_REG}, T_J = +25℃	V_{BAT} rising	102.3	103.9	105	%
	V_{BATOVP_FALL}		V_{BAT} falling	100.3	101.9	103	
Thermal Regulation and Thermal Shutdown							
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	Temperature increasing	TREG = 1 (120℃)		120		℃
			TREG = 0 (80℃)		80		
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing			150		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}				30		℃

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JEITA Thermistor Comparator (Buck Mode)							
T1 (0℃) Threshold Voltage on TS Pin	V_{T1}	Charge suspends if temperature T is below T1 (T < T1), as percentage of V_{REGN}		72.8	73.3	73.8	%
V_{T1} Falling		As percentage of V_{REGN}		71.2	71.7	72.2	
T2 (10℃) Threshold Voltage on TS Pin	V_{T2}	Charge sets to I_{CHG}/2 and the lower of 4.1V and V_{REG} if T1 < T < T2, as percentage of V_{REGN}		67.5	68	68.5	%
V_{T2} Falling		As percentage of V_{REGN}		66.3	66.8	67.3	
V_{T3} Rising	V_{T3}	As percentage of V_{REGN}		45.4	45.9	46.4	%
T3 (45℃) Threshold Voltage on TS Pin		Charge sets to the lower of 4.1V and V_{REG} if T3 < T < T4, as percentage of V_{REGN}		44	44.5	45	
V_{T4} Rising	V_{T4}	As percentage of V_{REGN}		34.9	35.4	36	%
T4 (60℃) Threshold Voltage on TS Pin		Charge suspends if T > T4, as percentage of V_{REGN}		33.5	34	34.6	
Cold or Hot Thermistor Comparator (Boost Mode)							
Cold Temperature Threshold (TS Pin Voltage Rising Threshold)	V_{BCOLD}	As percentage of V_{REGN} (approx. -10℃ w/ 103AT)		79.6	80.1	80.6	%
TS Voltage Falling (Exit Cold Range)		As percentage of V_{REGN}		78.6	79.1	79.6	
Cold or Hot Thermistor Comparator (Boost Mode)							
Hot Temperature Threshold (TS Pin Voltage Falling Threshold)	V_{BHOT}	As percentage of V_{REGN} (approx. 60℃ w/ 103AT)		30.5	31	31.7	%
TS Voltage Rising (Exit Hot Range)		As percentage of V_{REGN}		33.9	34.4	35	
Charge Over-Current Comparator (Cycle-by-Cycle)							
HSFET Cycle-by-Cycle Over-Current Threshold	I_{HSFET_OCP}	T_J = +25℃		6.8		10.1	A
System Overload Threshold	I_{BATFET_OCP}	T_J = +25℃		7.7			A
Charge Under-Current Comparator (Cycle-by-Cycle)							
LSFET Under-Current Falling Threshold	I_{LSFET_UCP}	Change rectifier from synchronous mode to non-synchronous mode			200		mA
PWM							
PWM Switching Frequency	f_{SW}	Oscillator frequency, T_J = +25℃	Buck mode	1380	1500	1620	kHz
			Boost mode	1380	1500	1620	
Maximum PWM Duty Cycle (1)	D_{MAX}				99		%
Boost Mode Operation							
Boost Mode Regulation Voltage	V_{OTG_REG}	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[1:0] = 10 (5.15V)		5	5.13	5.26	V
Boost Mode Regulation Voltage Accuracy	$V_{OTG\_REG\_ACC}$	V_{BAT} = 3.8V, I_{PMID} = 0A, BOOSTV[1:0] = 10 (5.15V)		-3		3	%
Exit Boost Mode due to Low Battery Voltage	V_{BATLOW_OTG}	V_{BAT} falling, MIN_BAT_SEL = 0		2.9	3	3.1	V
		V_{BAT} rising, MIN_BAT_SEL = 0		3.1	3.25	3.4	
		V_{BAT} falling, MIN_BAT_SEL = 1		2.48	2.57	2.66	
		V_{BAT} rising, MIN_BAT_SEL = 1		2.68	2.85	3.02	
OTG Mode Maximum Output Current	I_{OTG}	T_J = +25℃	BOOST_LIM = 0 (1.2A)	1.33	1.5	1.68	A
			BOOST_LIM = 1 (2A)	2.15	2.5	2.88	
OTG Over-Voltage Threshold	V_{OTG_OVP}	Rising threshold		5.85	6	6.22	V
HSFET Under-Current Falling Threshold	I_{OTG_HSZCP}	Change rectifier from synchronous mode to non-synchronous mode			150		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGN LDO							
REGN LDO Output Voltage		V_{REGN}	V_{VBUS} = 9V, I_{REGN} = 40mA	4.04	4.45	4.89	V
			V_{VBUS} = 5V, I_{REGN} = 20mA	4.72	4.85	4.96	
Logic I/O Pin Characteristics (nCE, PSEL, DCEN, SCL and SDA)							
Input Low Threshold	nCE	V_{IL}				0.4	V
Input High Threshold		V_{IH}		1.3			V
Input Low Threshold	PSEL, SCL, SDA	V_{IL}				0.4	V
Input High Threshold		V_{IH}		1.3			V
High-Level Leakage Current		I_{BIAS}	Pull up rail 1.8V, T_J = +25℃		0.1	1	μA
Output Low Threshold	DCEN	V_{OL}			0.1		V
Output High Threshold		V_{OH}			REGN		V
Logic I/O Pin Characteristics (nPG, STAT and nINT) – Open-Drain							
Low-Level Output Voltage		V_{OL}	Sink current 5mA			0.2	V

NOTE:
1. Guaranteed by design. Not production tested.

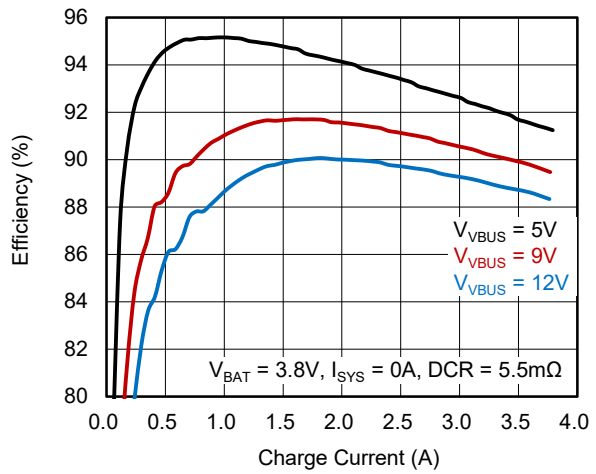
TIMING REQUIREMENTS

(T_J = +25℃, unless otherwise noted.)

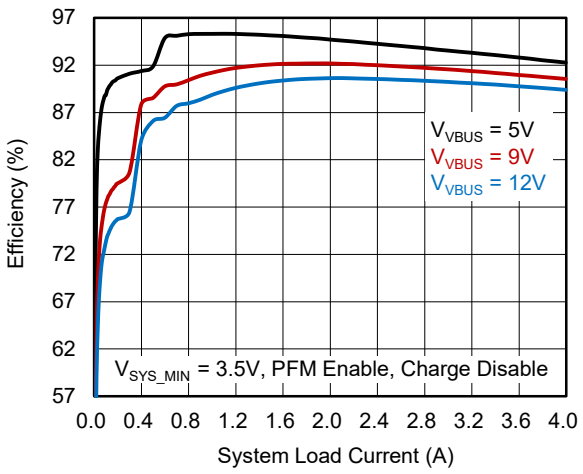
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up						
VBUS OVP Reaction Time	t_{ACOV}	V_{VBUS} rising above ACOV threshold to turn off Q2		0.1		μs
Wait Window for Bad Adaptor Detection	t_{BAD_SRC}			30		ms
Battery Charger						
Deglitch Time for Charge Termination	t_{TERM_DGL}			230		ms
Deglitch Time for Recharge	t_{RECHG_DGL}			230		ms
System Over-Current Deglitch Time to Turn off Q4	$t_{SYSOVLD\_DGL}$			112		μs
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}			1		μs
	t_{BATOVP_DCEN}	DCEN active	2.8	3.5	4.4	ms
Typical Charge Safety Timer Range	t_{SAFETY}	CHG_TIMER = 1	14.5	16	18	h
Typical Top-Off Timer Range	t_{TOP_OFF}	TOPOFF_TIMER[1:0] = 10 (35min)	31	35	39	min
nQON Timing and Ship Mode Timing						
nQON Negative Pulse Low Pulse Width to Turn on BATFET and Exit Ship Mode	$t_{SHIPMODE}$		0.9	1	1.2	s
nQON Low Time to Reset BATFET	t_{QON_RST}		9	10	11.5	s
BATFET off Time during Full System Reset	t_{BATFET_RST}		285	320	355	ms
Wait Delay for Entering Ship Mode	t_{SM_DLY}		11	12.3	13.5	s
Digital Clock and Watchdog Timer						
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 01, REGN LDO disabled		40.9		s
Digital Clock Frequency in Low Power	f_{LPDIG}	REGN LDO disabled		31		kHz
Digital Clock Frequency	f_{DIG}	REGN LDO enabled		500		kHz
I^2C Interface						
SCL Clock Frequency	f_{SCL}			400		kHz

TYPICAL PERFORMANCE CHARACTERISTICS

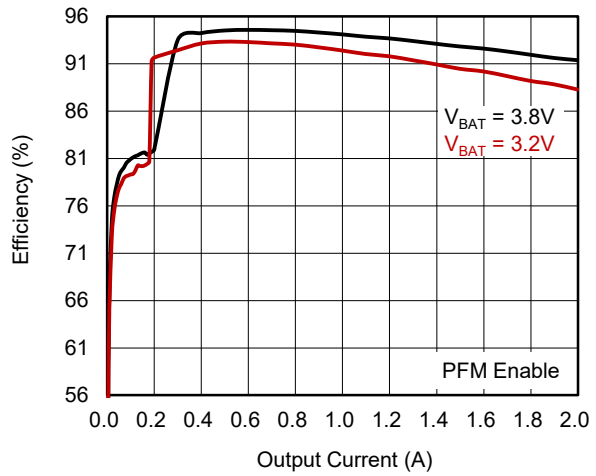
Charge Efficiency vs. Charge Current



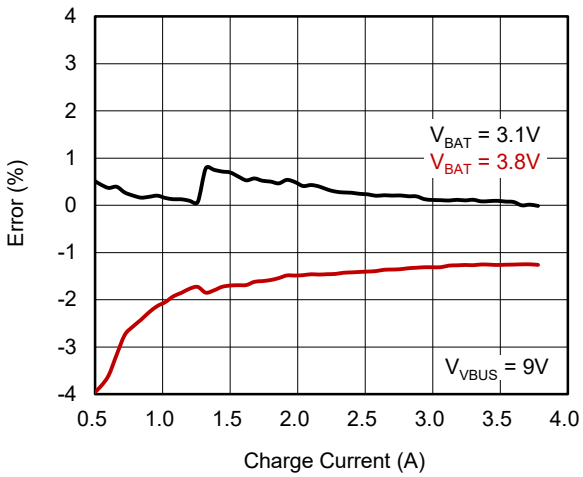
System Efficiency vs. System Load Current



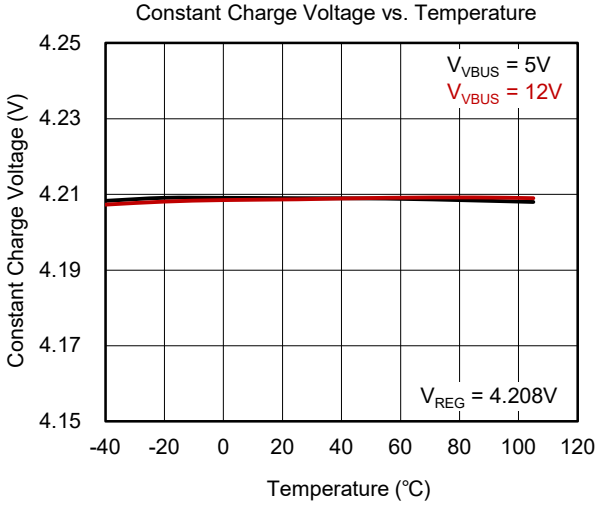
Boost Mode Efficiency vs. Output Current



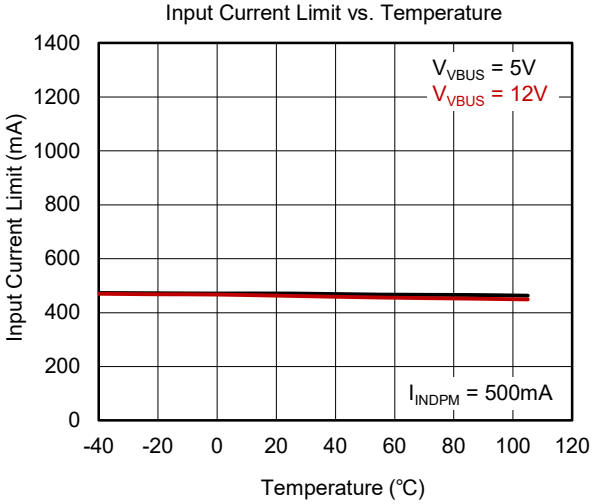
Charge Current Accuracy vs. Charge Current I²C Setting



Constant Charge Voltage vs. Temperature

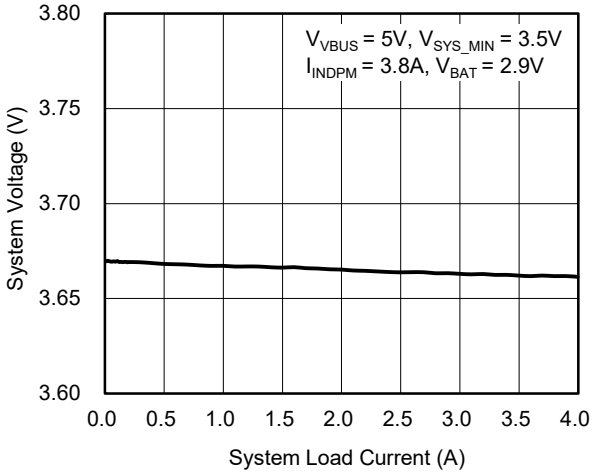


Input Current Limit vs. Temperature

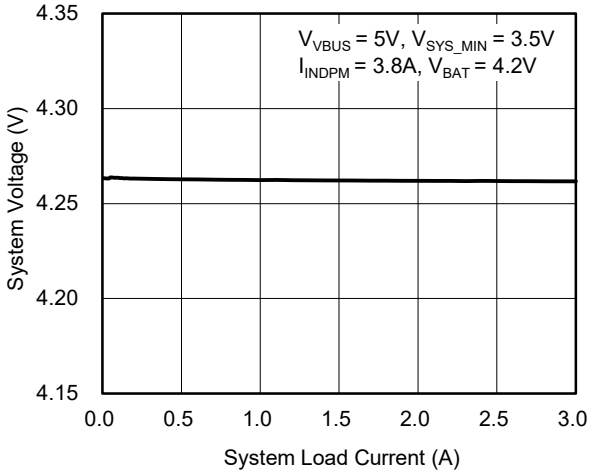


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

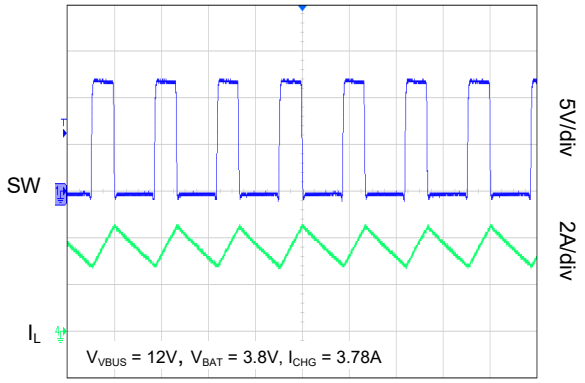
System Voltage vs. System Load Current



System Voltage vs. System Load Current

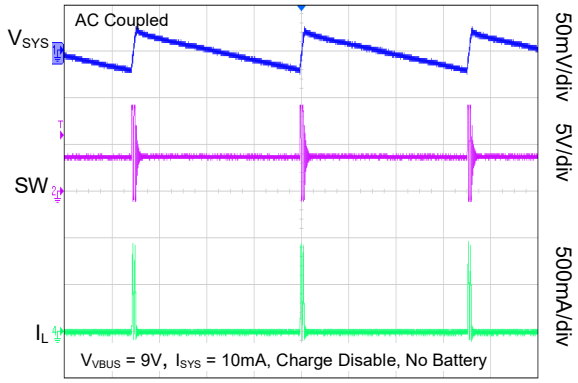


PWM Switching Waveform



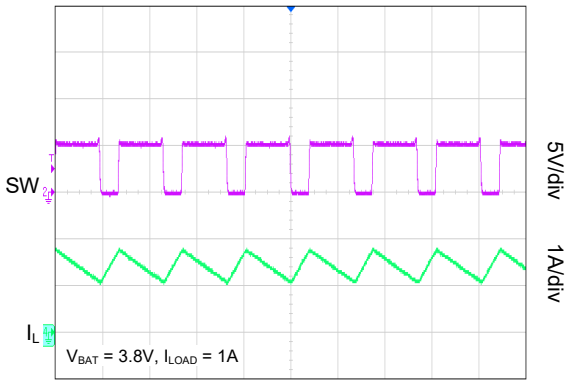
Time (500ns/div)

PFM Switching Waveform



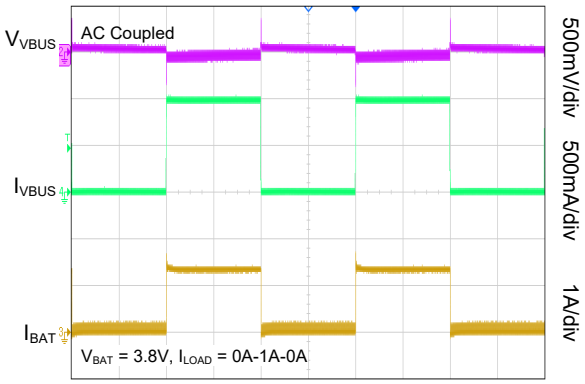
Time (10μs/div)

Boost Mode Switching Waveform



Time (500ns/div)

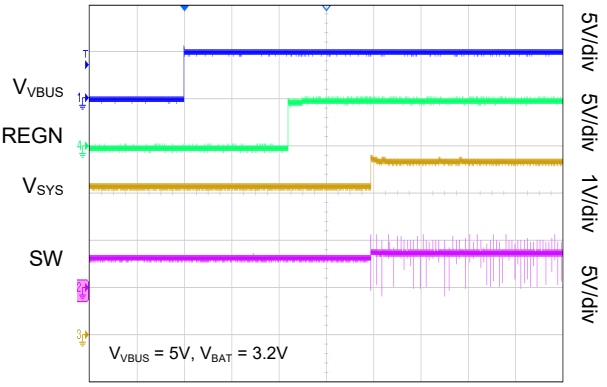
Boost Mode Load Transient



Time (5ms/div)

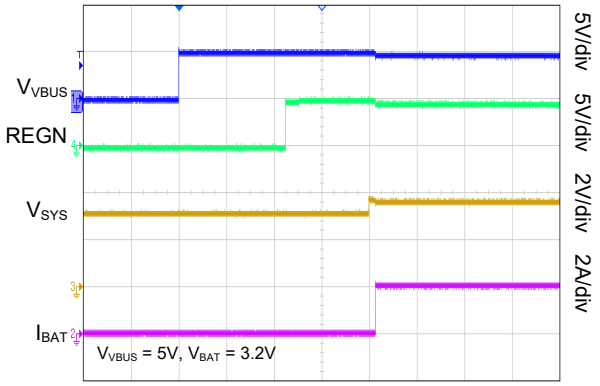
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power-Up with Charge Disable



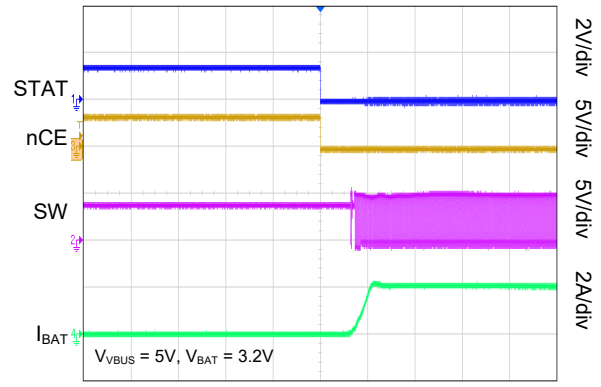
Time (100ms/div)

Power-Up with Charge Enable



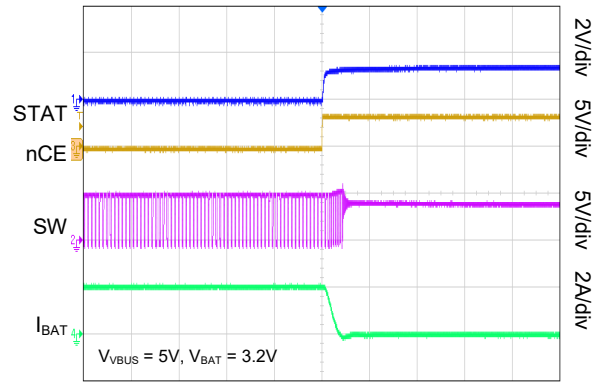
Time (100ms/div)

Charge Enable



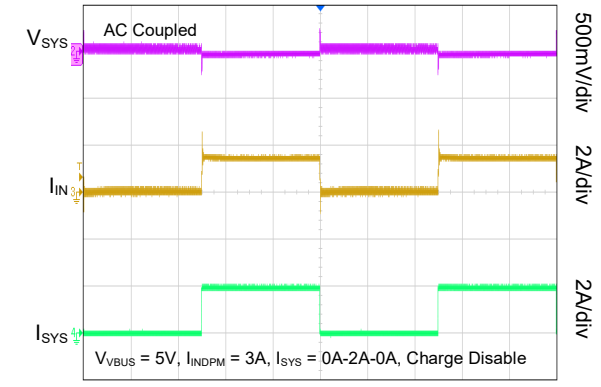
Time (50μs/div)

Charge Disable



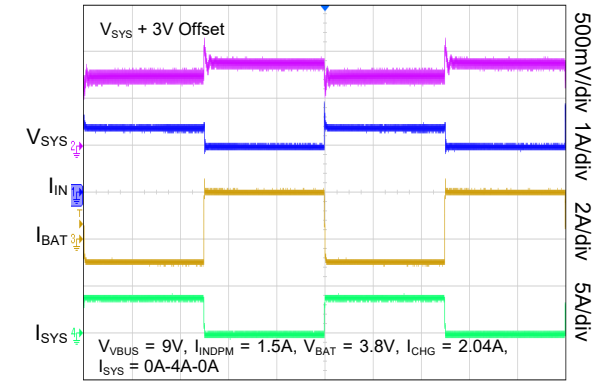
Time (10μs/div)

Input Current DPM Response without Battery



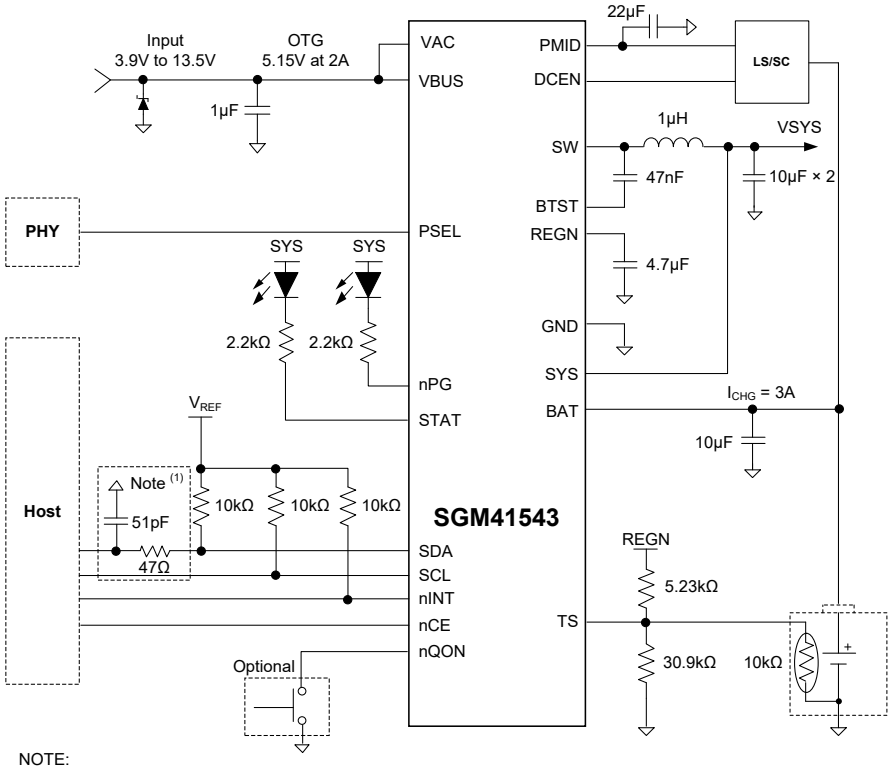
Time (2ms/div)

Load Transient during Supplement Mode



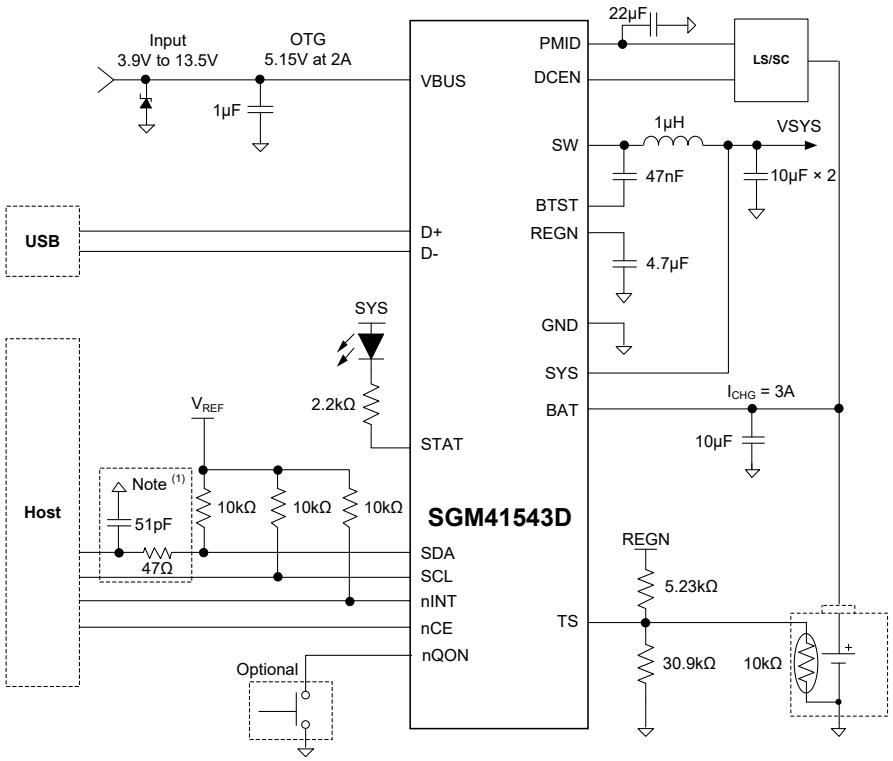
Time (2ms/div)

TYPICAL APPLICATION CIRCUITS



NOTE:
1. This section is recommended to be added.

Figure 1. SGM41543 Typical Application Circuit



NOTE:
1. This section is recommended to be added.

Figure 2. SGM41543D Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

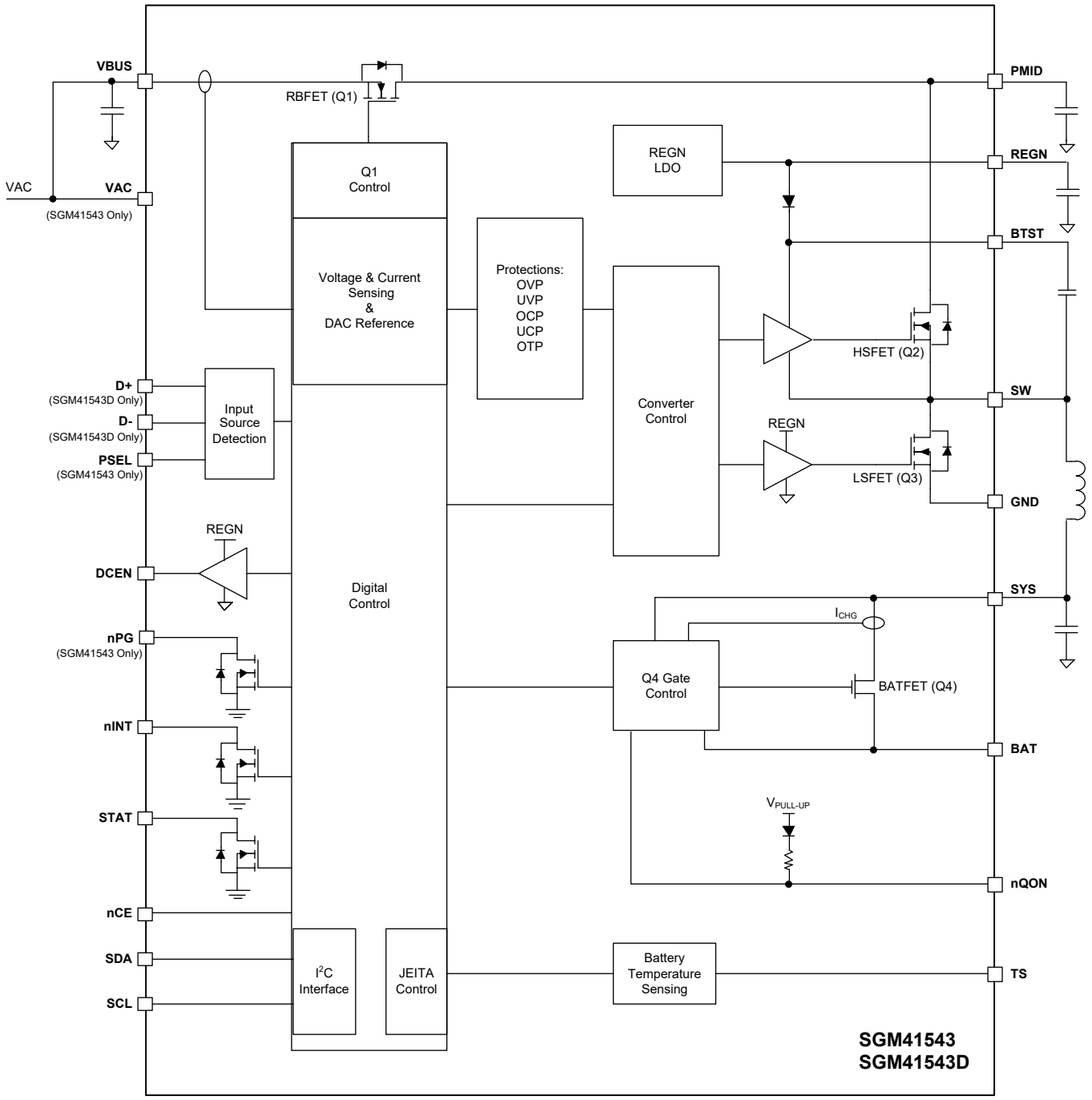


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM41543/SGM41543D are power management and charger devices for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The SGM41543/SGM41543D can accommodate a wide range of input sources including USB, wall adaptor and car chargers. It is optimized for 5V input (USB voltage) but is capable of operating with input voltages from 3.9V to 13.5V. It also supports JEITA profile for battery charging safety at high or low temperatures. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT) or both is another feature of the device. Battery charge current is programmable and can reach a maximum of 3.78A (charge). In the Boost mode, the battery voltage is boosted to power the VBUS pin (2A MAX) when it is a power receiving node (USB OTG) that is typically regulated to 5.15V.

The device may operate in several different modes:

In HIZ mode, the reverse blocking FET (Q1), internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it supplies DC power to the system through BATFET.

In the sleep mode, the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VBUS}) is not high enough for charging the battery. In other words, V_{VBUS} is smaller than V_{BAT} + V_{SLEEP} (where V_{SLEEP} is a small threshold) and Buck converter is not able to charge, even at its maximum duty cycle. The Boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VBUS} is almost equal to or smaller than V_{BAT}).

In supplement mode, the input source power is not enough to supply system demanded power and the battery assists by discharging to the system in parallel and providing the deficit.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I^2C interface will also be ready for communication and all registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time.

The discharge current through BATFET is continuously monitored. In the supplement mode, if a system overload (or short) occurs (I_{BAT} > I_{BATFET_OCP}), the BATFET is turned off immediately and BATFET_DIS bit is set to 1. The BATFET will not enable until the input source is applied or one of the BATFET Enable Mode (Exit Ship Mode) methods (explained later) is used to activate the BATFET.

Power-Up Process from the Input Power Source

Upon connection of an input source (VBUS), its voltage sensed from VAC pin (for SGM41543) or VBUS pin (for SGM41543D) is checked to turn on the internal REGN LDO regulator and the bias circuits (whether the battery is present or not). The input current limit is determined and set before the Buck converter is started. The sequences of actions when VBUS as input source is powered up are:

1. REGN LDO power-up.
2. Poor power source detection (qualification).
3. Input power source type detection. (Based on D+/D- or PSEL input. It is used to set the default input current limit (IINDPM[4:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The STAT pin can also be pulled up to REGN. The REGN enables when the following 2 conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

1. $V_{VBUS} > V_{VBUS\_PRESENT}$.
2. $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ (in Buck mode) or $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in Boost mode).

In HIZ state, the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is powered only by the battery in HIZ mode.

Poor Power Source Detection (Qualification)

When REGN LDO is powered, the input source (adaptor) is checked for its type and current capacity. To start the Buck converter, the input (VBUS) must meet the following conditions:

1. $V_{VBUS} < V_{VBUS\_OV}$.
2. $V_{VBUS} > V_{VBUSMIN\_RISE}$ during t_{BAD_SRC} test period (30ms TYP) in which the I_{BAD_SRC} (25mA TYP) current is pulled from VBUS.

If the test is failed, the conditions are repeatedly checked every two seconds. As soon as the input source passes qualification, the VBUS_GD bit in status register is set to 1 and a pulse is sent to the nINT pin to inform the host. Type detection will start as next step.

Input Power Source Type Detection

The input source detection will run through the D+/D- lines or the PSEL pin while REGN LDO is powered and after the VBUS_GD bit is set. The SGM41543D can detect the input source types, which include SDP/CDP/DCP and non-standard adaptor through the D+/D- pins following USB BC1.2 specification. The SGM41543 sets the input current limit through PSEL pin. A pulse is sent to nINT pin to inform the host when the input source type detection is completed. Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINDPM[4:0]) is changed to set current limit.
2. PG_STAT (power good) bit is set.
3. VBUS_STAT[2:0] register is updated to indicate USB or adaptor input source types.

The input current is always limited by the IINDPM[4:0] register and the limit can be updated by the host if needed.

Input Current Limit by PSEL (SGM41543)

PSEL pin interfaces with USB physical layer (PHY) for input current limit setting. The USB PHY device output is used to detect if the input is a USB host or a charging port. In the host-control mode, the host must enable IINDET_EN bit for reading the PSEL value and updating the IINDPM[4:0]. In the default mode, IINDPM[4:0] is updated automatically by PSEL value in real-time as given in Table 1.

Table 1. Input Current Limit Setting from PSEL

Input Detection	PSEL Pin	Input Current Limit (I_{LIM})	VBUS_STAT[2:0]
USB Host SDP	High	500mA	001
Adaptor	Low	2400mA	010

Input Current Limit by D+/D- Detection (SGM41543D)

The SGM41543D integrates a D+/D- based input source detection to set the input current limit when VBUS is plugged in. When input source is plugged in, the device starts USB BC1.2 detection and sets the SDP/CDP/DCP related input current limit. And if the data contact detection timer expires, the non-standard adaptor detection starts and then sets the input current limit. Please refer to Table 2 and Table 3.

Table 2. Non-Standard Adaptor Detection

Non-Standard Adaptor	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P7}	V_{D-} within V_{2P0}	2.1
Divider 2	V_{D+} within V_{1P2}	V_{D-} within V_{1P2}	2
Divider 3	V_{D+} within V_{2P0}	V_{D-} within V_{2P7}	1
Divider 4	V_{D+} within V_{2P7}	V_{D-} within V_{2P7}	2.4

DETAILED DESCRIPTION (continued)

Table 3. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (I_{INLIM})
USB SDP (USB500)	500mA
USB CDP	1.5A
USB DCP	2.4A
Divider 1	2.1A
Divider 2	2A
Divider 3	1A
Divider 4	2.4A
Unknown 5V Adaptor	500mA

Force Detection of Input Current Limit

The host can set IINDET_EN bit to 1 in host mode to force the device to run. And the IINDET_EN bit returns to 0 by itself and input result is updated after the detection is completed.

D+/D- Output Voltage Setting (SGM41543D)

The host can set D+/D- output voltages by DP_VSET[1:0] and DM_VSET[1:0] to HIZ, 0V, 0.6V or 3.3V. When BC1.2 detection runs, these bits are ignored.

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

A wide voltage range (3.9V to 5.4V, 5.9V to 9V, 10.5V to 12V) is supported for the input voltage limit setting in VINDPM[3:0] and VINDPM_OS[1:0]. 4.5V is the default for USB.

The device supports dynamic tracking of the battery voltage (VINDPM). VDPM_BAT_TRACK[1:0] bits can be used to enable tracking (00 to disable tracking) and set the tracking offset value. When the tracking is enabled, the input voltage limit will be set to the larger value between the VINDPM[3:0] and V_{BAT} + VDPM_BAT_TRACK[1:0]. The VDPM_BAT_TRACK[1:0] tracking offset can be set to 200mV, 250mV or 300mV. And this function only takes effect when VINDPM_OS[1:0] = 00.

DC/DC Converter Power-Up

The 1.5MHz switching converter composed of LSFET and HSFET is enabled, which can start switching when the input current limit is set. Converter is initiated with a soft-start when the system voltage is ramped up. If SYS voltage is less than 2.2V, the input current is limited to 200mA or IINDPM[4:0], depending on whichever is smaller, otherwise the limit is set to IINDPM[4:0].

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

When converter operates for battery charging, it acts as an efficient, fixed frequency synchronous Buck converter regardless of the input/output voltages and currents. However, it is capable of switching to PFM mode at light load when charging is disabled or when the detected battery voltage is less than minimum system voltage setting. PFM operation can be enabled or prevented in either Buck or Boost mode through using the PFM_DIS bit.

Boost Mode

The SGM41543/SGM41543D support USB On-The-Go. When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (Boost mode) with 1.5MHz switching frequency to supply power from the battery to that load. The 1.2A USB OTG output current limit requirement is achieved by programming, however, the Boost converter can deliver 2A to the output (default limit). Converter will be set to Boost mode if at least 30ms is passed from enabling this mode (OTG_CONFIG bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{BATLOW\_OTG}$.
2. $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in sleep mode).
3. Acceptable voltage range at TS pin ($V_{BHOT} < V_{TS} < V_{BCOLD}$).

The output voltage is set to V_{VBUS} = 5.15V and is maintained as long as V_{BAT} is above V_{BATLOW_OTG}. The output current can reach up to the programmed value by BOOST_LIM bit (2A or 1.2A). The VBUS_STAT[2:0] status register bits are set to 111 in Boost mode (OTG).

To minimize the output overshoot in Boost mode, the device starts with PFM first and then switches to PWM. As stated before, PFM can be avoided by using PFM_DIS bit in Buck and Boost modes.

DETAILED DESCRIPTION (continued)

Host Mode and Default Mode Operation with Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as if the watchdog timer is expired. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41543/SGM41543D operate like an autonomous charger. The battery is charged for 16 hours (default value for the fast charging safety timer). Then the charge stops while Buck converter continues to operate to power the system load. In this mode, WATCHDOG_FAULT bit is high.

Most of the flexibility features of the SGM41543/SGM41543D become available in the host mode when the device is controlled by a host with I^2C. By setting the WD_RST bit to 1, the charger mode changes from default mode to host mode. In this mode, the WATCHDOG_FAULT bit is low and all device parameters can be programmed by the host. To prevent the device watchdog from reset that results in going back to default mode, the host must disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_RST to prevent WATCHDOG_FAULT bit from being set. Every time a 1 is written to the WD_RST, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to their default values except for EN_ICHG_MON[1:0], IINDPM[4:0], PFM_DIS, SYS_MIN[2:0], MIN_BAT_SEL, Q1_FULLON, OVP[1:0], BOOSTV[1:0], VINDPM[3:0], VDPM_BAT_TRACK[1:0], BATFET_DIS, BATFET_DLY, VINDPM_INT_MASK, IINDPM_INT_MASK, REG_RST and VINDPM_OS[1:0] bits that keep their values unchanged.

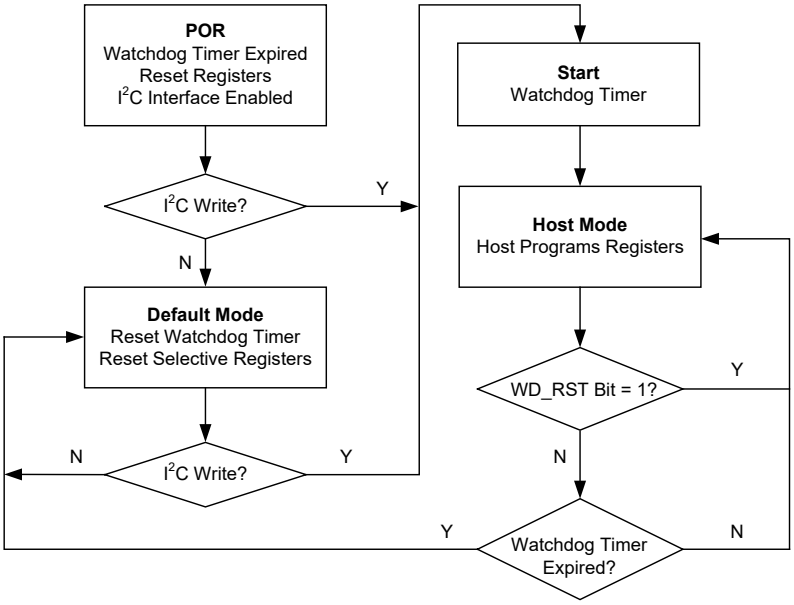


Figure 4. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41543/SGM41543D are designed for charging single-cell Li-Ion or Li-poly batteries with a charge current up to 3.78A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance (16mΩ) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if CHG_CONFIG = 1 and nCE pin is pulled low. In default mode, the SGM41543/SGM41543D run a charge cycle with the default parameters itemized in Table 4. At any moment, the host can control the charging operations by writing the registers.

Table 4. Charging Parameter Default Setting

Default Mode	SGM41543/SGM41543D
Charging Voltage (V_{REG})	4.208V
Charging Current (I_{CHG})	2.04A
Pre-Charge Current (I_{PRECHG})	180mA
Termination Current (I_{TERM})	180mA
Temperature Profile	JEITA
Safety Timer	16h

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

- NTC temperature fault is not asserted (TS pin).
- Safety timer fault is not asserted.
- BATFET is not forced off. (BATFET_DIS bit = 0).
- Charging enabled (3 conditions: CHG_CONFIG bit = 1, ICHG[5:0] register is not 0mA and nCE pin is low).
- Battery voltage is below the programmed full charge level (V_{REG}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{REG} - 100mV or V_{REG} - 200mV configured by VRECHG bit). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the nCE pin or CHG_CONFIG bit.

Normally a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode.

Charge Status Report

STAT is an open-drain output pin that reports the status of charge and can drive an LED for indication: a low indicates that charging is in progress, a high shows that charging is completed or disabled and alternating low/high (blinking) show a charging fault. The STAT may be disabled (keep the open-drain switch off) by setting EN_ICHG_MON[1:0] = 10 or 11.

The CHRG_STAT[1:0] status register reports the present charging phase and status by two bits: 00 = charging disabled, 01 = in pre-charge, 10 = in fast charging (constant current mode or constant voltage mode) and 11 = charging completed.

A negative pulse is sent on nINT pin to inform the host when a charging cycle is completed. In addition, the output status of STAT pin can be set by STAT_SET[1:0] bits, 00 = LED off (HIZ), 01 = LED on (low), 10 = LED blinking at 1s on 1s off, 11 = LED blinking at 1s on 3s off. This two bits only take effect when EN_ICHG_MON[1:0] = 01.

Battery Charging Profile

The SGM41543/SGM41543D feature a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 5. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are trickle charge (V_{BAT} < 2.2V), pre-charge and fast-charge (constant current and constant voltage).

Table 5. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHRG_STAT[1:0]
< 2.2V	I_{SHORT}	100mA	01
2.2V to 3.14V	I_{PRECHG}	180mA	01
> 3.14V	I_{CHG}	2.04A	10

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: The charge current will be less than the value in the register. The termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

DETAILED DESCRIPTION (continued)

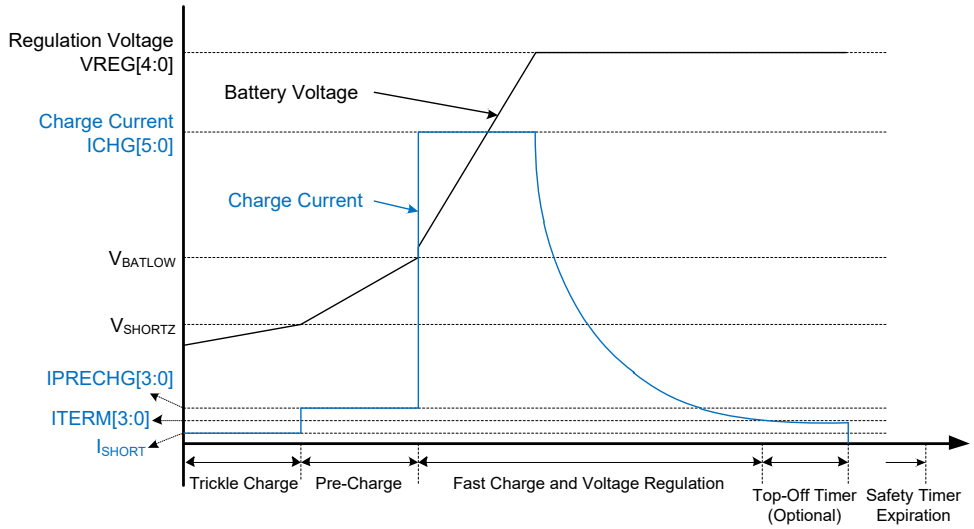


Figure 5. Battery Charging Profile

Charge Termination

A charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. Unless there is a high power demand for system and it needs to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck converter operates continuously to supply the system.

CHRG_STAT[1:0] bits are set to 11 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current, input voltage or junction temperature instead of charge current, termination will be temporarily prevented. EN_TERM bit is termination control bit and can be set to 0 to disable termination before it happens.

At low termination currents (60mA TYP), the offset in the internal comparator may give rise to a higher (+10mA to +20mA) actual termination current. A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current a chance to drop closer to the programmed value. The top-off delay timer has the same restrictions of the safety timer. As an example, under some conditions, if the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the termination timer will also be slowed down. The TOPOFF_ACTIVE bit reports the active/inactive status of the top-off timer. The CHRG_STAT[1:0] and TOPOFF_ACTIVE bits can be read to find status of the termination.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended.

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines.

DETAILED DESCRIPTION (continued)

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside the normal operating temperatures (typically 0℃ and 60℃). This functionality can be disabled if not needed. Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TS voltage within V_{T1} to V_{T4} window limits. If during the charge, battery gets too cold or too hot and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to be kept below 4.1V.

The SGM41543/SGM41543D exceed the JEITA requirement by their flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage is set to the lower of V_{REG} and 4.1V when JEITA_VSET_H = 0, the charge voltage is set to V_{REG} when JEITA_VSET_H = 1, and the charge current can be reduced down to 0%, 20% or 50% of fast charging current by the JEITA_ISET_H[1:0] bits. At cool temperatures (T1 - T2), the current setting can be reduced down to 50% or 20% of fast charging current selected by the JEITA_ISET_L bit when JEITA_ISET_L_EN = 1, and the charge voltage is set to V_{REG} when JEITA_VSET_L = 0, the charge voltage is set to the lower of V_{REG} and 4.1V when JEITA_VSET_L = 1. Additional, the cool threshold T2 and warm threshold T3 can be changed through JEITA_VT2[1:0] and JEITA_VT3[1:0], and the charge current can be disabled by setting JEITA_ISET_L_EN = 0.

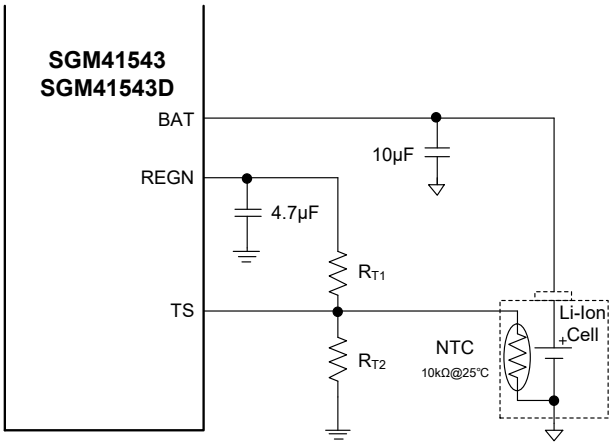


Figure 6. Battery Thermistor Connection and Bias Network

A 103AT-2 type thermistor is recommended to use for the SGM41543/SGM41543D. Other thermistors may be used and bias network (see Figure 6) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (1)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (2)$$

Where, V_{T1} and V_{T4} are T_{COLD} and T_{HOT} threshold voltages on TS pin as percentage to V_{REGN}, R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.35kΩ and R_{T2} = 31.88kΩ. The standard value is 5.23kΩ for R_{T1} and 30.9kΩ for R_{T2}.

DETAILED DESCRIPTION (continued)

Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable of monitoring the battery temperature for safety during the Boost mode. The temperature must remain within the V_{BCOLD} to V_{BHOT} thresholds, otherwise the Boost mode will be suspended and VBUS_STAT[2:0] bits are set to 000. Moreover, NTC_FAULT[2:0] register is updated to report Boost mode cold or hot condition. Once the temperature returns within the window, the Boost mode is resumed and NTC_FAULT[2:0] register is cleared to 000 (normal).

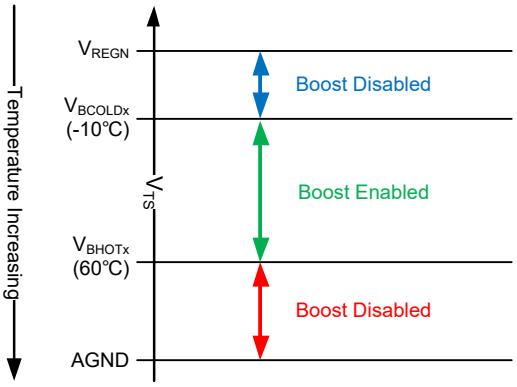


Figure 7. TS Pin Thermistor Temperature Window Settings in Boost Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, CHRG_FAULT[1:0] bits are set to 11 and a negative pulse is sent to nINT pin. By default, the charge time limit is 2 hours if the battery voltage does not rise above V_{BATLOW} threshold. And it is 16 hours if it goes above V_{BATLOW}. This feature is optional and can be disabled by clearing EN_TIMER bit. The 16 hours limit can also be reduced to 7 hours by clearing CHG_TIMER bit.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation, JEITA cool or thermal regulation. Because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 7 hours and the charger is regulating the input current (IINDPM_STAT bit = 1) in the whole charging cycle, the actual safety time will be 14 hours. Clearing the TMR2X_EN bit will disable the half clock rate feature.

The safety timer is paused if a fault occurs or charger is in supplement mode, charging is suspended. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling nCE pin or CHG_CONFIG bit, the timer resets and restarts a new timing.

Narrow Voltage DC (NVDC) Design in SGM41543/SGM41543D

The SGM41543/SGM41543D feature an NVDC design using the BATFET that connects the system to the battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Buck converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. SYS_MIN[2:0] register sets the minimum system voltage (default 3.5V). If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is lower than the minimum system voltage. The system voltage is regulated to 180mV (TYP) above the minimum system voltage setting. The battery gradually gets charged and its voltage rises above the minimum system voltage and lets BATFET change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 50mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. Charging is disabled and the battery voltage is above the minimum system voltage setting.

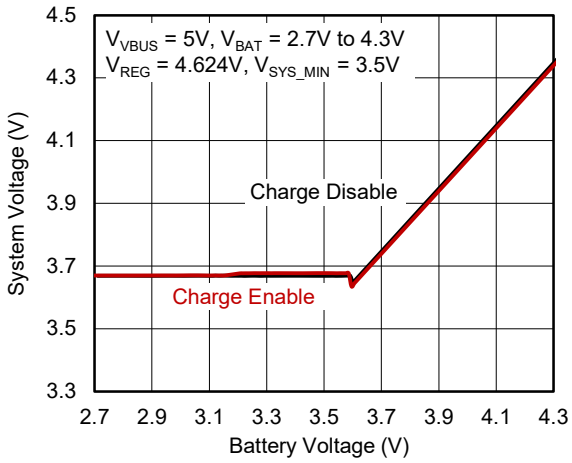


Figure 8. System Voltage vs. Battery Voltage

DETAILED DESCRIPTION (continued)

SGM41543/SGM41543D Dynamic Power Management (DPM)

The SGM41543/SGM41543D feature a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adaptor overloading or to meet the maximum current limits specified in the USB specs. Overloading an input source may result in either current trying to exceed the input current limit (I_{INDPM}) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the VSYS regulating to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 9 summarizes the DPM behavior (IINDPM type) for a design example with a 9V/1.2A adaptor, 3.2V battery, 2.8A charge current setting and 3.4V minimum system voltage setting.

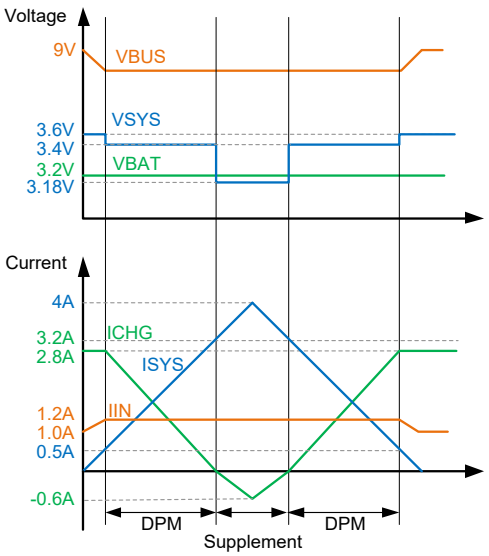


Figure 9. DPM Behavior Plot

Battery Supplement Mode

If the system voltage drops below the battery voltage, the BATFET gradually starts to turn on. The threshold margin is 50mV if V_{SYS_MIN} setting is less or larger than V_{BAT}. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation) such that the BATFET V_{DS} stays at 30mV. At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Use of the MOSFET linear mode at lower currents prevents swinging oscillation from entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 10. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

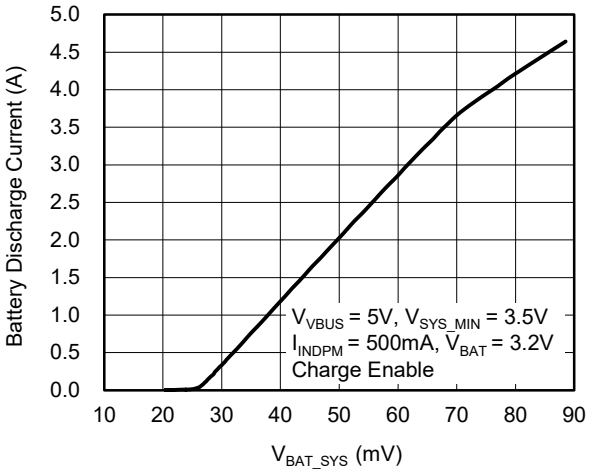


Figure 10. BATFET Gate Regulation V-I Curve

BATFET Control for System Power Reset and Ship Mode

Ship Mode (BATFET Disable)

Ship mode is usually used when the system is stored or in idle state for a long time or is in shipping. In such conditions, it is better to completely disconnect battery and make system voltage zero to minimize the leakage and extend the battery life. To enter ship mode, the BATFET has to be forced off by setting BATFET_DIS bit. The BATFET turns off immediately if BATFET_DLY bit is 0, or turns off after a t_{SM_DLY} delay (12.3 seconds) if BATFET_DLY is set.

DETAILED DESCRIPTION (continued)

Exit Ship Mode (BATFET Enable)

To exit the ship mode and enable the BATFET, one of the following can be applied:

With the chip no powered by VBUS:
1. Connect the adaptor to the input with a valid voltage to the VBUS input.
2. Pull nQON pin from logic high to low to enable BATFET, for example, by shorting nQON to GND. The negative pulse width should be at least a $t_{SHIPMODE}$ (1s TYP) for deglitching.

With the chip already powered by VBUS:
3. Clear BATFET_DIS bit by using host and I^2C.
4. Set REG_RST to 1 to reset all registers.
5. Apply a negative pulse to nQON pin (same as 2).

Full System Reset with BATFET Using nQON

When the input source is not present, the BATFET can act as a load on/off switch between the system and battery. This feature can be used to apply a power-on reset to the system. Host can toggle BATFET_DIS bit to cycle power off/on and reset the system. A push-button connected to nQON pin or a negative pulse can also be used to manually force a system power cycle when BATFET is ON (BATFET_DIS bit = 0). For this function, a negative logic pulse with a minimum width of t_{QON_RST} (10s TYP) must be applied to the nQON pin that results in a temporary BATFET turn-off for t_{BATFET_RST} (320ms TYP) that automatically turns on afterward. Setting BATFET_RST_EN to 0 can disable the function.

In summary, the nQON pin controls BATFET and system reset in two different ways:

1. Enable BATFET: Applying an nQON logic high to low transition with longer than $t_{SHIPMODE}$ deglitch time (negative pulse) turns on BATFET to exit ship mode (Figure 11 left). HIZ is also enabled (EN_HIZ = 1) when exiting shipping mode. After exiting shipping mode, the host can disable HIZ (EN_HIZ = 0). OTG cannot be enabled (OTG_CONFIG = 1) until HIZ is disabled.

2. Reset BATFET: By applying a logic low for a duration of at least t_{QON_RST} to nQON pin while VBUS is not powered and BATFET is allowed to turn on (BATFET_DIS bit = 0), the BATFET turns off for t_{BATFET_RST} and then it is re-enabled resulting in a system power-on reset (Figure 11 right). This function can be disabled by clearing BATFET_RST_EN bit.

A typical push button circuit for nQON is given in Figure 12.

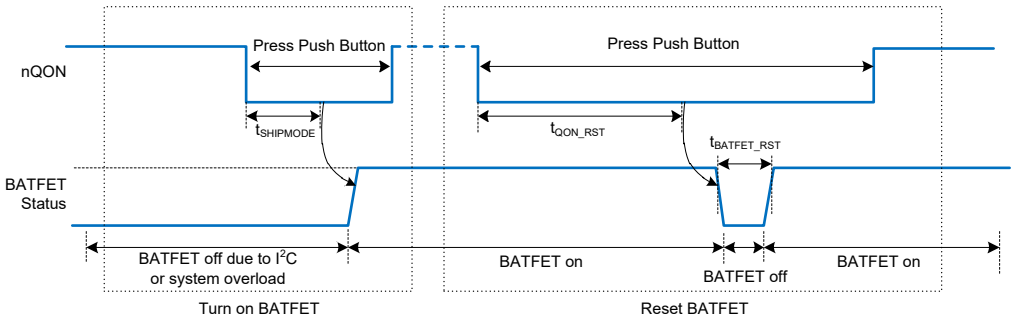


Figure 11. nQON Enable and Reset BATFET Timing

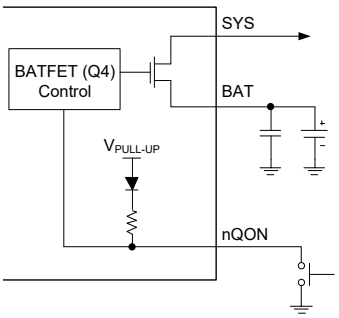


Figure 12. nQON Manual Operation Circuit

DETAILED DESCRIPTION (continued)

Status Outputs Pins (STAT and nINT)

Power Good Indication (PG_STAT Bit)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
- Device is not in sleep mode: $V_{VBUS} > V_{BAT} + V_{SLEEP}$.
- Input source is not poor: $V_{VBUS} > V_{VBUSMIN\_RISE}$ when I_{BAD_SRC} (25mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection.

Charge Status (STAT Pin)

Charging state is indicated with the open-drain STAT pin as explained in Table 6. This pin is able to drive an LED (see Figure 1 or Figure 2). The functionality of the STAT pin is disabled if the EN_ICHG_MON[1:0] bits are set to 10 or 11.

Table 6. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charging completed	High (LED OFF)
Charging is disabled or in sleep mode	High (LED OFF)
Charge is suspended due to input over-voltage, TS fault, timer faults or system over-voltage or Boost mode is suspended (TS fault)	1Hz Blinking
EN_ICHG_MON[1:0] = 01, controlled by register only, no matter with charging state	STAT_SET[1:0]

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time.

The following events can generate an interrupt pulse:

1. Faults reflect in REG0x09 register (watchdog, Boost overload, charge faults and battery over-voltage).
2. Charging is completed.
3. PSEL or D+/D- detection identifies a connected source (USB or adaptor).
4. Input source voltage enters the "input good" range:
   a) V_{VBUS} exceeds V_{BAT} (not in sleep mode).
   b) V_{VBUS} comes below V_{VBUS_OV}.
   c) V_{VBUS} remains above $V_{VBUSMIN\_RISE}$ when I_{BAD_SRC} (25mA TYP) load current is applied.
5. Input removes or out of the "input good" range.
6. A DPM event (VINDPM or IINDPM) occurs (a maskable interrupt).

Once a fault/flag happens, the INT pulse is asserted immediately and the fault/flag bits are updated in REG0x09 and REG0x0E. Fault/flag status is not reset in the register until the host reads it. A new fault will not assert a new INT pulse until the host reads REG0x09 and all the previous faults are cleared. Therefore, in order to read the current time faults, the host must read REG0x09 two times consecutively. The first read returns the history of the fault register status (from the time of the last read or reset) and the second one checks the current active faults. As an exception, the NTC_FAULT bit reports the actual real-time status of TS pin.

Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adaptor, in order to signal adaptor to increase/decrease output voltage. To enable the interface, the EN_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting either the PUMPX_UP or PUMPX_DN bit to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate pulse sequence in progress and the device pulses the input current limit between current limit set forth by IINDPM[4:0] register and the 100mA current limit. When the pulse sequence is completed, the input current limit is returned to value set by IINDPM[4:0] register and the PUMPX_UP or PUMPX_DN bit is cleared. In addition, the EN_PUMPX can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as setting forth by the IINDPM[4:0] register immediately. When EN_PUMPX bit is low, writing to PUMPX_UP and PUMPX_DN bits would be ignored, which has no effect on VBUS current limit.

DETAILED DESCRIPTION (continued)

SGM41543/SGM41543D Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (VBUS and VSYS) and switch currents are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as described below.

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage (ACOV)

Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit that is programmable by OVP[1:0] in REG0x06. It is selectable among 5.5V, 6.5V, 10.5V and 14V (default) for USB or 5V, 9V or 12V adaptors respectively.

Each time VBUS exceeds the OVP limit, an INT pulse is asserted. As long as the over-voltage persists, the CHRG_FAULT[1:0] bits are set to 01 in REG0x09. Fault will be cleared to 00 if the voltage comes back below limit (and a hysteresis threshold) and host reads the fault register. Charger resumes its normal operation when the voltage comes back below OVP limit.

2. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold is 350mV + V_{SYS_REG} (system regulation voltage + 350mV). Once a SYSOVP occurs, switching stops to clamp any overshoot and a 27mA sink current is applied to SYS to pull the voltage down.

Boost Mode Voltage and Current Monitoring

In Boost mode, the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Soft-Start on VBUS

Boost mode begins with a soft-start to prevent large inrush currents when it is enabled.

2. Output Short Protection for VBUS

Short circuit protection is provided for VBUS output in Boost mode. To accept different types of load connected to VBUS and OTG adaptation, an accurate constant current regulation control is implemented for Boost mode. In case of a short circuit on VBUS pin, the Q1 turns off and retries 7 times (Hiccup). If short is not removed after retries, the OTG will be disabled by clearing OTG_CONFIG bit. Also, an INT pulse is sent and the BOOST_FAULT bit is set to 1 in REG0x09. When the host activates the Boost mode again, the BOOST_FAULT bit will be cleared.

3. Output Over-Voltage Protection for VBUS

In Boost mode, converter stops switching and exits Boost mode (by clearing OTG_CONFIG bit) if VBUS voltage rises above regulation and exceeds the V_{OTG_OVP} over-voltage limit (6V TYP). An INT pulse is sent and the BOOST_FAULT bit is set to 1.

SGM41543/SGM41543D Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in Buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the THERM_STAT bit to 1. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the junction temperature exceeds T_{SHUT} (+150℃), thermal shutdown protection arises in which the converter is turned off, CHRG_FAULT[1:0] bits are set to 10 in the fault register and an INT pulse is sent.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

Boost Mode Thermal Protections

Similar to Buck mode, T_J is monitored in Boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (+150 ℃), the Boost mode will be disabled (OTG_CONFIG bit clears). If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the Boost can recover again by re-enabling OTG_CONFIG bit by host.

DETAILED DESCRIPTION (continued)

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 3.9% above the battery regulation voltage setting. In case of a BATOVP, charging or external direct charging stops right away, the BAT_FAULT bit is set to 1 and an INT pulse is sent.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level ($V_{BAT\_DPL\_FALL}$), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{SHORT} current (100mA TYP) first as long as $V_{BAT} < V_{SHORTZ}$. When battery voltage is increased and $V_{SHORTZ} < V_{BAT} < V_{BATLOW}$, the charge current will increase to the pre-charge current level programmed in the IPRECHG[3:0] register.

Battery Over-Current Protection for System

The BATFET will latch off, if its current limit is exceeded due to a short or large overload on the system ($I_{BAT} > I_{BATFET\_OCP}$). To reset this latch off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41543/ SGM41543D parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41543 operates as a slave device that address is 0x0A (0AH), while the SGM41543D operates with address 0x0B (0BH). It has sixteen 8-bit registers, numbered from REG0x00 to REG0x0F. A register read beyond REG0x0F returns 0xFF.

Physical Layer

The standard I²C interface of SGM41543/SGM41543D supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started through taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 13. All transactions are started by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is generated by master when SCL is high and a high to low transition on the SDA. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

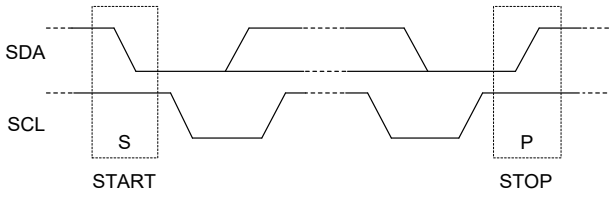


Figure 13. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the HIGH period of the clock. The state of the SDA can only change when the clock (SCL) is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 14.

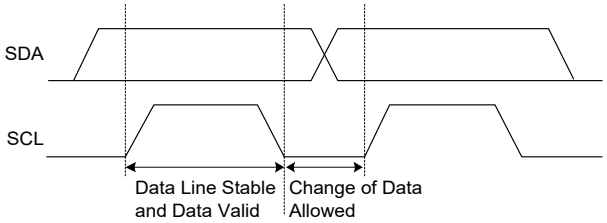


Figure 14. I²C Bus Bit Transfer

DETAILED DESCRIPTION (continued)

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 15 shows the byte transfer process with I^2C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a stop condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and the eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accesses in the next byte(s). The data transfer transaction is shown in Figure 16.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 17 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 18), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

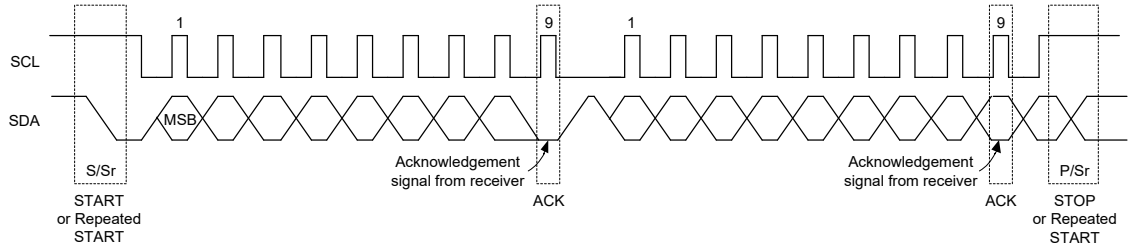


Figure 15. Byte Transfer Process

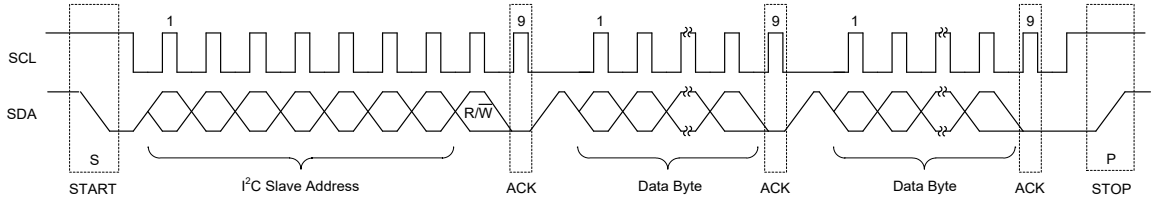


Figure 16. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

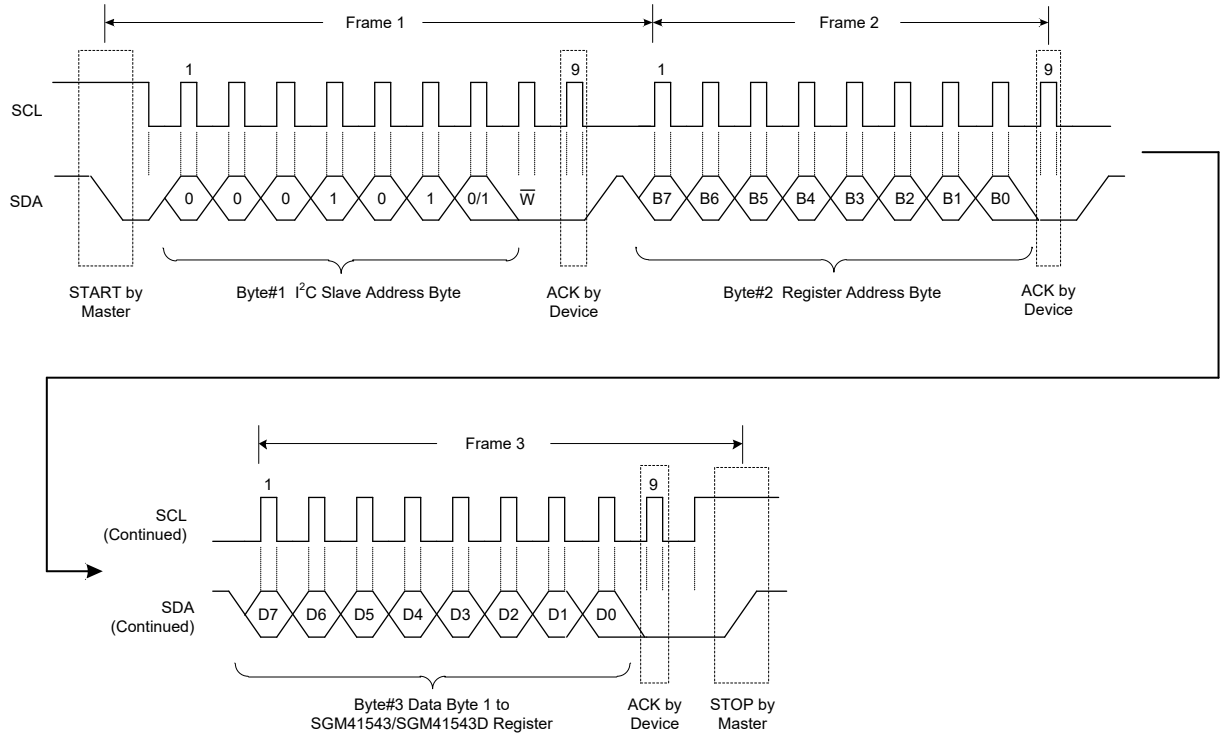


Figure 17. A Single Write Transaction

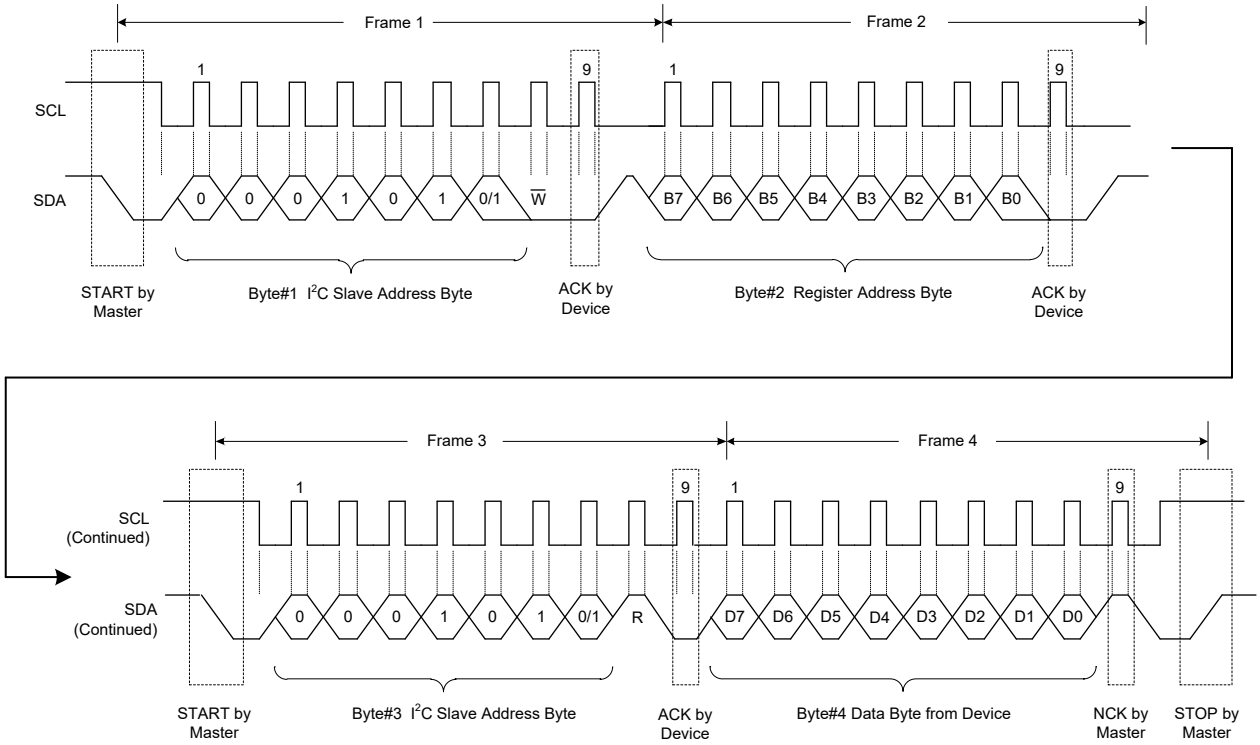


Figure 18. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41543/ SGM41543D, as explained in Figure 19 and Figure 20. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

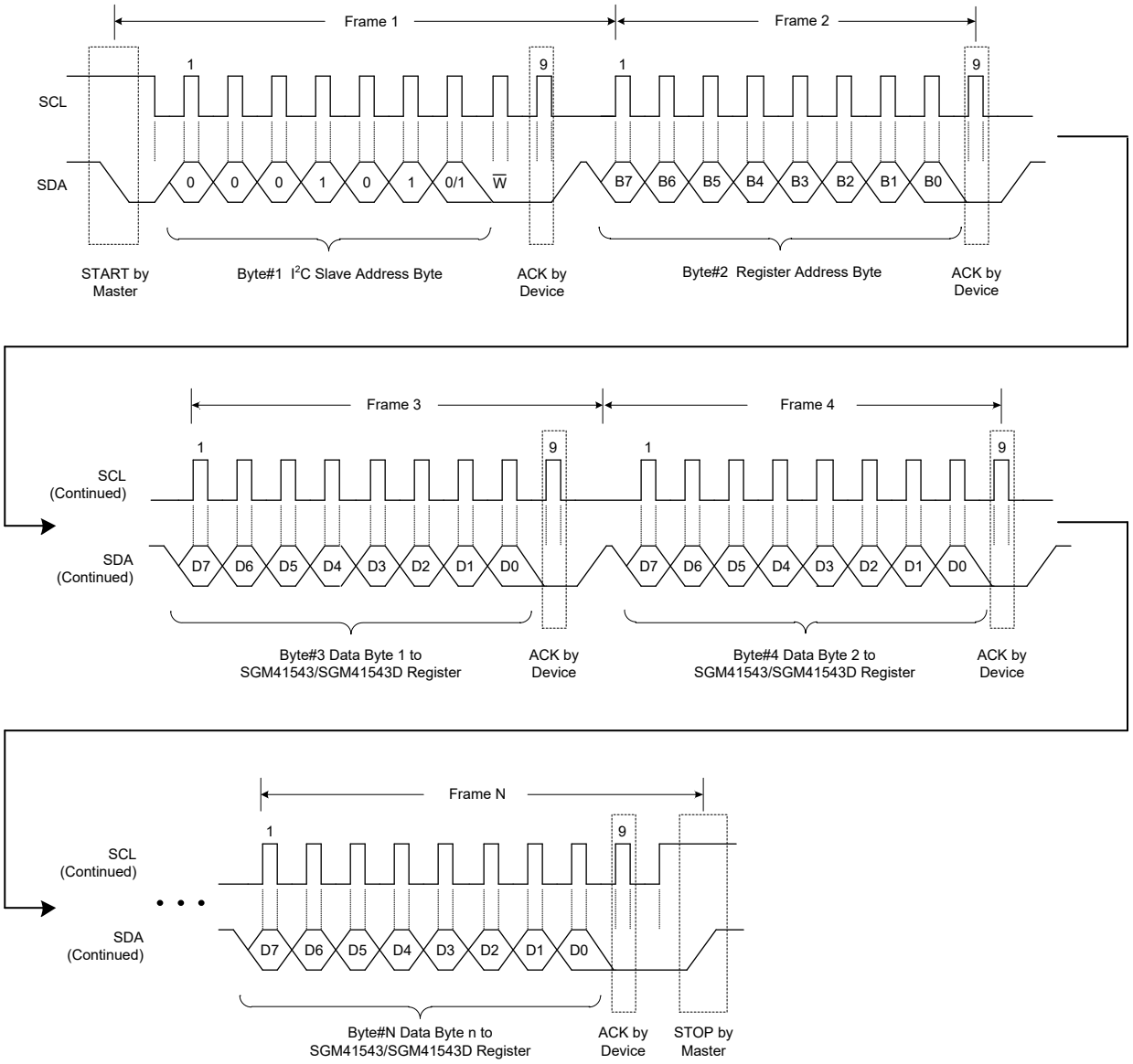


Figure 19. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

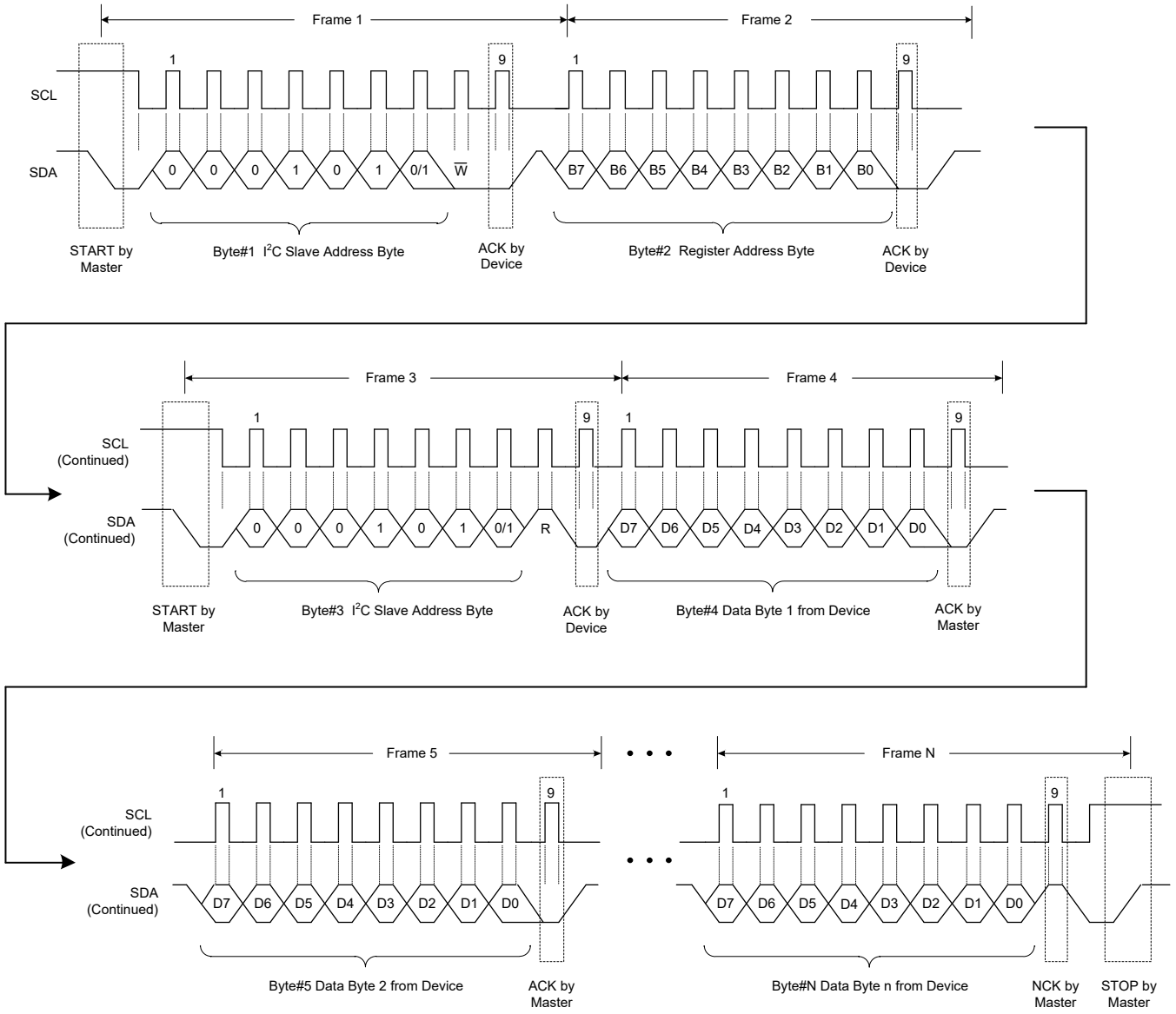


Figure 20. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
CHARGE	0x08[4:3] 0x09[5:4]	—	—	—	0x01[4]
VREG	0x0A[4]	—	—	0x04[7:3]	—
VREG_FT	—	—	—	0x0F[7:6]	0x0F[7:6]
ICHG	—	—	—	0x02[5:0]	—
IPRECHG	—	—	—	0x03[7:4]	—
ITERM	—	—	—	0x03[3:0]	0x05[7]
VRECHG	—	—	—	0x04[0]	—
CHG_TIMER	0x09[5:4]	—	—	0x05[2]	0x05[3]
TOPOFF_TIMER	0x0A[3]	—	—	0x04[2:1]	0x04[2:1]
TMR2X	—	—	—	—	0x07[6]
VINDPM	0x0A[6]	—	0x0A[1]	0x06[3:0] 0x0F[1:0]	—
VDPM_BAT_TRACK	—	—	—	0x07[1:0]	0x07[1:0]
IINDPM	0x0A[5]	—	0x0A[0]	0x00[4:0]	—
Q1_FULLON	—	—	—	0x02[6]	—
VBUS	0x08[7:5] 0x0A[7]	—	—	—	—
PG	0x08[2]	—	—	—	—
IINDET	—	—	—	—	0x07[7]
INPUT_DET_DONE	0x0E[7] (SGM41543)	0x0E[7] (SGM41543D)	—	—	—
EN_ICHG_MON	—	—	—	0x00[6:5]	0x00[6:5]
STAT_SET	—	—	—	0x0F[3:2]	0x00[6:5]
SYS_MIN	0x08[0]	—	—	0x01[3:1]	—
HIZ MODE	—	—	—	—	0x00[7]
WATCHDOG	0x09[7]	—	—	0x05[5:4]	0x05[5:4]
WD_RST	—	—	—	—	0x01[6]
OTG	0x08[7:5]	—	—	0x06[5:4]	0x01[5]
MIN_BAT_SEL	—	—	—	0x01[0]	—
BOOST_LIM	—	—	—	0x02[7]	—
BATFET	—	—	—	0x07[3]	0x07[5]
BATFET_RST	—	—	—	—	0x07[2]
PFM	—	—	—	—	0x01[7]
DCEN	—	—	—	0x0F[4]	—
ARDCEN_ITS	—	—	—	0x05[6]	—
PUMPX	—	—	—	0x0D[6] 0x0D[5]	0x0D[7]
DP_VSET	—	—	—	0x0D[4:3]	—
DM_VSET	—	—	—	0x0D[2:1]	—
JEITA	0x09[2:0]	—	—	—	0x0D[0]
JEITA_VT2	—	—	—	0x0C[3:2]	—
JEITA_VT3	—	—	—	0x0C[1:0]	—
JEITA_VSET_L	—	—	—	0x0C[7]	—
JEITA_VSET_H	—	—	—	0x07[4]	—
JEITA_ISET_L	—	—	—	0x05[0]	0x0C[6]
JEITA_ISET_H	—	—	—	0x0C[5:4]	—
TREG	0x08[1]	—	—	0x05[1]	—
TSHUT	0x09[5:4]	—	—	—	—
BUS OVP	0x0A[2] 0x09[5:4]	—	—	0x06[7:6]	—
BAT OVP	0x09[3]	—	—	—	—
BOOST FAULT	0x09[6]	—	—	—	—
REG_RST	—	—	—	—	0x0B[7]

REGISTER MAPS (continued)

I²C Slave Address of SGM41543/SGM41543D: 0x0A/0x0B

Bit Types:

R: Read only

R/W: Read/Write

n: Parameter code formed by the bits as an unsigned binary number.

REG0x00: Input Current Limit Register [Reset = 0x17]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	EN_HIZ	0	R/W	Enable HIZ Mode 0 = Disable (default) 1 = Enable In HIZ mode, the VBUS pin is effectively disconnected from internal circuit. Some leakage current may exist.		REG_RST or Watchdog
D[6:5]	EN_ICHG_MON[1:0]	00	R/W	Enable STAT Pin Function 00 = Enable following charging state (default) 01 = Enable following STAT_SET[1:0] bits 10 = Disable (float pin) 11 = Disable (float pin) These bits turn on or off the function of the STAT open-drain output pin (charge status or customer customized indicator).		REG_RST
D[4:0]	IINDPM[4:0]	10111	R/W	IINDPM[4] 1 = 1600mA	Input Current Limit Value (n: 5 bits): = 100 + 100n (mA) Offset: 100mA Range: 100mA (00000) - 3.1A (11110), 3.8A (11111) Default: 2400mA (10111), not typical IINDPM changes after an input source detection. Host can overwrite IINDPM after input source detection is completed.	REG_RST
				IINDPM[3] 1 = 800mA		
				IINDPM[2] 1 = 400mA		
				IINDPM[1] 1 = 200mA		
				IINDPM[0] 1 = 100mA		

REGISTER MAPS (continued)

REG0x01: Charger Control 1 Register [Reset = 0x1A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PFM_DIS	0	R/W	Enable PFM Mode 0 = Enable (default) 1 = Disable Enable pulse frequency modulation. PFM is normally used to save power at light load by reducing converter switching frequency.	REG_RST
D[6]	WD_RST	0	R/W	I^2C Watchdog Timer Reset 0 = Normal (default) 1 = Reset Watchdog timer reset control bit. Write 1 to this bit to avoid watchdog expiry. WD_RST resets to 0 after watchdog timer reset (expiry).	REG_RST or Watchdog
D[5]	OTG_CONFIG	0	R/W	Enable OTG 0 = OTG disable (default) 1 = OTG enable This bit has priority over charge enable in the CHG_CONFIG.	REG_RST or Watchdog
D[4]	CHG_CONFIG	1	R/W	Enable Battery Charging 0 = Charge disable 1 = Charge enable (default) Charge is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low.	REG_RST or Watchdog
D[3:1]	SYS_MIN[2:0]	101	R/W	Minimum System Voltage 000 = 2.6V 001 = 2.8V 010 = 3V 011 = 3.2V 100 = 3.4V 101 = 3.5V (default) 110 = 3.6V 111 = 3.7V Minimum System Voltage Value. Offset: 2.6V Range: 2.6V (000) - 3.7V (111) Default: 3.5V (101)	REG_RST
D[0]	MIN_BAT_SEL	0	R/W	Minimum Battery Voltage for OTG Mode 0 = 3V V_{BAT} falling (default) 1 = 2.57V V_{BAT} falling Default: V_{BAT} falling, V_{BATLOW_OTG} = 3V. V_{BAT} rising, V_{BATLOW_OTG} = 3.25V.	REG_RST

REGISTER MAPS (continued)

REG0x02: Charge Current Limit Register [Reset = 0XA2]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	BOOST_LIM	1	R/W	Boost Mode Current Limit 0 = 1.2A 1 = 2A (default) The current limit options listed values are the minimum specs. Actual value is typically higher.		REG_RST or Watchdog
D[6]	Q1_FULLON	0	R/W	VBUS FET Switch (Q1) 0 = Use higher R_{DSON} if I_{INDPM} < 700mA (for better accuracy) (default) 1 = Use lower R_{DSON} always (fully ON for better efficiency) Control the on-resistance of Q1 (VBUS switch) for better input current measurement accuracy. In Boost mode, full FET is always used.		REG_RST
D[5:0]	ICHG[5:0]	100010	R/W	ICHG[5] 1 = 1920mA	Fast Charge Current Value (n: 6 bits): = 60n (mA) Offset: 0mA Range: 0mA (000000) - 3780mA (111111) Default: 2040mA (100010) Note: Setting I_{CHG} = 0mA disables charge.	REG_RST or Watchdog
				ICHG[4] 1 = 960mA		
				ICHG[3] 1 = 480mA		
				ICHG[2] 1 = 240mA		
				ICHG[1] 1 = 120mA		
				ICHG[0] 1 = 60mA		

REG0x03: Pre-Charge and Termination Current Limit Register [Reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	IPRECHG[3:0]	0	R/W	IPRECHG[3] 1 = 480mA	Pre-Charge Current Limit (n: 4 bits): = 60 + 60n (mA) (n ≤ 12) Offset: 60mA Range: 60mA (0000) - 780mA (1100) Default: 180mA (0010) Note: Values above 12D = 1100 (780mA) are clamped to 12D = 1100 (780mA).	REG_RST or Watchdog
		0	R/W	IPRECHG[2] 1 = 240mA		
		1	R/W	IPRECHG[1] 1 = 120mA		
		0	R/W	IPRECHG[0] 1 = 60mA		
D[3:0]	ITERM[3:0]	0	R/W	ITERM[3] 1 = 480mA	Termination Current Limit (n: 4 bits): = 60 + 60n (mA) Offset: 60mA Range: 60mA (0000) - 960mA (1111) Default: 180mA (0010)	REG_RST or Watchdog
		0	R/W	ITERM[2] 1 = 240mA		
		1	R/W	ITERM[1] 1 = 120mA		
		0	R/W	ITERM[0] 1 = 60mA		

REGISTER MAPS (continued)

REG0x04: Battery Voltage Limit Register [Reset = 0x58]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:3]	VREG[4:0]	0	R/W	VREG[4] 1 = 512mV	Charge Voltage Limit (n: 5 bits): = 3856 + 32n (mV) if n ≤ 24, n≠15; = 4.352V if n = 15 Offset: 3.856V Range: 3.856V (00000) - 4.624V (11000) Default: 4.208V (01011) Special Value: 4.352V (01111) Note: Values above 24D = 11000 (4.624V) are clamped to 24D = 11000 (4.624V).	REG_RST or Watchdog
		1	R/W	VREG[3] 1 = 256mV		
		0	R/W	VREG[2] 1 = 128mV		
		1	R/W	VREG[1] 1 = 64mV		
		1	R/W	VREG[0] 1 = 32mV		
D[2:1]	TOPOFF_TIMER[1:0]	00	R/W	Top-Off Timer 00 = Disabled (default) 01 = 15 minutes 10 = 35 minutes 11 = 45 minutes The charge extension time is added after the termination condition is detected. If disabled, charging terminates as soon as termination conditions are met.		REG_RST or Watchdog
D[0]	VRECHG	0	R/W	Battery Recharge Threshold 0 = 100mV below VREG[4:0] (default) 1 = 200mV below VREG[4:0] A recharge cycle will start if a fully charged battery voltage drops below VREG - VRECHG settings. The switching frequency is set to 1500kHz or 500kHz by setting this bit to 0 or 1.		REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x05: Charger Control 2 Register [Reset = 0x9F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_TERM	1	R/W	Charging Termination Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[6]	ARDCEN_ITS	0	R/W	DCEN Reset Enable or ITERM Timer Setting 0 = Allow resetting DCEN or set 230ms (default) 1 = Don't allow resetting DCEN or set 16ms When DCEN = 1 and IBUS over-current occurs, set this bit 0 or 1 to allow resetting DCEN or not. When DCEN = 0, set this bit 0 or 1 to set ITERM detection timer to 230ms or 16ms.	REG_RST or Watchdog
D[5:4]	WATCHDOG[1:0]	01	R/W	Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s Expiry time of the watchdog timer if it is not reset.	REG_RST or Watchdog
D[3]	EN_TIMER	1	R/W	Charge Safety Timer Enable 0 = Disable 1 = Enable (default) When it is enabled, the pre-charge and fast charge periods are included in the timing.	REG_RST or Watchdog
D[2]	CHG_TIMER	1	R/W	Charge Safety Timer Setting 0 = 7h 1 = 16h (default)	REG_RST or Watchdog
D[1]	TREG	1	R/W	Thermal Regulation Threshold 0 = 80℃ 1 = 120℃ (default) For Buck mode.	REG_RST or Watchdog
D[0]	JEITA_ISET_L (0℃ - 10℃)	1	R/W	JEITA Charging Current 0 = 50% of I_{CHG} 1 = 20% of I_{CHG} (default) When JEITA_ISET_L_EN = 1.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x06: Charger Control 3 Register [Reset = 0xE6]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:6]	OVP[1:0]	11	R/W	VAC Pin OVP Threshold 00 = 5.5V 01 = 6.5V (5V input) 10 = 10.5V (9V input) 11 = 14V (12V input) (default) OVP threshold for input supply.		REG_RST
D[5:4]	BOOSTV[1:0]	10	R/W	Boost Mode Voltage Regulation 00 = 4.85V 01 = 5.00V 10 = 5.15V (default) 11 = 5.30V		REG_RST
D[3:0]	VINDPM[3:0]	0110	R/W	VINDPM[3] 1 = 800mV	VINDPM Threshold (n: 4 bits): = Offset + 0.1n (V) Offset: 3.9V (VINDPM_OS[1:0] = 00, default) Range: 3.9V (0000) - 5.4V (1111) Default: 4.5V (0110) Offset: 5.9V (VINDPM_OS[1:0] = 01) Range: 5.9V (0000) - 7.4V (1111) Offset: 7.5V (VINDPM_OS[1:0] = 10) Range: 7.5V (0000) - 9V (1111) Offset: 10.5V (VINDPM_OS[1:0] = 11) Range: 10.5V (0000) - 12V (1111)	REG_RST
				VINDPM[2] 1 = 400mV		
				VINDPM[1] 1 =200mV		
				VINDPM[0] 1 =100mV		

REG0x07: Charger Control 4 Register [Reset = 0x4C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IINDET_EN	0	R/W	Input Current Limit Detection 0 = Not in input current limit detection (default) 1 = Force input current limit detection when VBUS is present Reload with 0 when input detection is completed.	REG_RST or Watchdog
D[6]	TMR2X_EN	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = Safety timer slows down during DPM, JEITA cool, or thermal regulation (default) Slow down by a factor of 2.	REG_RST or Watchdog
D[5]	BATFET_DIS	0	R/W	Disable BATFET 0 = Allow BATFET (Q4) to turn on (default) 1 = Turn off BATFET (Q4) after a t_{SM_DLY} delay time (REG0x07 D[3]) t_{SM_DLY} is typically 12.3 seconds.	REG_RST
D[4]	JEITA_VSET_H (45℃ - 60℃)	0	R/W	JEITA Charging Voltage 0 = Set charge voltage to the lower of 4.1V and V_{REG} (default) 1 = Set charge voltage to V_{REG}	REG_RST or Watchdog
D[3]	BATFET_DLY	1	R/W	BATFET Turn Off Delay Control 0 = Turn off BATFET immediately 1 = Turn off BATFET after t_{SM_DLY} (default) BATFET_DIS bit is set.	REG_RST
D[2]	BATFET_RST_EN	1	R/W	Enable BATFET Reset 0 = Disable BATFET reset 1 = Enable BATFET reset (default)	REG_RST or Watchdog
D[1:0]	VDPM_BAT_ TRACK[1:0]	00	R/W	Dynamic VINDPM Tracking 00 = Disable (V_{INDPM} set by register) (default) 01 = V_{BAT} + 200mV 10 = V_{BAT} + 250mV 11 = V_{BAT} + 300mV Set V_{INDPM} to track V_{BAT} voltage. Actual V_{INDPM} is the larger of VINDPM[3:0] value and this register value.	REG_RST

REGISTER MAPS (continued)

REG0x08: Charger Status 1 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VBUS_STAT[2:0]	xxx	R	VBUS Status Register (SGM41543D) 000 = No input 001 = USB host SDP 010 = USB CDP (1.5A) 011 = USB DCP (2.4A) 101 = Unknown adaptor (500mA) 110 = Non-standard adaptor (1A/2A/2.1A/2.4A) 111 = OTG VBUS Status Register (SGM41543) 000 = No input 001 = USB host SDP (500mA) → PSEL HIGH 010 = Adaptor 2.4A → PSEL LOW 111 = OTG Other values are reserved. Current limit value is reported in IINDPM[4:0] register.	N/A
D[4:3]	CHRG_STAT[1:0]	xx	R	Charging Status 00 = Charge disable 01 = Pre-charge (V_{BAT} < V_{BATLOW}) 10 = Fast charging (constant current or voltage) 11 = Charging terminated	N/A
D[2]	PG_STAT	x	R	Input Power Status (VBUS in good voltage range and not poor) 0 = Input power source is not good 1 = Input power source is good	N/A
D[1]	THERM_STAT	x	R	Thermal Regulation Status 0 = Not in thermal regulation 1 = In thermal regulation	N/A
D[0]	VSYS_STAT	x	R	System Voltage Regulation Status 0 = Not in VSYS_MIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In VSYS_MIN regulation (V_{BAT} < V_{SYS_MIN})	N/A

REG0x09: Fault Status Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WATCHDOG_FAULT	x	R	Watchdog Fault Status 0 = Normal (no fault) 1 = Watchdog timer expired	N/A
D[6]	BOOST_FAULT	x	R	Boost Mode Fault Status 0 = Normal 1 = VBUS is overloaded in OTG, or VBUS OVP, or battery voltage is too low (any condition that prevents Boost starting)	N/A
D[5:4]	CHRG_FAULT[1:0]	xx	R	Charging Fault Status 00 = Normal 01 = Input fault (VBUS OVP or V_{BAT} < V_{VBUS} < 3.8V) 10 = Thermal shutdown 11 = Charge safety timer expired	N/A
D[3]	BAT_FAULT	x	R	Battery Fault Status 0 = Normal 1 = Battery over-voltage (BATOVP)	N/A
D[2:0]	NTC_FAULT[2:0]	xxx	R	JEITA Condition Based on Battery NTC Temperature Measurement 000 = Normal 010 = Warm (Buck mode only) 011 = Cool (Buck mode only) 101 = Cold 110 = Hot NTC fault bits are updated in real-time and do not need a read to reset.	N/A

REGISTER MAPS (continued)

REG0x0A: Charger Status 2 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_GD	x	R	Good Input Source Detected 0 = A good VBUS is not attached 1 = A good VBUS is attached	N/A
D[6]	VINDPM_STAT	x	R	Input Voltage Regulation (Dynamic Power Management) 0 = Not in VINDPM 1 = In VINDPM	N/A
D[5]	IINDPM_STAT	x	R	Input Current Regulation (Dynamic Power Management) 0 = Not in IINDPM 1 = In IINDPM	N/A
D[4]	CV_STAT	x	R	CV Mode Status Indicator when DCEN = 0 0 = VBAT is lower than VREG 1 = VBAT approaches to VREG	N/A
D[3]	TOPOFF_ACTIVE	x	R	Active Top-Off Timer Counting Status 0 = Top-off timer is not counting 1 = Top-off timer is counting	N/A
D[2]	ACOV_STAT	x	R	Input Over-Voltage Status (AC adaptor is the input source) 0 = No over-voltage (no ACOV) 1 = Over-voltage is detected (ACOV)	N/A
D[1]	VINDPM_INT_MASK	0	R/W	VINDPM Event Detection Interrupt Mask 0 = Allow VINDPM INT pulse (default) 1 = Mask VINDPM INT pulse	REG_RST
D[0]	IINDPM_INT_MASK	0	R/W	IINDPM Event Detection Mask 0 = Allow IINDPM to send INT pulse (default) 1 = Mask IINDPM INT pulse	REG_RST

REG0x0B: Part Information Register [Reset = 0x4X]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/W	Register Reset 0 = No effect (keep current register settings) (default) 1 = Reset R/W bits of all registers to the default and reset safety timer (it also resets itself to 0 after register reset is completed.)	REG_RST
D[6:2]	PN[4:0]	1 0 0 x 0	R	Part ID 10000 = SGM41543 10010 = SGM41543D	N/A
D[1:0]	DEV_REV[1:0]	xx	R	Revision	N/A

REGISTER MAPS (continued)

REG0x0C: Charger Control 5 Register [Reset = 0x75]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	JEITA_VSET_L (0℃ - 10℃)	0	R/W	JEITA Charging Voltage 0 = Set charge voltage to V_{REG} (default) 1 = Set charge voltage to the lower of 4.1V and V_{REG}	REG_RST or Watchdog
D[6]	JEITA_ISET_L_EN (0℃ - 10℃)	1	R/W	Charge Enable during Cool Temperature 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[5:4]	JEITA_ISET_H[1:0] (45℃ - 60℃)	11	R/W	Charge Current Setting during Warm Temperature 00 = 0% of I_{CHG} 01 = 20% of I_{CHG} 10 = 50% of I_{CHG} 11 = 100% of I_{CHG} (default) In warm condition, the safety timer does not become 2X.	REG_RST or Watchdog
D[3:2]	JEITA_VT2[1:0]	01	R/W	JEITA Cool Threshold Setting 00 = V_{T2} = 70.75% (5.5℃) 01 = V_{T2} = 68.25% (10℃) (default) 10 = V_{T2} = 65.25% (15℃) 11 = V_{T2} = 62.25% (20℃)	REG_RST or Watchdog
D[1:0]	JEITA_VT3[1:0]	01	R/W	JEITA Warm Threshold Setting 00 = V_{T3} = 48.25% (40℃) 01 = V_{T3} = 44.75% (45℃) (default) 10 = V_{T3} = 40.75% (50.5℃) 11 = V_{T3} = 37.75% (54.5℃)	REG_RST or Watchdog

REG0x0D: Charger Control 6 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_PUMPX	0	R/W	Current Pulse Control Enable 0 = Disable (default) 1 = Enable (PUMPX_UP and PUMPX_DN)	REG_RST or Watchdog
D[6]	PUMPX_UP	0	R/W	Current Pulse Control Voltage Up Enable 0 = Disable (default) 1 = Enable This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	REG_RST or Watchdog
D[5]	PUMPX_DN	0	R/W	Current Pulse Control Voltage Down Enable 0 = Disable (default) 1 = Enable This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	REG_RST or Watchdog
D[4:3]	DP_VSET[1:0]	00	R/W	D+ Output Voltage Setting 00 = HIZ (default) 01 = 0V 10 = 0.6V 11 = 3.3V Register bits are reset to default value when input source is plugged in and can be changed after D+/D- detection is completed.	REG_RST or Watchdog
D[2:1]	DM_VSET[1:0]	00	R/W	D- Output Voltage Setting 00 = HIZ (default) 01 = 0V 10 = 0.6V 11 = 3.3V Register bits are reset to default value when input source is plugged in and can be changed after D+/D- detection is completed.	REG_RST or Watchdog
D[0]	JEITA_EN	1	R/W	JEITA Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0E: Charger Flag Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	INPUT_DET_DONE	x	R	VBUS Input Detection Done Flag 0 = Normal 1 = Detection done PSEL or DPDM detection done flag after VBUS plug-in or set IINDET_EN = 1.	NA
D[6:0]	Reserved	xxxxxxx	R	Reserved	NA

REG0x0F: Charger Control 7 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	VREG_FT	00	R/W	VREG Fine Tuning 00 = Disable (default) 01 = V_{REG} + 8mV 10 = V_{REG} - 8mV 11 = V_{REG} - 16mV	REG_RST or Watchdog
D[5]	Reserved	0	R/W	Reserved	REG_RST or Watchdog
D[4]	DCEN	0	R/W	DCEN Pin Output Control 0 = Low (default) 1 = High When BATOVP time reaches t_{BATOVP_DCEN}, the bit resets to default.	REG_RST or Watchdog
D[3:2]	STAT_SET[1:0]	00	R/W	STAT Pin Output Setting 00 = LED off (HIZ) (default) 01 = LED on (low) 10 = LED blinking 1s on 1s off 11 = LED blinking 1s on 3s off This bits only takes effect when EN_ICHG_MON[1:0] = 01.	REG_RST or Watchdog
D[1:0]	VINDPM_OS[1:0]	00	R/W	VINDPM Offset 00 = 3.9V (default) 01 = 5.9V 10 = 7.5V 11 = 10.5V	REG_RST

APPLICATION INFORMATION

The SGM41543/SGM41543D are typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I^2C interface) and a single-cell Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Design

Small energy storage elements (inductor and capacitor) can be used since the high frequency (1.5MHz) switching converter is used in the SGM41543/SGM41543D. Inductor should tolerate current which is higher than the maximum charge current (I_{CHG}) plus half the inductor peak to peak ripple current (ΔI) without saturation:

$$I_{SAT} > I_{CHG} + \frac{\Delta I}{2} \quad (3)$$

The inductor ripple current is determined by the input voltage (V_{VBUS}), duty cycle ($D = V_{BAT}/V_{VBUS}$), switching frequency (f_S = 1.5MHz) and the inductance (L). In CCM:

$$\Delta I = \frac{V_{VBUS} \times D \times (1-D)}{f_S \times L} \quad (4)$$

Inductor ripple current is maximum when D ≈ 0.5. In the practical designs, inductor peak to peak current ripple is selected in a range from 20% to 40% of the maximum DC current $\Delta I = (0.2 \sim 0.4) \times I_{CHG}$ for a good trade-off between inductor size and efficiency. Selecting the higher ripple allows choosing of smaller inductance.

For each application, V_{VBUS} and I_{CHG} are known, so L can be calculated from (4) and current rating of the inductor can be selected from (3). Choose an inductor that has small DCR and core losses at 1.5MHz to have high efficiency and cool operation at full load.

Input Capacitor Design

Select low ESR ceramic input capacitor (X7R or X5R) with sufficient voltage and RMS ripple current rating for decoupling of the input switching ripple current (I_{CIN}). The RMS ripple current in the worst case is around the $I_{CHG}/2$ when D ≈ 0.5. If the converter does not operate at D ≈ 50%, in the worst case, the capacitor RMS current can be estimated from (5) in which D is the closest operating duty cycle to 0.5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

For SGM41543/SGM41543D, place C_{IN} across PMID and GND pins close to the chip. Voltage rating of the capacitor must be at least 25% higher than the normal input voltage to minimize voltage derating. For a 13.5V input voltage, the preferred rating is 25V or higher.

A C_{IN} = 22μF is suggested.

Output Capacitor Design

The output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

And the output voltage ripple can be calculated by:

$$\Delta V_O = \frac{V_{OUT}}{8LC_{OUT}f_S^2}\left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (7)$$

Increasing L or C_{OUT} (the LC filter) can reduce the ripple. The internal loop compensation of the device is optimized for > 20μF ceramic output capacitor. 10V, X7R (or X5R) ceramic capacitors are recommended for the output.

Input Power Supply Considerations

To power the system from the SGM41543/SGM41543D, either an input power source with a voltage range from 3.9V to 13.5V and at least 100mA current rating should power VBUS, or a single-cell Li-Ion battery with voltage higher than V_{BAT_UVLOZ} should be connected to BAT pin of the device. The input source must have enough current rating to allow maximum power delivery through charger (Buck converter) to the system.

APPLICATION INFORMATION (continued)

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.5MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. A graphical guideline for the current loops and their frequency content is provided in Figure 21. The following considerations can help to make a better layout.

1. Place the input capacitor between PMID and GND pins as close as possible to the chip with the shortest copper connections (avoid vias). Choose the smallest capacitor size.

2. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

3. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths short enough and on the same layer. A GND copper layer under the component layer helps to reduce noise emissions. Note that the DC current and AC current paths are in the layout and keep them short and decoupled as much as possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).

5. Place decoupling capacitors close to the IC pins with the shortest copper connections.

6. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

7. Select proper sizes for the vias and ensure that enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.

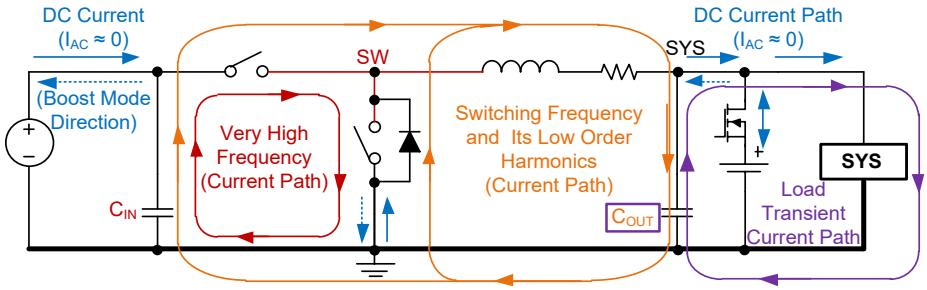


Figure 21. The Paths and Loops Carrying High Frequency, DC Currents and Very High Frequency (for Layout Design Consideration)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2023 – REV.A.2 to REV.A.3	Page
Updated Detailed Description section	All
Updated Electrical Characteristics section	10
Updated Functional Block Diagram section	16

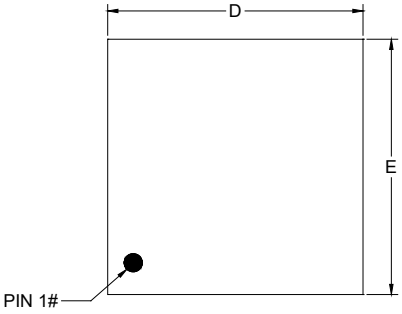
MAY 2023 – REV.A.1 to REV.A.2	Page
Updated Typical Application Circuits section	15

MARCH 2023 – REV.A to REV.A.1	Page
Updated Register Maps section	37

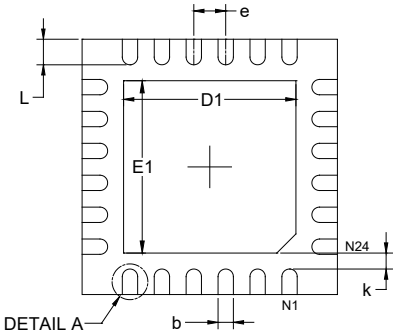
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

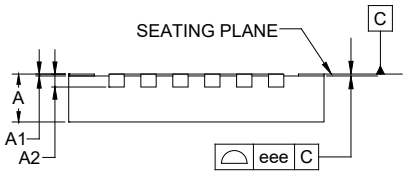
TQFN-4×4-24L



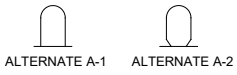
TOP VIEW



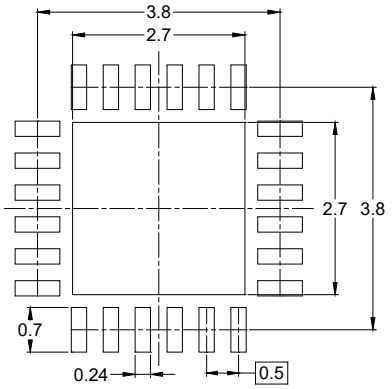
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



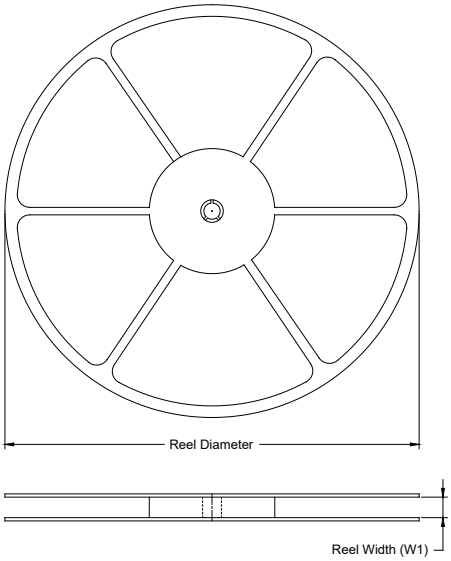
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e	0.500 BSC		
k	0.200 MIN		
L	0.300	-	0.500
eee	0.080		

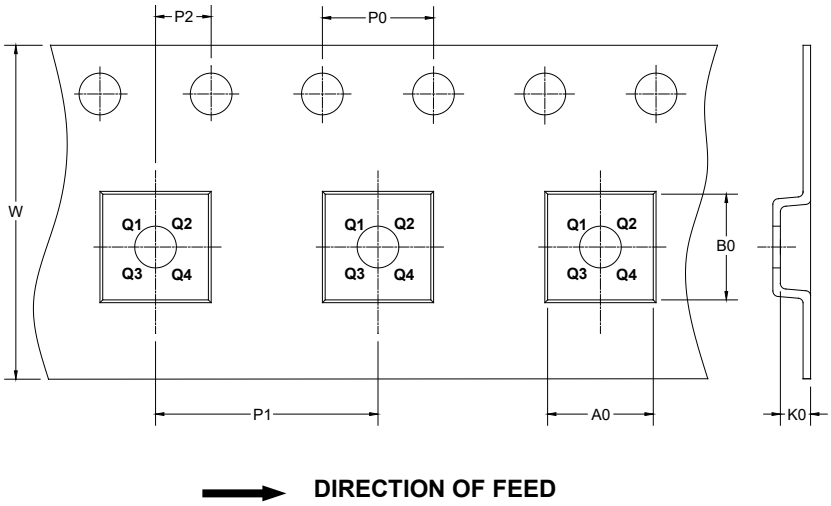
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



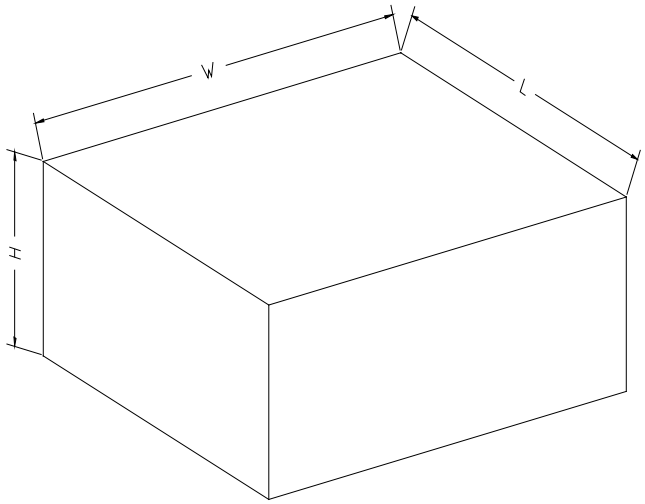
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002