SGM61310
4V to 36V Input, 1A Synchronous Buck Converter in SOT Package

GENERAL DESCRIPTION

The SGM61310 is a synchronous Buck converter with a wide input voltage range of 4V to 36V. This device can deliver up to 1A to the output over a wide input voltage. It is an easy-to-use device with power switches and peak current mode control compensation all integrated in a small 6-pin package. A typical 1.8ms soft-start ramp is also included to minimize the inrush current. This device can be easily used in various industrial applications powered from unregulated sources.

This device employs cycle-by-cycle peak current limit, output over-voltage protection and thermal shutdown with auto recovery. The current limit is implemented for switches to prevent overheating (and thermal shutdown) when an output short is detected. Auto recovery after over-current, output short, overheating or over-voltage fault maintains the system operational with no shutdown.

The SGM61310 operates at 700kHz switching frequency to support use of relatively small inductors for an optimized solution size. In light load condition, the SGM61310A enters in the pulse skip modulation (PSM) mode to improve high efficiency, while the SGM61310B works in the forced pulse width modulation (FPWM) mode to achieve low output ripple.

The SGM61310 is available in a Green SOT-23-6 package.

FEATURES

- **Documentation Available to Aid Functional Safety System Design**
- **Wide 4V to 36V Input Voltage Range**
- **Up to 1A Continuous Output Current**
- **Minimum Switching On-Time: 60ns**
- **700kHz Fixed Switching Frequency**
- **98% Maximum Duty Cycle**
- **Monotonic Startup with Pre-Biased Output**
- **Internal Short-Circuit Protection with Hiccup Mode**
- **Precision Enable**
- **Integrated Synchronous Rectification**
- **Internal Compensation for Ease of Use**
- **Pin-to-Pin Compatible with SGM61410 and SGM61306**
- **SGM61310A: PSM at Light Load Condition**
- **SGM61310B: FPWM at Light Load Condition**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Grid Infrastructure: Advanced Metering Infrastructure
Motor Drive: AC Inverters, VF Drives, Servos, Field Actuators
Factory and Building Automation: PLC, Industrial PC, Elevator Control, HVAC Control
Aftermarket Automotive: Camera
General Purpose Wide V_{IN} Power Supplies

TYPICAL APPLICATION

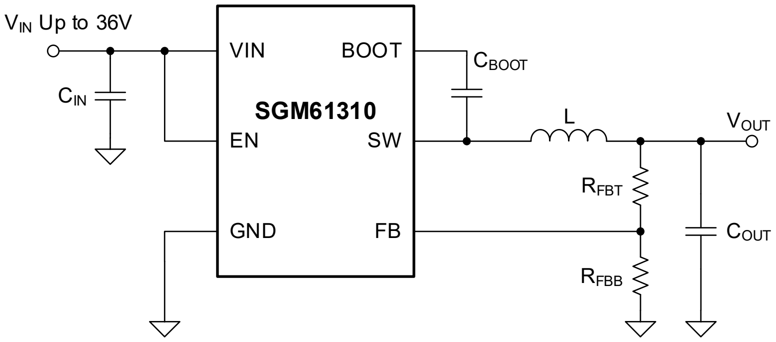


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61310A	SOT-23-6	-40℃ to +125℃	SGM61310AXN6G/TR	03UXX	Tape and Reel, 3000
SGM61310B	SOT-23-6	-40℃ to +125℃	SGM61310BXN6G/TR	03VXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

YYY X X

- X — Date Code - Week
- X — Date Code - Year
- YYY — Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages:
- VIN to GND .... -0.3V to 38V
- EN to GND .... -0.3V to (V_{IN} + 0.3V)
- FB to GND .... -0.3V to 5.5V

Output Voltages:
- SW to GND .... -0.3V to (V_{IN} + 0.3V)
- SW to GND (Less than 10ns Transient) .... -3.5V to 38V
- BOOT to SW .... -0.3V to 5.5V

Package Thermal Resistance
- SOT-23-6, θ_{JA} .... 134.3℃/W
- SOT-23-6, θ_{JB} .... 31℃/W
- SOT-23-6, θ_{JC} .... 77℃/W

Junction Temperature .... +150℃

Storage Temperature Range .... -65℃ to +150℃

Lead Temperature (Soldering, 10s) .... +260℃

ESD Susceptibility

HBM 2500V

CDM 750V

RECOMMENDED OPERATING CONDITIONS

Input Voltages:
- VIN to GND .... 4V to 36V
- EN .... 0V to V_{IN}

Output Current Range, I_{OUT} .... 0A to 1A

Operating Junction Temperature Range ...... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

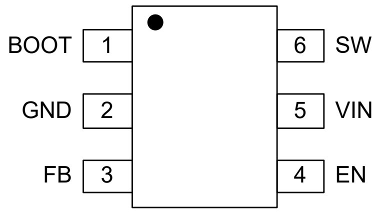
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOT-23-6

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	P	Bootstrap Pin. Place a 0.1μF capacitor (C_{BOOT}) between BOOT and SW pins close to the device to provide the required drive voltage for the high-side switch.
2	GND	G	Power Ground Terminals. It is connected to the source of low-side FET internally. Connect to system ground, ground side of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
3	FB	A	Feedback (Sense) Pin for Output Voltage and Programming. It is normally regulated at 1V. Tap an output feedback resistor divider to this pin.
4	EN	A	Precision Enable Input to the Converter. Do not float. Pull up to 1.23V (TYP) to enable the device or pull down to 1.1V (TYP) to disable it. Can be tied to VIN pin. Precision enable input allows adjustable UVLO by external resistor divider.
5	VIN	P	Input Supply Voltage Pin. VIN powers the internal control circuitry and the power converter. Decouple this pin for very high frequency and high di/dt transitions, with small and high frequency ceramic capacitors placed as close as possible between VIN and GND pins. Input under-voltage is protected by a UVLO comparator.
6	SW	P	Switching Node. Connection point of the internal converter lower and upper power MOSFETs. Connect this pin to the output inductor and the bootstrap capacitor.

NOTE: 1. A = analog, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4V to 36V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (VIN Pin)							
Under-Voltage Lockout Thresholds	V_{IN_UVLO}	Rising threshold		3.48	3.7	4	V
		Falling threshold		3.13	3.3	3.5	
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	Hysteresis			400		mV
Quiescent Supply Current (1)	I_Q	V_{EN} = 3.3V, V_{FB} = 1.1V, non-switching	SGM61310A		75	100	μA
			SGM61310B		1800	2100	
Shutdown Supply Current	I_{SD}	V_{EN} = 0V			3	6	μA
Enable (EN Pin)							
Enable Input High-Level for V_{OUT}	V_{EN_TH}	V_{EN} rising		1.15	1.23	1.32	V
Enable Input Low-Level for V_{OUT}	V_{EN_TL}	V_{EN} falling		1	1.1	1.2	V
Enable Input Hysteresis for V_{OUT}	V_{EN_HYS}	Hysteresis			130		mV
Enable Input Leakage Current	I_{LKG_EN}	V_{EN} = 3.3V			10		nA
Voltage Reference (FB Pin)							
Feedback Voltage (2)	V_{FB}			0.97	1	1.034	V
Feedback Leakage Current	I_{LKG_FB}	V_{FB} = 1.2V			0.2		nA
Current Limits and Hiccup							
High-side Current Limit	I_{SC}	V_{IN} = 12V		1.4	1.7	1.95	A
Low-side Current Limit	I_{LS_LIMIT}	V_{IN} = 12V		0.7	0.9	1.15	A
Zero Cross Detector Threshold	I_{L_ZC}	PSM variants only			0.02		A
Negative Current Limit	I_{L_NEG}	FPWM variants only			-0.6		A
MOSFETs							
High-side MOSFET On-Resistance	R_{DSON_HS}	T_J = +25℃, V_{IN} = 12V			480		mΩ
Low-side MOSFET On-Resistance	R_{DSON_LS}	T_J = +25℃, V_{IN} = 12V			265		mΩ
Thermal Shutdown							
Thermal Shutdown	T_{SD_RISING}	Shutdown threshold			170		℃
Thermal Shutdown Hysteresis	T_{HYS}				20		℃

NOTES:

1. This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
2. MIN and MAX limits are 100% production tested at +25℃ except for V_{FB}, which is tested at -40℃ to +125℃.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 4V to 36V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Characteristics						
Operating Input Voltage Range	V_{IN}		4		36	V
Adjustable Output Voltage Regulation (3)	V_{OUT}	PSM mode	-1.5%		2.5%	
Adjustable Output Voltage Regulation (3)	V_{OUT}	FPWM mode	-1.5%		1.5%	
Input Supply Current when in Regulation	I_{SUPPLY}	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, R_{FBT} = 1MΩ, PSM variant		94		μA
Maximum Switch Duty Cycle (4)	D_{MAX}			98%		
FB Pin Voltage Required to Trip Short-Circuit Hiccup Mode	V_{HC}			0.4		V
Switch Voltage Dead Time	t_D			6		ns

NOTES:

3. Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24V, I_{OUT} = 0A to full load.

4. In dropout, the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $f_{MIN} = 1/(t_{ON\_MAX} + t_{OFF\_MIN})$. $D_{MAX} = t_{ON\_MAX}/(t_{ON\_MAX} + t_{OFF\_MIN})$.

TIMING REQUIREMENTS

(V_{IN} = 4V to 36V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Switching On-Time	t_{ON_MIN}	I_{OUT} = 1A		60		ns
Minimum Switching Off-Time	t_{OFF_MIN}	I_{OUT} = 1A		100		ns
Maximum Switching On-Time	t_{ON_MAX}			7.5		μs
Internal Soft-Start Time	t_{SS}			1.8		ms
Time between Current-Limit Hiccup Burst	t_{HC}			135		ms

SWITCHING CHARACTERISTICS

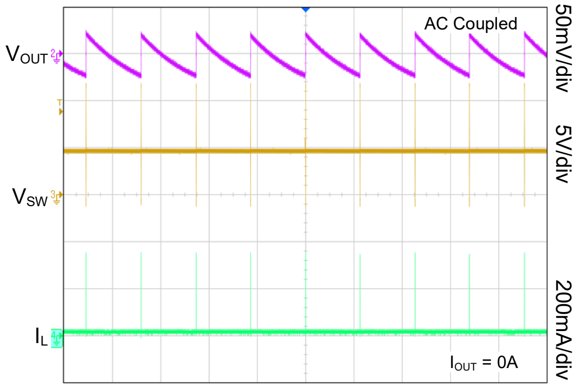
(V_{IN} = 4V to 36V, T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator						
Internal Oscillator Frequency	f_{OSC}			700		kHz

TYPICAL PERFORMANCE CHARACTERISTICS

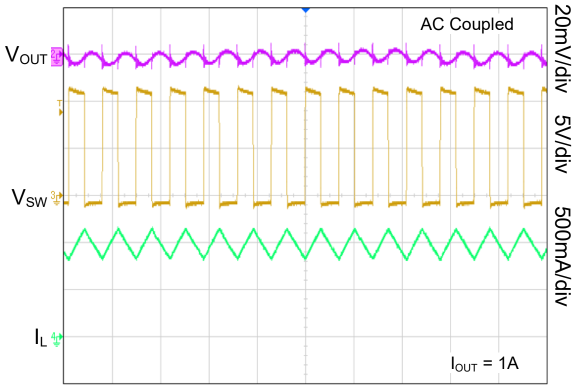
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 700kHz, L = 15μH, C_{OUT} = 22μF, unless otherwise noted.

Output Voltage Ripple



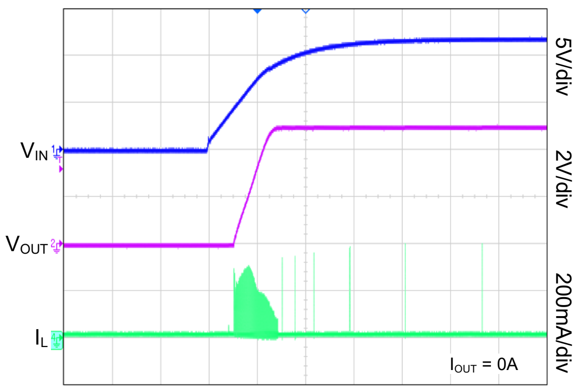
Time (10ms/div)

Output Voltage Ripple



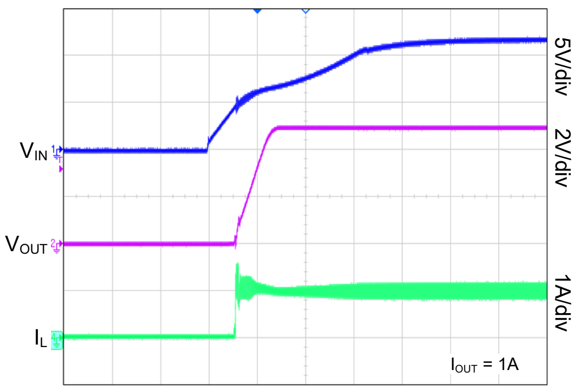
Time (2μs/div)

VIN Startup



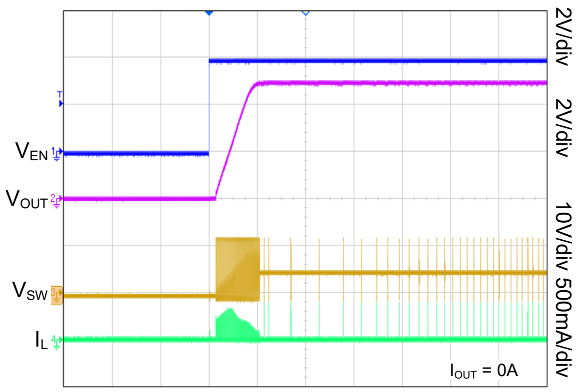
Time (2ms/div)

VIN Startup



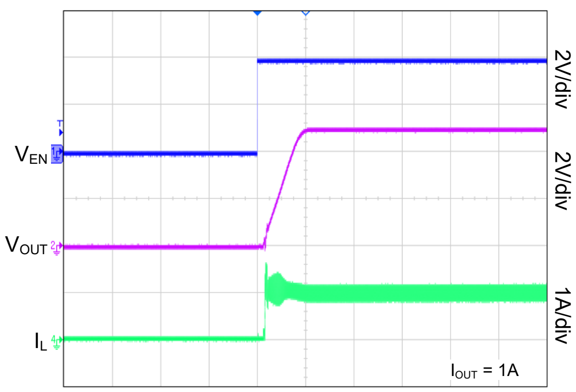
Time (2ms/div)

EN Startup



Time (2ms/div)

EN Startup

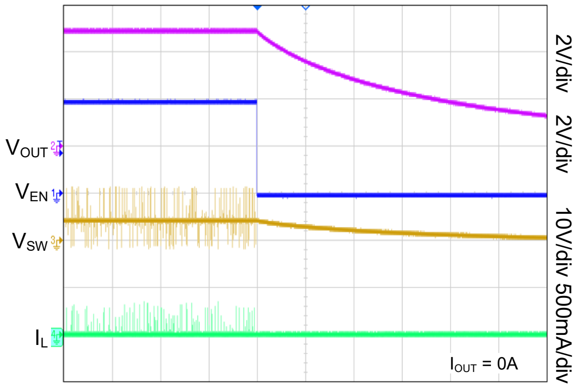


Time (2ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

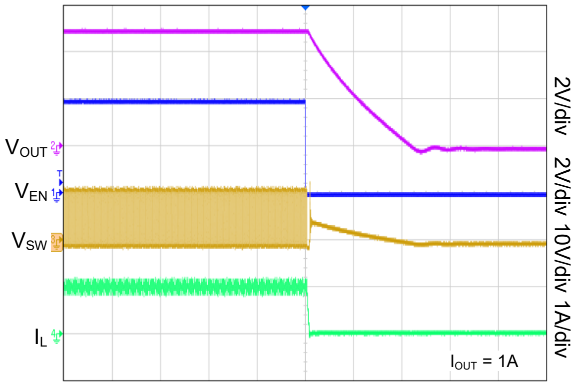
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 700kHz, L = 15μH, C_{OUT} = 22μF, unless otherwise noted.

EN Shutdown



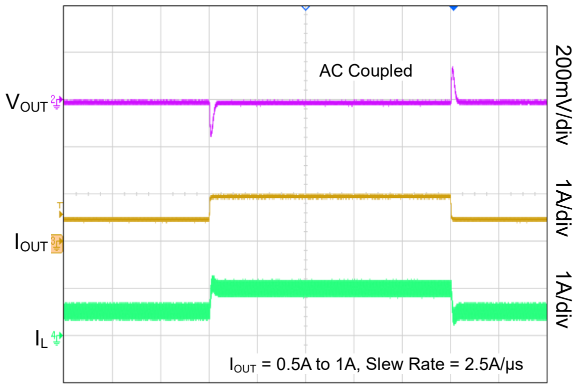
Time (500ms/div)

EN Shutdown



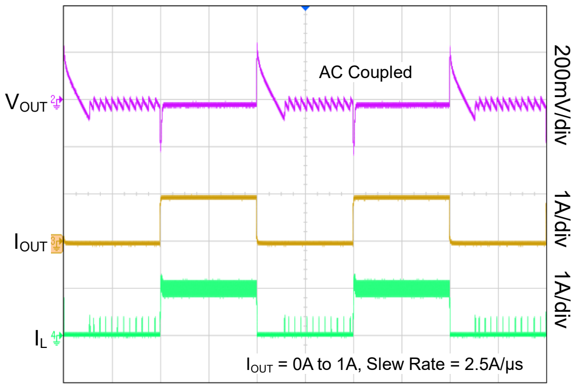
Time (50μs/div)

Load Transient



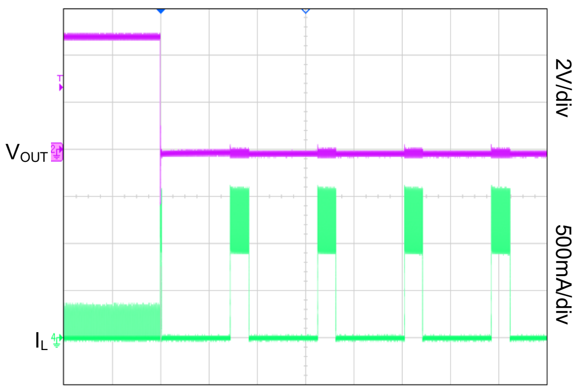
Time (200μs/div)

Load Transient



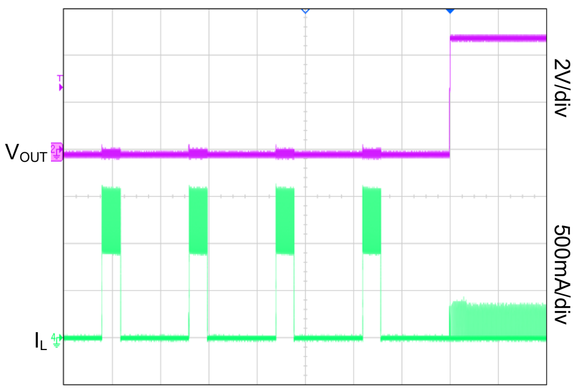
Time (500μs/div)

Short-Circuit Protection



Time (100ms/div)

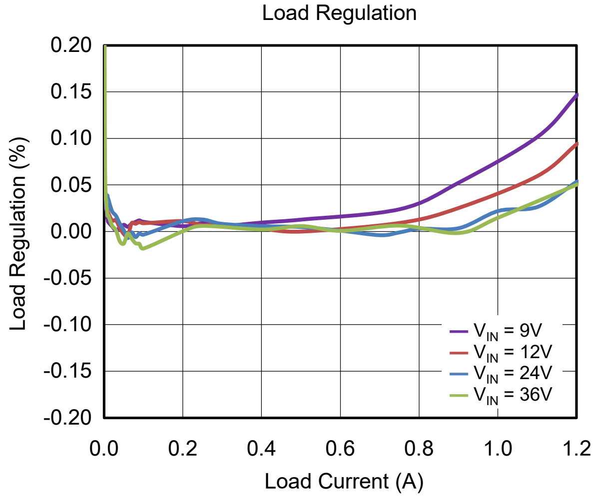
Short-Circuit Recovery

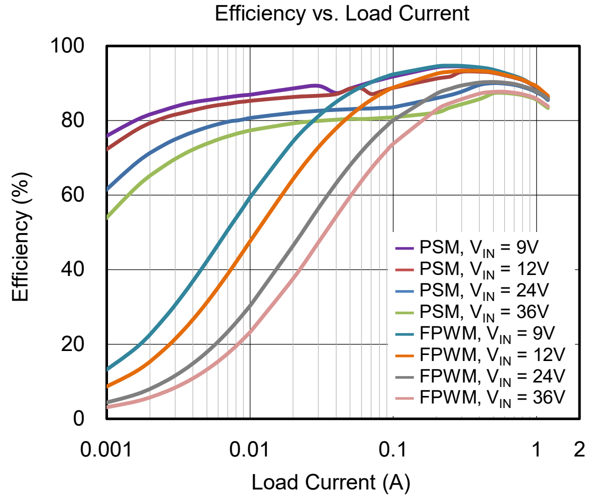


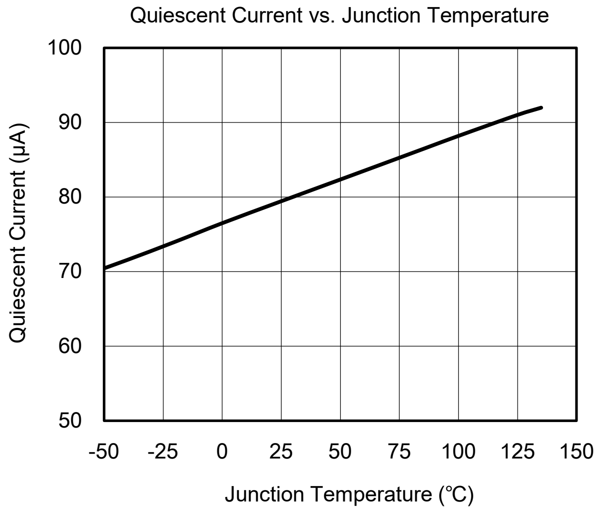
Time (100ms/div)

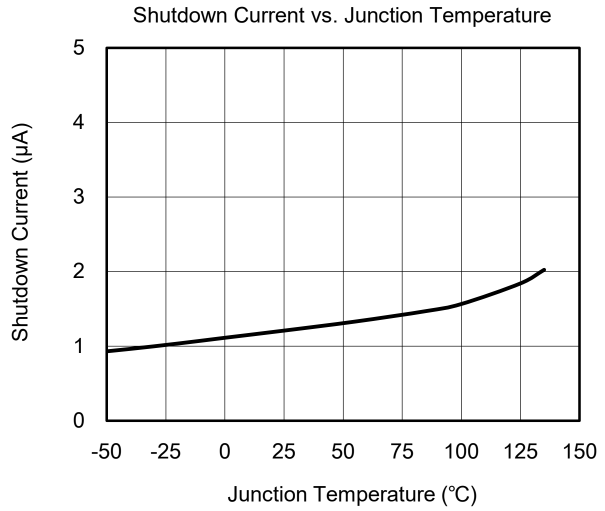
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

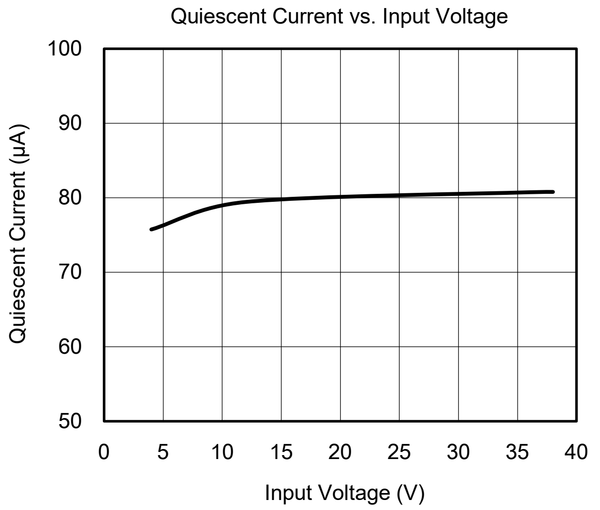
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 700kHz, L = 15μH, C_{OUT} = 22μF, unless otherwise noted.

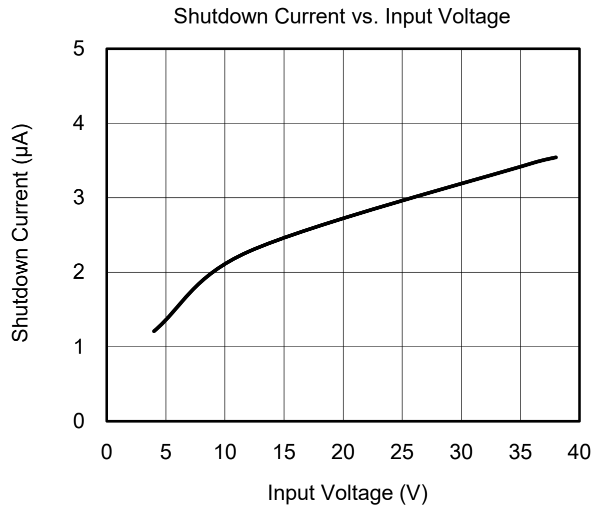






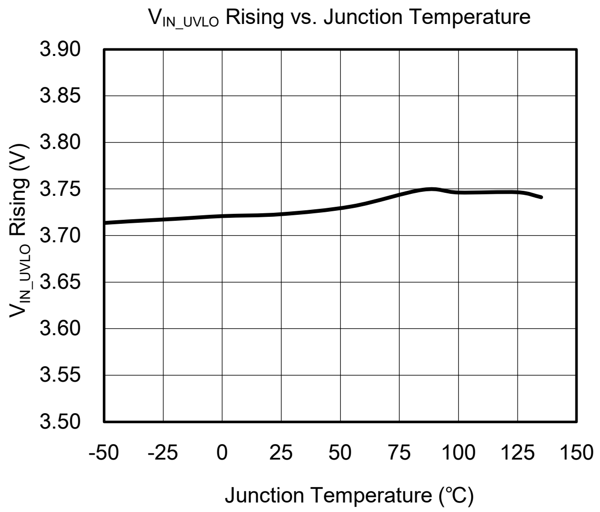


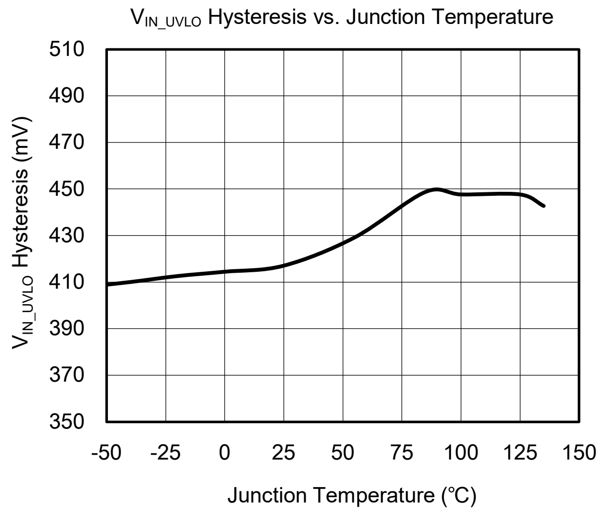


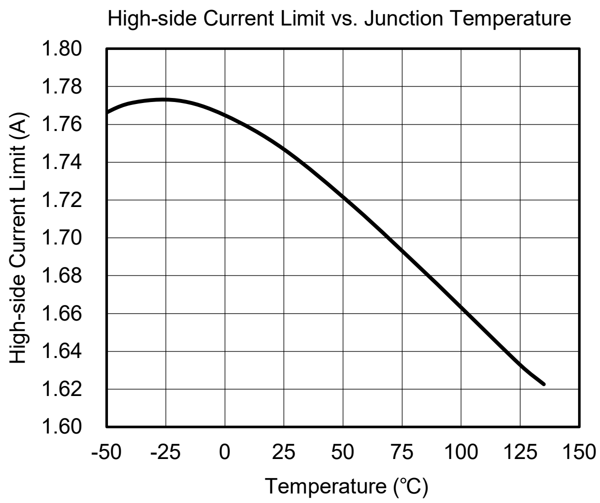


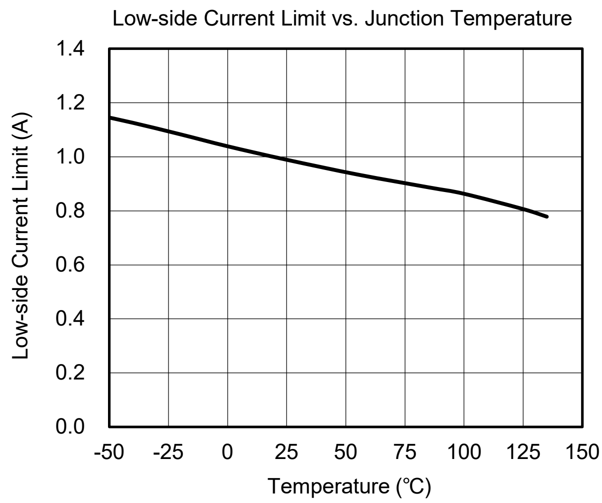
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

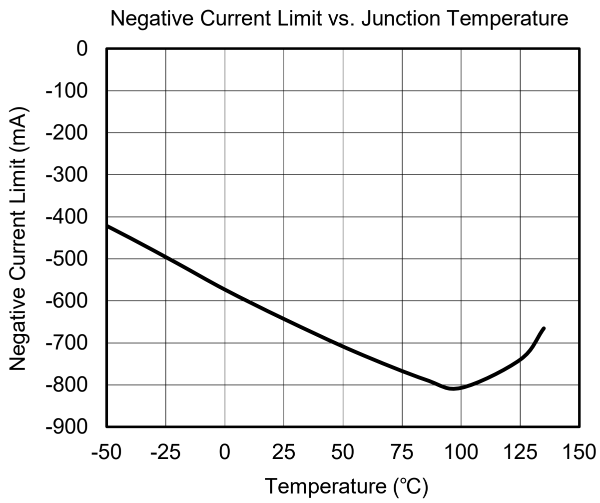
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 700kHz, L = 15μH, C_{OUT} = 22μF, unless otherwise noted.











FUNCTIONAL BLOCK DIAGRAM

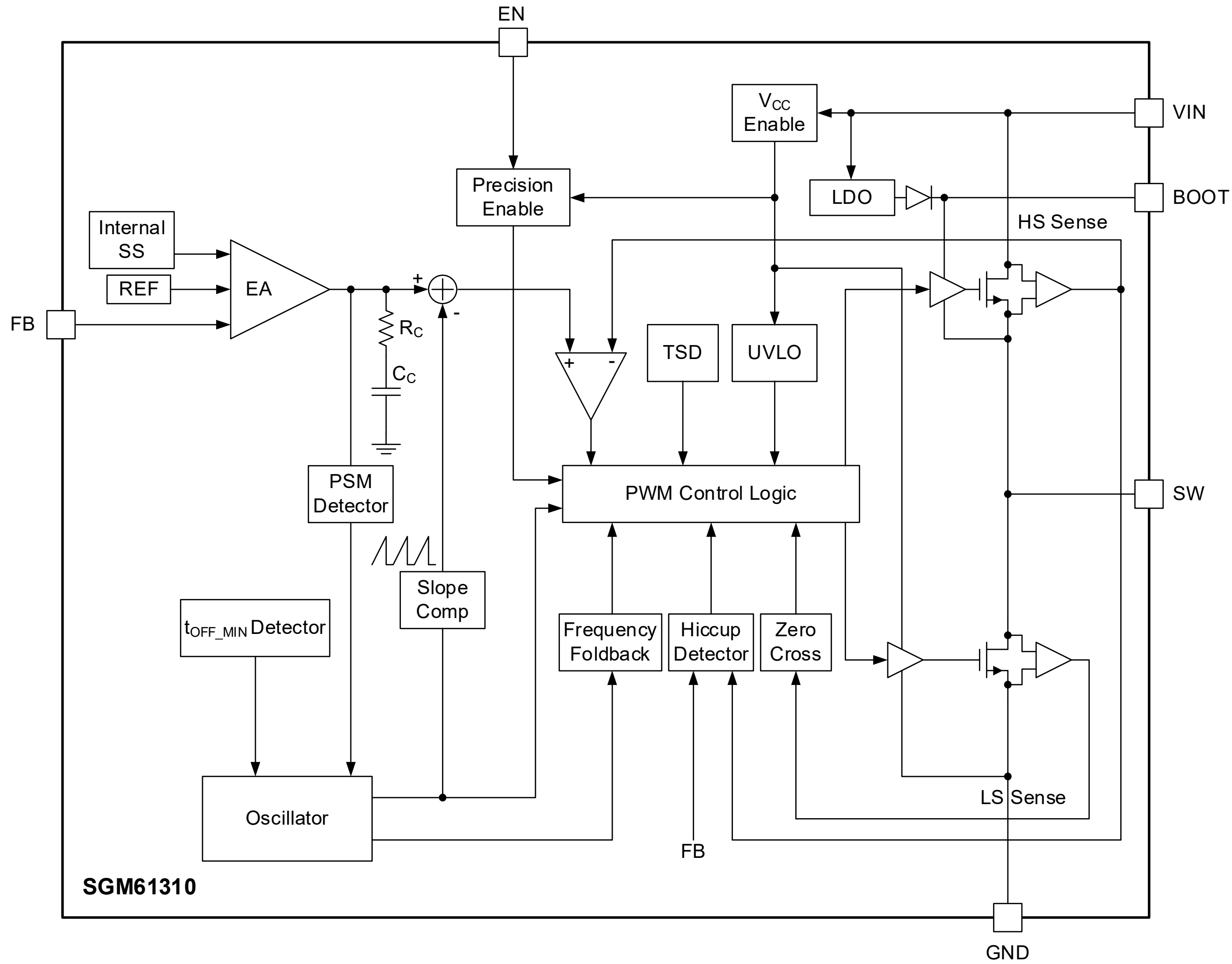


Figure 2. Block Diagram

DETALED DESCRIPTION

Overview

The SGM61310A and SGM61310B are 1A output synchronous Buck regulators with internal compensation and peak current mode control. They can operate from an input voltage range of 4V to 36V. These devices need a few external components and provide an easy and small size power supply solution for industrial applications with good thermal performance. With 75μA quiescent current and 3μA shutdown current, they are also well suited for battery-powered applications.

Both devices normally operate at fixed 700kHz frequency. At light load condition, the SGM61310A enters PSM mode to keep high efficiency. But the SGM61310B maintains FPWM mode to keep low output ripple and tight voltage regulation at light loads.

Accurate EN input threshold and internal soft-start time (1.8ms) add more design flexibility to these devices. Additional features such as thermal shutdown, input under-voltage lockout, cycle-by-cycle current limit, and short-circuit protection (hiccup mode) are also provided.

Switching Frequency and Current Mode Control

The Functional Block Diagram and basic waveforms of these Buck synchronous regulators are shown in Figure 2 and Figure 3. The N-MOSFETs are used for high-side (HS) and low-side (LS) (synchronous rectifier) switches. The HS duty cycle ($D = t_{ON}/t_{SW}$) is controlled in closed loop to regulate and maintain the output voltage at a constant level. The switching period is $t_{SW} = 1/f_{SW}$, and the HS on-time is t_{ON}. When HS is turned on, the SW node voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} - V_{OUT})/L slope. When HS is turned off, the LS is turned on after a very short dead time to avoid shoot-through, and I_L ramps down with -V_{OUT}/L slope. When the inductor current is continuous (either due to sufficient load, or FPWM), the output voltage is proportional to the input voltage and duty cycle ($V_{OUT} = D \times V_{IN}$) if component parasitics are ignored.

The output voltage is sensed by a resistor divider through FB pin and is regulated by feedback loop. This voltage is compared to an accurate reference and the voltage error signal is used as set point for an inner current loop that adjusts the peak inductor current. The input to the current loop is clamped to a fixed level to limit the maximum peak current and is compared to the actual peak current, sensed by the voltage drop across the HS switch to control the HS switch on-time. The loop internal compensation allows easy and stable design of the power supply with a few external elements for almost any output capacitor arrangement.

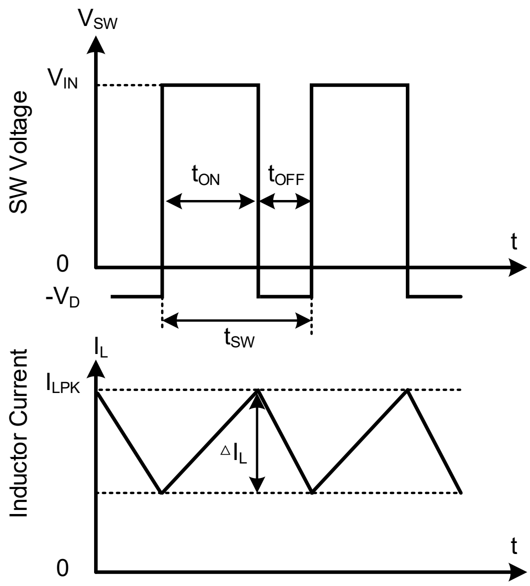


Figure 3. Converter Switching Waveforms in CCM

Output Voltage Setting

The output voltage can be stepped down to as low as the 1V reference voltage (V_{REF}). An external feedback resistor divider along with the internal reference is used to set the output voltage (V_{OUT}) as shown in Figure 4. The V_{REF} is compared to the V_{FB} voltage and the control loop adjusts the duty cycle to null the V_{REF} - V_{FB}.

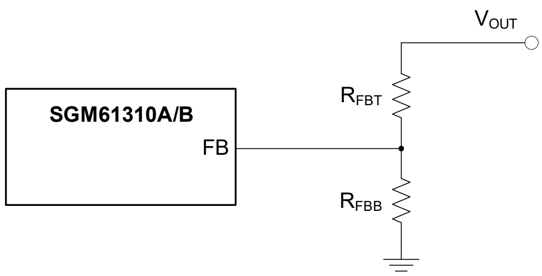


Figure 4. Output Voltage Setting

Use Equation 1 to calculate the output voltage:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

DETALED DESCRIPTION (continued)

Use 1% or higher quality resistors with low thermal tolerance for an accurate and thermally stable output voltage. The low-side resistor R_{FBB} is selected based on the desired current in the divider. Typically, a 10kΩ to 100kΩ resistor is selected for R_{FBB}. Lower R_{FBB} values increase loss and reduce light load efficiency. However, improve V_{OUT} accuracy in PSM. Large R_{FBT} values (> 1MΩ) are not recommended because the feedback path impedance will be too high and more noise sensitive. If a large R_{FBT} value is necessary, the PCB layout design will be more critical because the feedback path must be short and away from noise sources such as SW node or inductor body.

EN Input

The EN pin is an input and must not be left open. The simplest way to enable the device is to connect this pin to VIN pin via a resistor. This allows for self-startup of the SGM61310 when $V_{IN} > V_{UVLO}$. This pin can also be used to turn the device on or off with logic or analog signals. If V_{EN} < 1.1V (TYP), the device will shut down. Only if V_{EN} > 1.23V (TYP) the device will start operation. The system UVLO level can be increased accurately with a resistor divider (see Figure 5). This feature can be used for power supply sequencing which is required for proper power-up of the system voltage rails. It can also be used as protection, such as preventing supply battery from depletion. Control of the enable input by logic signals may also be used for sequencing or protection.

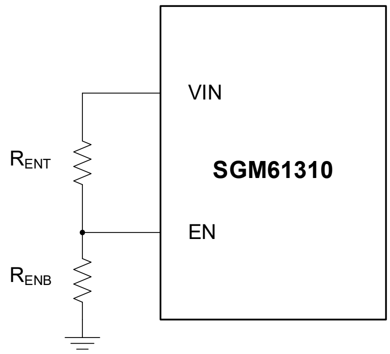


Figure 5. Changing the System UVLO

Minimum On-Time and Off-Time

The shortest duration for the high-side switch on-time (t_{ON_MIN}) is 110ns (TYP). For the off-time (t_{OFF_MIN}), the minimum value is 80ns (TYP). The duty cycle (or equivalently the V_{OUT}/V_{IN} ratio) range in CCM operation is limited by t_{ON_MIN} and t_{OFF_MIN} depending on the switching frequency. The minimum and maximum allowed duty cycles are given by Equations 2 and 3:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \tag{2}$$

$$D_{MAX} = 1 - (t_{OFF\_MIN} \times f_{SW}) \tag{3}$$

Note that the duty cycle has a more limited range at higher frequencies. D_{MAX} limits the lowest V_{IN} voltage for a given V_{OUT}.

For any given output voltage, the switching frequency is an important factor to maximize efficiency and input voltage range and minimize solution size. The highest input voltage can be calculated from:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \tag{4}$$

Due to losses in heavy load conditions, there is a small increase in duty cycle and the actual V_{IN_MAX} is higher than Equation 4 prediction.

The minimum V_{IN} is estimated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{ON\_MIN}} \tag{5}$$

Compensation and Feed-Forward Capacitor (C_{FF})

The SGM61310A/B is internally compensated (see Figure 2) and is stable over the entire f_{SW} and V_{OUT} operating range. However, the phase margin can be low for some ranges of V_{OUT} when low ESR ceramic capacitors are used in the output. In such cases, it is recommended to use a feed-forward capacitor (C_{FF}) in parallel with the R_{FBT} to improve the transient response as shown in Figure 6.

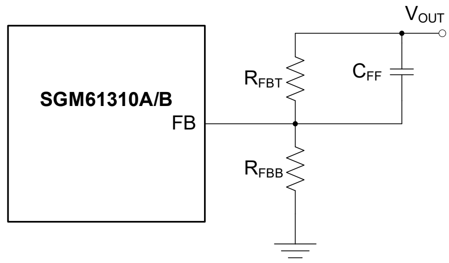


Figure 6. Improving Loop Compensation by Feed-Forward Capacitor

The C_{FF} in parallel with R_{FBT} places an additional zero before the loop cross over frequency and boosts the phase margin. The zero will be located at:

$$f_{Z\_CFF} = \frac{1}{2\pi \times C_{FF} \times R_{FBT}} \tag{6}$$

It also adds an extra pole after the zero at:

$$f_{P\_CFF} = \frac{1}{2\pi \times C_{FF} \times R_{FBT} \parallel R_{FBB}} \tag{7}$$

DETALED DESCRIPTION (continued)

While the zero increases the phase at the crossover frequency, the pole helps keeping the required gain margin after the crossover frequency.

If for similar C_{OUT} values, other R_{FBT} values are used, adjust the C_{FF} such that ($C_{FF} \times R_{FBT}$) is unchanged. C_{FF} must also be modified if C_{OUT} is changed. For C_{OUT} capacitors with lower ESR, larger C_{FF} values are needed. For example, with electrolytic capacitors (large ESR), the location of ESR zero, (Equation 8), is typically low enough for phase boost at crossover and C_{FF} is not needed.

$$f_{Z\_ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \quad (8)$$

Note that C_{FF} increases the feedback of the output ripple and the coupled noise to the FB node. A large C_{FF} value can deteriorate the V_{OUT} regulation. If significant derating for the C_{FF} value at cold operating temperatures is expected, it is better to use larger C_{OUT} capacitance rather than increasing the nominal C_{FF} value.

BOOT (Bootstrap Voltage)

The gate driver of the high-side N-MOSFET switch requires a voltage higher than V_{IN} that is present on its drain. A bootstrap voltage regulator is integrated to provide this voltage which is powered by bootstrapping through a small ceramic capacitor placed between the BOOT and SW pins. C_{BOOT} is charged in each cycle when the LS switch is turned on ($V_{SW} \approx 0V$) and discharges to the boot regulator when the HS switch is turned on ($V_{SW} \approx V_{IN}$). A 0.1μF ceramic capacitor with 16V or higher rated voltage is recommended.

Thermal Shutdown (TSD)

If the junction temperature exceeds +170℃ (TYP), the device will shut down. It will recover automatically with a normal power-up sequence and soft-start when the temperature falls below +150℃ (TYP).

Over-Current Protection and Short-Circuit Protection (Hiccup Mode)

Cycle-by-cycle current limit for both peak and valley currents (upper and lower switches peak currents) are included in the SGM61310A/B. If the OCP/SCP persists, it will enter hiccup mode to avoid thermal shutdown. The HS switch over-current protection is natural in peak current mode control. In each cycle, the HS current sensing starts a short time (blanking time) after it is turned on. The slope compensation ramp is deducted from the EA (Error Amplifier) output to avoid subharmonic oscillations and the result is compared to the HS current to determine the HS turn-off time (on-time). See Figure 2 for details. Before comparison, the EA output is clamped to a fixed maximum threshold (I_{HS_LIMIT}) to limit the current. So, the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

When the LS switch is turned on, the inductor current starts falling. The LS current is sensed while it is on and the switch will not be turned off at the end of cycle if this current is still higher than its limit (I_{LS_LIMIT}) and keeps conducting until the current falls below I_{LS_LIMIT}. Hiccup mode is considered to protect the device from overheating and damage in severe over-current conditions.

Functional Modes

Shutdown Mode

The EN input controls the device ON/OFF condition. If V_{EN} < 1.1V (TYP), the device will shut down. The device will also turn off if either V_{IN} falls below its UVLO threshold.

Active Mode

If V_{EN} is above its precision threshold, and V_{IN} is above its UVLO levels, the device will be activated. EN pin can be connected to V_{IN} to allow self-startup when V_{IN} voltage is in the 4V to 36V operating range. UVLO and EN settings in active mode are explained in the previous sections. Four operating modes are possible depending on the load current (ΔI_L = inductor peak-to-peak current ripple):

1. CCM: Fixed frequency continuous conduction mode: both SGM61310A and SGM61310B operate in CCM when $I_{OUT} > \Delta I_L/2$.

2. DCM: Fixed frequency discontinuous conduction mode: only for SGM61310A (PSM), the switching frequency does not change when $I_{OUT} < \Delta I_L/2$.

3. PSM: Pulse skip modulation mode (SGM61310A only): the switching frequency reduces at very light load operation, when the EA (Error Amplifier) output falls below V_{PSM}.

4. FPWM: Forced pulse width modulation mode for SGM61310B only: it operates with fixed frequency at light load operation.

Continuous Conduction Mode (CCM)

In CCM operation, the frequency is fixed and the output voltage ripple will be minimal. The maximum output current of 1A is supplied in CCM operation.

DETALED DESCRIPTION (continued)

Light Load Operation with PSM (SGM61310A)

If the output current of the SGM61310A falls below $\Delta I_L/2$, its operating mode changes to DCM (also called diode emulation mode or DEM). In DCM, the LS switch is turned off when its current reverses direction and drops to I_{L_ZC} (I_{L_ZC} = 20mA TYP). Switching and conduction losses in DCM are lower than FPWM operation at light load condition, even before entering PSM. At light load condition, the device enters PSM to keep its high efficiency. PSM mode is activated when the EA (Error Amplifier) output falls below V_{PSM}. In PSM, f_{SW} is reduced to maintain regulation. With reduced frequency, the switching losses are also dropped and efficiency is improved.

Light Load Operation with FPWM (SGM61310B)

For FPWM option, SGM61310B is locked in PWM mode from full load to no load. Negative inductor currents are allowed at light load to continue PWM operation. It is a tradeoff that sacrifices light load efficiency for lower output ripple, better output regulation and keeping witching frequency fixed. To avoid fatal negative current in the LS switch, this current is limited at I_{L_NEG} (I_{L_NEG} = -630mA TYP).

APPLICATION INFORMATION

The design method for the SGM61310A/B Buck converters is explained in this section. Schematic of a basic design is shown in Figure 7. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

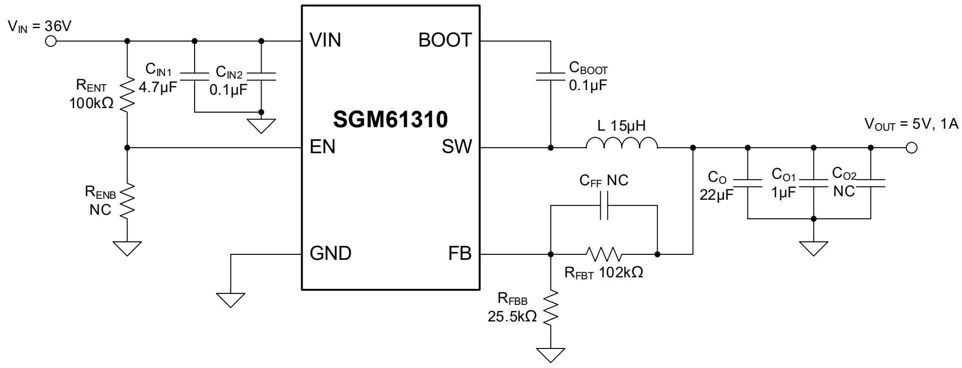


Figure 7. SGM61310 Basic Application Schematic

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_O) values are provided in Table 1 to simplify component selection. Consider the following notes when using this table.

1. Choose the inductance for V_{IN} = 36V.
2. C_O values in the table are actual derated values. Use higher nominal values for ceramic capacitors.
3. Left R_{FBB} floating to set V_{OUT} = 1V.
4. If any other R_{FBT} value is designed, resize C_{FF} to keep (C_{FF} × R_{FBT}) unchanged if C_{FF} is needed.
5. If the selected output capacitance has high ESR, the C_{FF} is not necessary for extra phase boost.

Table 1. Some Typical L, C_{OUT} Values for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
700	3.3	10	22	51.7	22.1
700	5	15	22	102	25.5
700	24	27	4.7	230	10

Design Requirements

The design process will be explained by an example with the required input parameters listed in Table 2.

Table 2. Design Example Parameters

Design Parameter	Example Value
Input voltage, V_{IN}	12V (TYP), range from 6V to 36V
Output voltage, V_{OUT}	5V
Maximum output current, I_{OUT_MAX}	1A
Output overshoot/undershoot (0A to 1A)	5%
Output voltage ripple	50mV
Operating frequency	700kHz

Output Voltage Setting

An external resistor divider is used to set the output voltage as shown in Figure 6. Use Equation 9 to set V_{OUT}:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{9}$$

where V_{REF} = 1V is the internal reference. For example, by choosing R_{FBB} = 25.5kΩ, the R_{FBT} value for 5V output will be calculated as 102kΩ.

Switching Frequency

The SGM61310A/B switching frequency is 700kHz (TYP). It may also drop due to frequency foldback when the duty cycle reaches its maximum or due to PSM operation.

Inductor

Three main inductor parameters that need to be designed are inductance, saturation current and rated current. The DCR is also an important factor for efficiency. Physical dimensions, form factor and shielded or non-shielded structure are other important factors that are selected based on the application. The inductance is designed by selecting the peak-to-peak current ripple (ΔI_L) that is given by Equation 10. ΔI_L is increased at higher input voltages, so V_{IN_MAX} is used in the equation. The minimum required inductance (L_{MIN}) is calculated from Equation 11. K_{IND} represents the ratio of inductor ripple current to the maximum output current (K_{IND} =$\Delta I_L/I_{OUT\_MAX}$). It is typically chosen between 20% to 40%.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{10}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{11}$$

APPLICATION INFORMATION (continued)

During a short or over-current, either RMS or peak inductor current can increase significantly. The inductor rated RMS and saturation current ratings should be higher than those peaks respectively. It is generally desired to choose a smaller inductance value to have faster transient response, smaller size, and lower DCR. However, reducing the inductance increases the current ripple that may result in over-current detection and triggering OCP before reaching full load current. Moreover, higher current ripple increases core, conduction, and capacitor losses. Output voltage ripple will also be higher with the same output capacitance. In general, choosing a too small inductance is not recommended for peak current mode control. On the other hand, too large inductance is also not recommended, because the reduced current ripple degrades the comparator signal to noise ratio. Selecting K_{IND} = 0.4 results in L_{MIN} = 15.3μH. A 15μH ferrite inductor with 2.1A RMS rating and 2.5A saturation current is selected as the closest standard value.

Output Capacitor

The main factors for designing C_{OUT} are output voltage ripple, control loop stability and the magnitude of output voltage overshoot/undershoot after a load transients.

The output voltage ripple has two main components. One is due to the AC current (ΔI_L) going through the capacitor ESR:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = I_{OUT} \times K_{IND} \times ESR \tag{12}$$

And the other one is caused by the charge and discharge of capacitor by the AC current (ΔI_L):

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{13}$$

These AC components are not in phase and the total peak-to-peak ripple is less than $\Delta V_{OUT\_ESR} + \Delta V_{OUT\_C}$.

In many applications, tight regulation in response to large and fast load transients is required. This can be a more severe condition on designing C_{OUT} value. Typically the control loop recovers the output voltage after four or five cycles and C_{OUT} should be large enough to provide the difference between current received from inductor and the current delivered to the load during this period. The minimum capacitance needed to limit the undershoot to V_{US} when the load steps up from I_{OL} to I_{OH} is given in Equation 14. Similarly, when the load steps from I_{OH} down to I_{OL}, C_{OUT} should be large enough to absorb the extra energy coming from the inductor without a large voltage overshoot (V_{OS}) as calculated in Equation 15:

$$C_{OUT} > \frac{4 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \tag{14}$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L \tag{15}$$

In this example, maximum acceptable ripple is 50mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50mV and K_{IND} = 0.4. Equation 12 results in ESR < 125mΩ and Equation 13 leads to C_{OUT} > 2.86μF. If the overshoot/undershoot transient requirement is 5% then $V_{US} = V_{OS}$ = 5% × V_{OUT} = 250mV. Equation 14 and 15, lead to C_{OUT} > 22.86μF and C_{OUT} > 5.85μF respectively. Now considering all conditions and including voltage derating of the ceramic capacitors, C_{OUT} is composed of a 22μF/16V ceramic capacitor parallel with a 1μF/16V ceramic capacitor.

Designing Feed-Forward Capacitor

Even though the SGM61310A/B is internally compensated, with low ESR ceramic capacitors, the phase margin can be low depending on the V_{OUT} and f_{SW} values. By adding an external feed-forward capacitor (C_{FF}) in parallel with the R_{FBT}, the phase margin can be improved (phase boost around crossover frequency). Without C_{FF}, and if ESR is very small, the crossover frequency (f_X) can be estimated from Equation 16, in which C_{OUT} is the actual derated value:

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \tag{16}$$

Then C_{FF} value can be estimated from:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \tag{17}$$

For slightly larger ESR values, choose a C_{FF} value that is less than that estimated by Equation 17. For larger ESR values, C_{FF} is not needed.

Input Capacitor

High frequency decoupling on the input supply pins is necessary for the device. A bulk capacitor may also be needed in some applications. Typically, 4.7μF to 10μF high quality ceramic capacitor (X5R, X7R or better) with voltage rating twice the maximum input voltage is recommended for decoupling capacitor. If the source is away from the device (> 5cm), some bulk capacitance is also needed to damp the voltage spikes caused by the wiring or PCB trace parasitic inductances. In this example, 4.7μF/50V/X7R capacitors and a 0.1μF ceramic capacitor placed right beside the device V_{IN} and GND pins for very high-frequency filtering are used.

Bootstrap Capacitor

A 0.1μF/16V/X5R or X7R ceramic capacitor is recommended for C_{BOOT}.

APPLICATION INFORMATION (continued)

V_{IN} UVLO Adjustment

The system UVLO threshold can be increased using two external resistors R_{ENT} and R_{ENB} (see Figure 5) to form a voltage divider between VIN and EN pins. The UVLO comparator provides a rising threshold (power-up) and a falling threshold (power-down) for V_{IN}. Use Equation 18 to set the UVLO rising threshold.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (18)$$

V_{ENH} is the EN rising threshold (1.23V TYP). Choose a large value for R_{ENB} (e.g., 100kΩ), to minimize supply drain. The R_{ENT} value is given by:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1\right) \times R_{ENB} \quad (19)$$

The resulting falling threshold can be calculated from:

$$V_{IN\_RISING} = \left(V_{ENH} - V_{EN\_HYS}\right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (20)$$

In which the V_{EN_HYS} is 0.13V (TYP).

In this example, V_{IN_RISING} = 6.0V is needed that results in R_{ENT} = 387kΩ and a UVLO falling threshold of 5.36V.

Layout

Consider the following layout design guidelines for a high-quality power supply with good thermal and EMI performances.

1. Place C_{INx} as close as possible to the V_{IN} and PGND pins. C_{INx} and C_{Ox} return should be close together and connected on the top layer PGND pin/plane and pad.

2. Minimize FB trace length and keep both feedback resistors close to the FB pin. Bring the V_{OUT} sense trace from the point where V_{OUT} accuracy is important and keep it away from the noisy nodes (SW), preferably through another layer that is on the other side of a shield layer. Place C_{FF} close to R_{FBT}.

3. Use one of the mid-layers as ground plane for noise shielding and extra path for heat dissipation.

4. Connect the ground layer to only one ground point on the top layer. The feedback and enable circuit returns must be routed separately through the ground plane to avoid large load currents or high di/dt switching currents to flow in these sensitive analog ground traces. Bad grounding results in poor regulation and erratic output ripple.

5. Choose wide traces for V_{IN}, V_{OUT} and ground to minimize voltage drops and maximize efficiency.

6. Use an array of thermal vias (e.g., 6 filled vias) under the exposed pad and connect them to the ground planes on mid-layers and the bottom layer. Maximize the heat sinking copper areas and solidify them with metal coatings such that the die temperature remains below +125℃ in all operating conditions.

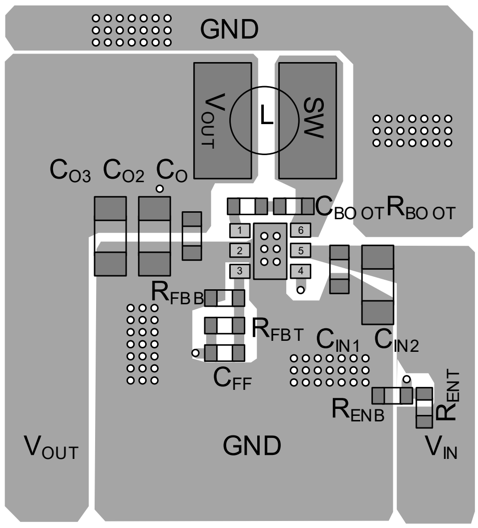


Figure 8. Top Layer

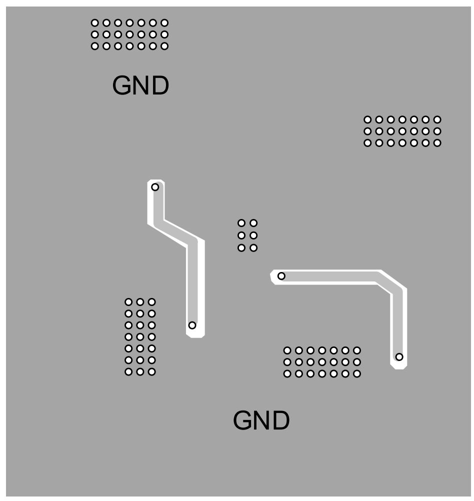


Figure 9. Bottom Layer

REVISION HISTORY

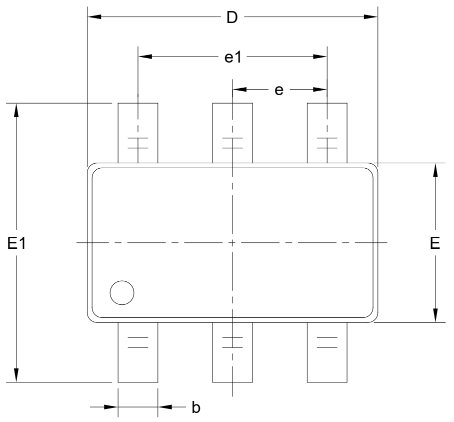
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

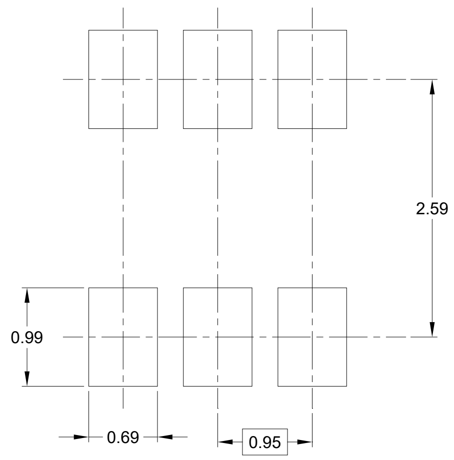
JULY 2024 – REV.A to REV.A.1	Page
Updated Package Thermal Resistance	2

Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

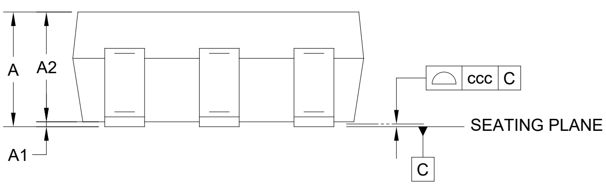
PACKAGE OUTLINE DIMENSIONS

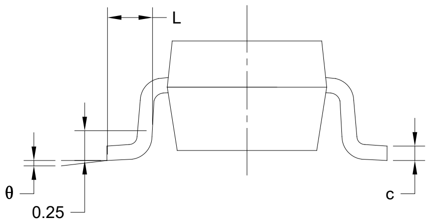
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



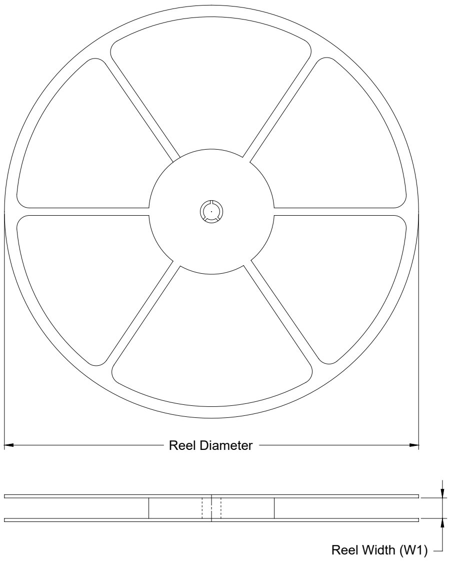


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

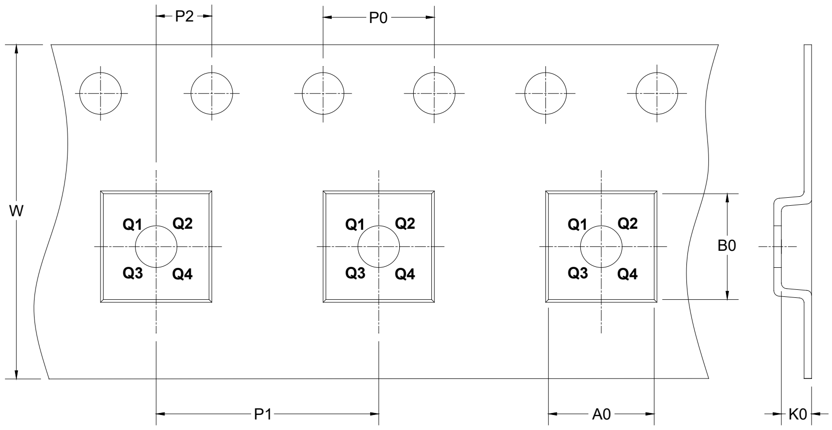
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

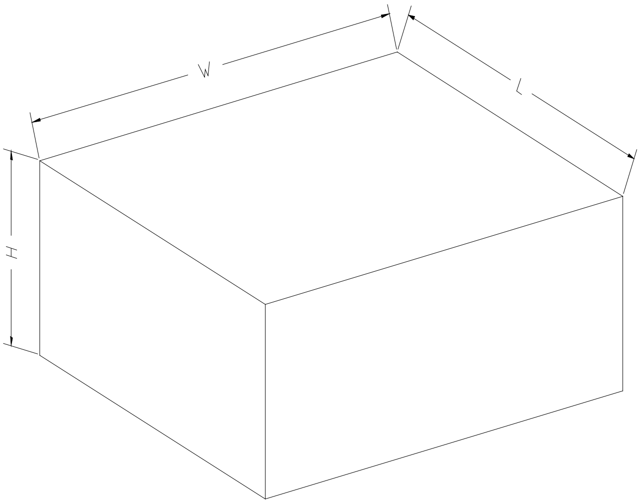
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002