SGM40666AS/SGM40666BS
High-Current Over-Voltage Protector

GENERAL DESCRIPTION

The SGM40666AS and SGM40666BS are over-voltage protection devices designed to protect low voltage systems from damage with a high voltage supply up to +31V_{DC} and +40V_{PEAK} (10s with 50mA current limit). The SGM40666AS withstands +90V/-400V while the SGM40666BS can also withstand surges up to +80V/-400V without damage.

The integrated 27mΩ (TYP) R_{ON} FET allows it to pass through 4.5A continuous current. The FET is turned off when the input voltage exceeds the over-voltage threshold, which can be adjusted between 4V and 22V with the optional external resistors.

When the OVLO input is set below the external OVLO select threshold (0.26V TYP), the SGM40666AS and SGM40666BS automatically choose the internal trip thresholds that are preset to 6.79V typically. SGMICRO provides customized OVP threshold options for 22.2V/15.3V/10.5V/6.35V/5.95V. Please contact us if necessary.

The open-drain output (nACOK) indicates a stable power supply between minimum V_{IN} and V_{OVLO}.

The SGM40666AS and SGM40666BS are available in a Green WLCSP-1.65×1.24-12B package.

FEATURES

- **Wide Power Supply Voltage Range: 2.5V to 28V**
- **Input Voltage up to 40V with 50mA Current Limit for 10s Duration**
- **Integrated Switch On-Resistance: 27mΩ (TYP)**
- **Wide Adjustable OVLO Threshold Range: 4V to 22V**
- **Internal Over-Voltage Protection Threshold: 6.79V (TYP)**
- **Surge Immunity**
  - **SGM40666AS: Up to +90V/-400V Surge Immunity**
  - **SGM40666BS: Up to +80V/-400V Surge Immunity**
- **32.3V Clamping Circuit Trigger Threshold when Rising Slope > 4.5V/μs (SGM40666AS)**
- **45V Clamping Circuit Trigger Threshold (SGM40666BS)**
- **Over-Voltage Shutdown Response: 50ns (TYP)**
- **Start-Up Debounce Time: 16.5ms**
- **Soft-Start Function**
- **Enable Function**
- **Thermal Shutdown Protection**
- **Power Good Flag**
- **Available in a Green WLCSP-1.65×1.24-12B Package**

APPLICATIONS

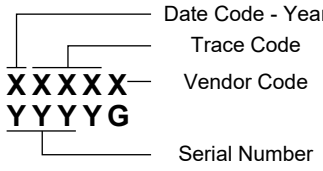
Battery Charging Ports
Mobile Phones
Tablet Computers

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40666AS	WLCSP-1.65×1.24-12B	-40℃ to +85℃	SGM40666ASYG/TR	XXXXX MDLYG	Tape and Reel, 3000
SGM40666BS	WLCSP-1.65×1.24-12B	-40℃ to +85℃	SGM40666BSYG/TR	XXXXX G5YYG	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- IN ..... -0.3V to 31V (1)
- IN (Peak for 10s Duration, 50mA Limit) ..... -0.3V to 40V (1)
- OUT ..... -0.3V to V_{IN} + 0.3V
- OVLO ..... -0.3V to 25V
- nACOK, nEN ..... -0.3V to 6V

IN, OUT Continuous Current 4.5A (2)
IN, OUT Peak Current (10ms) 8A
Package Thermal Resistance
- WLCSP-1.65×1.24-12B, θ_{JA} ..... 66.2℃/W
- WLCSP-1.65×1.24-12B, θ_{JB} ..... 12.8℃/W
- WLCSP-1.65×1.24-12B, θ_{JC} ..... 31.3℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4kV
CDM 1kV
Air Gap Discharge on IN Pin (IEC 61000-4-2) 20kV
Contact Discharge on IN Pin (IEC 61000-4-2) 12kV

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.5V to 28V (3)
Operating Junction Temperature Range ..... -40℃ to +125℃

NOTES:
1. Non-frequent repeated peak voltage during the input surge transient and ESD transient is not subject to this rating value, which may be higher than 40V in the surge test.
2. Continuous current limit may vary with the circuit board thermal dissipation condition.
3. If protection discharging is triggered, the discharging keeps until the supply falls below the hysteresis range. Continuously force driving during discharging with a voltage in the hysteresis range can cause overstress and even damage the device. Supply voltage within the hysteresis range is not recommended.

ESD SENSITIVITY CAUTION

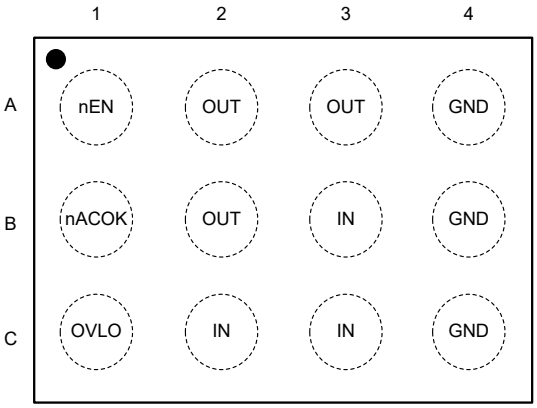
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.65×1.24-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	nEN	Device Enable Pin. Active low to enable the IN to OUT pass path.
A2, A3, B2	OUT	Output Pin. Internal switch output.
A4, B4, C4	GND	Ground.
B1	nACOK	Open-Drain Flag Output for Power Good. When the input voltage is stable between the minimum V_{IN} and V_{OVLO}, nACOK is driven low. nACOK is high impedance if thermal shutdown occurs.
B3, C2, C3	IN	Input and Device Supply Pin. Use a 0.1μF ceramic capacitor near to the device.
C1	OVLO	Over-Voltage Protection Threshold Adjustment. When the internal threshold is used, set the OVLO to connect to GND. Connect to a resistor divider network to adjust the OVLO threshold.

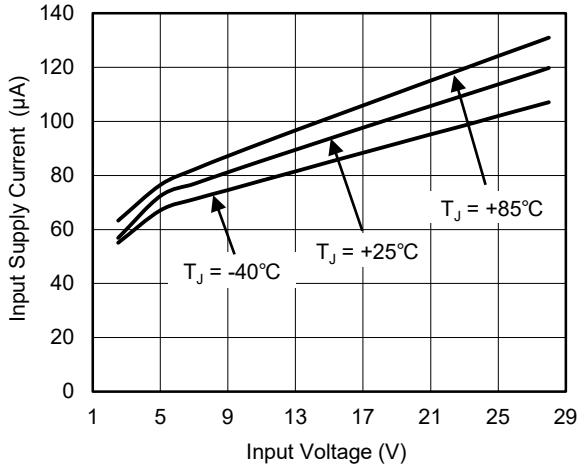
ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V to 28V, C_{IN} = 0.1μF, T_J = -40℃ to +85℃, typical values are at V_{IN} = 5V, I_{IN} ≤ 3A, T_J = +25℃, unless otherwise noted.)

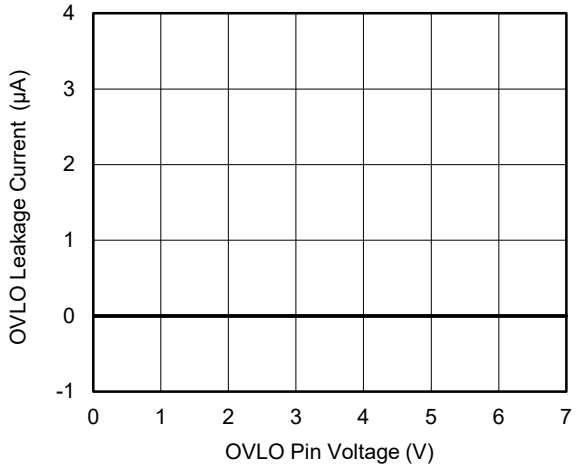
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.5		28	V
Input Supply Current	I_{IN}	V_{IN} = 5V		75	105	μA
OVLO Supply Current	I_{IN_Q}	V_{OVLO} = 3V, V_{IN} = 5V, V_{OUT} = 0V		80	110	μA
Internal Over-Voltage Protection Threshold	V_{IN_OVLO}	V_{IN} rising	6.63	6.79	6.95	V
		V_{IN} falling	6.58	6.70		
V_{BG} Reference	V_{BG}		1.163	1.191	1.220	V
Adjustable OVLO Threshold Range			4		22	V
External OVLO Select Threshold	V_{OVLO_SELECT}		0.24	0.26	0.29	V
Switch On-Resistance	R_{ON}	V_{IN} = 5V, I_{OUT} = 0.5A, T_J = +25℃		27	37	mΩ
OUT Load Capacitance	C_{OUT}	V_{IN} = 5V, T_J = +25℃			1000	μF
OVLO Parasitic Capacitance	C_{P_OVLO}	T_J = +25℃		24		pF
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO} = 1.3V, T_J = +25℃	-100		100	nA
IN Leakage Voltage by OVLO	V_{IN_LEAK}	V_{OVLO} = 20V, V_{IN} = unconnected, R_{OVLO} = 1MΩ			0.2	V
Thermal Shutdown				150		℃
Thermal Shutdown Hysteresis				20		℃
Digital Signal (nACOK, nEN)						
nACOK Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA, see Figure 1		0.08	0.32	V
nACOK Leakage Current	I_{ACOK_LEAK}	$V_{I/O}$ = 3.3V, nACOK de-asserted, T_J = +25℃, see Figure 1			1	μA
nEN Input Low Threshold	V_{LTH}				0.4	V
nEN Input High Threshold	V_{HTH}		1.2			V
nEN Input Leakage	I_{nEN_LEAK}	V_{IN} = 5V, T_J = +25℃			1	μA
Timing Characteristics						
Debounce Time	t_{DEB}	Time from V_{IN} > 2.5V to the time V_{OUT} starts rising, T_J = +25℃		16.5		ms
Soft-Start Time	t_{SS}	Time from V_{IN} > 2.5V to soft-start off, T_J = +25℃		33		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, C_{LOAD} = 10μF, V_{OUT} from 10% to 90%, T_J = +25℃		1.6		ms
Switch Turn-Off Time	t_{OFF}	V_{IN} > V_{IN_OVLO} to V_{OUT} = 80% of V_{IN}, R_L = 100Ω, with 20% overdrive, for the case of using the internal threshold, T_J = +25℃		50		ns
Switch Turn-Off Propagation Delay	t_{DELAY}	V_{OVLO} > V_{BG} with 20% overdrive to output falling 10%, R_L = 100Ω, for the case of using external threshold, T_J = +25℃		50		ns

TYPICAL PERFORMANCE CHARACTERISTICS

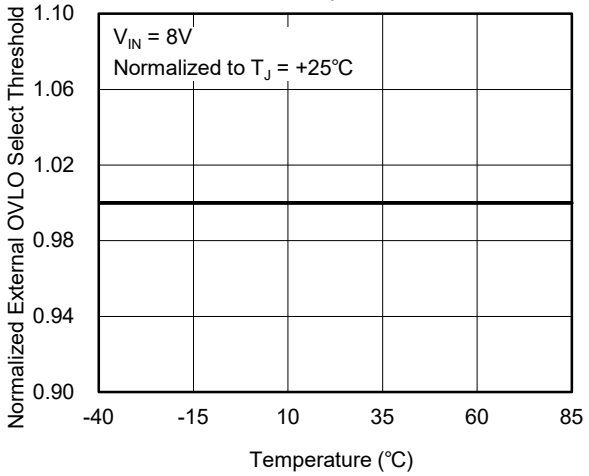
Input Supply Current vs. Input Voltage



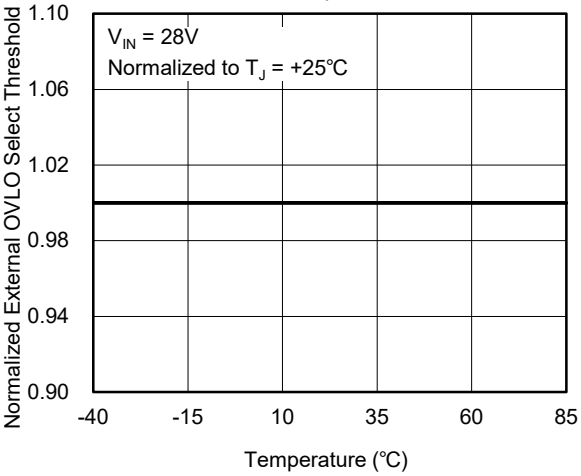
OVLO Leakage Current vs. OVLO Pin Voltage



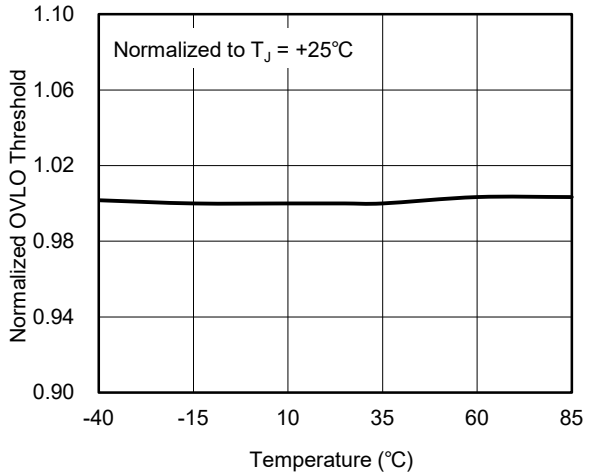
Normalized External OVLO Select Threshold vs. Temperature



Normalized External OVLO Select Threshold vs. Temperature

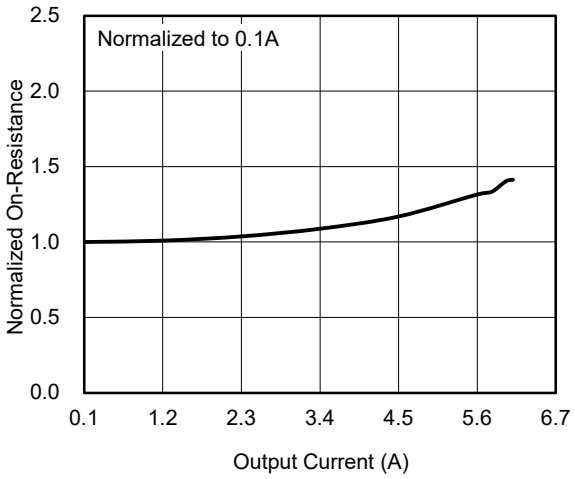


Normalized OVLO Threshold vs. Temperature

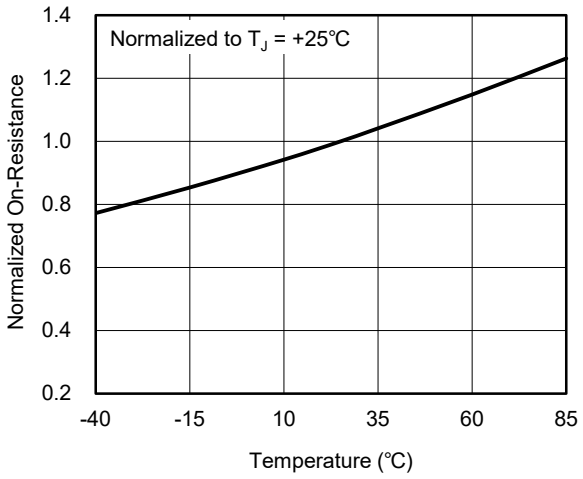


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

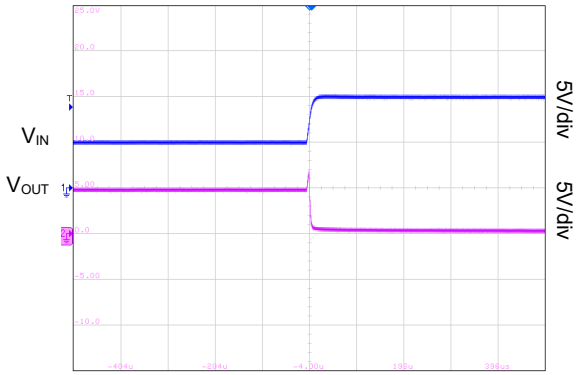
Normalized On-Resistance vs. Output Current



Normalized On-Resistance vs. Temperature

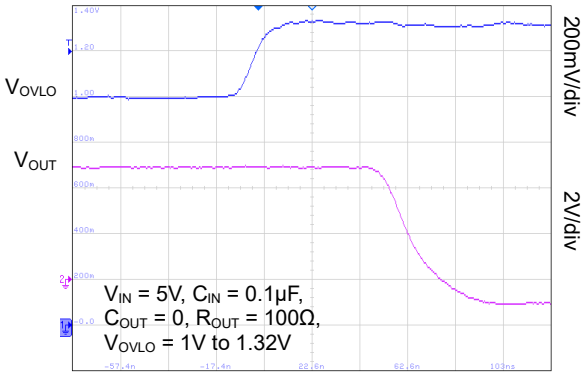


Over-Voltage Fault Response



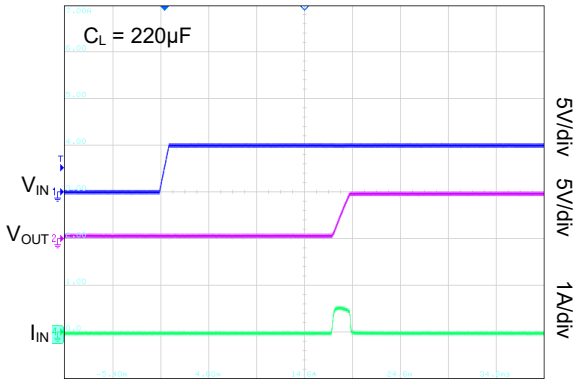
Time (100μs/div)

Over-Voltage Fault Response_OVLO



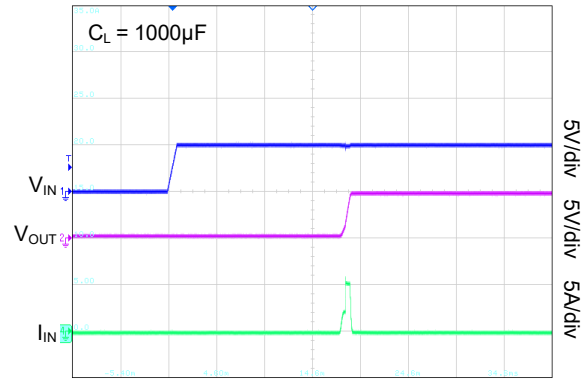
Time (20ns/div)

Power-Up Response



Time (5ms/div)

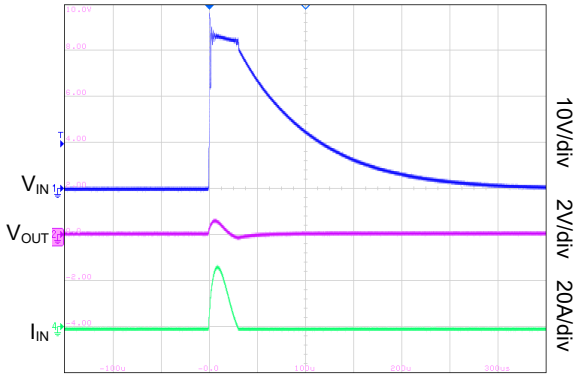
Power-Up Response



Time (5ms/div)

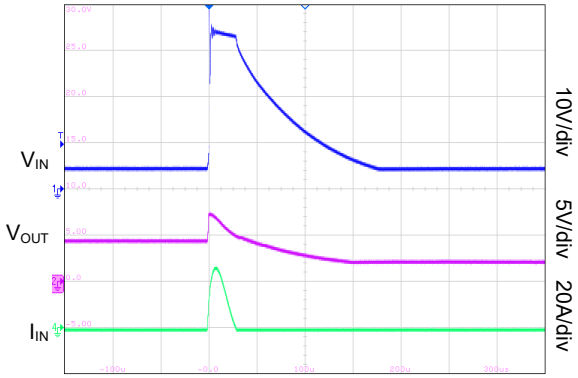
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

IN-GND 90V Surge Discharge Waveforms
(Off-State)



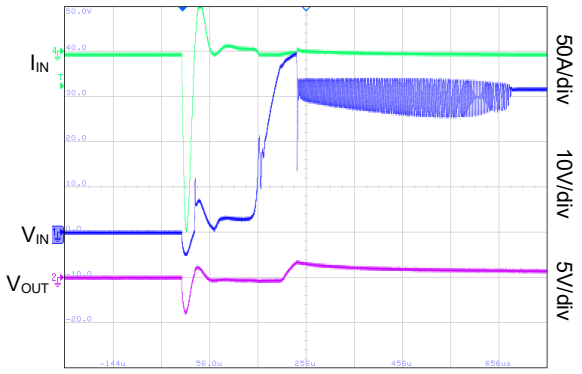
Time (50μs/div)

IN-GND 90V Surge Discharge Waveforms
(On-State)



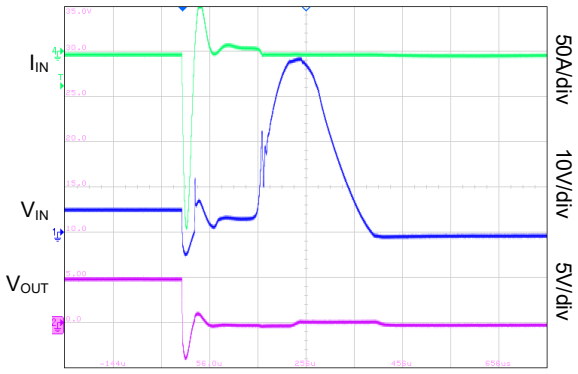
Time (50μs/div)

IN-GND -400V Surge Discharge Waveforms
(Off-State)



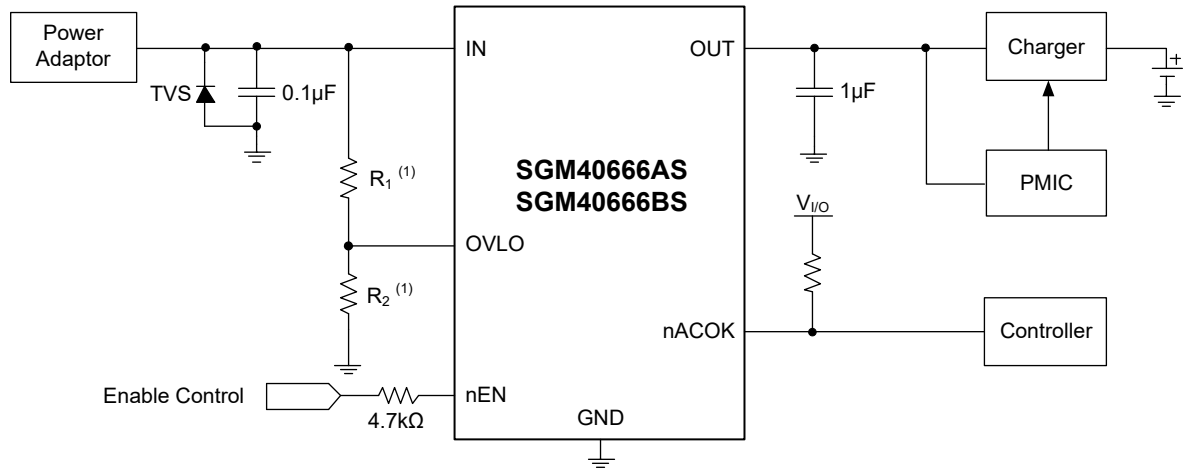
Time (100μs/div)

IN-GND -400V Surge Discharge Waveforms
(On-State)



Time (100μs/div)

TYPICAL APPLICATION CIRCUIT



NOTE:
1. Voltage divider networks R_1 and R_2 are only used for adjustable OVLO. When using the default OVP threshold, connect OVLO to GND directly.

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

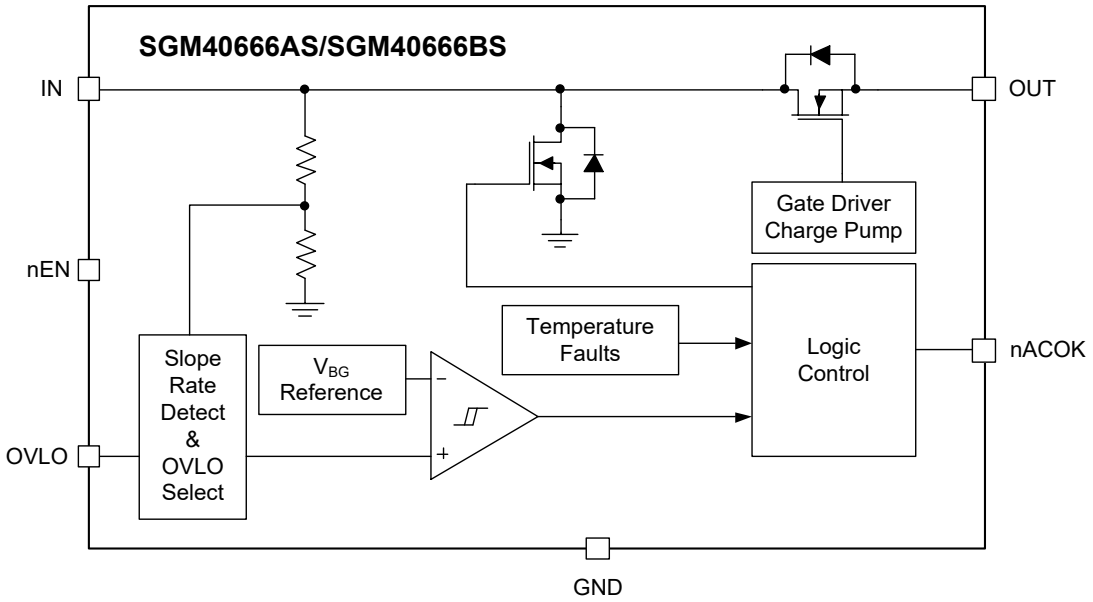
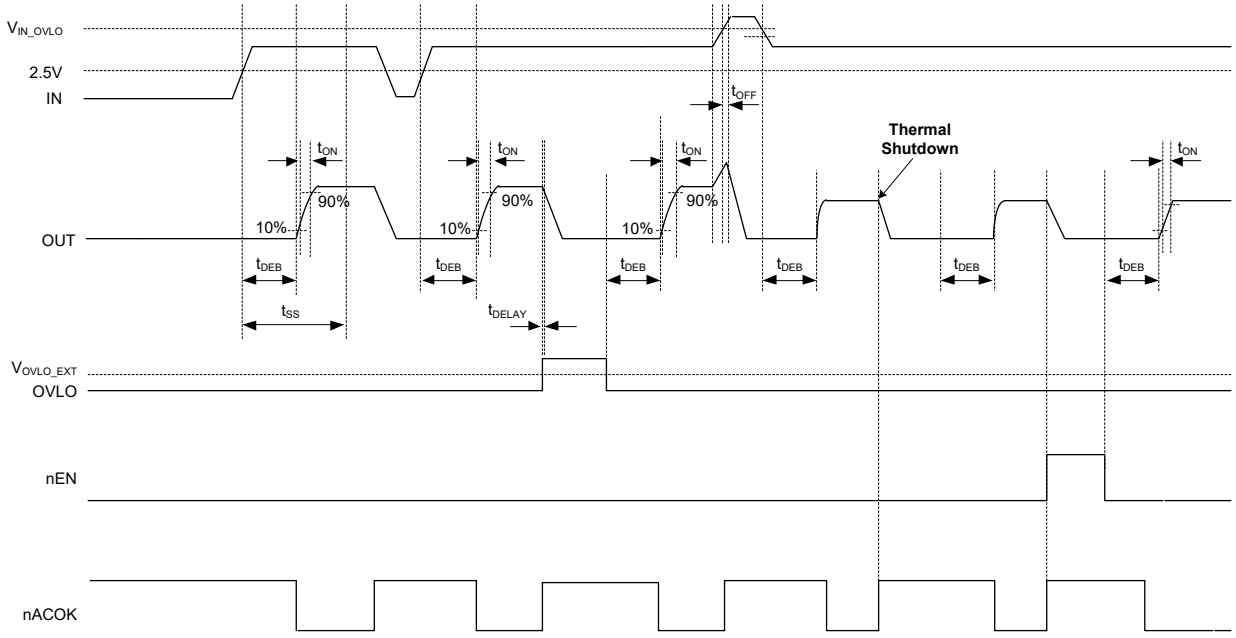


Figure 2. Block Diagram

TIMING DIAGRAM



NOTE: The waveforms can not be scaled.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

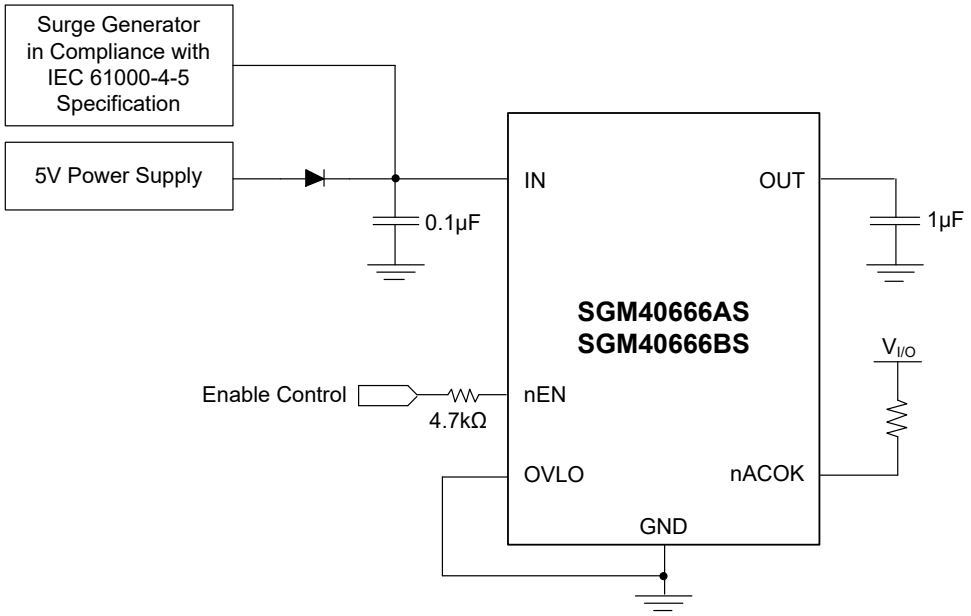


Figure 4. Surge Up Test Circuit

DETAILED DESCRIPTION

The SGM40666AS and SGM40666BS are designed to protect low voltage systems from damage with a high voltage supply up to +31V_{DC} and +40V_{PEAK} (10s with 50mA current limit). The SGM40666AS withstands +90V/-400V while the SGM40666BS can also withstand surges up to +80V/-400V without damage. Surge up tests are performed according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal 27mΩ (TYP) low R_{ON} FET is turned off to prevent damage to the protected components. A built-in 16.5ms (TYP) debounce time prevents turning the internal FET on falsely during start-up.

Device Operation

The SGM40666AS and SGM40666BS have a timing logic controlled charge pump, which is used as gate driver of the internal FET. If the internal trip threshold is used, the charge pump is enabled when V_{IN} < V_{IN_OVLO}, while if external trip threshold is used, it is enabled when V_{OVLO} < V_{OVLO_EXT}.

The charge pump turns the internal FET on after a 16.5ms (TYP) debounce delay (see Figure 3), then soft-start function limits the FET inrush current for another 16.5ms (TYP). Once V_{IN} rises above V_{OVLO_THRESH}, the FET is turned off.

Enable Function

The IC has an enable pin that is used to enable or disable the device. Pull nEN high to turn off the internal pass FET, while pull it low to turn on the FET, and the IC enters the start-up routine.

Over-Voltage Lockout (OVLO)

The typical over-voltage lockout (OVLO) thresholds of the SGM40666AS and SGM40666BS are 6.79V.

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until V_{IN} falls below the OVP falling trip level.

External Adjustable OVLO

The devices detect the voltage on the OVLO pin to check if an external divider exists.

If the OVLO pin is connected to GND, the OVLO value set internally will be applied.

When an external resistor divider network is connected to the OVLO pin and V_{OVLO} > V_{OVLO_SELECT} (0.26V TYP), then this external resistor divider determines the $V_{IN\_OVLO\_EXT}$. At present, $V_{IN\_OVLO\_EXT}$, V_{BG}, and R_1 are known, R_2 can be given by Equation 1:

$$V_{IN\_OVLO\_EXT} = V_{BG} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

This external resistor divider network is completely independent of the internal resistor divider network.

Note that OVLO pin must not be floating.

Surge Protection

The SGM40666AS integrates a clamping circuit to suppress the input surge voltage. When V_{IN} voltage rises sharply (typically > 4.5V/μs) above 32.3V, the internal clamping circuit will be triggered to discharge the surge energy to the ground.

The SGM40666BS discharges the surge energy to the ground when surge voltage rises above 45V.

Thermal Shutdown Protection

The SGM40666AS and SGM40666BS have the thermal shutdown protection. If the junction temperature exceeds +150℃ (TYP), the internal FET turns off. And the devices exit thermal shutdown if the junction temperature cools down by 20℃ (TYP).

nACOK Output

The device has an open-drain nACOK output that indicates a stable power source to the host. When the input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce delay, nACOK goes to low. A pull-up resistor is set from nACOK to the host system logic I/O voltage. nACOK is high impedance if thermal shutdown occurs.

USB OTG Support

When used in an OTG application, the SGM40666AS and SGM40666BS can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. Once the voltage at IN exceeds the minimum input voltage of 2.5V and after debounce time, the main power switch will be fully turned on, reducing the voltage drop from OUT to IN significantly.

APPLICATION INFORMATION

IN Bypass Capacitor

Place a 0.1μF ceramic bypass capacitor between IN and GND pins as close as possible to the device for most applications. When the power source has significant inductance because of long lead length, the device clamps the overshoot because of LC tank circuit.

Output Capacitor

The soft-start function is provided by the slow turn-on time, which allows the SGM40666AS and SGM40666BS to charge an output capacitor (up to 1000μF typically) without shutting down because of over-current condition.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

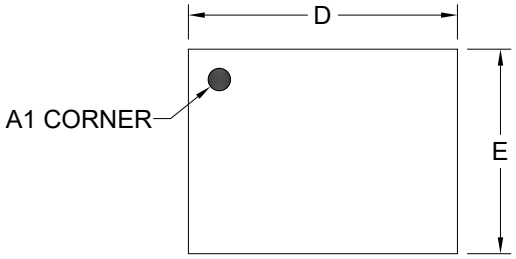
APRIL 2026 – REV.A.1 to REV.A.2	**Page**
Updated Absolute Maximum Ratings section	2

MAY 2024 – REV.A to REV.A.1	**Page**
Updated Functional Block Diagram section	8

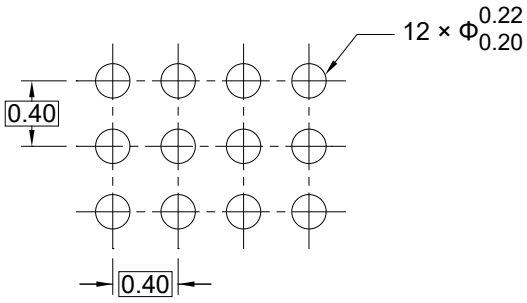
Changes from Original to REV.A (NOVEMBER 2022)	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

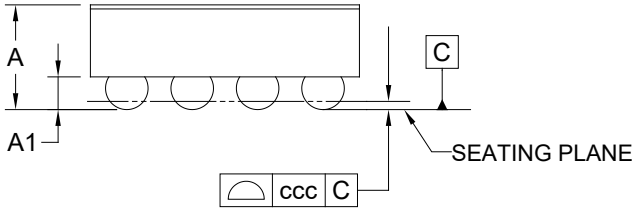
WLCSP-1.65×1.24-12B



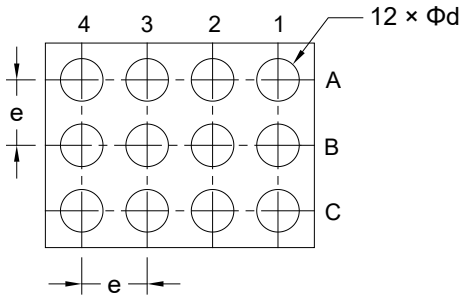
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



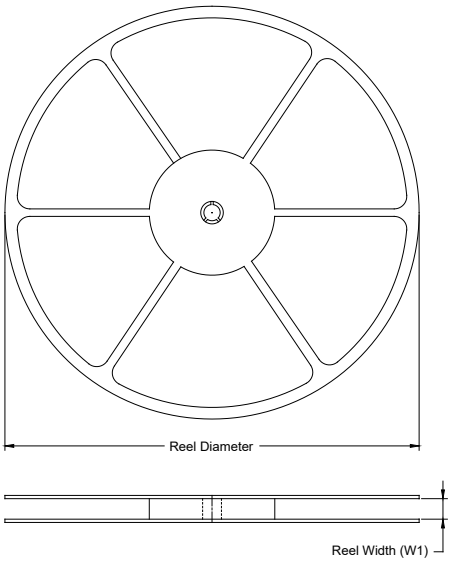
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.685
A1	0.180	-	0.220
D	1.615	-	1.675
E	1.210	-	1.270
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

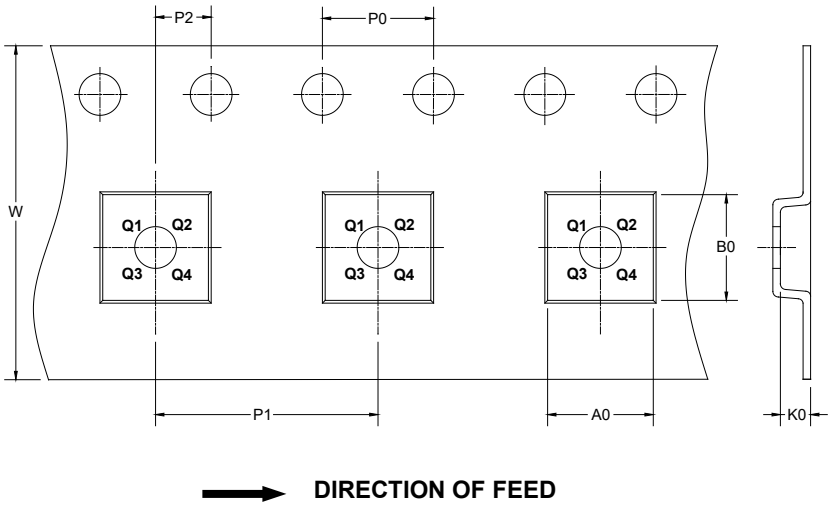
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.65×1.24-12B	7″	9.5	1.38	1.80	0.82	4.0	4.0	2.0	8.0	Q2

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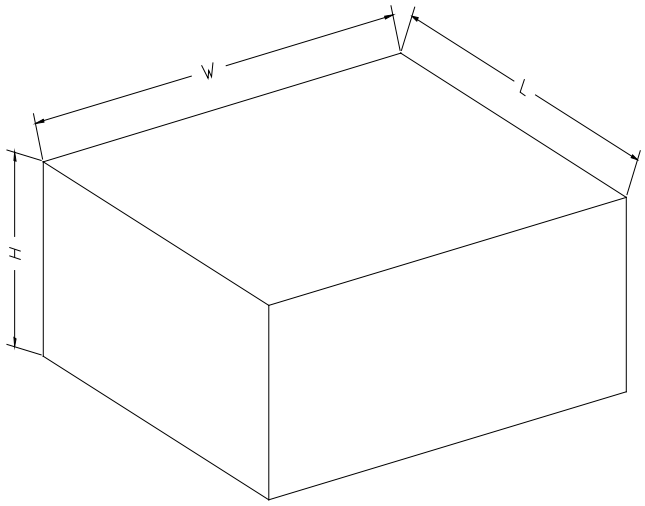
CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

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