SGM41607
I²C Controlled Fast Single-Cell 12A Switched-Cap Charger with Bypass Mode

GENERAL DESCRIPTION

The SGM41607 is an efficient 12A switched-capacitor battery charging device with I²C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.4V to 11.5V input voltage range (VBUS) from smart wall adapters or wireless charger. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the mode.

A two-phase switched-capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. Necessary protection features for safe charging performance including over-voltage protection by external OVPFET (Q_{OVP}) and input reverse blocking (using an internal NFET) are provided.

A high accuracy ADC with 15-bit effective resolution is also included to measure VBAT, IBAT, VAC, VOUT, VBUS, IBUS, TSBUS, TSBAT, TDIE (9 channels) for better management of the charge process.

The SGM41607 is available in a Green WLCSP-3.2×3.35 -56B package.

FEATURES

- **Efficiency Optimized Switched Capacitor Architecture**
  - **Up to 12A Output Current**
  - **3.4V to 11.5V Input Voltage Range**
  - **187.5kHz to 750kHz Switching Frequency Setting**
  - **96.3% Efficiency for 10A Fast Charging**
- **6A Charging in Bypass Mode**
- **Comprehensive Integrated Protection Features**
  - **External VBAT, IBAT, IBUS Regulation with External OVPFET**
  - **Input/Output Over-Voltage Protection (VBUS_OVP, VAC_OVP, VOUT_OVP)**
  - **Input/VOUT/C_{FLY} Short-Circuit Protection (VBUS_SCP, VOUT_SCP, C_{FLY} SCP)**
  - **Input Over-Current Protection (IBUS_OCP)**
  - **Input Under-Current Protection (IBUS_UCP)**
  - **Battery Over-Voltage Protection (VBAT_OVP)**
  - **IBAT Over-Current Protection (IBAT_OCP)**
  - **Converter Over-Current (CONV_OCP)**
- **9-Channel 15-Bit (Effective) ADC Converter**
  - **VBAT, IBAT, VAC, VOUT, VBUS, IBUS, TSBUS, TSBAT and TDIE for Monitoring**

APPLICATIONS

Smart Phone, Tablet PC

TYPICAL APPLICATION

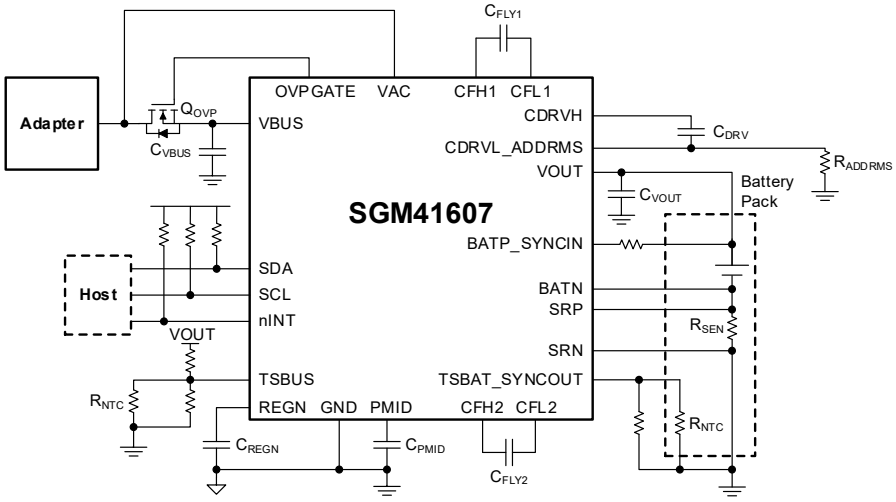


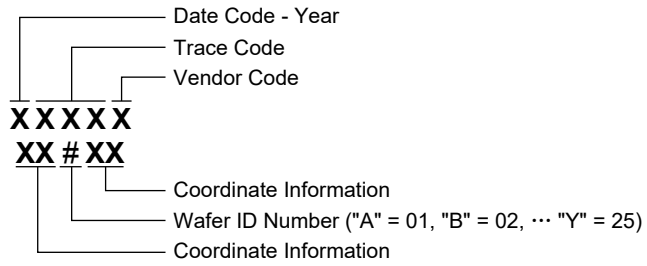
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41607	WLCSP-3.2×3.35-56B	-40℃ to +85℃	SGM41607YG/TR	SGM 41607YG XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VAC (Converter not Switching) ..... -0.3V to 35V
OVPGATE - VBUS ..... -22V to 12V
VBUS, PMID (Converter not Switching)..... -0.3V to 22V
VOUT ..... -0.3V to 6V
CFH1, CFH2 to VOUT ..... -0.3V to 6V
CFL1, CFL2 ..... -0.3V to 6V
nINT, SDA, SCL, CDRVL_ADDRMS, REGN..... -0.3V to 6V
BATP_SYNCIN ..... -0.3V to 6V
TSBUS, TSBAT_SYNCOUT ..... -0.3V to 6V
CDRVH ..... -0.3V to 20V
SRP, SRN, BATN ..... -0.3V to 1.8V
SRP to SRN ..... -0.5V to 0.5V
VOUT - VBUS ..... -16V to 6V
Sink Current, nINT 6mA
Package Thermal Resistance
WLCSP-3.2×3.35-56B, θ_{JA} ..... 27.9℃/W
WLCSP-3.2×3.35-56B, θ_{JB} ..... 4.3℃/W
WLCSP-3.2×3.35-56B, θ_{JC} ..... 10.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VAC ..... 3.4V to 18V
VBUS (Bypass Mode) ..... 3.4V to 5.5V
VBUS (Voltage Divider Mode) ..... 5.5V to 11.5V
VOUT ..... 3V to 5.5V
I_{VOUT} (Voltage Divider Mode) ..... 0A to 12A
I_{VOUT} (Bypass Mode) ..... 0A to 6A
PMID - VOUT (Voltage Divider Mode)..... 0V to 5.5V
(CFH1 - VOUT), CFL1 ..... 0V to 5.5V
(CFH2 - VOUT), CFL2 ..... 0V to 5.5V
BATP_SYNCIN ..... 0V to 5.5V
SRP, SRN, BATN ..... 0V to 1.5V
(SRP - SRN) ..... -0.05V to 0.05V
TSBUS, TSBAT_SYNCOUT ..... 0V to 3V
SDA, SCL, CDRVL_ADDRMS, nINT ..... 0V to 5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

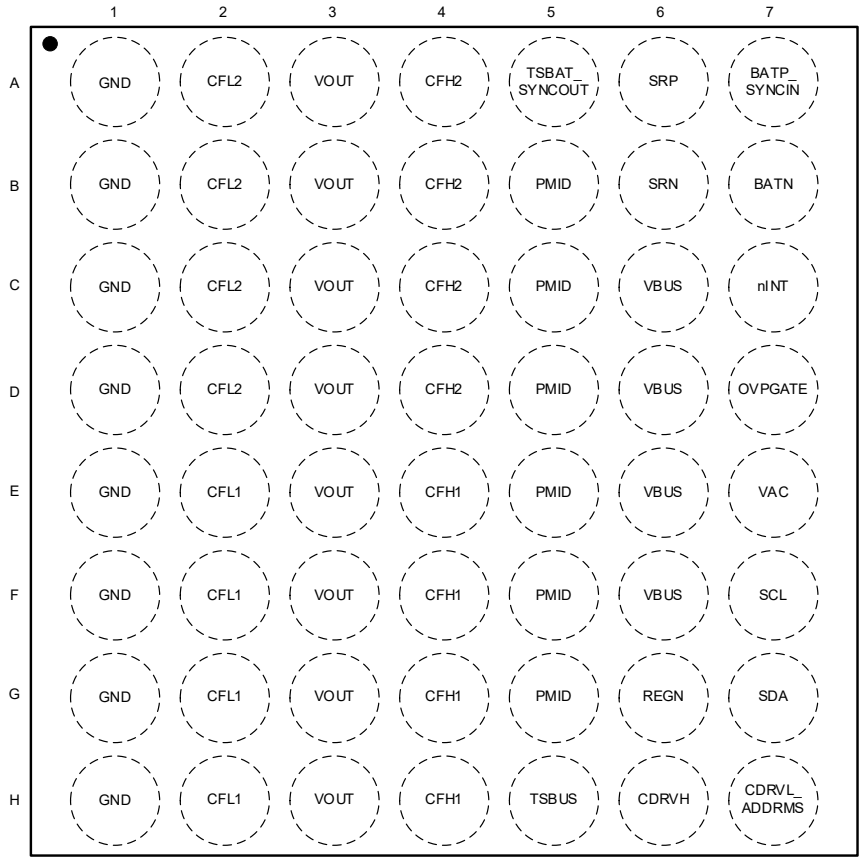
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.2×3.35-56B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1, B1, C1, D1, E1, F1, G1, H1	GND	P	Power Ground Pins.
A2, B2, C2, D2	CFL2	P	Phase 2 Flying Capacitor Negative Pins. Connect at least three 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close to the device as possible.
A3, B3, C3, D3, E3, F3, G3, H3	VOUT	P	Power Output Pins. Place a 22μF capacitor between this pin and GND.
A4, B4, C4, D4	CFH2	P	Phase 2 Flying Capacitor Positive Pins. Connect at least three 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close to the device as possible.
A5	TSBAT_SYNCOUT	AIO	Battery Temperature Sense Input and SYNCOUT for Master Configuration. Connect it to the battery NTC thermistor. See the TSBAT section for choosing the resister divider values. If configured as a Master IC for parallel charging, this pin functions as SYNCOUT, and is connected to SYNCIN of the Slave IC via a 1kΩ pull-up resistor to REGN.
A6	SRP	AI	Battery Current Sensing Positive Input. Place a 2mΩ or 5mΩ (R_{SNS}) shunt resistor between SRP and SRN pin. Short SRP and SRN together if not used.
A7	BATP_SYNCIN	AI	Battery Voltage Sensing Positive Input and SYNCIN for Slave Configuration. Connect a 100Ω resistor between BATP_SYNCIN and positive terminal of battery pack. If configured as a Slave IC for parallel charging, this pin functions as SYNCIN, and is connected to TSBAT_SYNCOUT of the Master IC.
B5, C5, D5, E5, F5, G5	PMID	P	Power Stage Supply Input Pins. Bypass them with at least 10μF ceramic capacitor to GND
B6	SRN	AI	Battery Current Sensing Negative Input. Place a 2mΩ or 5mΩ (R_{SNS}) shunt resistor between SRP and SRN pin. Short SRP and SRN together if not used.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
B7	BATN	AI	Battery Voltage Sensing Negative Input. Connect a 100Ω resistor between BATN and negative terminal of the battery pack.
C6, D6, E6, F6	VBUS	P	Device Power Input Pins. Use one 1μF or larger ceramic capacitors between VBUS and GND pins close to the device.
C7	nINT	DO	Open-Drain Interrupt Output Pin. Pull it up to the logic high rail with a 10kΩ resistor. It is normally high but generates a low 256μs pulse when a charge fault occurs to notify the host.
D7	OVPGATE	AO	External NFET Gate Control Pin. Connect to the gate of the external OVPFET (Q_{OVP}).
E2, F2, G2, H2	CFL1	P	Phase 1 Flying Capacitor Negative Pins. Connect at least three 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close to the device as possible.
E4, F4, G4, H4	CFH1	P	Phase 1 Flying Capacitor Positive Pins. Connect at least three 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close to the device as possible.
E7	VAC	AI	Adapter DC Voltage Sense Pin. Connect it to the drain of the external OVPFET.
F7	SCL	DI	I²C Interface Clock Line
G6	REGN	AO	5V LDO Output. Place a 4.7μF capacitor between this pin and GND.
G7	SDA	DIO	I²C Interface Data Line
H5	TSBUS	AI	Adapter Temperature Voltage Sense Input. Connect it to the cable connector NTC thermistor and the external resistor divider that is pulled up to VOUT.
H6	CDRVH	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADDRMS.
H7	CDRVL_ADDRMS	AIO	Charge Pump for Gate Drive. Connect a 0.22μF MLCC capacitor between CDRVH and CDRVL_ADDRMS. During POR, this pin is also used to assign the address of the device and the operation mode of the device as Standalone, Master, or Slave. See Table 2 for detailed function.

NOTE: AI = Analog Input, AO = Analog Output, AIO = Analog Input/Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input/Output, P = Power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VAC Quiescent Current	I_{Q_VAC}	ADC disabled, charge disabled, Q_{OVP} used, V_{VAC_OVP} = 6.5V (VAC_OVP[2:0] = 111),V_{VAC} = 12V, V_{VBUS} = 0V, V_{VOUT} = 0V, VAC_OVP activated		420	570	μA
VBUS Quiescent Current	I_{Q_VBUS}	ADC disabled, charge disabled, Q_{OVP} used, V_{VBUS} = 8V, V_{VAC} = 8V (excluding the pull-down current at VBUS pin)		50	75	μA
		ADC enabled, charge enabled, Q_{OVP} used, V_{VBUS} = 8V > (2 × V_{VOUT}), f_{SW} = 500kHz		16.2		mA
Battery Only Quiescent Current	I_{Q_VOUT}	ADC disabled, charge disabled, VBUS not present, V_{VAC} = 0V, V_{VOUT} = 5V		14	40	μA
		ADC enabled, charge disabled (after 1-shot ADC conversion complete), VBUS not present, V_{VAC} = 0V, V_{VOUT} = 5V		14		μA
VAC UVLO Rising Threshold	$V_{VAC\_UVLO\_R}$	V_{VAC} rising		2.95	3.35	V
VAC UVLO Hysteresis	$V_{VAC\_UVLO\_HYS}$			150		mV
VOUT UVLO Rising Threshold	$V_{OUT\_UVLO\_R}$	VOUT pin, V_{VOUT} rising, for active I²C		1.9	2.25	V
VOUT UVLO Hysteresis	$V_{OUT\_UVLO\_HYS}$			150		mV
VBAT Present Rising Threshold	$V_{BAT\_PRESENT\_R}$	BATP_SYNCIN pin, V_{BATP} rising		2.8	3.05	V
VBAT Present Hysteresis	$V_{BAT\_PRESENT\_HYS}$			85		mV
External OVP Control						
External FET Gate Drive Voltage	$V_{OVPGATE}$	V_{VAC} = 8V, measured from gate to source, with minimum 8nF C_{GS}		8.2		V
VAC Present Rising Threshold	$V_{VAC\_PRESENT\_R}$	V_{VAC} rising		3.05	3.4	V
VAC Present Hysteresis	$V_{VAC\_PRESENT\_HYS}$			200		mV
VAC OVP Rising Threshold Range	$V_{VAC\_OVP\_R}$	I²C programmable	6.5		17	V
VAC OVP Threshold Accuracy	$V_{VAC\_OVPR\_ACC}$	V_{VAC_OVP} = 6.5V, initial accuracy, T_J = +25℃	-3.5		2	%
		V_{VAC_OVP} = 11V, initial accuracy, T_J = +25℃	-3.5		2	%
		V_{VAC_OVP} = 14V, initial accuracy, T_J = +25℃	-3.5		2	%
		V_{VAC_OVP} = 17V, initial accuracy, T_J = +25℃	-3.5		2	%
VAC OVP Rising Deglitch Time	$t_{VAC\_OVPR\_DEG}$	Deglitch between V_{VAC} rising (5V/μs) above $V_{VAC\_OVP\_R}$ and triggering the protection action		100		ns
VBUS Pull-Down Resistance	R_{PDN_VBUS}	VBUS_PDN_EN = 1		6		kΩ
VAC Pull-Down Resistance	R_{PDN_VAC}			120		Ω
VAC Pull-down Timeout	t_{VAC_PD}			400		ms
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 8V, I_{REGN} = 20mA		5		V
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 8V, V_{REGN} = 4.5V		48		mA
Switched Cap Chargers						
VBUS to VOUT Resistance	$R_{DROPOUT}$	Bypass mode		12		mΩ
R_{DSON} of Reverse Blocking FET	R_{DS_QRB}	V_{VBUS} = 9V		3.5		mΩ
R_{DSON} of Q_{CH1}	R_{DS_QCH1}	V_{PMID} = 9V		13		mΩ
R_{DSON} of Q_{DH1}	R_{DS_QDH1}	V_{CFLY} = 4.5V		7.5		mΩ
R_{DSON} of Q_{CL1}	R_{DS_QCL1}	V_{VOUT} = 4.5V		7.5		mΩ
R_{DSON} of Q_{DL1}	R_{DS_QDL1}	V_{CFLY} = 4.5V		7.5		mΩ
R_{DSON} of Q_{CH2}	R_{DS_QCH2}	V_{PMID} = 9V		13		mΩ
R_{DSON} of Q_{DH2}	R_{DS_QDH2}	V_{CFLY} = 4.5V		7.5		mΩ
R_{DSON} of Q_{CL2}	R_{DS_QCL2}	V_{VOUT} = 4.5V		7.5		mΩ
R_{DSON} of Q_{DL2}	R_{DS_QDL2}	V_{CFLY} = 4.5V		7.5		mΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Protection						
nINT Low Pulse Duration when a Protection Occurs	t_{INT}			256		μs
VBUS OVP Rising Threshold Range	$V_{BUS\_OVP\_R}$	I²C programmable, 50mV per step, 8.85V by default	5.95		12.3	V
VBUS OVP Threshold Hysteresis	$V_{BUS\_OVP\_HYS}$			250		mV
VBUS OVP Threshold Accuracy	$V_{BUS\_OVPR\_ACC}$	$V_{BUS\_OVP\_R}$ = 10V, initial accuracy, T_J = +25℃	-3.5		2.0	%
VBUS OVP Rising Deglitch Time	$t_{VBUS\_OVPR\_DEG}$	Deglitch between V_{VBUS} rising above $V_{BUS\_OVP\_R}$ and triggering protection action		2		μs
VBUS OVP Alarm Rising Range	$V_{BUSOVP\_ALM\_R}$	I²C programmable, 50mV per step, 8.8V by default	6		12.35	V
VBUS OVP Alarm Hysteresis	$V_{BUSOVP\_ALM\_HYS}$			50		mV
VBUS OVP Alarm Accuracy	$V_{BUSOVP\_ALM\_ACC}$	V_{VBUS} = 9.4V, initial accuracy, T_J = +25℃	-3.5		2.5	%
IBUS OCP Threshold Range	I_{BUS_OCP}	I²C programmable, 250mA per step, 5.75A by default	3		6.75	A
IBUS OCP Threshold Accuracy	$I_{BUS\_OCP\_ACC}$	I_{BUS_OCP} = 3A, T_J = +25℃	-4.5		4.5	%
IBUS OCP Deglitch Time	$t_{IBUS\_OCP\_DEG}$	Deglitch between I_{BUS} rising above I_{BUS_OCP} and trigger protection action		50		μs
IBUS OCP Alarm Threshold Range	$I_{BUSOCP\_ALM\_R}$	I²C programmable, 50mA per step, 5.5A by default	0.45		6.8	A
IBUS OCP Alarm Hysteresis	$I_{BUS\_OCP\_ALM\_HYS}$			50		mA
IBUS OCP Alarm Threshold Accuracy	$I_{BUSOCP\_ALM\_ACC}$	$I_{BUSOCP\_ALM\_R}$ = 3A, T_J = +25℃	-4.5		4.5	%
IBUS UCP Rising Threshold	$I_{BUS\_UCP\_R}$	Rising, BUSUCP = 0b	200	300	400	mA
		Rising, BUSUCP = 1b	400	500	600	mA
IBUS UCP Falling Threshold	$I_{BUS\_UCP\_F}$	Falling, BUSUCP = 0b	50	150	250	mA
		Falling, BUSUCP = 1b	150	250	350	mA
IBUS UCP Deglitch Time	$t_{IBUS\_UCP\_DEG}$	IBUS_UCP_FALL_DEG = 0		10		μs
		IBUS_UCP_FALL_DEG = 1		5		ms
VOUT OVP Rising Threshold Range	$V_{OUT\_OVP\_R}$	4.9V by default	4.7	4.9	5.1	V
VOUT OVP Threshold Hysteresis	$V_{OUT\_OVP\_HYS}$			200		mV
VOUT OVP Threshold Accuracy	$V_{OUT\_OVPR\_ACC}$	$V_{OUT\_OVP\_R}$ = 4.9V	-4.1		4.1	%
VOUT OVP Rising Deglitch Time	$t_{VOUT\_OVP\_DEG}$	Deglitch between V_{VOUT} rising above $V_{OUT\_OVP\_R}$ and triggering protection action		5.5		μs
VDROP OVP Rising Threshold	V_{DROP_OVP}	I²C programmable, VDROP_THRESHOLD_SET = 0b		300		mV
		I²C programmable, VDROP_THRESHOLD_SET = 1b		400		mV
VDROP OVP Rising Threshold Deglitch	t_{VDROP_OVP}	Deglitch between V_{DROP} rising above V_{DROP_OVP} and triggering protection action. I²C programmable, VDROP_DEGLITCH_SET = 0b		8		μs
		Deglitch between V_{DROP} rising above V_{DROP_OVP} and triggering protection action. I²C programmable, VDROP_DEGLITCH_SET = 1b		5		ms
VBAT OVP Rising Threshold Range	$V_{BAT\_OVP\_R}$	I²C programmable, 25mV per step, 4.325V by default	3.475		5.05	V
VBAT OVP Threshold Hysteresis	$V_{BAT\_OVP\_HYS}$			100		mV
VBAT OVP Threshold Accuracy	$V_{BAT\_OVP\_ACC}$	$V_{BAT\_OVP\_R}$ = 4.325V, initial accuracy, T_J = +25℃	-0.5		0.5	%
VBAT OVP Rising Deglitch Time	$t_{VBAT\_OVPR\_DEG}$	Deglitch between V_{BAT} rising above $V_{BAT\_OVP\_R}$ and triggering protection action		50		μs
		During VBAT_REG		500		μs
VBAT OVP Falling Deglitch Time	$t_{VBAT\_OVPF\_DEG}$	Deglitch between V_{BAT} falling below V_{BAT_OVP} falling threshold		5		ms

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT OVP Alarm Rising Threshold Range	$V_{BATOVP\_ALM\_R}$	I²C programmable, 25mV per step, 4.2V by default	3.5		5.075	V
VBAT OVP Alarm Hysteresis	$V_{BATOVP\_ALM\_HYS}$	Falling		50		mV
VBAT OVP Alarm Accuracy	$V_{BATOVP\_ALM\_ACC}$	$V_{BATOVP\_ALM\_R}$ = 4.2V/4.4V/4.6V, initial accuracy, T_J = +25℃	-1		1	%
IBAT OCP Threshold Range	I_{BAT_OCP}	I²C programmable, 100mA per step, 11.2A by default	3		13	A
IBAT OCP Threshold Accuracy	$I_{BAT\_OCP\_ACC}$	I_{BAT_OCP} = 6A, R_{SNS} = 2mΩ	-3		3	%
		I_{BAT_OCP} = 11.2A, R_{SNS} = 2mΩ	-2.5		2.5	%
IBAT OCP Deglitch Time	$t_{IBAT\_OCP\_DEG}$	Deglitch between I_{BAT} rising above I_{BAT_OCP} and triggering protection action		50		μs
		during IBAT_REG		500		μs
IBAT OCP Alarm Rising Threshold Range	$I_{BATOCP\_ALM\_R}$	I²C programmable, 100mA per step, 11A by default	3		13	A
IBAT OCP Alarm Hysteresis	$I_{BATOCP\_ALM\_HYS}$			100		mA
IBAT OCP Alarm Threshold Accuracy	$I_{BATOCP\_ALM\_ACC}$	$I_{BATOCP\_ALM\_R}$ = 6A, initial accuracy, T_J = +25℃	-2		2	%
		$I_{BATOCP\_ALM\_R}$ = 11A, initial accuracy, T_J = +25℃	-2		2	%
IBAT UCP Alarm Threshold Range	I_{BATUCP_ALM}	I²C programmable, 50mA per step, 3A by default, R_{SNS} = 2mΩ	1		7.35	A
IBAT UCP Alarm Hysteresis	$I_{BATUCP\_ALM\_HYS}$	Rising		50		mA
IBAT UCP Alarm Threshold Accuracy	$I_{BATUCP\_ALM\_ACC}$	I_{BATUCP_ALM} = 3A, R_{SNS} = 2mΩ, initial accuracy, T_J = +25℃	-2.2		2.2	%
TSBUS Percentage Fault Threshold Range	TS_{BUS_FLT}	I²C programmable, 0.19531% per step, 4.1% by default	0		50	%
TSBUS Percentage Fault Accuracy	TS_{BUSFLT_ACC}	TS_{BUS_FLT} = 25%, initial accuracy, T_J = +25℃	-3		3	%
TSBAT Percentage Fault Threshold Range	TS_{BAT_FLT}	I²C programmable, 0.19531% per step, 4.1% by default	0		50	%
TSBAT Percentage Fault Accuracy	TS_{BATFLT_ACC}	TS_{BAT_FLT} = 25%, initial accuracy, T_J = +25℃	-3		3	%
Rising Internal (T_J) Shutdown	T_{DIE_OTP}			150		℃
Falling Hysteresis				30		℃
ADC Specification						
ADC Conversion Time for Each Channel	t_{ADC_CONV}	ADC_SAMPLE[1:0] = 00b		24		ms
		ADC_SAMPLE[1:0] = 01b		12		
		ADC_SAMPLE[1:0] = 10b		6		
		ADC_SAMPLE[1:0] = 11b		3		
ADC Resolution	ADC_{RES}	ADC_SAMPLE[1:0] = 00b		15		bit
		ADC_SAMPLE[1:0] = 01b		14		
		ADC_SAMPLE[1:0] = 10b		13		
		ADC_SAMPLE[1:0] = 11b		12		
ADC IBUS Current Readable in REG0x16 and REG0x17	I_{BUS_ADC}	Effective range, T_J = +25℃	0		6.25	A
		LSB		1		mA
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$	I_{BUS} = 1.5A, T_J = +25℃	-5		5	%
		I_{BUS} = 3A, T_J = +25℃	-3		3	%
ADC VBUS Voltage Readable in Registers in REG0x18 and REG0x19	V_{BUS_ADC}	Effective range, T_J = +25℃	0		14	V
		LSB		1		mV
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$	V_{VBUS} = 8V, ADC_RATE = 0b, T_J = +25℃	-2.5		2.5	%
ADC VAC Voltage Readable in Registers in REG0x1A and REG0x1B	V_{AC_ADC}	Effective range, T_J = +25℃	0		14	V
		LSB		1		mV
VAC ADC Accuracy	$V_{AC\_ADC\_ACC}$	V_{VAC} = 8V, ADC_RATE = 0b, T_J = +25℃	-2		2	%

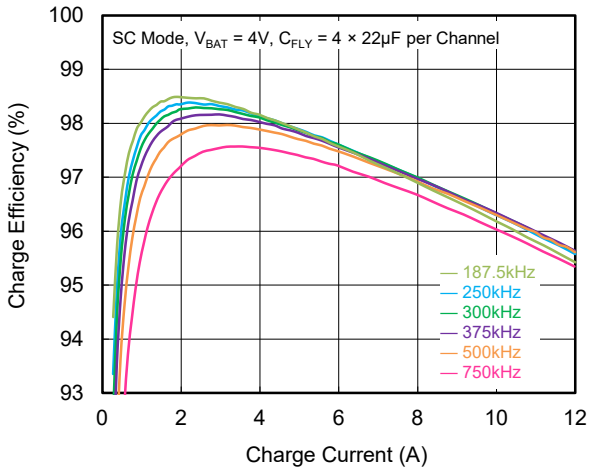
ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

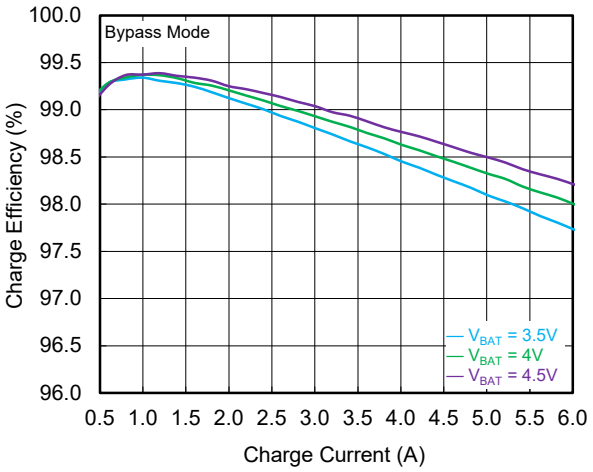
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC VOUT Voltage Readable in Registers in REG0x1C and REG0x1D	V_{OUT_ADC}	Effective range, T_J = +25℃	0		5	V
		LSB		1		mV
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	V_{VOUT} = 4.3V/4.4V/4.5V, ADC_RATE = 0b, initial accuracy, T_J = +25℃	-0.3		0.3	%
ADC VBAT Voltage Readable in Registers in REG0x1E and REG0x1F	V_{BAT_ADC}	Effective range, T_J = +25℃	0		5	V
		LSB		1		mV
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$	V_{BAT} = 4.3V/4.4V/4.5V, ADC_RATE = 0b, initial accuracy, T_J = +25℃	-0.3		0.3	%
ADC IBAT Current Readable in Registers in REG0x20 and REG0x21	I_{BAT_ADC}	Effective range, T_J = +25℃	0		12	A
		LSB		1		mA
IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$	I_{BAT} = 3A, R_{SNS} = 2mΩ, T_J = +25℃	-2		2	%
		I_{BAT} = 6A, R_{SNS} = 2mΩ, T_J = +25℃	-1.5		1.5	%
		I_{BAT} = 12A, R_{SNS} = 2mΩ, T_J = +25℃	-1.5		1.5	%
ADC TSBUS Pin Voltage	TS_{BUS_ADC}	Effective range, T_J = +25℃	0.2		2.7	V
ADC TSBUS Pin Percentage Readable in Registers in REG0x22 and REG0x23	TS_{BUS_ADC}	Effective range, T_J = +25℃	0		50	%
		LSB		0.09766		%
TSBUS ADC Accuracy	$TS_{BUS\_ADC\_ACC}$	V_{TSBUS} = 2V, V_{VOUT} = 4V, T_J = +25℃	-3		3	%
ADC TSBAT Pin Voltage	TS_{BAT_ADC}	T_J = +25℃	0.2		2.7	V
ADC TSBAT Pin Percentage Readable in Registers in REG0x24 and REG0x25	TS_{BAT_ADC}	Effective range, T_J = +25℃	0		50	%
		LSB		0.09766		%
TSBAT ADC Accuracy	$TS_{BAT\_ADC\_ACC}$	V_{TSBAT} = 2V, V_{VOUT} = 4V, T_J = +25℃	-3		3	%
ADC DIE Temperature Readable in Registers in REG0x26 and REG0x27	T_{DIE_ADC}	Effective range, T_J = +25℃	-40		150	℃
		LSB		0.5		℃
ADC Die Temperature	$T_{DIE\_ADC\_ACC}$	T_{DIE} = +150℃	146	150	154	℃
I²C Interface (SCL, SDA and nINT Pins)						
High Level Input Voltage	V_{IH_I2C}	SCL and SDA pins During rising from 0.3V to 1V, when SCL/SDA rises above 0.875V, it outputs High within 260ns	0.875			V
Low Level Input Voltage	V_{IL_I2C}	SCL and SDA pins During falling from 1V to 0.3V, when SCL/SDA falls below 0.4V, it outputs Low within 330ns.			0.4	V
Low Level Output Voltage	V_{OL_I2C}	Sink 2mA, SDA and nINT pins			0.4	V
SCL Clock Frequency	f_{SCL}		100		1000	kHz
Logic I/O Pin (TSBAT_SYNCOUT)						
High Level Output Voltage, TSBAT_ SYNCOUT Pin	$V_{OH\_TSBAT\_SYNCOUT}$	Connected to 1.8V	1.4			V
Low Level Output Voltage, TSBAT_ SYNCOUT Pin	$V_{OL\_TSBAT\_SYNCOUT}$	Sink 2mA			0.4	V
Logic Input Pin (BATP_SYNCIN)						
High Level Input Voltage, BATP_SYNCIN Pin	$V_{IH\_BATP\_SYNCIN}$		1.4			V
Low Level Input Voltage, BATP_SYNCIN Pin	$V_{IL\_BATP\_SYNCIN}$				0.4	V
Timing Requirement						
Switching Frequency	f_{SW}	FSW_SET[2:0] = 100b		500		kHz
If the part is in regulation, but below V_{DROP_OVP} for this amount of time, the part will stop switching.	$t_{REG\_TIMEOUT}$			650		ms
Time between Consecutive Faults for ALM Indication	$t_{ALM\_DEBOUNCE}$			1		μs

TYPICAL PERFORMANCE CHARACTERISTICS

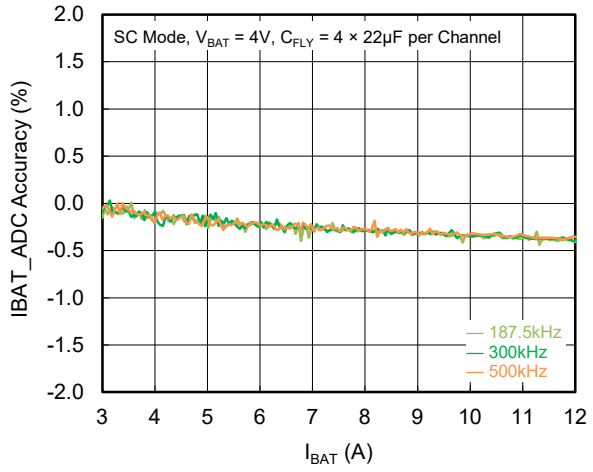
Charge Efficiency vs. Charge Current



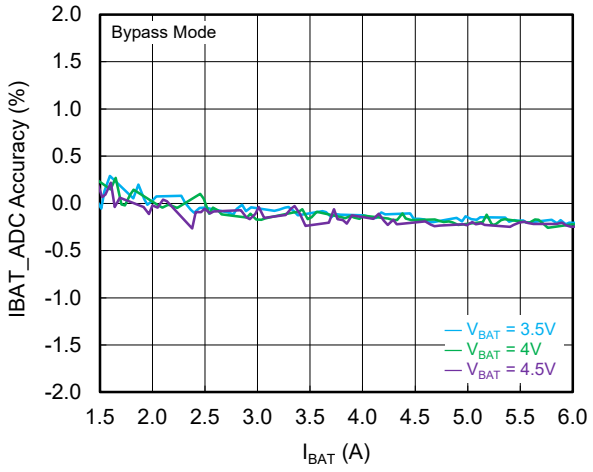
Charge Efficiency vs. Charge Current



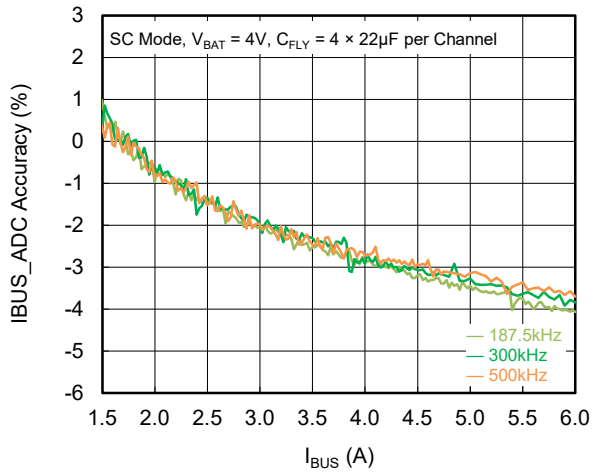
IBAT_ADC Accuracy vs. BAT Current



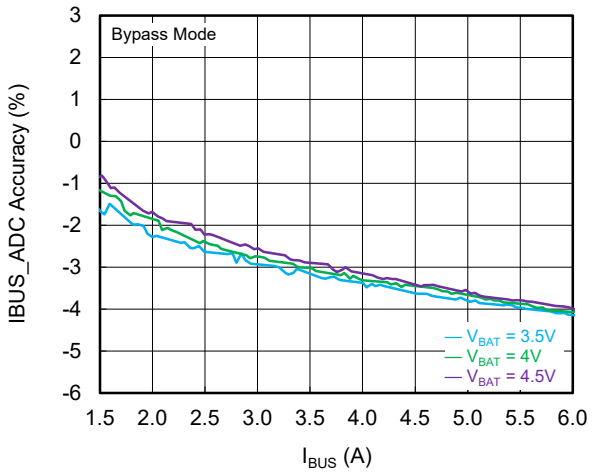
IBAT_ADC Accuracy vs. BAT Current



IBUS_ADC Accuracy vs. BUS Current

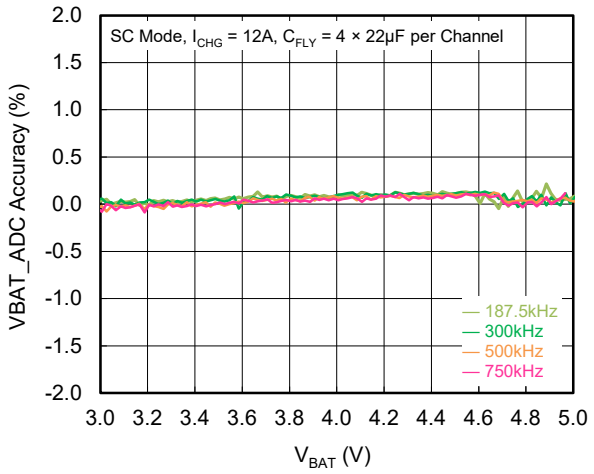


IBUS_ADC Accuracy vs. BUS Current

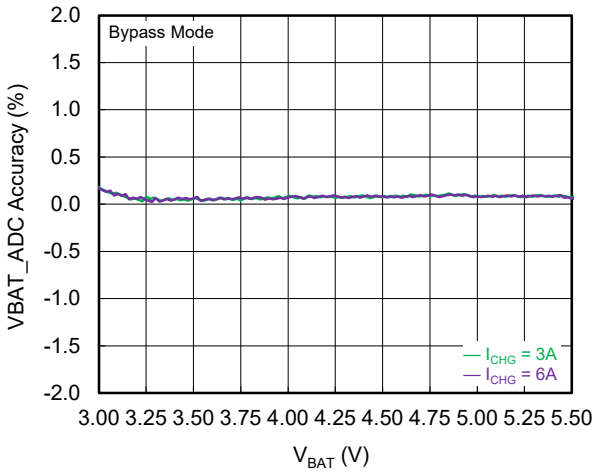


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

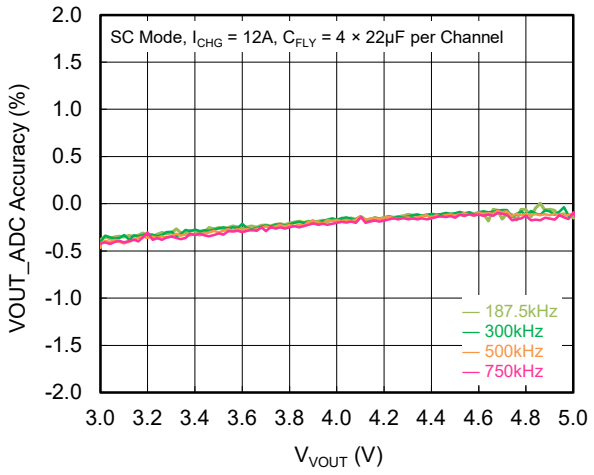
VBAT_ADC Accuracy vs. BAT Voltage



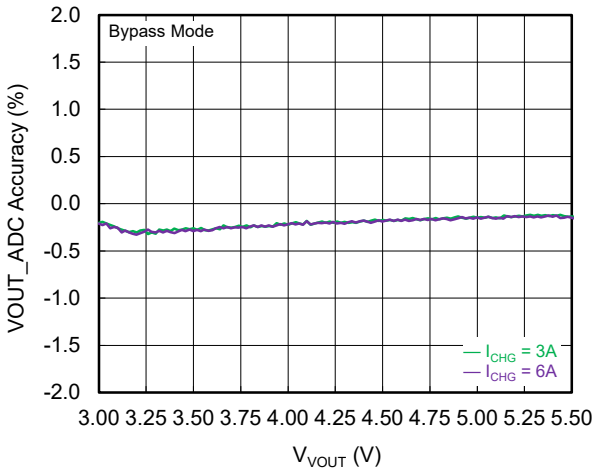
VBAT_ADC Accuracy vs. BAT Voltage



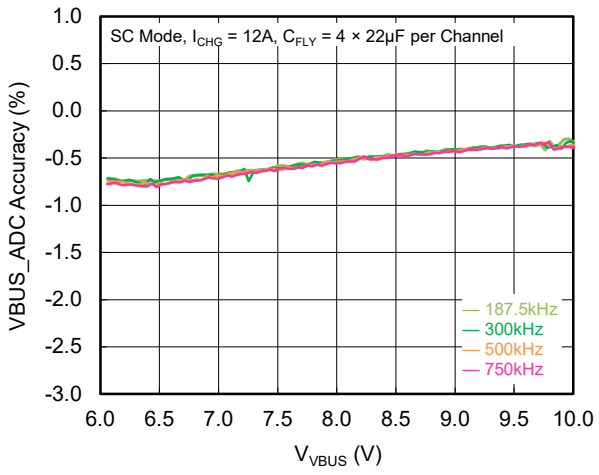
VOUT_ADC Accuracy vs. VOUT Voltage



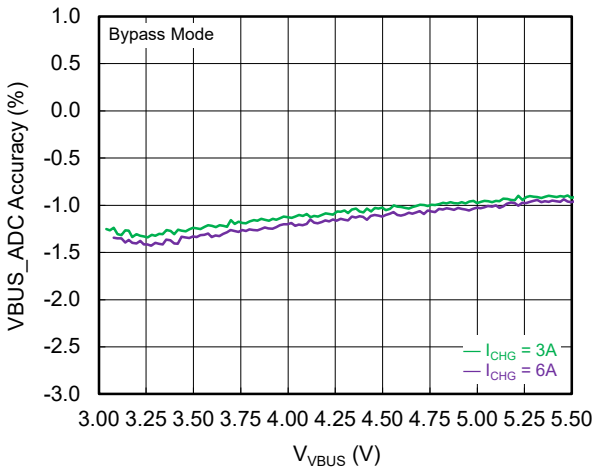
VOUT_ADC Accuracy vs. VOUT Voltage



VBUS_ADC Accuracy vs. BUS Voltage

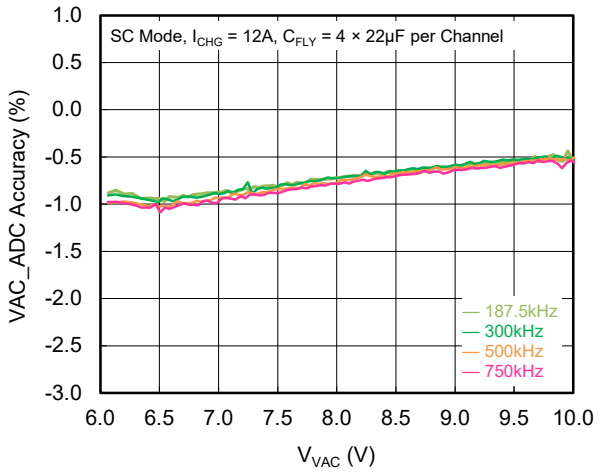


VBUS_ADC Accuracy vs. BUS Voltage

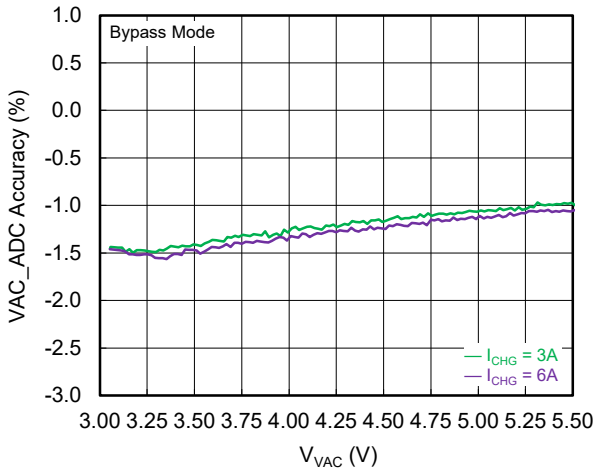


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

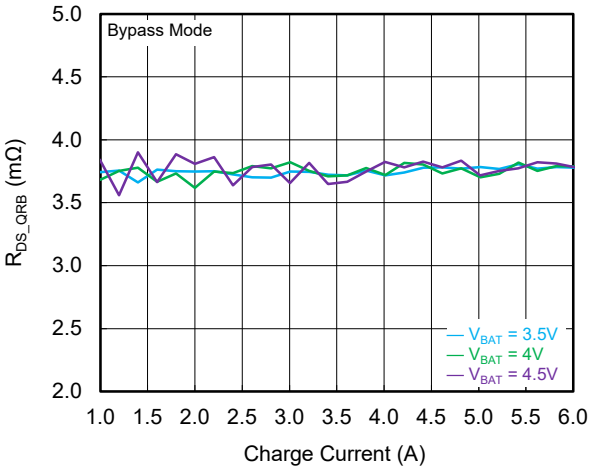
VAC_ADC Accuracy vs. VAC Voltage



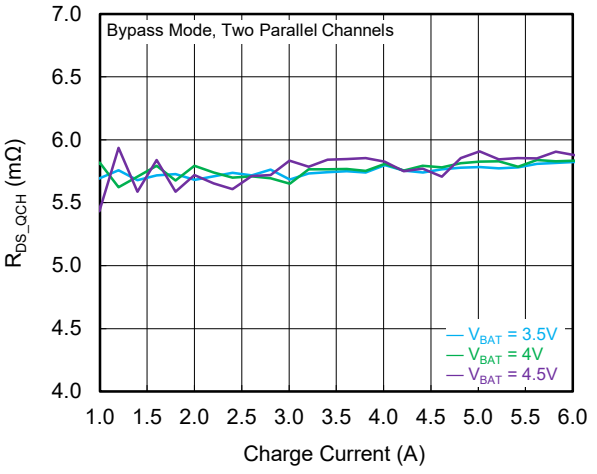
VAC_ADC Accuracy vs. VAC Voltage



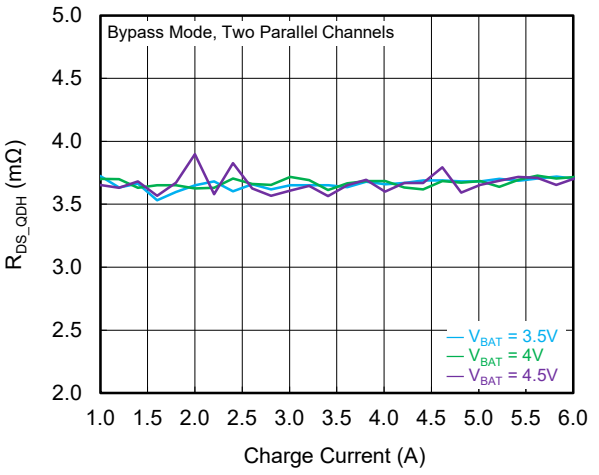
R_{DS_QRB} vs. Charge Current



R_{DS_QCH} vs. Charge Current



R_{DS_QDH} vs. Charge Current



FUNCTIONAL BLOCK DIAGRAM

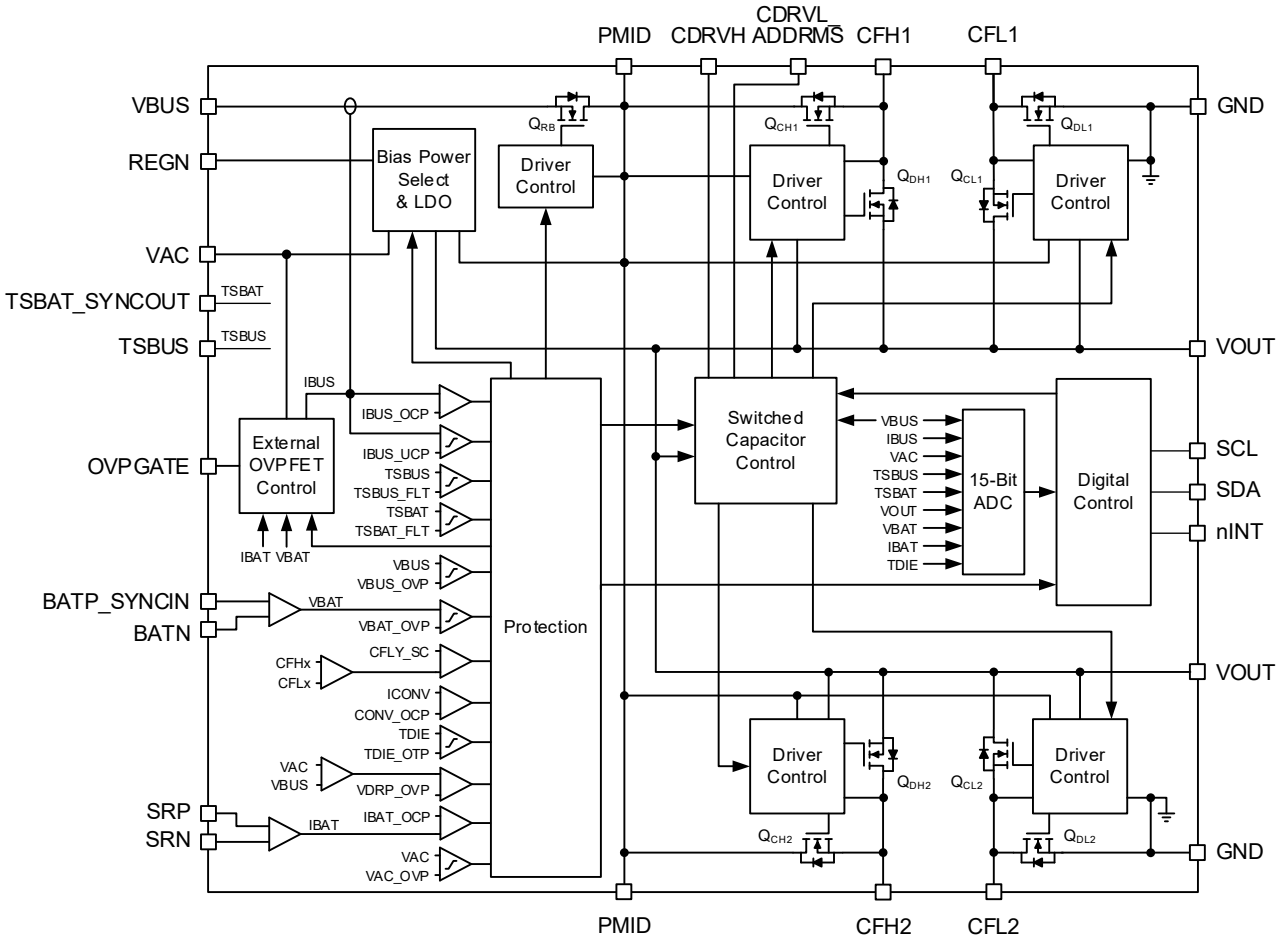


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

The SGM41607 is an efficient 12A battery charger that operates in voltage divider mode (switched-capacitor charge pump) or in bypass mode. A two-phase switched-capacitor core is integrated in the device to minimize the ripples and improve efficiency in the voltage divider mode. A FET control output for protection, a reverse blocking NFET and all other necessary protection features for safe charging are included. A high accuracy 15-bit ADC converter is also included to provide bus voltage, bus current, input voltage, output voltage, battery voltage, battery current, TSBUS, TSBAT and die temperature information for the charge management host via I²C serial interface.

Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. The basic principle of operation is shown in Figure 3. In Period 1, Q1 and Q3 are tuned on and V_{PMID} charges the C_{FLY} and the battery (in series) such that:

$$V_{CFLY} = V_{PMID} - V_{BAT} \quad (1)$$

In Period 2, Q2 and Q4 are turned on and C_{FLY} appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \quad (2)$$

Ignoring the small fluctuation of the capacitor and battery voltages in Period 1 and Period 2 in steady state operation, Equation 1 and Equation 2 can be combined to calculate capacitor voltage.

$$V_{CFLY} = V_{BAT} = V_{PMID}/2 \quad (3)$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID} \times I_{BUS} = V_{BAT} \times I_{BAT} \quad (4)$$

or

$$I_{BUS} = I_{BAT}/2 \quad (5)$$

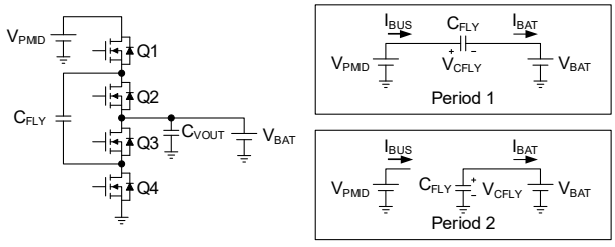


Figure 3. Voltage Divider Charger Operating Principle

Assuming no charge leakage path and considering R_{EFF} as the effective input to output resistance (due to the switch on-resistances and C_{FLY} losses), the divider can be modeled as shown in Figure 4. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The SGM41607 has two phases of such architecture operating at f_{SW} frequency with 180° phase difference. Each phase provides $I_{VOUT}/2$ at the VOUT node, so:

$$V_{VOUT} = ½V_{PMID} - ½R_{EFF} \times I_{VOUT} \quad (6)$$

At low switching frequencies, the capacitor charge sharing losses are dominant and $R_{EFF} \approx 1/(4f_{SW}C_{FLY})$. As frequency increases, R_{EFF} finally approaches $(R_{DS\_QCH} + R_{DS\_QDH} + R_{DS\_QCL} + R_{DS\_QDL})/2$.

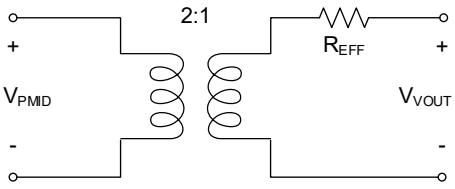


Figure 4. Model of Voltage Divider

The two-phase interleaved operation ensures a smooth input current and simplifies the noise filtering. The VOUT ripple can be estimated by first order approximation of C_{FLY} voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time (15ns, TYP).

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Bypass Mode

The SGM41607 is designed to operate in bypass mode when V_{VBUS} is close to the V_{VOUT}. When such valid voltage is present on VBUS, the device enters bypass mode and all switches between VBUS and VOUT are fully turned on while the other switches are kept off. When V_{VBUS} is near V_{VOUT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 6A (Maximum 6A continuous current is recommended in this mode).

The output voltage is close to the V_{VBUS} minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two phases in parallel. So the R_{EFF} in bypass mode is:

$$R_{EFF}\ (\text{Bypass mode}) \approx R_{DS\_QRB} + (R_{DS\_QCH1} + R_{DS\_QDH1}) \,||\, (R_{DS\_QCH2} + R_{DS\_QDH2}) \quad (7)$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

DETAILED DESCRIPTION (continued)

Charge System

The SGM41607 is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41607. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 5 shows the block diagram of a charge system using the SGM41607 along with other devices. In this system, the SGM41607 can be used to detect the presence of adapter by the PD controller, which is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41607) that provides high current charging. The communication between those devices is through I²C interface.

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 6. The switching charger manages both trickle charge and pre-charge phases. Upon the battery voltage reaching 3V, the adapter negotiates for a higher bus voltage and enables the SGM41607 for charging (either in bypass or voltage divider mode). When battery voltage reaches the V_{BAT_REG} point, the SGM41607 will notify the adapter to decrease current. This action progressively lowers the bus current below the $I_{BUS\_UCP\_F}$ threshold. Alarm availability, as shown in Table 1, is contingent on input power presence and state of charge.

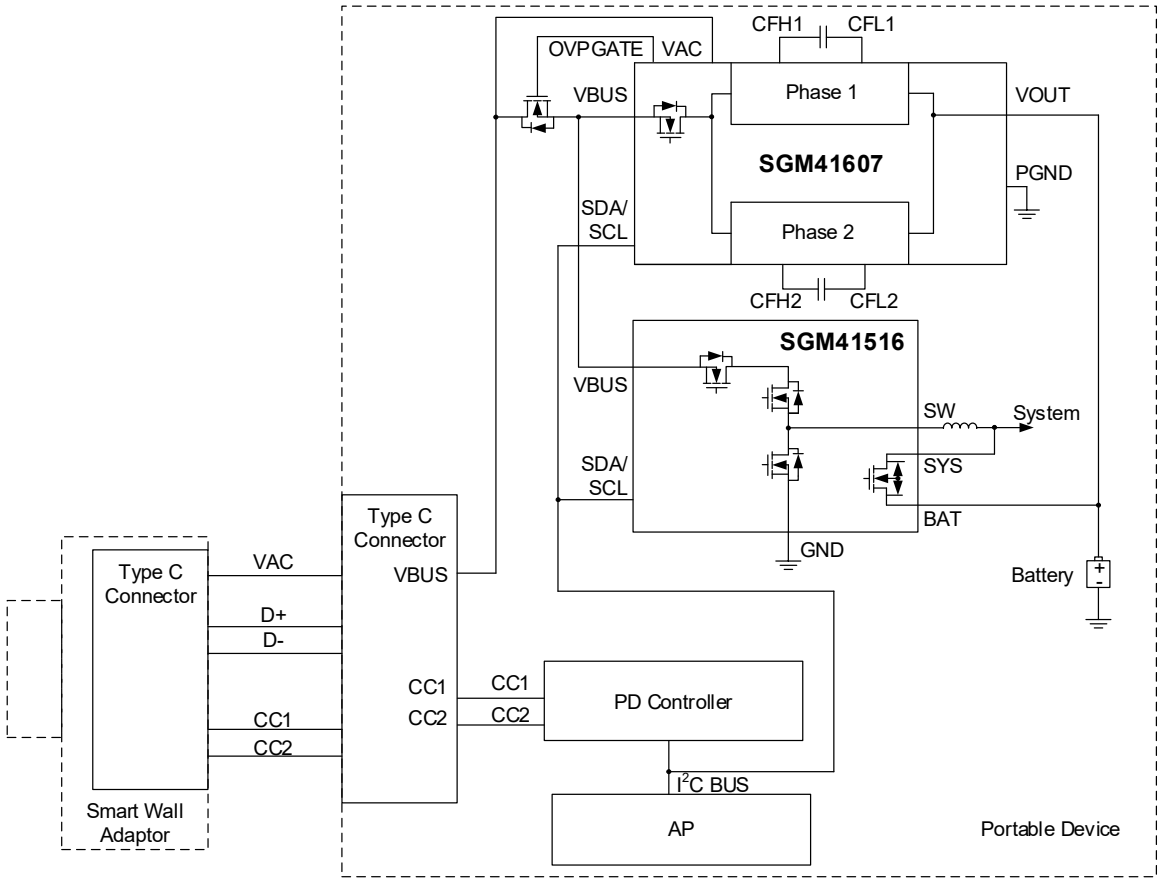


Figure 5. Simplified Charge System

DETAILED DESCRIPTION (continued)

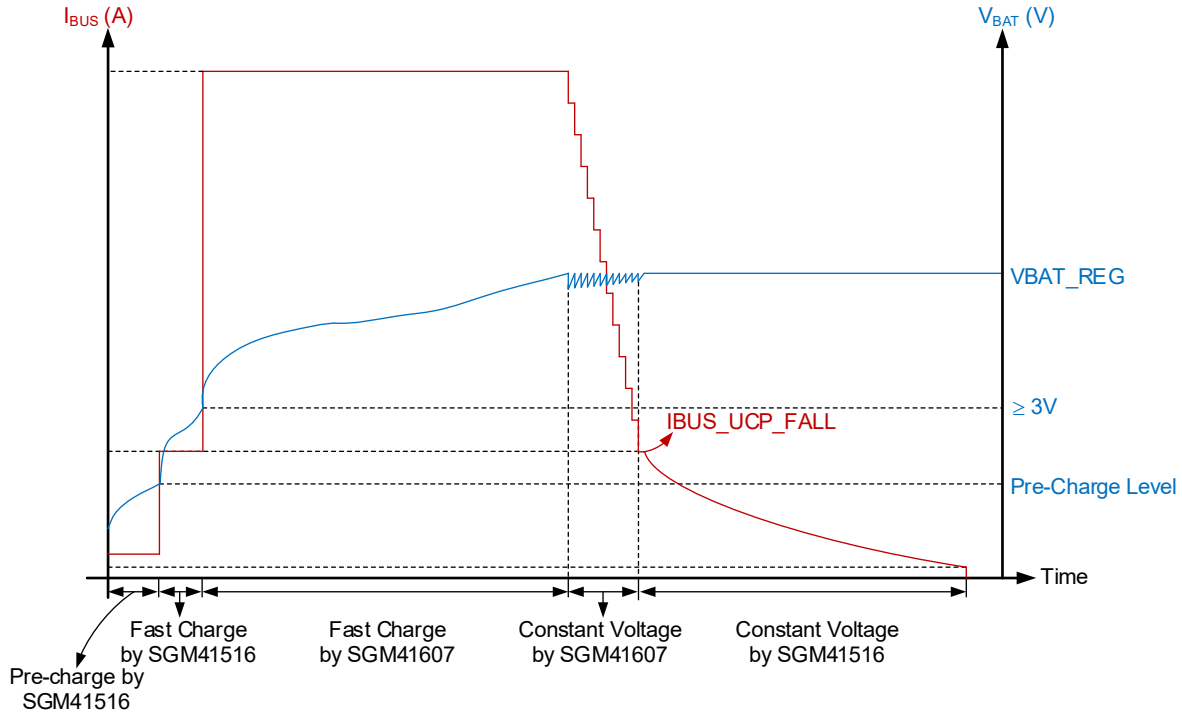


Figure 6. SGM41607 System Charging Profile

Table 1. ALM/FLT Function Activity

ALM/FLT Function	Battery Only	VAC PRESENT CHG_EN = 0	VAC PRESENT CHG_EN = 1
VBATOVP_ALM	Not Active	Not Active	Active
IBATOCP_ALM	Not Active	Not Active	Active
IBATUCP_ALM	Not Active	Not Active	Active
VBUSOVP_ALM	Not Active	Not Active	Active
IBUSOCP_ALM	Not Active	Not Active	Active
TSBUS_FLT	Not Active	Active	Active
TSBAT_FLT	Not Active	Active	Active
TDIEOTP_ALM	Not Active	Active	Active
TSBUS_TSBAT_ALM	Not Active	Active	Active

DETAILED DESCRIPTION (continued)

CDRVH and CDRVL_ADDRMS Functions

For the device to function correctly, a capacitor is required between the CDRVH and CDRVL_ADDRMS pins. The CDRVL_ADDRMS pin both sets the default I²C address and establishes the power-up VAC_OVP threshold for external OVPFET control. Table 2 details how to achieve the desired settings by pulling the CDRVL_ADDRMS pin to GND using various resistors.

Device Power-Up

The device selects its power source from either VBUS or VOUT (battery), prioritizing the higher voltage. A valid supply requires the selected voltage to exceed the respective $V_{VAC\_PRESENT\_R}$ or $V_{BAT\_PRESENT\_R}$ threshold. Once surpassing the applicable $V_{VAC\_UVLO\_R}$ or $V_{OUT\_UVLO\_R}$ level, the device initiates power consumption.

An enabled-by-default watchdog timer stops device switching if communication (read/write) is absent before its expiry. The watchdog timer flag persistently reads '1' on the first access. During initial device power-up, after address pin detection is complete, a nINT pulse is triggered to indicate a watchdog timeout. Host communication must await this initial nINT signal.

The device will not charge when first power-up because the default charging state is never enabled. The ADC is available before charging is enabled, so the host knows the system parameters before charging is enabled. The charger cannot be enabled if the VOUT voltage is not greater than 3V. The minimum charge voltage allowed on V_{VOUT} is 2.8V.

VBUS In-Range (VBUS_LO and VBUS_HI)

The VBUS_LO and VBUS_HI functions are included to avoid problems due to wrong VBUS setting for charging. If V_{VBUS} is less than (V_{VOUT} × 2.05) or above (V_{VOUT} × 2.344) in voltage divider mode, the device remains in charge initiation operation. If the bypass mode is selected, the range is from (V_{VOUT} × 1.025) to (V_{VOUT} × 1.172). Charging will start once V_{VBUS} is within the charge range. VBUS_HI is enabled for SS_TIMEOUT[2:0] time at startup, whereas VBUS_LO is enabled all the time.

Charging Start-Up

Prior to enabling charging, configure all protection thresholds to their desired values using registers REG0x00 to REG0x09 (VBAT_OVP, VBATOVP_ALM, IBAT_OCP, IBATOCP_ALM, IBATUCP_ALM, VAC_PROTECTION, VBUS_OVP, VBUSOVP_ALM, IBUS_OCP_UCP, IBUS_OCP_ALM). The *_OVP and *_OCP registers define thresholds which, if exceeded, cause the charger to stop switching. The *_ALM registers set interrupt thresholds alerting the host to take preventative action before reaching the critical OVP/OCP levels. Their settings depend on required host response time and system operating conditions.

When enabling charging, it is recommended to start with V_{VBUS} close to V_{VOUT} × 2.05. Upon enabling, confirm the CONV_ACTIVE_STAT bit is 1, indicating current flow to the battery. Increasing the bus voltage will raise the battery current. If a current limit source is used, the voltage can be boosted until the current limit is reached. Critically, the bus current (I_{BUS}) must reach the $I_{BUS\_UCP\_R}$ threshold within the time configured via SS_TIMEOUT[2:0] in register REG0x2B. Failure to meet this $I_{BUS\_UCP\_R}$ threshold within the timeout period will cause stopping charging, requiring a restart of the entire sequence.

ADC

The SGM41607 integrates a high accuracy 9-channel, 15-bit ADC converter to monitor input/output currents and voltages, TSBUS, TSBAT and the temperature of the device. The ADC is controlled by the ADC_CTRL0/1 register. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC_AVG bit enables or disables averaging. The ADC operates independent of the faults, unless the host sets the ADC_EN bit to 0.

Table 2. SGM41607 Operating Mode (Master, Slave, Standalone) and I²C Address Configuration

R_{ADDRMS} (kΩ)	I²C Address	VAC_OVP Setting	Operating mode
18	0x65	6.5V	Master
39	0x66	(Disabled)	Slave
75	0x65	6.5V	Standalone
Open (> 150)	0x66	6.5V	Standalone

DETAILED DESCRIPTION (continued)

The ADC can operate if V_{VAC} > $V_{VAC\_PRESENT\_R}$ or V_{VOUT} > $V_{BAT\_PRESENT\_R}$ condition is valid. Otherwise the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CTRL0 and ADC_CTRL1 registers. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

nINT Pin Related Registers

The open-drain nINT pin requires an external pull-up resistor. Normally high, it asserts low during the t_{INT} period to signal a fault or state change to the host. Its behavior is controlled through the INT_STAT, INT_FLAG, INT_MASK, FLT_STAT, FLT_FLAG and FLT_MASK registers. *_STAT registers reflect real-time device status, updating dynamically. *_FLAG registers latch event occurrences; and their bits are cleared upon read access. If the event still exists after reading and clearing the *_FLAG register, another nINT signal will still be sent. The *_MASK register allows masking nINT pin interrupts. However, *_STAT and *_FLAG registers continue updating regardless of whether nINT asserts low.

Parallel Operation

For higher-power systems, parallel operation of two SGM41607 devices reduces adapter requirements, cable losses, and system losses (see Figure 7). Configure device roles via the CDRVL_ADDRMS pin (refer to CDRVH and CDRVL_ADDRMS for details).

When the SGM41607 is set as master, TSBAT_SYNCOUT functions as SYNCOUT and BATP_SYNCIN as BATP. When it is set as slave, TSBAT_SYNCOUT serves as TSBAT and BATP_SYNCIN as SYNCIN. OVPGATE is exclusively controlled by the master, leaving the slave's OVPGATE pin floating. Connect a 1kΩ resistor between REGN and either the master's SYNCIN or the slave's SYNCOUT pin.

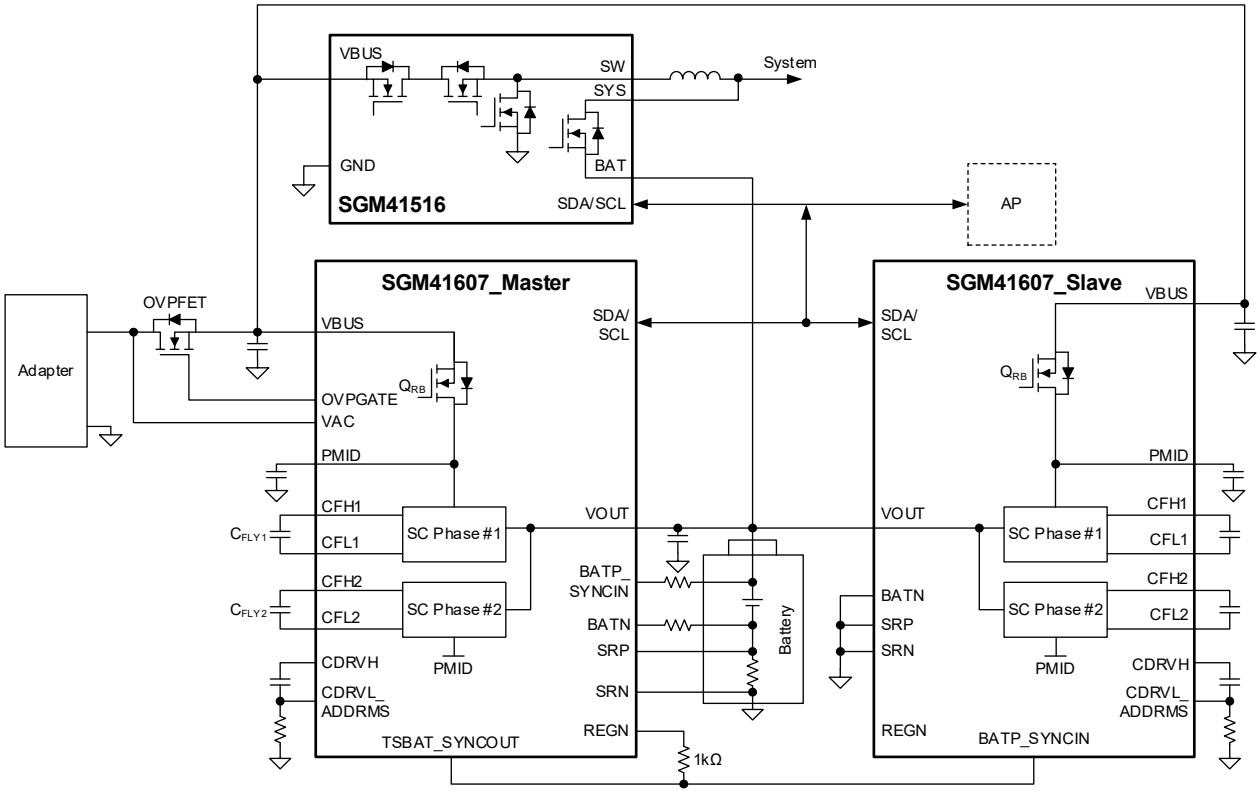


Figure 7. Parallel Operation of SGM41607

DETAILED DESCRIPTION (continued)

Device Modes and Protection Status

Table 3 shows the features and modes of the device depending on the conditions of the device.

Table 3. Device Modes and Protection Status

Functions Available	State						
	BAT-Only (V_{VAC} < $V_{VAC\_PRESENT}$)			V_{VAC} > $V_{VAC\_PRESENT}$			
	V_{VOUT} < $V_{BAT\_PRESENT}$	V_{VOUT} > $V_{BAT\_PRESENT}$		Charge Disabled		During Charge Soft-Start	Charging
	Regardless of ADC	ADC Not Enabled	ADC Enabled	ADC Not Enabled	ADC Enabled	Regardless of ADC	
I²C Allowed	Y	Y	Y	Y	Y	Y	Y
Allow User ADC Request		Y	Y	Y	Y	Y	Y
OVPFET Gate Driver				Y	Y	Y	Y
BAT OVP FLT			Y		Y	Y	Y
BAT OCP FLT						Y	Y
VAC OVP Protection				Y	Y	Y	Y
BUS OVP FLT						Y	Y
BUS OCP FLT						Y	Y
BUS UCP FLT							Y
VOUT_OVP				Y	Y	Y	Y
VBUS_ERROR				Y	Y	Y	Y
TSBUS FLT				Y	Y	Y	Y
TSBAT FLT				Y	Y	Y	Y
TDIE FLT				Y	Y	Y	Y
BATOVP ALM						Y	Y
BATOCP ALM						Y	Y
BUSOVP ALM						Y	Y
BUSOCP ALM						Y	Y
IBATUCP ALM						Y	Y
TSBUS ALM				Y	Y	Y	Y
TSBAT ALM				Y	Y	Y	Y
TDIEOTP ALM				Y	Y	Y	Y
PMID2OUT_UVP						Y	Y
PMID2OUT_OVP						Y	Y

Any protection fault activation forces Q_{RB} shutdown. Masking faults/alarms suppresses nINT assertion without compromising protection. Disabling faults/alarms persistently resets status flags and blocks interrupt generation.

DETAILED DESCRIPTION (continued)

VAC Over-Voltage Protection (VAC_OVP)

The SGM41607 monitors the adapter voltage on the VAC pin to control the external OVPFET using OVPGATE output. The VAC over-voltage protection circuit is powered by VAC and is enabled if V_{VAC} rises above $V_{VAC\_PRESENT\_R}$. If V_{VAC} is above $V_{VAC\_PRESENT\_R}$ threshold for at least $t_{VAC\_IN\_DEG}$ time, a 4.8V gate voltage is sent to the OVPGATE output to turn on the external OVPFET. If the V_{VAC} reaches the VAC_OVP threshold, the gate voltage starts to drop and eventually the OVPFET is fully turned off. Figure 8 shows the VAC_OVP and OVPGATE operation timings. The VAC_OVP threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC pin and the external OVPFET.

Input Short-Circuit Protection (VBUS_SCP)

The VBUS_SCP function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFET is turned on or if V_{VBUS} rises above $V_{VAC\_PRESENT\_R}$ threshold. If the V_{VBUS} falls below 2.5V, the OVPFET is turned off, and charging is stopped. CHG_EN bit is reset to 0 (disable charging).

During charging, if V_{PMID} is less than (2 × V_{VOUT} - 200mV) in divider mode or (V_{VOUT} - 100mV) in bypass mode, or if the Q_{RB} reverse current rises above 4A, the Q_{RB} and OVPFET are turned off, and charging is stopped. CHG_EN bit is reset to 0 (disable charging).

Input, Output and Battery Over-Voltage Protection (VBUS_OVP, VOUT_OVP and VBAT_OVP)

The VBUS_OVP, VOUT_OVP and VBAT_OVP functions detect input and output charge voltage conditions. If either input or output voltage is higher than the protection threshold, the charger is turned off, and CHG_EN bit is reset to 0 (disable charging). The VBUS_OVP function monitors VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBAT_OVP uses BATP_SYNCIN and BATN pins remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a series 100Ω resistor on the BATP_SYNCIN or BATN pin is required. The VBUS_OVP and VBAT_OVP thresholds can be set by I²C serial interface.

Input and Battery Over-Current Protection (IBUS_OCP and IBAT_OCP)

The IBUS_OCP function monitors the input current via Q_{RB}. If CHG_EN bit is set to enable charge, the Q_{RB} is turned on and the IBUS_OCP function starts detecting the input current. If the I_{BUS} reaches IBUS_OCP threshold, the device stops charging and resets CHG_EN bit to 0 (disable charging). The battery current is monitored by the voltage across an external 2mΩ/5mΩ series shunt resistor. This differential voltage is measured between BATN/SRP and SRN pins. If IBAT_OCP threshold is reached, the device stops charging and resets CHG_EN bit to 0 (disable charging). The IBUS_OCP and IBAT_OCP thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q_{RB}. After charging is started, a maximum 100s timer (set by the SS_TIMEOUT[2:0] bits in REG0x2B) is enabled and I_{BUS} current is compared with $I_{BUS\_UCP\_R}$ threshold (selected by the BUSUCP bit in REG0x2B). If I_{BUS} cannot exceed $I_{BUS\_UCP\_R}$ threshold within the 100s period, the charging will be stopped and CHG_EN bit is reset to 0 (disable charging). If I_{BUS} exceeds $I_{BUS\_UCP\_R}$ threshold within the 100s period, the timer is stopped and from then, if I_{BUS} falls below the $I_{BUS\_UCP\_F}$ threshold, the charging will be stopped and CHG_EN bit is reset to 0 (disable charging).

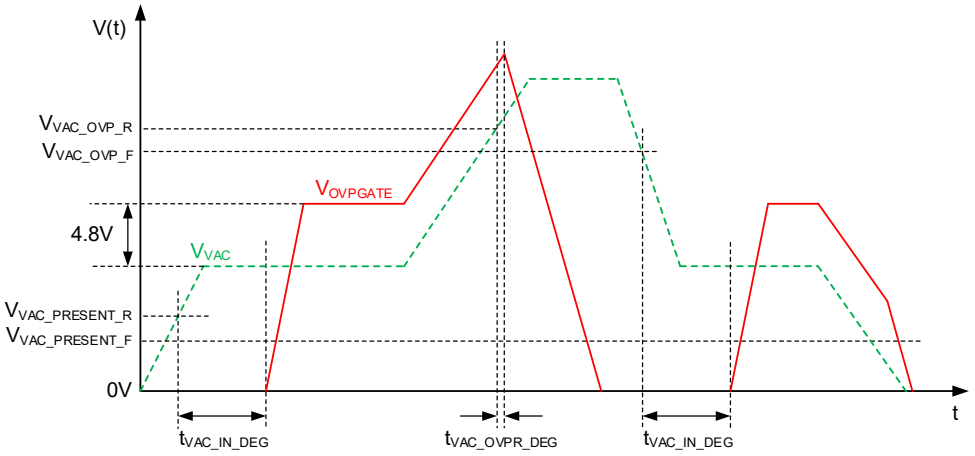


Figure 8. VAC_OVP and OVPGATE Operation Timings

DETAILED DESCRIPTION (continued)

VOUT Short-Circuit Protection (VOUT_SCP)

The VOUT_SCP function monitors the VOUT pin for short-circuit. This function is enabled during charging. If V_{VOUT} falls below 2V threshold, the charger is turned off and CHG_EN bit is reset to 0 (disable charging). Also, the PIN_DIAG_FLAG bit is set to 1, and a nINT pulse is generated.

C_{FLY} Short-Circuit Protection (CFLY_SCP)

The CFLY_SCP function identifies the health of flying capacitors before and during voltage divider switching (charging). The device initialization process is started after CHG_EN bit is set to 1 and MODE bit is set to 0. When V_{VBUS} is in the charge range, the flying capacitors (C_{FLY}) in both phases are pre-charged. A C_{FLY} short-circuit is detected if they cannot be charged, and the voltage between V_{CFHx} and V_{CFLx} remains below 2V. If so, the initialization process is stopped and CHG_EN bit is reset to 0 (disable charging). Even if C_{FLY} capacitors pass the short-circuit test in the initialization process, the CFLY_SCP function remains active and whenever a V_{CFLY} voltage falls below 2V, the charger is turned off and CHG_EN bit is reset to 0 (disable charging). The PIN_DIAG_FLAG bit is set to 1 and a nINT pulse is generated as well. During a CFLY_SCP event, other protection events such as IBUS_OCP, VBAT_OVP or CONV_OCP may occur.

Converter Over-Current Protection (CONV_OCP)

The CONV_OCP function monitors the converter switches operating currents cycle by cycle. If the Q_{CHx} and Q_{DLx} currents reach switching OCP threshold during voltage divider mode, the CONV_OCP_FLAG bit is set to 1 and a nINT pulse is generated, the charging is stopped and CHG_EN bit is reset to 0 (disable charging).

Regulation Feature

The SGM41607 has VBAT_REG, IBUS_REG and IBAT_REG functions to regulate the battery voltage, input and battery current for a short period before the system can re-adjust the conditions such that these functions can be disabled. The regulation thresholds can be set by I²C serial interface.

The VBAT_REG function monitors the differential voltage between BATP_SYNCIN and BATN pins and if the battery voltage is above the V_{BAT_REG} threshold, the OVPGATE voltage is controlled to regulate the battery voltage.

The IBUS_REG function monitors the current flowing through internal RBFET (Q_{RB}), and check whether the I_{BUS_REG} threshold is exceeded the I_{BUS_REG}, the OVPGATE voltage is controlled (reduced) to regulate the input current I_{BUS} to the setting value.

Similarly, the IBAT_REG function monitors the differential voltage between SRP and SRN pins to find the battery current and if the I_{BAT_REG} threshold is exceeded, the OVPGATE voltage is controlled (reduced) to regulate the charge current.

If any regulation condition is triggered, after 150ms deglitch, the corresponding *_REG_ACTIVE_FLAG bit is also set to 1, and a nINT pulse is generated. Then the host can negotiate with the adapter to reduce the current.

If VBAT or IBAT regulation functions is triggered and persist for 650ms, the charging will be stopped, REGULATION_EN and CHG_EN bit are reset to 0 (disable charging); If IBUS regulation functions is triggered and persist for 650ms, the charging will be stopped, IBUS_REG_EN and CHG_EN bits are reset to 0 (disable charging).The system should adjust the charging conditions to prevent the battery voltage and current regulation for more than 650ms (or prevent triggering of the VDROP_OVP).

Dropout Over-Voltage Protection (VDROP_OVP)

When VBAT_REG or IBUS_REG or IBAT_REG is active, a large voltage drop may appear on the external OVPFET and cause excessive power loss and heat. To avoid that, the VDROP_OVP function monitors the voltage drop between VAC and VBUS pins. If it is higher than V_{DROP_OVP} threshold with t_{VDROP_OVP} deglitch time (set by VDROP_DEGLITCH_SET bit in REG0x05), the charging will be stopped and CHG_EN bit is reset to 0 (disable charging). The V_{DROP_OVP} threshold and t_{VDROP_OVP} deglitch time can be programmed by I²C serial interface.

TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents charging in over-temperature condition. The die temperature is monitored and if the +150℃ threshold is reached, the charging is stopped and CHG_EN bit is reset to 0 (disable charging). The startup sequence cannot be initiated again until the die temperature falls down to +120℃.

DETAILED DESCRIPTION (continued)

Battery and Cable Connector Temperature Monitoring (TSBAT_FLT and TSBUS_FLT)

The device employs three dedicated temperature sensors for charging protection: TSBUS (cable connector), TSBAT (battery), and TDIE (internal junction). TSBUS and TSBAT exclusively activate with input power applied, operating through a resistor divider network powered by VOUT. An NTC thermistor must be connected in parallel with the low-side resistor (R_{T1}). Temperature faults trigger when the pin voltage crosses the falling-edge threshold (indicating high-temperature conditions), with thresholds programmable via TSBUS_FLT and TSBAT_FLT registers. A TSBUS_TSBAT_ALM interrupt generates when temperature reaches ±5% of the FLT setting; disabling these registers suppresses this alarm. Resistor selection requires matching values: for 10kΩ NTC use 10kΩ R_{T1}/R_{T2}, and for 100kΩ NTC use 100kΩ R_{T1}/R_{T2}. The voltage ratio V_{TSBUS}/V_{VOUT} or V_{TSBAT}/V_{VOUT} varies from 0% to 50%, determined by the following equation:

$$V_{TSBUS} \text{ or } V_{TSBAT} \text{ (V)} = \frac{\frac{1}{(\frac{1}{R_{NTC}}+\frac{1}{R_{T1}})}}{R_{T2}+(\frac{1}{R_{NTC}}+\frac{1}{R_{T1}})} \times V_{REGN} \quad (8)$$

The percentage of the TS pin voltage is determined by the following equation.

$$\text{TSBUS or TSBAT (\%)} = \frac{\frac{1}{(\frac{1}{R_{NTC}}+\frac{1}{R_{T1}})}}{R_{T2}+(\frac{1}{R_{NTC}}+\frac{1}{R_{T1}})} \quad (9)$$

The device additionally incorporates an internal die temperature monitor with configurable alarm threshold (TDIEOTP_ALM). Any unused temperature protection features (TSBUS, TSBAT, or TDIE) can be disabled by writing 1 to their respective disable bits (TSBUS_FLT_DIS, TSBAT_FLT_DIS, TDIE_OTP_DIS) in the CHRG_CTRL register. Upon triggering of TSBUS_FLT or TSBAT_FLT thresholds, the device forces CHG_EN to 0b, requiring re-initializing the startup sequence to resume charging. Using the TDIE_ALM register, an alarm can be set to notify the host when the device die temperature exceeds a threshold. When the alarm threshold is reached, the device does not automatically stop switching. The host can decide to take action to reduce the temperature, such as reducing the charging current. When the T_{DIE_OTP} threshold is reached, the device will automatically stop switching.

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

The device I²C Address is determined by the state of CDRVL_ADDRMS pin in the POR sequence, as described in CDRVH and CDRVL_ADDRMS functions section.

Table 4. Registers Main Function List

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
REG_RST	--	--	--	--	0x0B[7]	--
CHG_EN	--	--	--	--	0x0C[7]	--
CHG_MODE	--	--	--	0x31[0]	--	--
VDROP_OVP	0x2C[1]	0x2D[5]	0x2D[1]	0x05[4]	--	0x05[3]
WATCHDOG	--	0x0B[3]	--	0x0B[1:0]	0x0B[2]	--
FSW_SET	--	--	--	0x0B[6:4]	--	--
FSW_SHIFT	--	--	--	0x0C[4:3]	--	--
PMID2VOUT_OVP	0x2F[0]	0x2F[2]	--	--	--	--
PMID2VOUT_UVP	0x2F[1]	0x2F[3]	--	--	--	--
VBUS_OVP	0x10[5]	0x11[5]	0x12[5]	0x06[6:0]	--	--
VBUSOVP_ALM	0x0D[5]	0x0E[5]	0x0F[5]	0x07[6:0]	0x07[7]	--
IBUS_OCP	0x10[4]	0x11[4]	0x12[4]	0x08[3:0]	0x08[7]	--
IBUSOCP_ALM	0x0D[4]	0x0E[4]	0x0F[4]	0x09[6:0]	0x09[7]	--
VAC_OVP	0x05[7]	0x05[6]	0x05[5]	0x05[2:0]	--	--
CONV_OCP	--	0x0A[1]	--	--	--	--
VOUT_OVP	0x2C[0]	0x2D[4]	0x2D[0]	--	0x2B[3]	--
VBAT_OVP	0x10[7]	0x11[7]	0x12[7]	0x00[5:0]	0x00[7]	--
VBATOVP_ALM	0x0D[7]	0x0E[7]	0x0F[7]	0x01[5:0]	0x01[7]	--
IBAT_OCP	0x10[6]	0x11[6]	0x12[6]	0x02[6:0]	0x02[7]	--
IBATOCP_ALM	0x0D[6]	0x0E[6]	0x0F[6]	0x03[6:0]	0x03[7]	--
IBATUCP_ALM	0x0D[3]	0x0E[3]	0x0F[3]	0x04[6:0]	0x04[7]	--
VAC_PDN	--	--	--	--	0x2B[0]	--
VBUS_PDN	--	--	--	--	0x06[7]	--
IBUS_REG	0x30[6]	0x30[5]	0x30[4]	0x30[3:0]	0x30[7]	--
VBAT_REG	0x2C[3]	0x2D[7]	0x2D[3]	0x2C[5:4]	--	--
IBAT_REG	0x2C[2]	0x2D[6]	0x2D[2]	0x2C[7:6]	--	--
IBUS_UCP_RISE	--	0x08[6]	0x08[5]	0x2B[2]	--	--
IBUS_UCP_FALL	--	0x08[4]	--	--	--	0x2E[3]
SS_TIMEOUT	--	0x0A[3]	--	0x2B[7:5]		--
TSBUS_FLT	0x10[1]	0x11[1]	0x12[1]	0x28[7:0]	0x0C[2]	--
TSBAT_FLT	0x10[2]	0x11[2]	0x12[2]	0x29[7:0]	0x0C[1]	--
PIN_DIAG	--	0x0A[0]	--	--	--	--
TSBUS_TSBAT_ALM	0x10[3]	0x11[3]	0x12[3]	--	--	--
TDIE_OTP_ALM	0x10[0]	0x11[0]	0x12[0]	0x2A[7:0]	--	--
TDIE_OTP	0x0A[6]	0x0A[7]	--	--	0x0C[0]	--
VBUS_LO	0x0A[5]	--	--	--	--	0x2E[4]

REGISTER MAPS (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
VBUS_HI	0x0A[4]	--	--	--	--	--
CONV_SWITCHING	0x0A[2]	--	--	--	--	--
ADAPTER_INSERT	0x0D[2]	0x0E[2]	0x0F[2]	--	--	--
VBAT_INSERT	0x0D[1]	0x0E[1]	0x0F[1]	--	--	--
ADC_DONE	0x0D[0]	0x0E[0]	0x0F[0]	--	--	--
ADC_EN	--	--	--	--	0x14[7]	--
VBUS_ADC	--	--	--	--	0x15[7]	--
IBUS_ADC	--	--	--	--	0x14[0]	--
VAC_ADC	--	--	--	--	0x15[6]	--
VBAT_ADC	--	--	--	--	0x15[4]	--
IBAT_ADC	--	--	--	--	0x15[3]	--
VOUT_ADC	--	--	--	--	0x15[5]	--
TSBUS_ADC	--	--	--	--	0x15[2]	--
TSBAT_ADC	--	--	--	--	0x15[1]	--
TDIE_ADC	--	--	--	--	0x15[0]	--
REGULATION_EN	--	--	--	--	0x2B[4]	--
IBAT_RSNS	--	--	--	0x2B[1]	--	--

REGISTER MAPS (continued)

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a 1 clears the bit. Writing a '0' has no effect.

NOTE: Except for the specified bits, all other register bits are reset to their default values if a hard reset is triggered.

REG0x00: VBAT_OVP Register [reset = 0x22]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_OVP_DIS	0b	R/W	VBAT OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6]	Reserved	0b	R	Reserved	N/A
D[5:0]	VBAT_OVP[5:0]	100010b	R/W	VBAT OVP Protection Rising Threshold Setting Bits $V_{BAT\_OVP\_R}$ = 3.475V + VBAT_OVP[5:0] × 25mV Offset: 3.475V Range: 3.475V (000000b) – 5.05 (111111b) Default: 4.325V (100010b)	REG_RST

REG0x01: VBATOVP_ALM Register [reset = 0x1C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBATOVP_ALM_DIS	0b	R/W	VBAT OVP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6]	Reserved	0b	R	Reserved	N/A
D[5:0]	VBATOVP_ALM[5:0]	011100b	R/W	VBAT OVP Alarm Rising Threshold Setting Bits $V_{BATOVP\_ALM\_R}$ = 3.5V + VBATOVP_ALM[5:0] × 25mV Offset: 3.5V Range: 3.5V (000000b) – 5.075V (111111b) Default: 4.2V (011100b) The VBAT OVP alarm rising threshold should be set lower than $V_{BAT\_OVP\_R}$ to ensure proper operation.	REG_RST

REG0x02: IBAT_OCP Register [reset = 0x52]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_OCP_DIS	0b	R/W	IBAT OCP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6:0]	IBAT_OCP[6:0]	1010010b	R/W	IBAT OCP Protection Threshold Setting Bits I_{BAT_OCP} = 3A + IBAT_OCP[6:0] × 100mA Offset: 3A Range: 3A (0000000b) – 13A (1100100b) Default: 11.2A (1010010b)	REG_RST

REGISTER MAPS (continued)

REG0x03: IBATOCP_ALM Register [reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBATOCP_ALM_DIS	0b	R/W	IBAT OCP Alarm Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6:0]	IBATOCP_ALM[6:0]	1010000b	R/W	IBAT OCP Alarm Rising Threshold Setting Bits $I_{BATOCP\_ALM\_R}$ = 3A + IBATOCP_ALM[6:0] × 100mA Offset: 3A Range: 3A (0000000b) – 13A (1100100b) Default: 11A (1010000b) The IBAT OCP alarm rising threshold should be set lower than I_{BAT_OCP} to ensure proper operation.	REG_RST

REG0x04: IBATUCP_ALM Register [reset = 0x28]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBATUCP_ALM_DIS	0b	R/W	IBAT UCP Alarm Disable Bit 0 = Enable (default) 1 = Disable	REG_RST
D[6:0]	IBATUCP_ALM[6:0]	0101000b	R/W	IBAT UCP Alarm Threshold Setting Bits I_{BATUCP_ALM} = 1A + IBATUCP_ALM[6:0] × 50mA Offset: 1A Range: 1A (0000000b) – 7.35A (1111111b) Default: 3A (0101000b) The IBAT UCP alarm threshold should be set lower than I_{BAT_OCP} to ensure proper operation.	REG_RST

REG0x05: VAC_PROTECTION Register [reset = 0x07]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC_OVP_STAT	0b	R	VAC OVP Fault Status Bit 0 = Device not in VAC OVP fault status (default) 1 = Device in VAC OVP fault status	REG_RST
D[6]	VAC_OVP_FLAG	0b	RC	VAC OVP Fault Flag Bit 0 = No VAC OVP fault (default) 1 = VAC OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	REG_RST
D[5]	VAC_OVP_MASK	0b	R/W	Mask VAC OVP Fault Interrupt 0 = VAC OVP fault interrupt can work (default) 1 = Mask VAC OVP fault interrupt. VAC_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[4]	VDROP_ THRESHOLD_SET	0b	R/W	Voltage Difference between VAC and VBUS that will Cause the Device to Stop Switching 0 = 300mV (TYP) (default) 1 = 400mV (TYP)	N/A
D[3]	VDROP_DEGLITCH_ SET	0b	R/W	Deglitch Time after the Device Reaches the VDROP threshold before the part stops switching. 0 = 8μs (TYP) (default) 1 = 5ms (TYP)	REG_RST
D[2:0]	VAC_OVP[2:0]	111b	R/W	VAC OVP Protection Rising Threshold Setting Bits 000 = 11V 001 = 12V 010 = 13V 011 = 14V 100 = 15V 101 = 16V 110 = 17V 111 = 6.5V (default) Exceeding the programmed VAC threshold triggers OVPGATE to turn off OVPFET.	REG_RST

REGISTER MAPS (continued)

REG0x06: VBUS_OVP Register [reset = 0x3A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_PDN_EN	0b	R/W	VBUS Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, it will turn off the external OVPFET and discharge VBUS and PMID. This action is important during a hot-plug event to prevent transient over-voltages.	REG_RST
D[6:0]	VBUS_OVP[6:0]	0111010b	R/W	VBUS OVP Protection Rising Threshold Setting Bits. $V_{BUS\_OVP\_R}$ = 5.95V + VBUS_OVP[6:0] × 50mV Offset: 5.95V Range: 5.95V (0000000b) – 12.3V (1111111b) Default: 8.85V (0111010b)	REG_RST

REG0x07: VBUSOVP_ALM Register [reset = 0x38]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUSOVP_ALM_DIS	0b	R/W	VBUS OVP Alarm Disable Bit 0 = Enabled (Default) 1 = Disabled	REG_RST
D[6:0]	VBUSOVP_ALM[6:0]	0111000b	R/W	VBUS OVP Protection Rising Threshold Setting Bits $V_{BUSOVP\_ALM\_R}$ = 6V + VBUSOVP_ALM[6:0] × 50mV Offset: 6V Range: 6V (0000000b) – 12.35V (1111111b) Default: 8.8V (0111000b)	REG_RST

REG0x08: IBUS_OCP_UCP Register [reset = 0x0B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_OCP_DIS	0b	R/W	IBUS OCP Protection Disable bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6]	IBUS_UCP_RISE_FLAG	0b	RC	IBUS UCP Rise Event Flag 0 = No IBUS UCP rise event (default) 1 = IBUS UCP rise event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	REG_RST
D[5]	IBUS_UCP_RISE_MASK	0b	R/W	Mask IBUS UCP Rise Event Interrupt 0 = IBUS UCP rise event interrupt can work (default) 1 = Mask IBUS UCP rise event interrupt. IBUS_UCP_RISE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	IBUS_UCP_FALL_FLAG	0b	RC	IBUS UCP Fall Event Flag 0 = No IBUS UCP fall event (default) 1 = IBUS UCP fall event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	REG_RST
D[3:0]	IBUS_OCP[3:0]	1011b	R/W	IBUS OCP Protection Threshold Setting Bits I_{BUS_OCP} = 3A + IBUS_OCP[3:0] × 250mA Offset:3A Range: 3A (0000b) – 6.75A (1111b) Default: 5.75A (1011b)	REG_RST

REGISTER MAPS (continued)

REG0x09: IBUSOCP_ALM Register [reset = 0x65]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUSOCP_ALM_DIS	0b	R/W	IBUS OCP Alarm Disable bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[6:0]	IBUSOCP_ALM[6:0]	1100101b	R/W	IBUS OCP Alarm Rising Threshold Setting Bits $I_{BUSOCP\_ALM\_R}$ = 0.45A + IBUSOCP_ALM[6:0] × 50mA Offset:0.45A Range: 0.45A (0000000b) – 6.8A (1111111b) Default: 5.5A (1100101b) The IBUS OCP alarm rising threshold should be set lower than I_{BUS_OCP} to ensure proper operation.	REG_RST

REG0x0A: CONVERTER_STAT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TDIE_OTP_FLAG	0b	RC	TDIE Over-Temperature Fault Flag Bit 0 = No TDIE over-temperature fault (default) 1 = TDIE over-temperature fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	REG_RST
D[6]	TDIE_OTP_STAT	0b	R	TDIE Over-Temperature Fault Status Bit 0 = Device not in TDIE over-temperature fault status (default) 1 = Device in TDIE over-temperature fault status	REG_RST
D[5]	VBUS_LO_STAT	0b	R	VBUS_LO Status Bit 0 = Not in VBUS_LO status (default) 1 = In VBUS_LO status	REG_RST
D[4]	VBUS_HI_STAT	0b	R	VBUS_HI Status Bit 0 = Not in VBUS_HI status (default) 1 = In VBUS_HI status	REG_RST
D[3]	SS_TIMEOUT_FLAG	0b	RC	Soft-Start Timeout Flag Bit 0 = No soft-start timeout event (default) 1 = Soft-start timeout event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	CONV_ACTIVE_STAT	0b	R	Converter Active Status Bit 0 = Converter not running (default) 1 = Converter running	N/A
D[1]	CONV_OCP_FLAG	0b	RC	CONV_OCP Fault Flag Bit 0 = No CONV_OCP fault (default) 1 = CONV_OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	PIN_DIAG_FLAG	0b	RC	Pin Diagnosis Fail Fault Flag When switching is enabled, certain conditions are checked on the C_{FLY} and VOUT pins to assure proper operation. 0 = Normal (default) 1 = C_{FLY} short or VOUT pin short fault has occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	REG_RST

REGISTER MAPS (continued)

REG0x0B: CONTROL Register [reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0b	R/WC	0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default values and then this bit is automatically reset to 0.	REG_RST
D[6:4]	FSW_SET[2:0]	100b	R	Switched-Cap Converter Switching Frequency Setting Bits 000 = 187.5kHz 001 = 250kHz 010 = 300kHz 011 = 375kHz 100 = 500kHz (default) 101 - 111 = 750kHz If operation mode is master or slave, max PWM frequency is 500kHz.	N/A
D[3]	WDT_FLAG	0b	RC	Watchdog Timeout Fault Flag Bit 0 = No watchdog timeout fault (default) 1 = Watchdog timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	REG_RST
D[2]	WDT_DIS	0b	R/W	Watchdog Enable Bit 0 = Watchdog enabled (default) 1 = Watchdog disabled	REG_RST
D[1:0]	WDT_TIMER[1:0]	00b	R/W	Watchdog Timer Setting Bits (Cleared by any completed read or write I²C transaction) 00 = 0.5s (default) 01 = 1s 10 = 5s 11 = 30s	REG_RST

REG0x0C: CHRG_CTRL Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CHG_EN	0b	R/W	Charge Enable Bit 0 = Disabled (default) 1 = Enabled. If any fault has occurred, device returns to standby mode and this bit is automatically cleared to 0.	REG_RST or Watchdog
D[6:5]	MS[1:0]	00b	R	Master, Slave, or Standalone Operation 00 = Standalone (default) 01 = Slave 10/11 = Master	REG_RST
D[4:3]	FREQ_SHIFT[1:0]	00b	R/W	Bits of Adjusting Switching Frequency 00 = Nominal frequency (default) 01 = Nominal frequency +10% 10 = Nominal frequency -10% 11 = Spread spectrum varies frequency ±10%	REG_RST
D[2]	TSBUS_FLT_DIS	0b	R/W	TSBUS_FLT Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[1]	TSBAT_FLT_DIS	0b	R/W	TSBAT_FLT Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST
D[0]	TDIE_OTP_DIS	0b	R/W	TDIE OTP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	REG_RST

REGISTER MAPS (continued)

REG0x0D: INT_STAT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBATOVP_ALM_STAT	0b	R	VBAT OVP Alarm Status Bit 0 = Device not in VBAT OVP alarm status (default) 1 = Device in VBAT OVP alarm status	N/A
D[6]	IBATOCP_ALM_STAT	0b	R	IBAT OCP Alarm Status Bit 0 = Device not in IBAT OCP alarm status (default) 1 = Device in IBAT OCP alarm status	N/A
D[5]	VBUSOVP_ALM_STAT	0b	R	VBUS OVP Alarm Status Bit 0 = Device not in VBUS OVP alarm status (default) 1 = Device in VBUS OVP alarm status	N/A
D[4]	IBUSOCP_ALM_STAT	0b	R	IBUS OCP Alarm Status Bit 0 = Device not in IBUS OCP alarm status (default) 1 = Device in IBUS OCP alarm status	N/A
D[3]	IBATUCP_ALM_STAT	0b	R	IBAT UCP Alarm Status Bit 0 = Device not in IBAT UCP alarm status (default) 1 = Device in IBAT UCP alarm status	N/A
D[2]	ADAPTER_INSERT_STAT	0b	R	Adapter Insert Status Bit 0 = Device not in ADAPTER_INSERT status (default) 1 = Device in ADAPTER_INSERT status	N/A
D[1]	VBAT_INSERT_STAT	0b	R	VBAT_INSERT Status Bit 0 = Device not in VBAT_INSERT status (default) 1 = Device in VBAT_INSERT status	N/A
D[0]	ADC_DONE_STAT	0b	R	ADC Conversion Status Bit In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = Conversion not complete (default) 1 = Conversion complete	N/A

REGISTER MAPS (continued)

REG0x0E: INT_FLAG Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBATOVP_ALM_FLAG	0b	RC	Mask VBAT OVP Alarm Interrupt 0 = VBAT OVP alarm interrupt can work (default) 1 = Mask VBAT OVP alarm interrupt. VBATOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[6]	IBATOCP_ALM_FLAG	0b	RC	Mask IBAT OCP Alarm Interrupt 0 = IBAT OCP alarm interrupt can work (default) 1 = Mask IBAT OCP alarm interrupt. IBATOCP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[5]	VBUSOVP_ALM_FLAG	0b	RC	Mask VBUS OVP Alarm Interrupt 0 = VBUS OVP alarm interrupt can work (default) 1 = Mask VBUS OVP alarm interrupt. VBUSOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	N/A
D[4]	IBUSOCP_ALM_FLAG	0b	RC	IBUS OCP Alarm Flag Bit 0 = No IBUS OCP alarm (default) 1 = IBUS OCP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	IBATUCP_ALM_FLAG	0b	RC	IBAT UCP Alarm Flag Bit 0 = No IBAT UCP alarm (default) 1 = IBAT UCP alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	ADAPTER_INSERT_FLAG	0b	RC	Adapter Insert Event Flag This bit is set to 1 if $V_{VAC} > V_{VAC\_PRESENT\_R}$. 0 = No adapter insert event 1 = Adapter insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the adapter is absent, reading this bit will reset it to 0	N/A
D[1]	VBAT_INSERT_FLAG	0b	RC	VBAT Insert Event Flag If ADC_EN bit = 1 or $V_{VAC} > V_{VAC\_PRESENT\_R}$ or $V_{VBUS} > V_{BUS\_PRESENT\_R}$, this bit will set to 1 when $V_{BATP} > V_{BAT\_PRESENT\_R}$. 0 = No VBAT insert event 1 = VBAT insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the battery is absent, reading this bit will reset it to 0.	N/A
D[0]	ADC_DONE_FLAG	0b	RC	ADC Conversion Complete Event Flag Bit In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = Normal (default) 1 = ADC conversion has completed. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x0F: INT_MASK Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBATOVP_ALM_MASK	0b	R/W	Mask VBAT OVP Alarm Interrupt 0 = VBAT OVP alarm interrupt can work (default) 1 = Mask VBAT OVP alarm interrupt. VBATOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	IBATOCP_ALM_MASK	0b	R/W	Mask IBAT OCP Alarm Interrupt 0 = IBAT OCP alarm interrupt can work (default) 1 = Mask IBAT OCP alarm interrupt. IBATOCP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	VBUSOVP_ALM_MASK	0b	R/W	Mask VBUS OVP Alarm Interrupt 0 = VBUS OVP alarm interrupt can work (default) 1 = Mask VBUS OVP alarm interrupt. VBUSOVP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	IBUSOCP_ALM_MASK	0b	R/W	Mask IBUS OCP Fault Interrupt 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[3]	IBATUCP_ALM_MASK	0b	R/W	Mask IBAT UCP Fault Interrupt 0 = IBAT UCP fault interrupt can work (default) 1 = Mask IBAT UCP fault interrupt. IBAT UCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[2]	ADAPTER_INSERT_MASK	0b	R/W	Mask ADAPTER_INSERT Event Interrupt 0 = ADAPTER_INSERT event interrupt can work (default) 1 = Mask ADAPTER _INSERT event interrupt. ADAPTER_INSERT_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VBAT_INSERT_MASK	0b	R/W	Mask VBAT_INSERT Event Interrupt 0 = VBAT_INSERT event interrupt can work (default) 1 = Mask VBAT_INSERT event interrupt. VBAT_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	ADC_DONE_MASK	0b	R/W	Mask ADC Complete Event Interrupt 0 = ADC_DONE event interrupt can work (default) 1 = Mask ADC_DONE event interrupt. ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x10: FLT_STAT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_OVP_STAT	0b	R	VBAT OVP Fault Status Bit 0 = Device not in VBAT OVP fault status (default) 1 = Device in VBAT OVP fault status	N/A
D[6]	IBAT_OCP_STAT	0b	R	IBAT OCP Fault Status Bit 0 = Device not in IBAT OCP fault status (default) 1 = Device in IBAT OCP fault status	N/A
D[5]	VBUS_OVP_STAT	0b	R	VBUS OVP Fault Status Bit 0 = Device not in VBUS OVP fault status (default) 1 = Device in VBUS OVP fault status	N/A
D[4]	IBUS_OCP_STAT	0b	R	IBUS OCP Fault Status Bit 0 = Device not in IBUS OCP fault status (default) 1 = Device in IBUS OCP fault status	N/A
D[3]	TSBUS_TSBAT_ALM_STAT	0b	R	TSBUS and TSBAT Alarm Status Bit 0 = TSBUS or TSBAT threshold is not within 5% of the TSBUS_FLT or TSBAT_FLT set threshold (default) 1 = TSBUS or TSBAT threshold is within 5% of the TSBUS_FLT or TSBAT_FLT set threshold	N/A
D[2]	TSBAT_FLT_STAT	0b	R	TSBAT_FLT Status Bit 0 = Device not in TSBAT_FLT status (default) 1 = Device in TSBAT_FLT status	N/A
D[1]	TSBUS_FLT_STAT	0b	R	TSBUS_FLT Status Bit 0 = Device not in TSBUS_FLT status (default) 1 = Device in TSBUS_FLT status	N/A
D[0]	TDIEOTP_ALM_STAT	0b	R	TDIE Over-Temperature Alarm Status Bit 0 = Device not in TDIE over-temperature alarm status (default) 1 = Device in TDIE over-temperature alarm status	N/A

REGISTER MAPS (continued)

REG0x11: FLT_FLAG Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_OVP_FLAG	0b	RC	VBAT OVP Fault Flag Bit 0 = No VBAT OVP fault (default) 1 = VBAT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	IBAT_OCP_FLAG	0b	RC	IBAT OCP Fault Flag Bit 0 = No IBAT OCP fault (default) 1 = IBAT OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	VBUS_OVP_FLAG	0b	RC	VBUS OVP Fault Flag Bit 0 = No VBUS OVP fault (default) 1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	IBUS_OCP_FLAG	0b	RC	IBUS OCP Fault Flag Bit 0 = No IBUS OCP fault (default) 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	TSBUS_TSBAT_ALM_FLAG	0b	RC	TSBUS_TSBAT Alarm Flag Bit 0 = No TSBUS_TSBAT alarm (default) 1 = TSBUS_TSBAT alarm has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[2]	TSBAT_FLT_FLAG	0b	RC	TSBAT_FLT Flag Bit 0 = No TSBAT Fault (default) 1 = TSBAT fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	TSBUS_FLT_FLAG	0b	RC	TSBUS_FLT Flag Bit 0 = No TSBUS Fault (default) 1 = TSBUS fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	TDIEOTP_ALM_FLAG	0b	RC	TDIE Over-Temperature Alarm Flag Bit 0 = No TDIE over-temperature alarm (default) 1 = TDIE over-temperature alarm has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER MAPS (continued)

REG0x12: FLT_MASK Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_OVP_MASK	0b	R/W	Mask VBAT OVP Fault Interrupt 0 = VBAT OVP fault interrupt can work (default) 1 = Mask VBAT OVP fault interrupt. VBAT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[6]	IBAT_OCP_MASK	0b	R/W	Mask IBAT OCP Fault Interrupt 0 = IBAT OCP fault interrupt can work (default) 1 = Mask IBAT OCP fault interrupt. IBAT_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[5]	VBUS_OVP_MASK	0b	R/W	Mask VBUS OVP Fault Interrupt 0 = VBUS OVP fault interrupt can work (default) 1 = Mask VBUS OVP fault interrupt. VBUS_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[4]	IBUS_OCP_MASK	0b	R/W	Mask IBUS OCP Fault Interrupt 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[3]	TSBUS_TSBAT_ALM_MASK	0b	R/W	Mask TSBUS_TSBAT Alarm Interrupt 0 = TSBUS_TSBAT alarm interrupt can work (default) 1 = Mask TSBUS_TSBAT alarm interrupt. TSBUS_TSBAT_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	TSBAT_FLT_MASK	0b	R/W	Mask TSBAT_FLT Interrupt 0 = TSBAT_FLT interrupt can work (default) 1 = Mask TSBAT_FLT interrupt. TSBAT_FLT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	TSBUS_FLT_MASK	0b	R/W	Mask TSBUS_FLT Interrupt 0 = TSBUS_FLT interrupt can work (default) 1 = Mask TSBUS_FLT interrupt. TSBUS_FLT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	TDIEOTP_ALM_MASK	0b	R/W	Mask TDIE OTP Alarm Interrupt 0 = TDIE OTP alarm interrupt can work (default) 1 = Mask TDIE OTP alarm interrupt. TDIEOTP_ALM_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REG0x13: DEVICE_INFO Register [reset = 0x98]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	1001b	R	Reserved	N/A
D[3:0]	DEVICE_ID[3:0]	1000b	R	Device ID 1000 = SGM41607	N/A

REGISTER MAPS (continued)

REG0x14: ADC_CTRL0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0b	R/W	ADC Conversion Enable 0 = Disabled (default) 1 = Enabled Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0. All channel conversions can be enabled even when the device is not during switching.	REG_RST or Watchdog
D[6]	ADC_RATE	0b	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = 1-shot conversion	REG_RST
D[5]	ADC_AVG	0b	R/W	ADC Average Enable Bit 0 = Single value (default) 1 = Running average	REG_RST
D[4]	ADC_AVG_INIT	0b	R/W	ADC Average Initial Value Setting Bit 0 = Start average using the existing register value (default) 1 = Start average using a new conversion	REG_RST
D[3:2]	ADC_SAMPLE[1:0]	00b	R/W	ADC Sample Speed 00 = 15-bit (default) 01 = 14-bit 10 = 13-bit 11 = 12-bit	REG_RST
D[1]	Reserved	0b	R	Reserved	N/A
D[0]	IBUS_ADC_DIS	0b	R/W	IBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST

REG0x15: ADC_CTRL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_ADC_DIS	0b	R/W	VBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[6]	VAC_ADC_DIS	0b	R/W	VAC ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[5]	VOUT_ADC_DIS	0b	R/W	VOUT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[4]	VBAT_ADC_DIS	0b	R/W	VBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[3]	IBAT_ADC_DIS	0b	R/W	IBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[2]	TSBUS_ADC_DIS	0b	R/W	TSBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[1]	TSBAT_ADC_DIS	0b	R/W	TSBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[0]	TDIE_ADC_DIS	0b	R/W	TDIE ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST

REGISTER MAPS (continued)

REG0x16: IBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_POL	0b	R	Polarity of the 15-bit ADC IBUS Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	IBUS_ADC[14:8]	0000000b	R	High 7 Bits of the ADC IBUS Data (1mV resolution) MSB<6:0>: 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA	N/A

REG0x17: IBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	00h	R	Low Byte of the ADC IBUS Data (1mV resolution) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA	N/A

REG0x18: VBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_POL	0b	R	Polarity of the 15-bit ADC VBUS Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	VBUS_ADC[14:8]	0000000b	R	High 7 Bits of the ADC VBUS Data (1mV resolution) MSB<6:0>:16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

REG0x19: VBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	00h	R	Low Byte of the ADC VBUS Data (1mV resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x1A: VAC_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VAC_POL	0b	R	Polarity of the 15-bit ADC VAC Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	VAC_ADC[14:8]	0000000b	R	High 7 Bits of the ADC VAC Data (1mV resolution) MSB<6:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

REG0x1B: VAC_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VAC_ADC[7:0]	00h	R	Low Byte of the ADC VAC Data (1mV resolution) LSB<7:0>: 128mV, 64mV,32mV,16mV,8mV,4mV,2mV,1mV	N/A

REGISTER MAPS (continued)

REG0x1C: VOUT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VOUT_POL	0b	R	Polarity of the 15-bit ADC VOUT Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	VOUT_ADC[14:8]	0000000b	R	High 7 Bits of the ADC VOUT Data (1mV resolution) MSB<6:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

REG0x1D: VOUT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	00h	R	Low Byte of the ADC VOUT Data (1mV resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x1E: VBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_POL	0b	R	Polarity of the 15-bit ADC VBAT Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	VBAT_ADC[14:8]	0000000b	R	High 7 Bits of the ADC VBAT Data (1mV resolution) MSB<6:0>: 16384mV, 8192mV, 4096mV, 2048mV, 1024mV, 512mV, 256mV	N/A

REG0x1F: VBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	00h	R	Low Byte of the ADC VBAT Data (1mV resolution) LSB<7:0>: 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV, 1mV	N/A

REG0x20: IBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_POL	0b	R	Polarity of the 15-bit ADC IBAT Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:0]	IBAT_ADC[14:8]	0000000b	R	High 7 Bits of the ADC IBAT Data (1mA resolution) MSB<6:0>: 16384mA, 8192mA, 4096mA, 2048mA, 1024mA, 512mA, 256mA	N/A

REG0x21: IBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	00h	R	Low Byte of the ADC IBAT Data (1mA resolution) LSB<7:0>: 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA, 1mA	N/A

REGISTER MAPS (continued)

REG0x22: TSBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSBUS_POL	0b	R	Polarity of the 10-bit ADC TSBUS Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:2]	Reserved	00000b	R	Reserved	N/A
D[1:0]	TSBUS_ADC[9:8]	00b	R	High 2 Bits of the ADC TSBUS Data (0.09766% resolution) TSBUS Pin Voltage as a Percentage of VOUT MSB<1:0>: 50%, 25%	N/A

REG0x23: TSBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_ADC[7:0]	00h	R	Low Byte of the ADC TSBUS Data (0.09766% resolution) TSBUS Pin Voltage as a Percentage of VOUT LSB<7:0>: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%	N/A

REG0x24: TSBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSBAT_POL	0b	R	Polarity of the 10-bit ADC TSBAT Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:2]	Reserved	00000b	R	Reserved	N/A
D[1:0]	TSBAT_ADC[9:8]	00b	R	High 2 Bits of the ADC TSBAT Data (0.09766% resolution) TSBAT Pin Voltage as a Percentage of VOUT MSB<1:0>: 50%, 25%	N/A

REG0x25: TSBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_ADC[7:0]	00h	R	Low Byte of the ADC TSBAT Data (0.09766% resolution) TSBAT Pin Voltage as a Percentage of VOUT LSB<7:0>: 12.5%, 6.25%, 3.125%, 1.5625%, 0.78125%, 0.39063%, 0.19531%, 0.09766%	N/A

REG0x26: TDIE_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TDIE_POL	0b	R	Polarity of the 9-bit ADC TDIE Data (reported in two's complement) 0 = Positive (default) 1 = Negative	N/A
D[6:1]	Reserved	000000b	R	Reserved	N/A
D[0]	TDIE_ADC[8]	0b	R	High 1 Bit of the ADC TDIE Data (0.5℃ resolution) DIE Temperature = 5℃ + TDIE_ADC[8:0] × 0.5℃ MSB<0>: 128℃	N/A

REG0x27: TDIE_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	00h	R	Low Byte of the ADC TDIE Data (0.5℃ resolution) LSB<7:0>: 64℃, 32℃,16℃, 8℃, 4℃, 2℃, 1℃, 0.5℃	N/A

REGISTER MAPS (continued)

REG0x28: TSBUS_FLT Register [reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBUS_FLT[7:0]	15h	R/W	TSBUS Percentage Fault Threshold Setting Bits TS_{BUS_FLT} = TSBUS_FLT[7:0] × 0.19531% Offset: 0% Range: 0% (00000000b) – 50% (11111111b) Default: 4.1% (00010101b)	REG_RST

REG0x29: TSBAT_FLT Register [reset = 0x15]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TSBAT_FLT[7:0]	15h	R/W	TSBAT Percentage Fault Threshold Setting Bits TS_{BAT_FLT} = TSBAT_FLT[7:0] × 0.19531% Offset: 0% Range: 0% (00000000b) - 50% (11111111b) Default: 4.1% (00010101b)	REG_RST

REG0x2A: TDIE_ALM Register [reset = 0xC8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIEOTP_ALM[7:0]	C8h	R/W	TDIE OTP Alarm Rising Threshold Setting Bits $T_{DIEOTP\_ALM\_R}$ = 30℃ + TDIEOTP_ALM[7:0] × 0.5℃ Offset: 30℃ Default: 130℃ (11001000b) The TDIE OTP alarm rising threshold should be set lower than T_{DIE_OTP} to ensure proper operation.	REG_RST

REG0x2B: REG_CTRL Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	SS_TIMEOUT[2:0]	000b	R/W	Soft Start Timeout Setting Bits After soft start timeout, the device checks if I_{BUS} is above IBUS UCP threshold. 000 = Timeout disabled (default) 001 = 12.5ms 010 = 25ms 011 = 50ms 100 = 100ms 101 = 400ms 110 = 1.5s 111 = 100s	N/A
D[4]	REGULATION_EN	0b	R/W	VBAT & IBAT Regulation Enable Bit. If $t_{REG\_TIMEOUT}$ is exceeded, this bit is reset to 0. 0 = Disabled (default) 1 = Enabled	N/A
D[3]	VOUT_OVP_DIS	0b	R/W	VOUT OVP Protection Disable Bit 0 = Enabled (default) 1 = Disabled	N/A
D[2]	BUSUCP	0b	R/W	BUSUCP Setting Bit 0 = $I_{BUS\_UCP\_R}$ = 300mA, $I_{BUS\_UCP\_F}$ = 150mA (default) 1 = $I_{BUS\_UCP\_R}$ = 500mA, $I_{BUS\_UCP\_F}$ = 250mA	REG_RST
D[1]	IBAT_RSNS	0b	R/W	External IBAT Current Sense Resistor Setting Bit 0 = 2mΩ (default) 1 = 5mΩ	N/A
D[0]	VAC_PD_EN	0b	R/W	When the bit is enabled, pull down VAC for 400ms to discharge any bulk input cap on VAC. 0 = Disabled (default) 1 = Enabled	REG_RST

REGISTER MAPS (continued)

REG0x2C: REG_THRESHOLD Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	IBAT_REG[1:0]	00b	R/W	IBAT Regulation Threshold Setting 00 = 200mA below IBAT_OCP[6:0] setting (default) 01 = 300mA below IBAT_OCP[6:0] setting 10 = 400mA below IBAT_OCP[6:0] setting 11 = 500mA below IBAT_OCP[6:0] setting	N/A
D[5:4]	VBAT_REG[1:0]	00b	R/W	VBAT Regulation Threshold Setting 00 = 50mV below VBAT_OVP[5:0] setting (default) 01 = 100mV below VBAT_OVP[5:0] setting 10 = 150mV below VBAT_OVP[5:0] setting 11 = 200mV below VBAT_OVP[5:0] setting	N/A
D[3]	VBAT_REG_ACTIVE_STAT	0b	R	VBAT_REG Active Status Bit 0 = Device not in VBAT_REG status (default) 1 = Device in VBAT_REG status	N/A
D[2]	IBAT_REG_ACTIVE_STAT	0b	R	IBAT_REG Active Status Bit 0 = Device not in IBAT_REG status (default) 1 = Device in IBAT_REG status	N/A
D[1]	VDROP_OVP_STAT	0b	R	VDROP OVP Fault Status Bit 0 = Device not in VDROP OVP fault status (default) 1 = Device in VDROP OVP fault status	N/A
D[0]	VOUT_OVP_STAT	0b	R	VOUT OVP Fault Status Bit 0 = Device not in VOUT OVP fault status (default) 1 = Device in VOUT OVP fault status	N/A

REG0x2D: REG_FLAG_MASK Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBAT_REG_ACTIVE_FLAG	0b	RC	VBAT_REG Active Event Flag Bit 0 = No VBAT_REG active event (default) 1 = VBAT_REG active event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[6]	IBAT_REG_ACTIVE_FLAG	0b	RC	IBAT_REG Active Event Flag Bit 0 = No IBAT_REG active event (default) 1 = IBAT_REG active event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	VDROP_OVP_FLAG	0b	RC	VDROP OVP Fault Flag Bit 0 = No VDROP OVP fault (default) 1 = VDROP OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	VOUT_OVP_FLAG	0b	RC	VOUT OVP Fault Flag Bit 0 = No VOUT OVP fault (default) 1 = VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	VBAT_REG_ACTIVE_MASK	0b	R/W	Mask VBAT_REG Active Status Change Event Interrupt 0 = VBAT_REG active status change event interrupt can work (default) 1 = Mask VBAT_REG active status change event interrupt. VBAT_REG_ACTIVE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	IBAT_REG_ACTIVE_MASK	0b	R/W	Mask IBAT_REG Active Status Change Event Interrupt 0 = IBAT_REG active status change event interrupt can work (default) 1 = Mask IBAT_REG active status change event interrupt. IBAT_REG_ACTIVE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VDROP_OVP_MASK	0b	R/W	Mask VDROP OVP Fault Interrupt 0 = VDROP OVP fault interrupt can work (default) 1 = Mask VDROP OVP fault interrupt. VDROP_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[0]	VOUT_OVP_MASK	0b	R/W	Mask VOUT OVP Fault Interrupt 0 = VOUT OVP fault interrupt can work (default) 1 = Mask VOUT OVP fault interrupt. VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST

REGISTER MAPS (continued)

REG0x2E: DEGLITCH Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	Reserved	000b	R	Reserved	N/A
D[4]	VBUS_LO_DEG	0b	R/W	Low VBUS Error Detection Deglitch Time Setting Bit 0 = 10μs (default) 1 = 10ms	REG_RST
D[3]	IBUS_UCP_FALL_DEG	0b	R/W	IBUS UCP Protection Deglitch Time Setting Bits 0 = 10μs (default) 1 = 5ms	REG_RST
D[2:0]	Reserved	000b	R	Reserved	N/A

REG0x2F: PMID2OUT_OVP_UVP Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000b	R	Reserved	N/A
D[3]	PMID2OUT_UVP_FLAG	0b	RC	PMID2VOUT_UVP_ FLAG Bit 0 = Normal (default) 1 = PMID2VOUT_UVP status changed	N/A
D[2]	PMID2OUT_OVP_FLAG	0b	RC	PMID2VOUT_OVP_ FLAG Bit 0 = Normal (default) 1 = PMID2VOUT_OVP status changed	N/A
D[1]	PMID2OUT_UVP_STAT	0b	R	PMID2VOUT_UVP_STAT Bit 0 = Not in PMID2VOUT_UVP_STAT (default) 1 = In PMID2VOUT_UVP_STAT	REG_RST
D[0]	PMID2OUT_OVP_STAT	0b	R	PMID2VOUT_OVP_STAT Bit 0 = Not in PMID2VOUT_OVP_STAT (default) 1 = PMID2VOUT_OVP_STAT	REG_RST

REG0x30: IBUS_REG Register [reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_REG_EN	0b	R/W	IBUS Regulation Enable Bit 0 = Disabled (default) 1 = Enabled	N/A
D[6]	IBUS_REG_ACTIVE_STAT	0b	R	IBUS_REG Active Status Bit 0 = Device not in IBUS_REG status (default) 1 = Device in IBUS_REG status	N/A
D[5]	IBUS_REG_ACTIVE_FLAG	0b	RC	IBUS_REG Active Event Flag Bit 0 = No IBUS_REG active event (default) 1 = IBUS_REG active event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[4]	IBUS_REG_ACTIVE_MASK	0b	R/W	Mask IBUS_REG Active Status Change Event Interrupt 0 = IBUS_REG active status change event interrupt can work (default) 1 = Mask IBUS_REG active status change event interrupt. IBUS_REG_ACTIVE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3:0]	IBUS_REG[3:0]	1010b	R/W	IBUS Regulation Value Setting Bits When the IBUS regulation loop is active, a nINT is sent. I_{BUS_REG} = 3A + IBUS_REG[3:0] × 250mA Default: 5.5A (1010b)	REG_RST

REG0x31: MODE Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	Reserved	0000000b	R	Reserved	N/A
D[0]	MODE	0b	R/W	This bit decides the operation mode. 0 = 2:1 Voltage divider mode (default) 1 = Bypass mode	REG_RST or Watchdog

APPLICATION INFORMATION

Design Requirements

The SGM41607 operates under smart wall adapter protocols (USB_PD PPS/programmable adapters) demanding precise voltage/current input for optimal charging. Although supporting 12A charging in voltage divider mode, this configuration presents significant thermal challenges. Design implementation requires rigorous assessment of power dissipation, spatial constraints, and operating environments to ensure viable performance.

Input Capacitors (C_{VAC}, C_{VBUS} and C_{PMID})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For $C_{VAC,}$ use at least a 1μF/25V low ESR bypass ceramic capacitor placed close to the VAC and GND pins. The C_{VBUS} and C_{PMID} are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, 10μF/25V or larger X5R ceramic capacitors are sufficient for C_{PMID}, 1μF/25V or larger X5R ceramic capacitors are sufficient for C_{VBUS}. Considering the DC bias derating of the ceramic capacitors, the X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFET (Q_{OVP})

The maximum recommended V_{VBUS} input range is 11.5V. If the supplied V_{VAC} voltage is above 11.5V, or if regulation functions are needed during load or wall adapter transients, an external OVPFET is recommended between the USB connector and the SGM41607. Choose a low R_{DSON} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors (C_{FLY})

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to half of the input voltage. To trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of the V_{VOUT} as a good starting point. The C_{FLY} for each phase can be calculated by Equation 10:

$$C_{FLY} = \frac{I_{BAT}}{4f_{SW}V_{CFLY\_RPP}} = \frac{I_{BAT}}{8\%f_{SW}V_{OUT}} \quad (10)$$

where I_{BAT} is the charging current and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

The default switching frequency is f_{SW} = 500kHz. It can be adjusted by FSW_SET[2:0] bits in REG0x0B. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}).

C_{FLY} capacitor selection requires rigorous assessment of current rating, ESR, and capacitance with bias voltage derating. As these capacitors operate at half-input voltage, derating significantly impacts effective capacitance. Optimal design employs four 22μF/10V capacitors per phase (8 per device). While minimum three capacitors are permissible, reduced counts increase output voltage/current ripple and degrade efficiency. Using more than 4 capacitors per phase will not significantly improve the output voltage, current ripple, or efficiency.

Output Capacitor (C_{VOUT})

C_{VOUT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{VOUT} value results in less output voltage ripple, but due to the dual-phase operation, the C_{VOUT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{VOUT} as given in Equation 11:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT\_RPP}} \quad (11)$$

where t_{DEAD} is the dead time between the two phases and V_{VOUT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{OUT}.

C_{VOUT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically a 22μF/10V, X5R or better grade ceramic capacitors placed close to the VOUT and GND pins provide stable performance.

External Bootstrap Capacitor (C_{DRV})

The bootstrap capacitors C_{DRV} provide the gate driver supply voltage for the internal high-side switches (Q_{CH1} and Q_{CH2}). Place a 220nF/25V low ESR ceramic capacitor between CDRVH and CDRVL_ADDRMS pins.

APPLICATION INFORMATION (continued)

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41607. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to GND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close to the device as possible with small pad areas to reduce switching noise and EMI.
6. Connect or reference all quiet signals to the GND pin.
7. Connect and reference all power signals to the GND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.

TYPICAL APPLICATION CIRCUITS

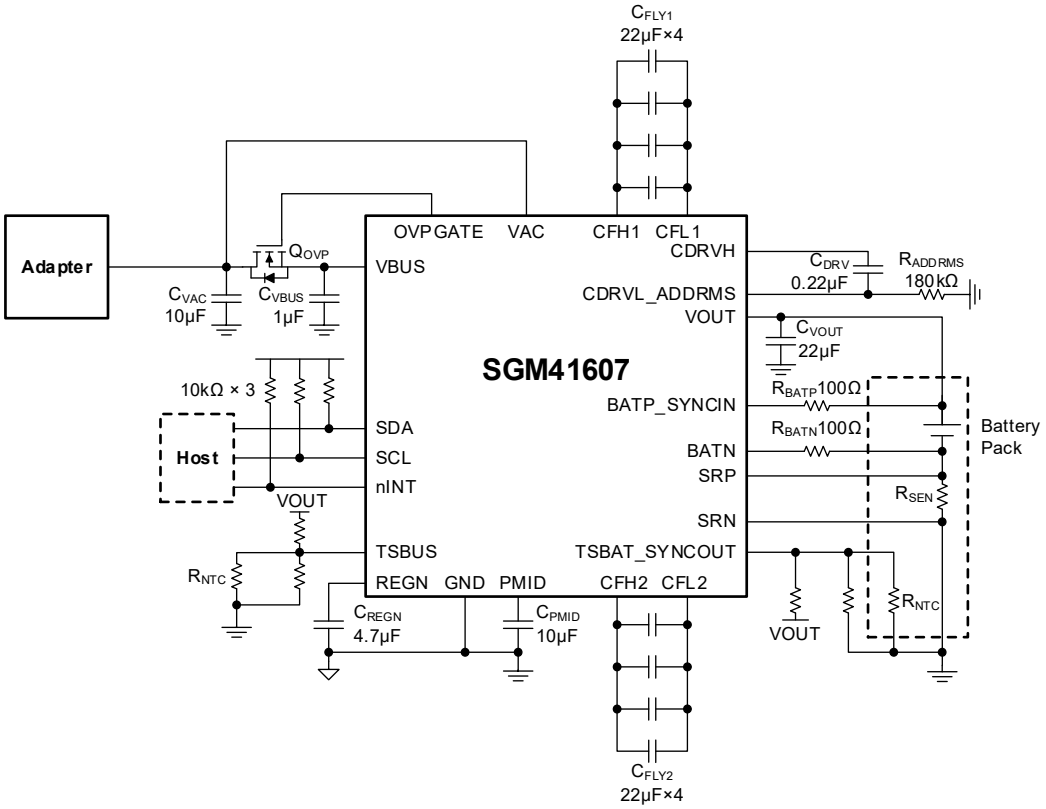


Figure 9. Typical Application in Standalone Mode

TYPICAL APPLICATION CIRCUITS (continued)

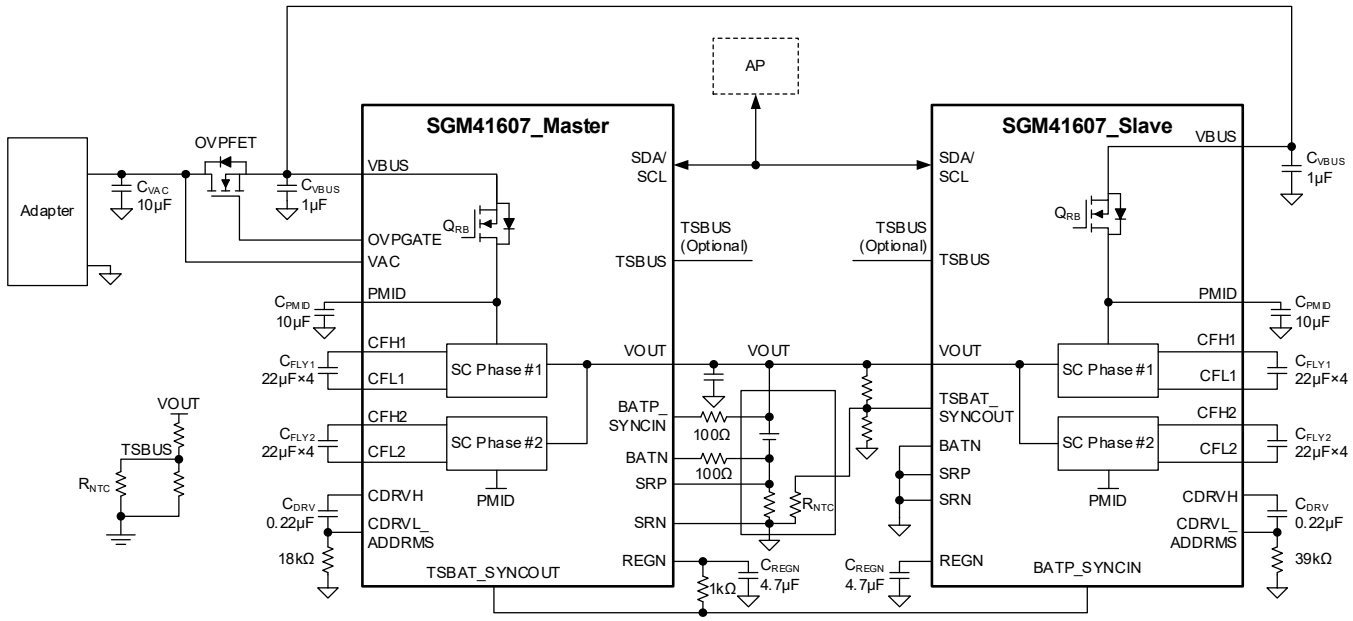


Figure 10. Typical Application in Parallel Mode

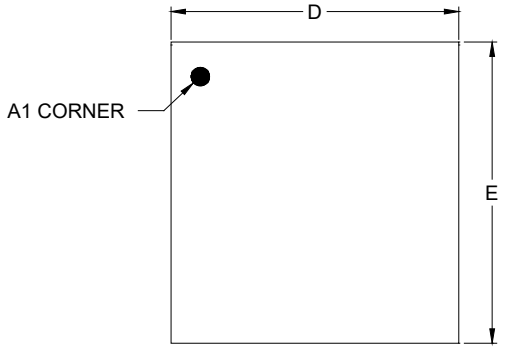
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

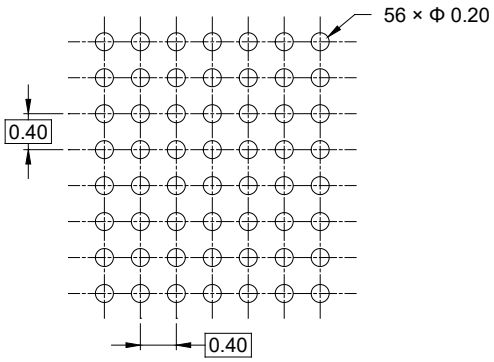
Changes from Original to REV.A (JUNE 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

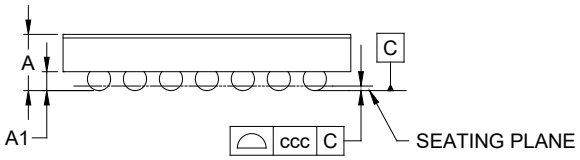
WLCSP-3.2×3.35-56B



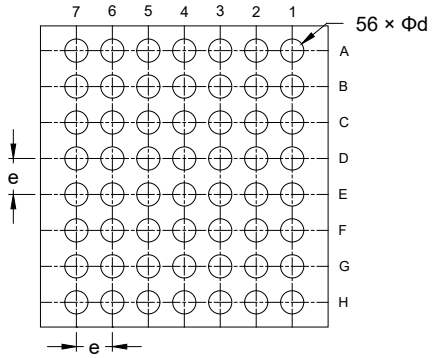
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



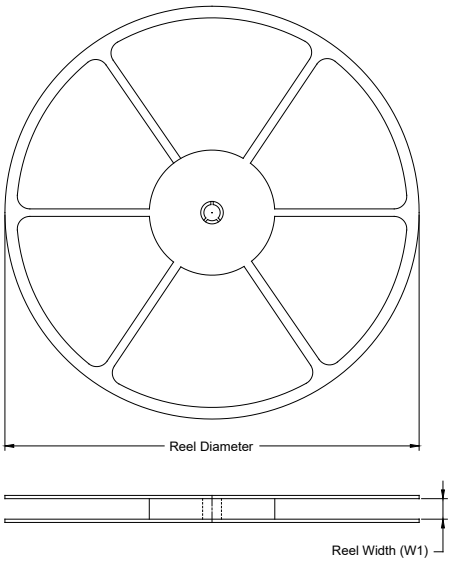
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.663
A1	0.190	-	0.230
D	3.170	-	3.230
E	3.320	-	3.380
d	0.228	-	0.288
e	0.400 BSC		
ccc	0.050		

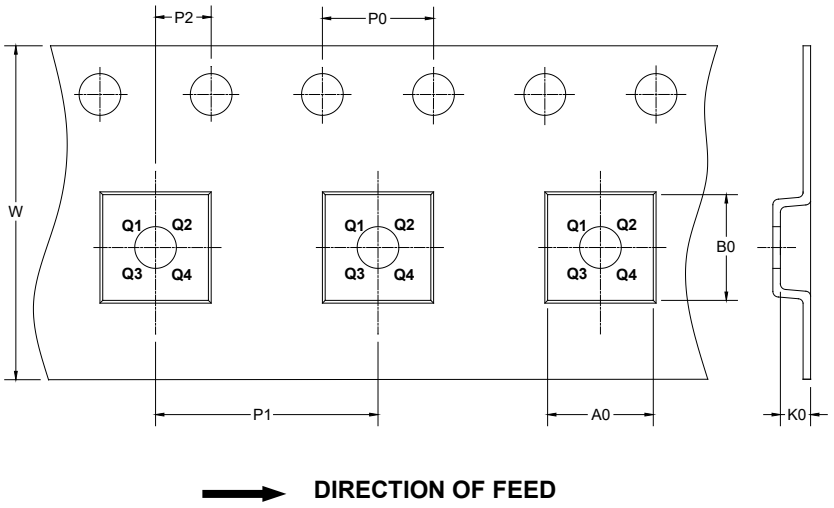
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



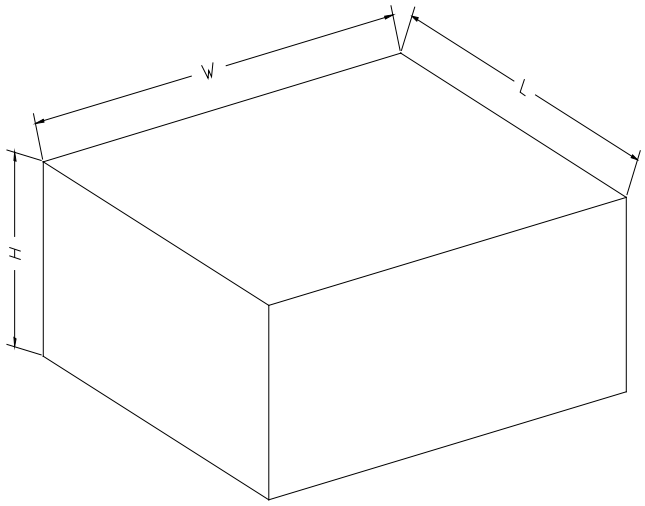
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.2×3.35-56B	13"	12.4	3.52	3.52	0.81	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002