

GENERAL DESCRIPTION

The SGM40679B has two symmetrical paths, which is designed for match with the differential transmission pairs for USB Type-C transmission stripe lines. When the voltage on the DN pin or the DP pin exceeds the typical common-mode range, the paths will be disconnected to ensure that no high direct current voltage is transmitted separately to the DSN pin or the DSP pin.

This SGM40679B is biased between the VCC and GND pins with a low current, and the bias voltage range is from 2.3V to 5.5V. When the two paths are biased to 1V by the Type-C receiver or the transmitter without DC isolation capacitors, the performance is guaranteed.

The SGM40679B is available in a Green UTDFN-1.1×0.9-6L package.

FEATURES

- **Insertion Loss:**
 - ♦ 0.5dB at 1.5GHz
 - ♦ 0.6dB at 2.5GHz
- **In Compliance with Gen-1 and Gen-2 Eye Masking**
- **Low Bias Current: 24μA (TYP), V_{CC} = 2.3V to 5.5V**
- **-40°C to +125°C Operating Temperature Range**
- **Available in a Green UTDFN-1.1×0.9-6L Package**

APPLICATIONS

USB Type-C RX/TX Over-Voltage Protection

FUNCTIONAL BLOCK DIAGRAM

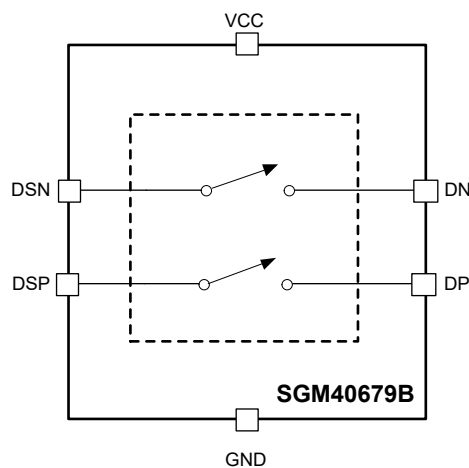


Figure 1. Block Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40679B	UTDFN-1.1×0.9-6L	-40°C to +125°C	SGM40679BXUER6G/TR	00	Tape and Reel, 3000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC}..... -0.3V to 6V
 Surge ⁽¹⁾ -20V to 20V
 Package Thermal Resistance
 UTDFN-1.1×0.9-6L, θ_{JA}..... 254.9°C/W
 UTDFN-1.1×0.9-6L, θ_{JB}..... 122.4°C/W
 UTDFN-1.1×0.9-6L, θ_{JC}..... 172.1°C/W
 Junction Temperature..... +135°C
 Storage Temperature Range..... -65°C to +150°C
 Lead Temperature (Soldering, 10s)..... +260°C
 ESD Susceptibility ⁽²⁾
 CDM ±1000V

NOTES:

1. For Surge, DN and DP comply with IEC61000-4-2.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range2.3V to 5.5V
 Junction Temperature Range..... -40°C to +125°C
 Operating Temperature Range..... -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

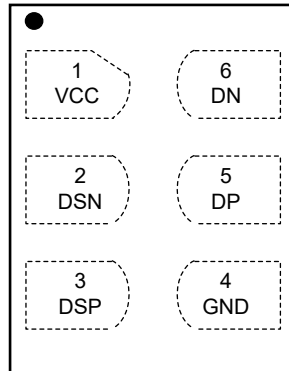
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM40679B (TOP VIEW)



UTDFN-1.1×0.9-6L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VCC	Positive Bias Input Pin. Set the bias voltage of this pin within the range of 2.3V to 5.5V to enable the conduction of the switching path.
2	DSN	One End of Differential Passing Path, Facing the Native Circuit Being Protected.
3	DSP	One End of Differential Passing Path, Facing the Native Circuit Being Protected.
4	GND	Ground Reference Input. Conducting performance is guaranteed when the passing paths biased to 1V with reference to this pin.
5	DP	One End of Differential Passing Path, Facing the Foreign Port.
6	DN	One End of Differential Passing Path, Facing the Foreign Port.

ELECTRICAL CHARACTERISTICS(Full = -40°C to +125°C, typical values are at T_A = +25°C, V_{CC} = 3.3V, unless otherwise noted.)

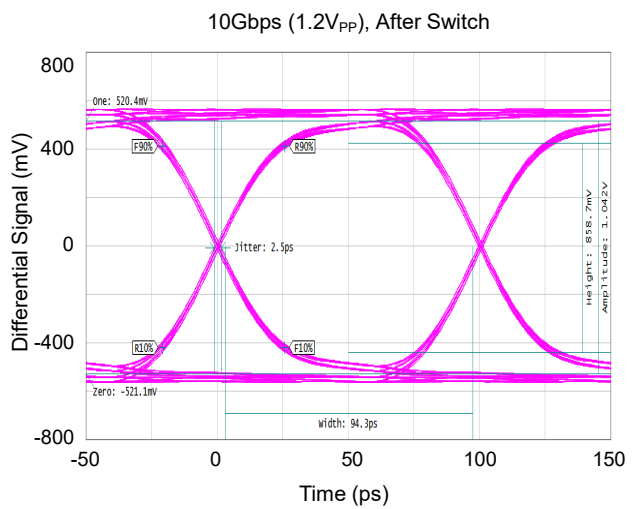
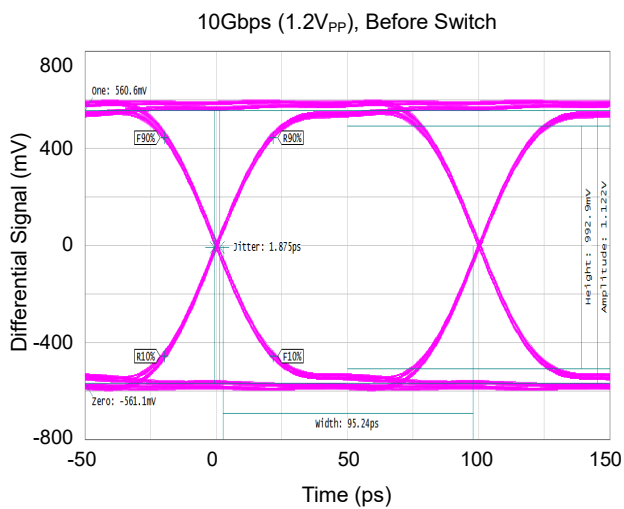
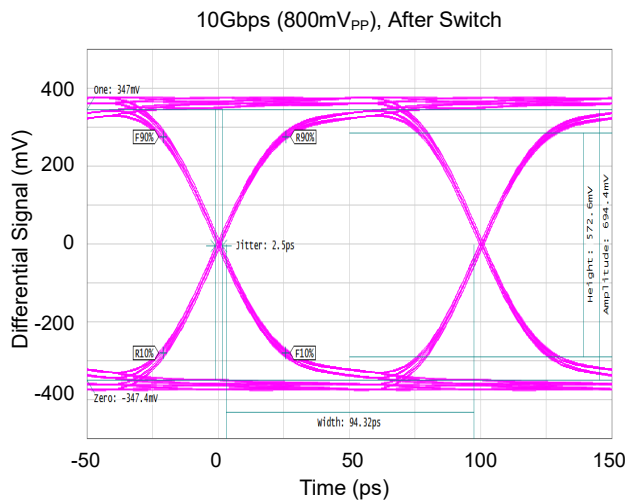
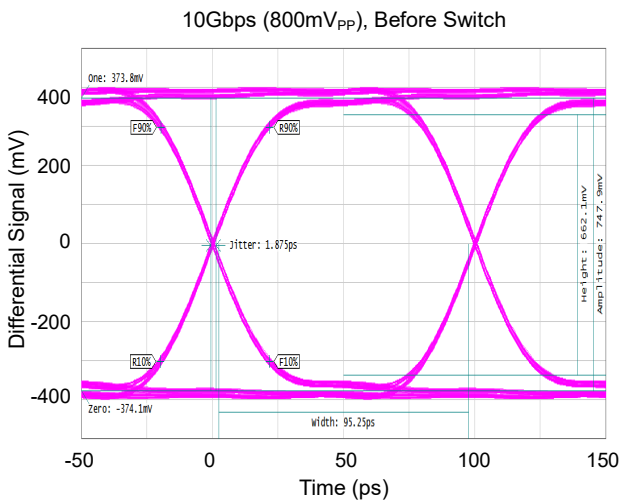
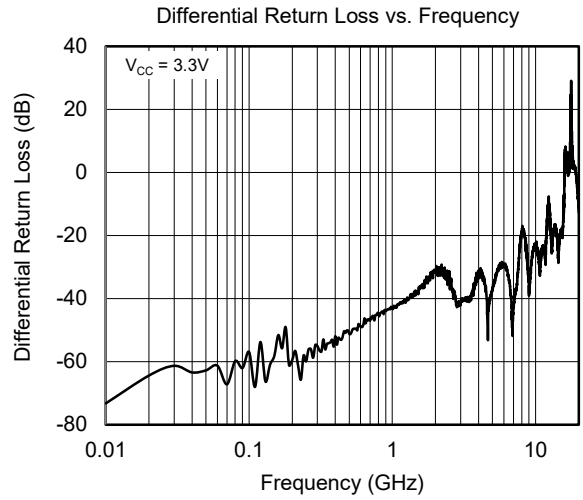
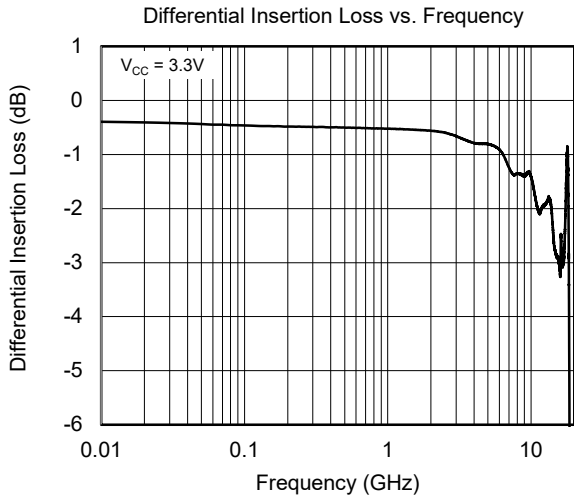
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General Circuit Parameters						
Supply Voltage	V _{CC}		2.3	3.3	5.5	V
Supply Current	I _{CC}	V _{CC} = 2.3V to 5.5V, differential port input = 0V		24	52	μA
On-Resistance	R _{ON}	V _{I/O} = 0.4V, I _{SINK} = 8mA, Test Circuit 1		4.2	6.5	Ω
Channel Resistance Mismatch	ΔR _{ON}	V _{I/O} = 0.4V, I _{SINK} = 8mA, Test Circuit 1		0.1	0.4	
Off Leakage Current	I _{OZ}	V _{DSP/N} = 3.6V, Test Circuit 2		0.65	5	μA
On Leakage Current	I _{ON}	V _{DSP/N} = 1V or 3V, Test Circuit 3		0.6	2	μA
On State Impedance to GND	Z _{ON}	V _{DSP/N} = 1V or 3V	1	5		MΩ
Dynamic Characteristics						
Port DN	C _{ON}	V _{DP/N} = 0V, f = 2.5GHz		0.6	1.1 ⁽¹⁾	pF
Port DP				0.6	1.1 ⁽¹⁾	pF
Port DN	C _{OFF}	V _{CC} = 0V, V _{DP/N} = 0V, f = 2.5GHz		0.4	0.8 ⁽¹⁾	pF
Port DP				0.4	0.8 ⁽¹⁾	pF
Port DSN				0.4	0.8 ⁽¹⁾	pF
Port DSP				0.4	0.8 ⁽¹⁾	pF
Differential Insertion Loss	IL	f ₀ = 1.5GHz		0.5	1.1 ⁽¹⁾	dB
		f ₀ = 2.5GHz		0.6	1.2 ⁽¹⁾	dB
Differential -3dB Band Width	BW	With respect to signal level at 100MHz, Test Circuit 4	10 ⁽¹⁾			GHz
Differential Return Loss	RL	f ₀ = 1.5GHz	18 ⁽¹⁾	23		dB
		f ₀ = 2.5GHz	15 ⁽¹⁾	20		dB
Input Over-Voltage Protection						
Input/Output DC Voltage	V _{OVP}		-0.5		20	V
Analog Input/Output Voltage	V _{I/O}		0		3.6	V
Analog Input /Output Port Continuous Current	I _{I/O}			5		mA
Over-Voltage Protection Threshold	V _{OVP_TH}		2.8	3.3	3.6	V
OVP Response Time	t _{OVP}	Between trigger voltage and peaking, Test Circuit 5		110		ns
OVP Recovery Time	t _{OVP_RECOVERY}	Between trigger voltage and 90% input voltage		1		μs
Timing Requirements						
Propagation Delay	t _{PD}	R _L = 50Ω, C _L = 5pF, V _{CC} = 2.3V to 5.5V		115		ps
Skew of Opposite Transitions of Same Output	t _{SK(P)}	R _L = 50Ω, C _L = 5pF, V _{CC} = 2.3V to 5.5V, Test Circuit 6		20		ps

NOTE:

- Specified by design and characterization, not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, unless otherwise noted.



TYPICAL APPLICATION CIRCUIT

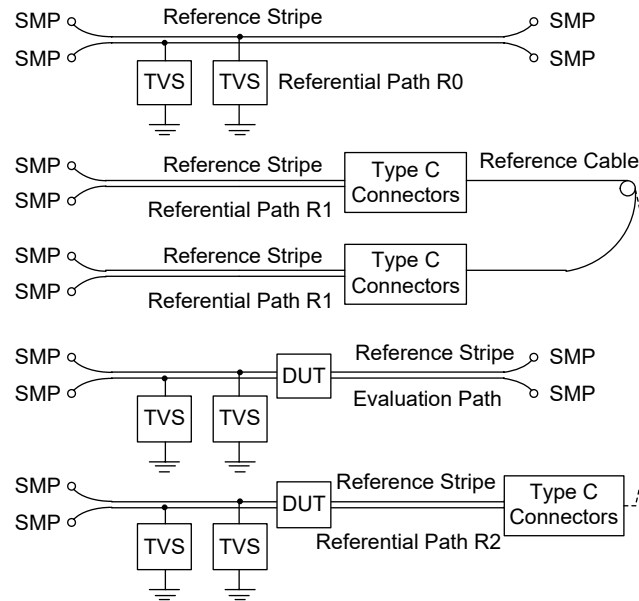


Figure 2. Simplified Schematic

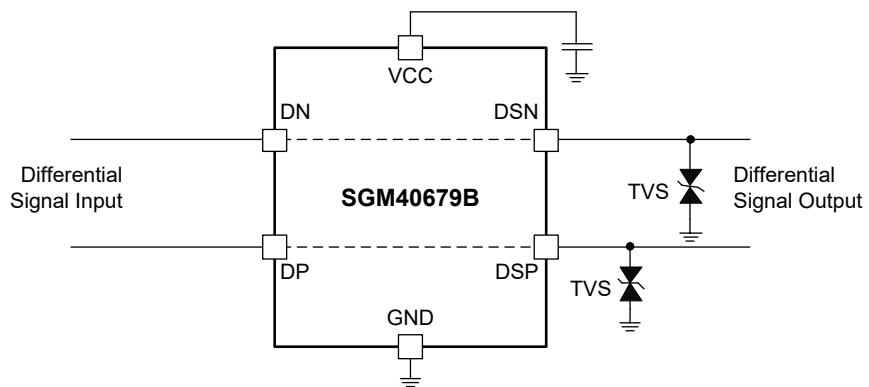
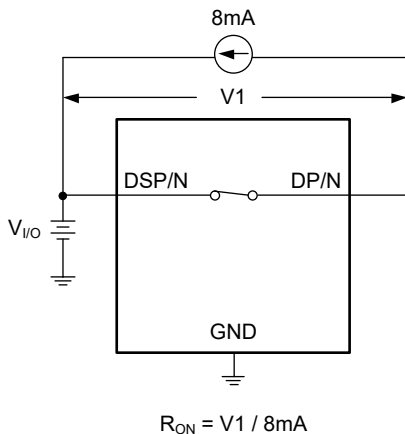
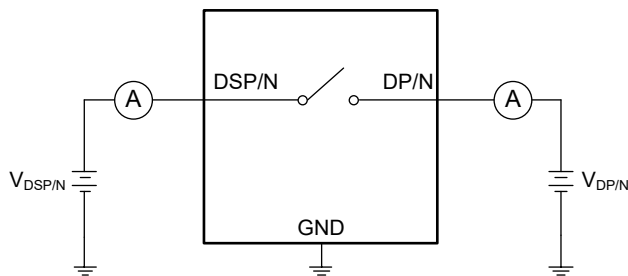


Figure 3. Typical Application Circuit Placement

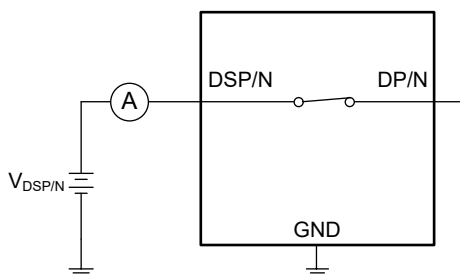
TEST CIRCUITS



Test Circuit 1. On-Resistance

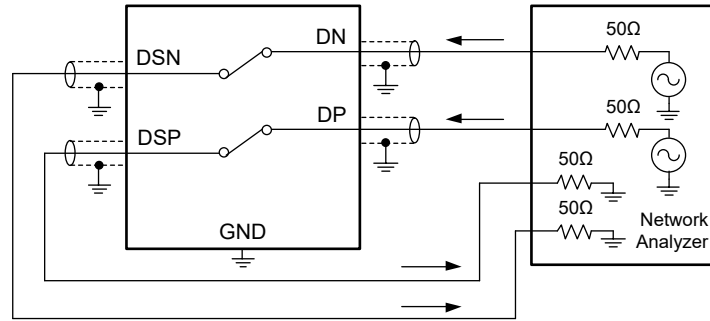


Test Circuit 2. Off Leakage



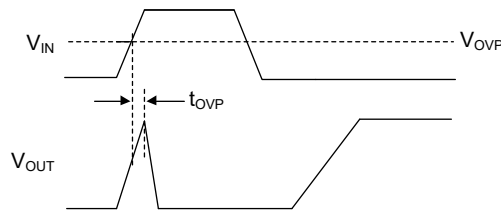
Test Circuit 3. On Leakage

TEST CIRCUITS (continued)

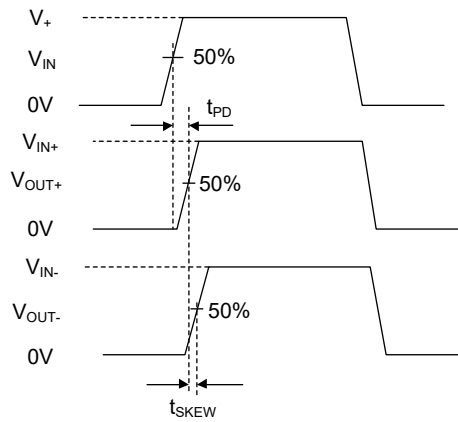


Attenuation = $20\log(V_{OUT}/V_{IN})$

Test Circuit 4. -3dB Bandwidth



Test Circuit 5. Over-Voltage Protection



Test Circuit 6. Output Signal Skew

REVISION HISTORY

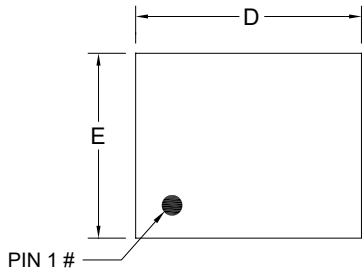
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (APRIL 2026)	Page
Changed from product preview to production data.....	All

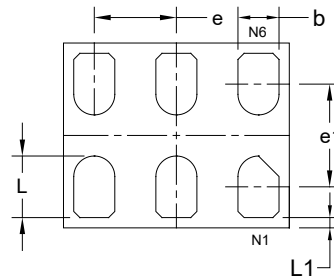
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

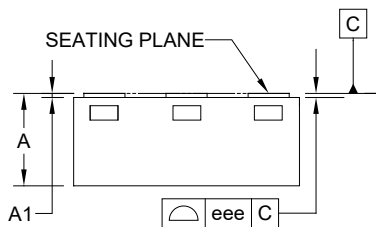
UTDFN-1.1×0.9-6L



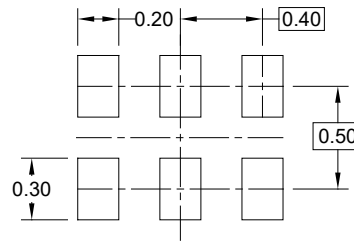
TOP VIEW



BOTTOM VIEW



SIDE VIEW



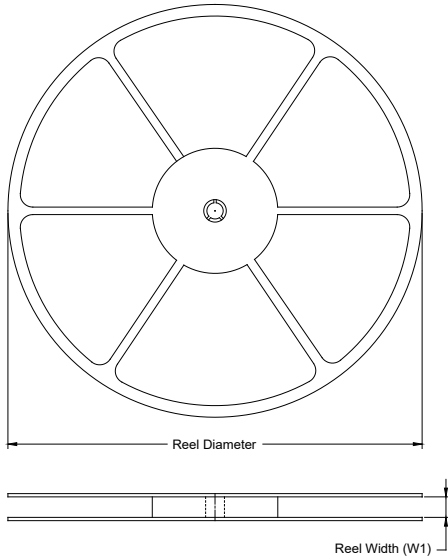
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.400	-	0.500
A1	0.000	-	0.050
b	0.150	-	0.250
D	1.000	-	1.200
E	0.800	-	1.000
e	0.400 BSC		
e1	0.500 BSC		
L	0.200	-	0.400
L1	0.000	-	0.100
eee	0.050		

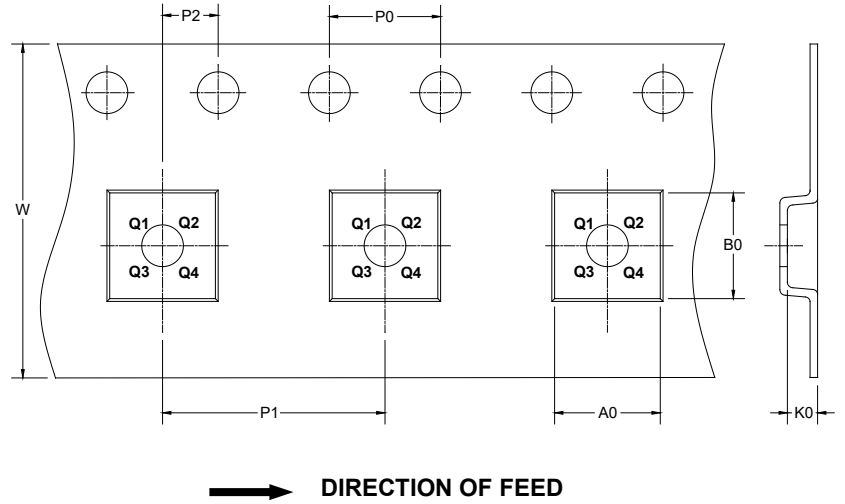
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

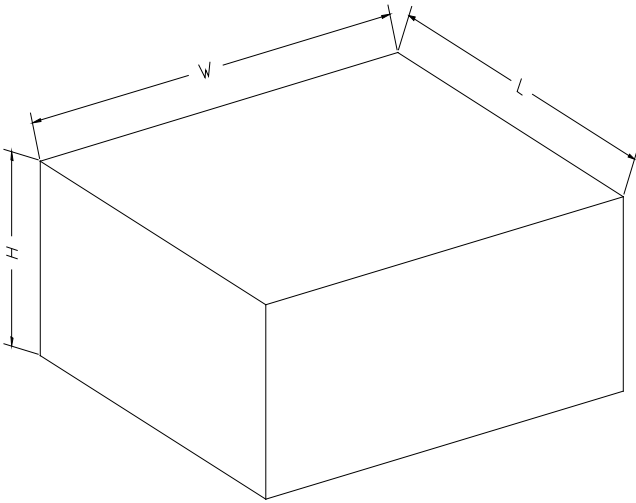
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.1×0.9-6L	7"	9.5	1.02	1.22	0.60	4.0	4.0	2.0	8.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

D00002