74HEF4069
Hex Unbuffered Inverter

GENERAL DESCRIPTION

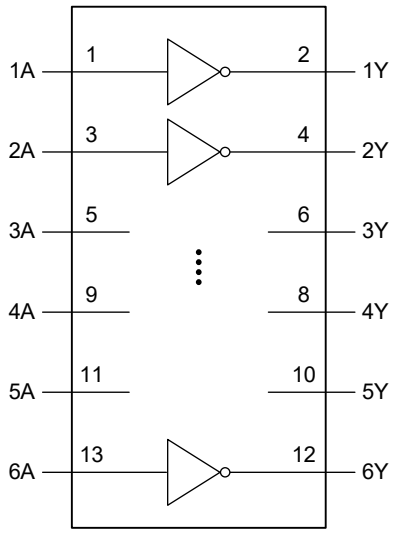
The 74HEF4069 is a hex unbuffered inverter which can accept a wide supply voltage range from 3V to 13.2V. The clamp diodes of inputs allow the use of current limiting resistors to connect inputs to the voltage exceeding supply voltage.

The 74HEF4069 is available in Green SOIC-14, TSSOP-14 and TQFN-2.5×3-14L packages. It operates over a temperature range of -40℃ to +125℃.

FEATURES

- **Wide Supply Voltage Range: 3V to 13.2V**
- **Parametric Ratings: 5V, 10V and 13.2V**
- **Low Power Dissipation**
- **Support Fully Static Operation**
- **Characteristics of Standardized Symmetrical Outputs**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-14, TSSOP-14 and TQFN-2.5×3-14L Packages**

LOGIC DIAGRAM



APPLICATIONS

Oscillator

Logic Inverter

High-Input-Impedance Amplifier

FUNCTION TABLE

INPUT	OUTPUT
1A, 2A, 3A, 4A, 5A, 6A	**1Y, 2Y, 3Y, 4Y, 5Y, 6Y**
H	L
L	H

H = High Voltage Level

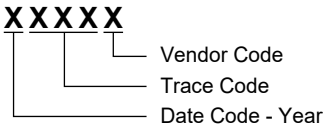
L = Low Voltage Level

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HEF4069	SOIC-14	-40℃ to +125℃	74HEF4069XS14G/TR	74HEF4069XS14 XXXXX	Tape and Reel, 2500
	TSSOP-14	-40℃ to +125℃	74HEF4069XTS14G/TR	1YF XTS14 XXXXX	Tape and Reel, 4000
	TQFN-2.5×3-14L	-40℃ to +125℃	74HEF4069XTWB14G/TR	1YGTWB XXXXX	Tape and Reel, 10000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{DD} ..... -0.5V to 14V
Input Voltage Range, V_I [(1)] ..... -0.5V to MIN(14V, V_{DD} + 0.5V)
Output Voltage Range, V_O [(1)] . -0.5V to MIN(14V, V_{DD} + 0.5V)
Input Clamp Current, I_{IK} (V_I < -0.5V or V_I > V_{DD} + 0.5V) ..... ±10mA
Output Clamp Current, I_{OK} (V_O < -0.5V or V_O > V_{DD} + 0.5V) ..... ±10mA
Input/Output Current, $I_{I/O}$ ..... ±10mA
Supply Current, I_{DD} 50mA
Junction Temperature [(2)] ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility [(3)] [(4)]
HBM ..... ±6000V
CDM ..... ±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{DD} ..... 3V to 13.2V
Input Voltage Range, V_I ..... 0V to V_{DD}
Output Voltage Range, V_O ..... 0V to V_{DD}
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

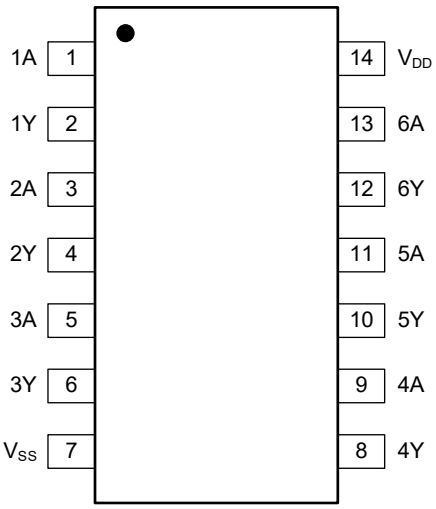
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

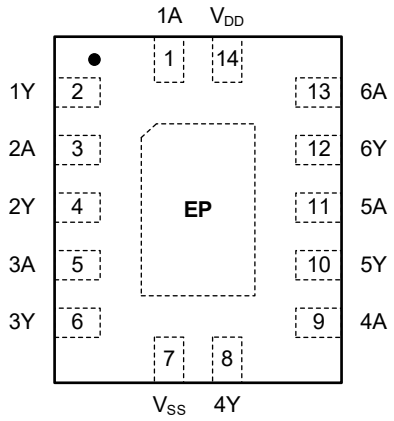
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-14/TSSOP-14

(TOP VIEW)



TQFN-2.5×3-14L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 3, 5, 9, 11, 13	1A, 2A, 3A, 4A, 5A, 6A	Inputs.
2, 4, 6, 8, 10, 12	1Y, 2Y, 3Y, 4Y, 5Y, 6Y	Outputs.
7	V_{SS}	Ground.
14	V_{DD}	Supply Voltage.
Exposed Pad	EP	TQFN-2.5×3-14L package only. Connect to V_{SS} or floating.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, V_{SS} = 0V, V_I = V_{SS} or V_{DD}, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	$\|I_O\|$ < 1μA	V_{DD} = 5V	Full	4			V
			V_{DD} = 10V	Full	8			
			V_{DD} = 13.2V	Full	10			
Low-Level Input Voltage	V_{IL}	$\|I_O\|$ < 1μA	V_{DD} = 5V	Full			1	V
			V_{DD} = 10V	Full			2	
			V_{DD} = 13.2V	Full			3.2	
High-Level Output Voltage	V_{OH}	$\|I_O\|$ < 1μA	V_{DD} = 5V	Full	4.95			V
			V_{DD} = 10V	Full	9.95			
			V_{DD} = 13.2V	Full	13.15			
Low-Level Output Voltage	V_{OL}	$\|I_O\|$ < 1μA	V_{DD} = 5V	Full			0.05	V
			V_{DD} = 10V	Full			0.05	
			V_{DD} = 13.2V	Full			0.05	
High-Level Output Current	I_{OH}	V_O = 2.5V	V_{DD} = 5V	Full		-10.5	-5	mA
		V_O = 4.6V	V_{DD} = 5V	Full		-1.9	-1	
		V_O = 9.5V	V_{DD} = 10V	Full		-2.5	-1.2	
		V_O = 12V	V_{DD} = 13.2V	Full		-6.2	-3	
Low-Level Output Current	I_{OL}	V_O = 0.4V	V_{DD} = 5V	Full	1	1.8		mA
		V_O = 0.5V	V_{DD} = 10V	Full	1.2	2.4		
		V_O = 1.5V	V_{DD} = 13.2V	Full	3.6	7.3		
Input Leakage Current	I_I	V_I = V_{DD} or GND	V_{DD} = 13.2V	Full		±0.01	±1	μA
Supply Current	I_{DD}	All valid input combinations, I_O = 0A	V_{DD} = 5V	Full		0.01	7.5	μA
			V_{DD} = 10V	Full		0.01	15	
			V_{DD} = 13.2V	Full		0.01	30	
Input Capacitance	C_I	Digital inputs		+25℃		11		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-to-Low Propagation Delay	t_{PHL}	nA to nY	V_{DD} = 5V, 7.82ns + (0.26ns/pF)C_L (1)	Full		23	33	ns
			V_{DD} = 10V, 8ns + (0.19ns/pF)C_L (1)	Full		19	28	
			V_{DD} = 13.2V, 9.01ns + (0.17ns/pF)C_L (1)	Full		19	27	
Low-to-High Propagation Delay	t_{PLH}	nA to nY	V_{DD} = 5V, 8.15ns + (0.23ns/pF)C_L (1)	Full		20	32	ns
			V_{DD} = 10V, 6.84ns + (0.18ns/pF)C_L (1)	Full		16	26	
			V_{DD} = 13.2V, 5.62ns + (0.18ns/pF)C_L (1)	Full		15	24	
High-to-Low Output Transition Time	t_{THL}	Output nY	V_{DD} = 5V, 7.05ns + (0.56ns/pF)C_L (1)	Full		36	55	ns
			V_{DD} = 10V, 10.54ns + (0.45ns/pF)C_L (1)	Full		33	46	
			V_{DD} = 13.2V, 10.63ns + (0.42ns/pF)C_L (1)	Full		33	46	
Low-to-High Output Transition Time	t_{TLH}	Output nY	V_{DD} = 5V, 7.89ns + (0.51ns/pF)C_L (1)	Full		36	55	ns
			V_{DD} = 10V, 13.13ns + (0.4ns/pF)C_L (1)	Full		35	53	
			V_{DD} = 13.2V, 16.86ns + (0.38ns/pF)C_L (1)	Full		35	53	

NOTE:

1. The extrapolation formula (C_L in pF) can be used to calculate the typical values for both propagation delay and output transition time.

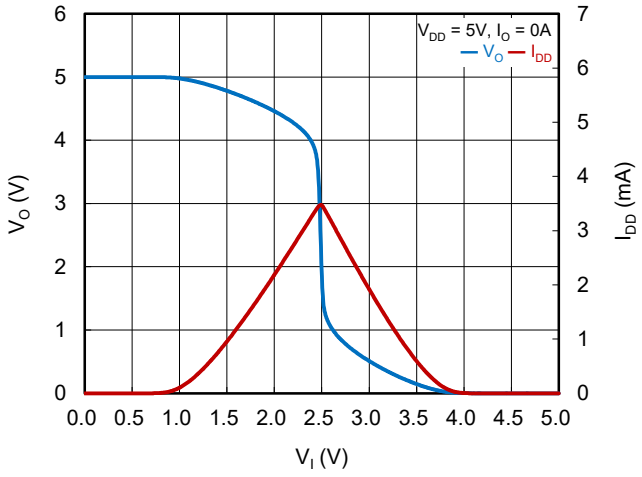
Dynamic Power Dissipation

(V_{SS} = 0V, t_R = t_F ≤ 20ns, T_A = +25℃, unless otherwise noted.)

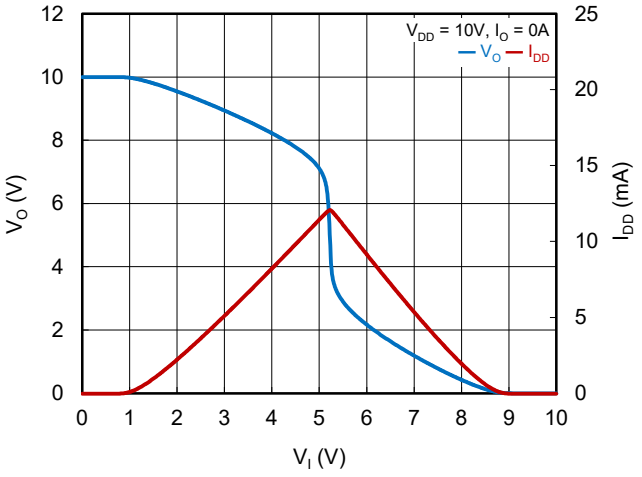
PARAMETER	SYMBOL	CONDITIONS	TYPICAL FORMULA	WHERE
Dynamic Power Dissipation	P_D	V_{DD} = 5V	$P_D = 3500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = 1MHz. f_o = output frequency in MHz. C_L = output load capacitance in pF. $\Sigma(f_o \times C_L)$ = sum of the outputs. V_{DD} = supply voltage in Volts.
		V_{DD} = 10V	$P_D = 24500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	
		V_{DD} = 13.2V	$P_D = 52400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	

TYPICAL PERFORMANCE CHARACTERISTICS

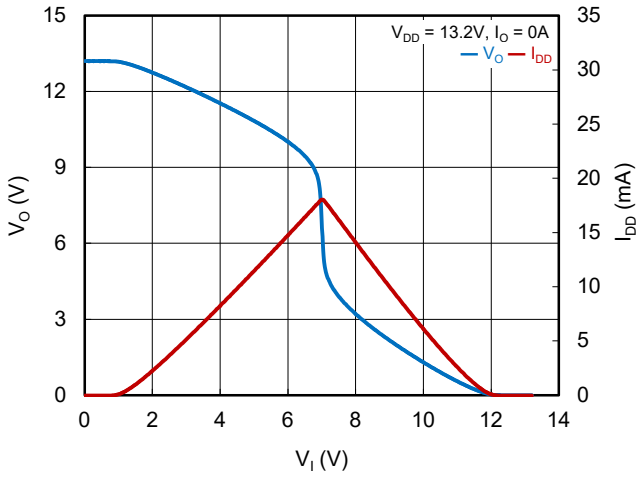
Output Voltage/Supply Current vs. Input Voltage



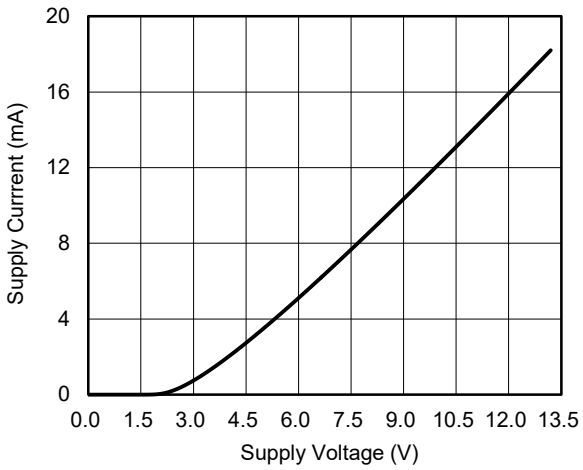
Output Voltage/Supply Current vs. Input Voltage



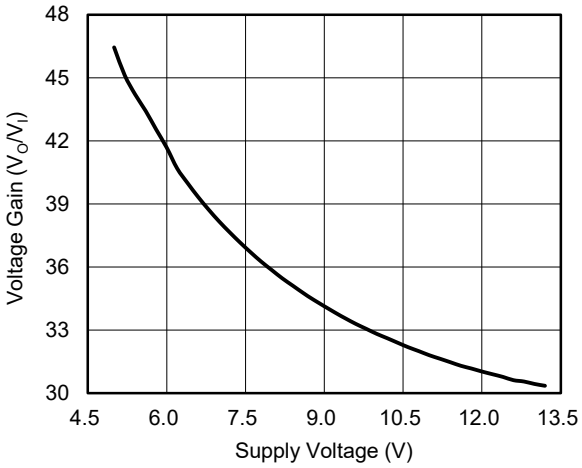
Output Voltage/Supply Current vs. Input Voltage



Supply Current vs. Supply Voltage (1)



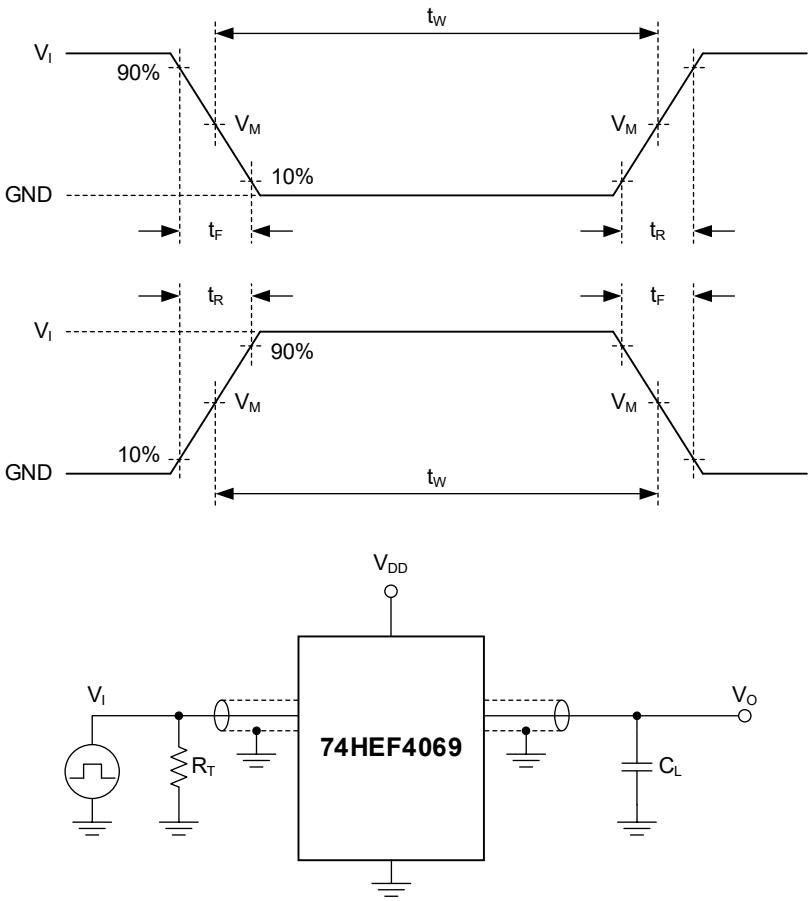
Voltage Gain vs. Supply Voltage (1)



NOTE:

1. The curves are measured using the circuit shown in Figure 6.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

C_L: Load capacitance (includes jig and probe).

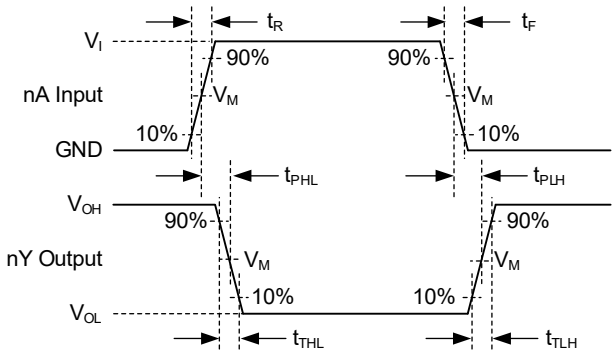
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD
V_{DD}	V_I	t_R, t_F	C_L
3V to 13.2V	V_{SS} or V_{DD}	≤ 20ns	50pF

WAVEFORMS



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nA) to Output (nY) Propagation Delay Times and Transition Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{DD}	V_I	V_M (1)	V_M
3V to 13.2V	V_{SS} or V_{DD}	0.5 × V_{DD}	0.5 × V_{DD}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 20ns.

APPLICATION INFORMATION

Figure 3 to Figure 6 show some typical application examples of 74HEF4069.

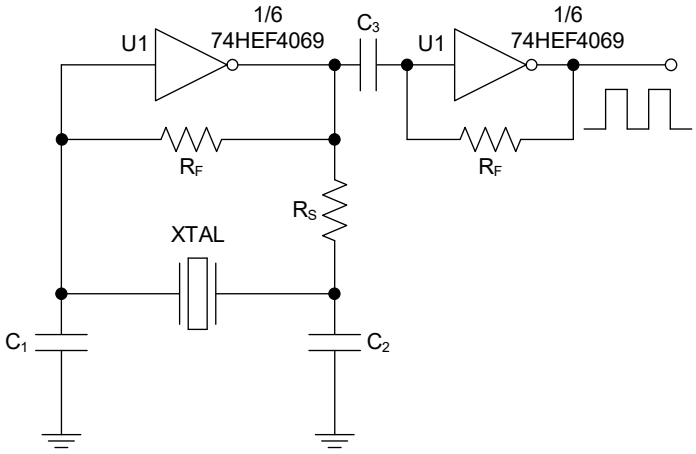


Figure 3. Typical Crystal Oscillator

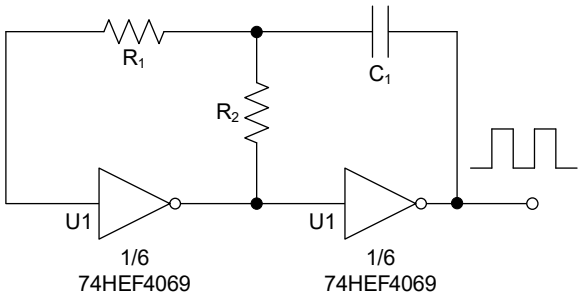


Figure 4. Typical RC Oscillator

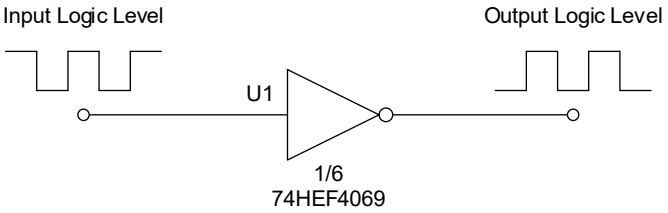


Figure 5. Typical Logic Inverter

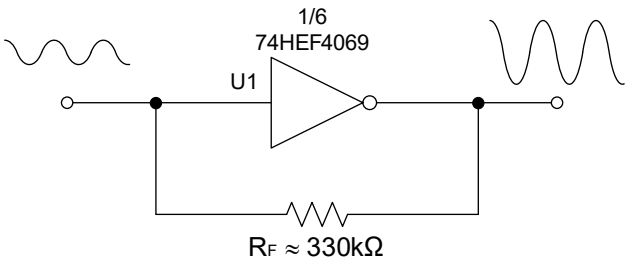


Figure 6. Typical High-Input-Impedance Amplifier

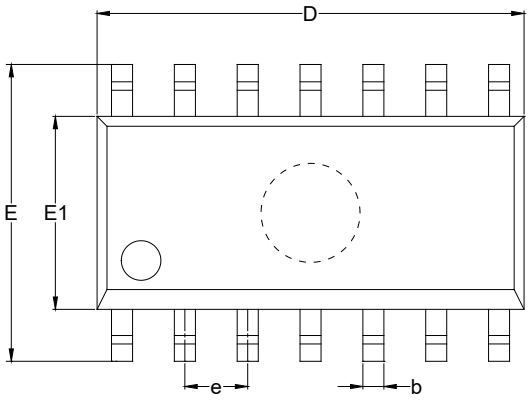
REVISION HISTORY

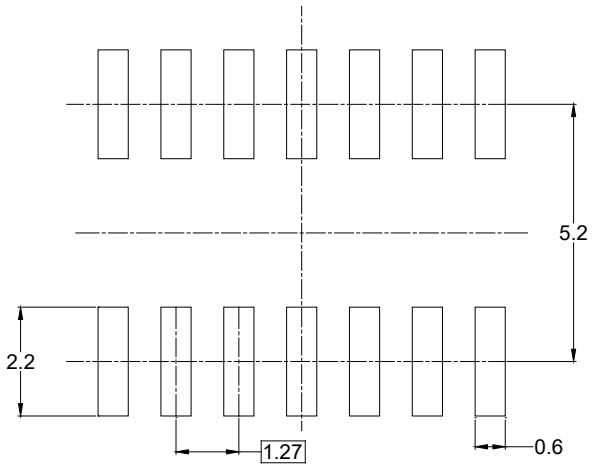
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (SEPTEMBER 2025)	Page
Changed from product preview to production data	All

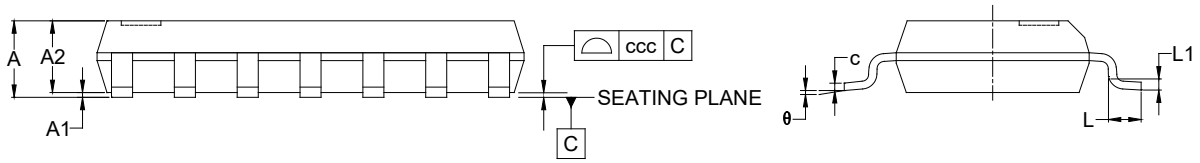
PACKAGE OUTLINE DIMENSIONS

SOIC-14





RECOMMENDED LAND PATTERN (Unit: mm)

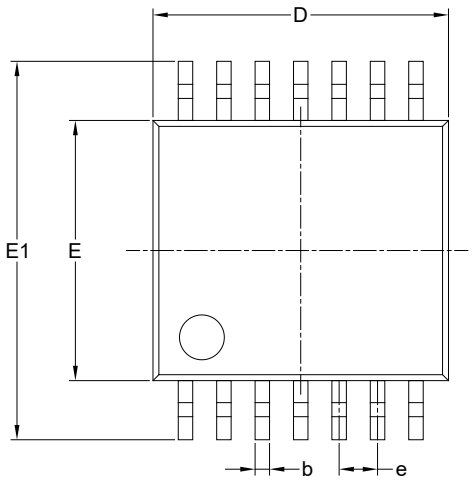


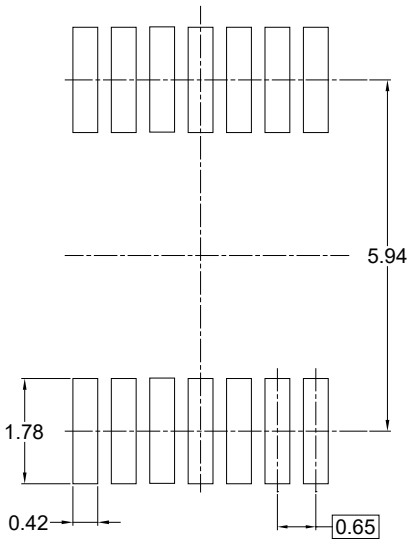
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	-
b	0.310	-	0.510
c	0.100	-	0.250
D	8.450	-	8.850
E	5.800	-	6.200
E1	3.800	-	4.000
e	1.270 BSC		
L	0.400	-	1.270
L1	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

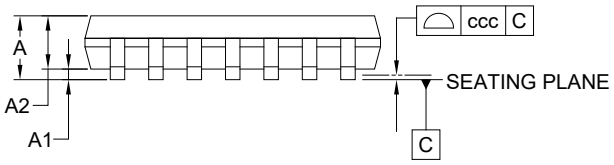
PACKAGE OUTLINE DIMENSIONS

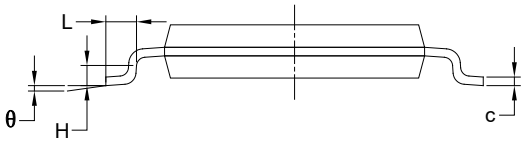
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



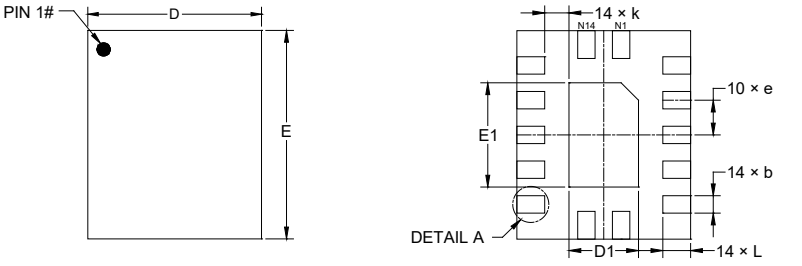


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

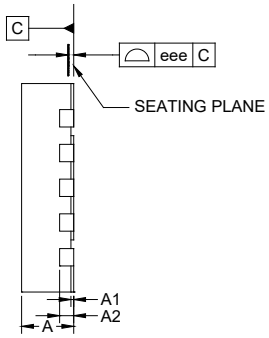
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

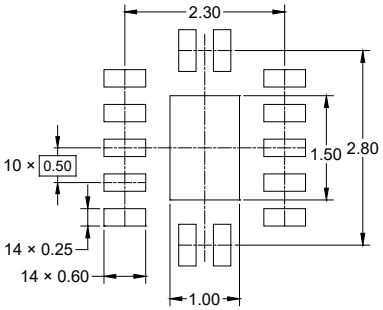
PACKAGE OUTLINE DIMENSIONS

TQFN-2.5×3-14L



TOP VIEW **BOTTOM VIEW**





SIDE VIEW **RECOMMENDED LAND PATTERN** (Unit: mm)

ALTERNATE A-1 ALTERNATE A-2

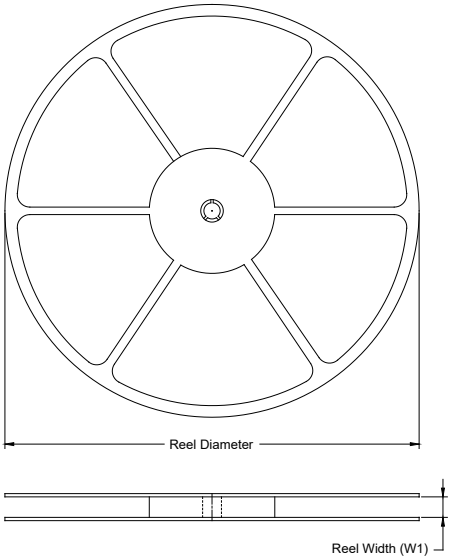
DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	2.400	-	2.600
D1	0.900	-	1.100
E	2.900	-	3.100
E1	1.400	-	1.600
e		0.500 BSC	
k		0.350 REF	
L	0.300	-	0.500
eee		0.080	

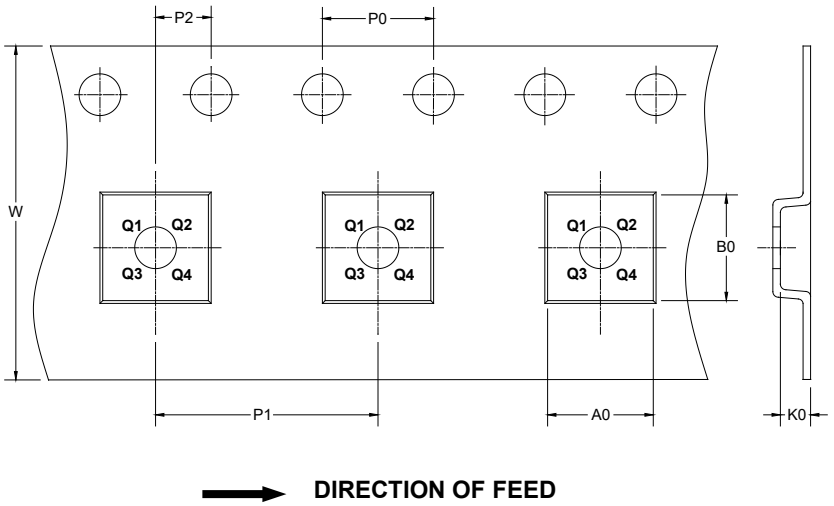
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



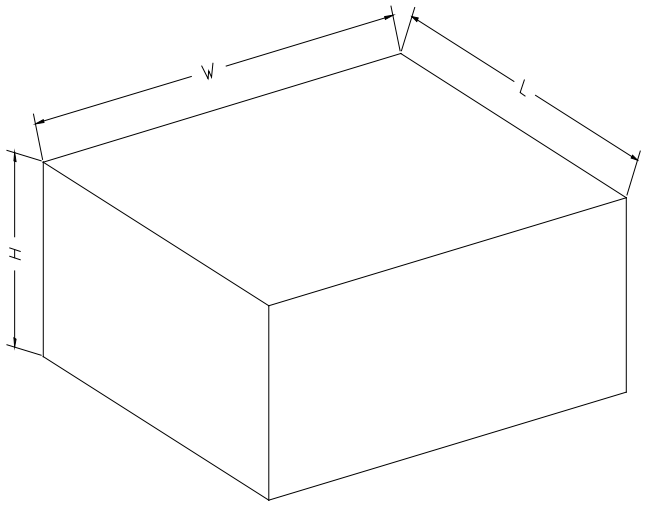
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-14	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-2.5×3-14L	13"	12.4	2.80	3.30	1.15	4.0	4.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002