



# SGM4523

## 5V, Bidirectional 4:1, 2-Channel Multiplexer with Injection Current Control

### GENERAL DESCRIPTION

The SGM4523 is a 4:1, 2-channel CMOS analog multiplexer with injection current control. The device has two control inputs that can be used as selecting one of the 4 channels (Sx) to connect to the common terminal (Dx). The multiplexer supports bidirectional signal transmission in the voltage range from GND to  $V_{DD}$ .

All logic inputs of the SGM4523 are allowed to be equal to the power supply voltage and compatible with TTL and CMOS logic thresholds standards during normal operation of the power supply. Besides, all control inputs are also designed with fail-safe function. It allows the voltage of all control pins within the maximum absolute withstand voltage range to exceed the  $V_{DD}$  without damaging the device.

The injection current control function of the SGM4523 allows signals on disabled signal channels to exceed the  $V_{DD}$  without affecting the enabled signal channel. In addition, all pins of the SGM4523 except GND are not designed with internal diodes path to the  $V_{DD}$  pin, so as not to damage the components connected to the power pin and avoid injecting reverse current into the power supply.

The SGM4523 is available in Green TSSOP-16 and TQFN-2.5×3.5-16L packages. It operates over an operating temperature range of -40°C to +125°C.

### FEATURES

- **$V_{DD}$  Operation Range: 1.62V to 5.5V**
- **Injection Current Control**
- **Back-Powering Protection**  
**No ESD Diodes between All Ports and  $V_{DD}$**
- **Bidirectional Signal Path**
- **Rail-to-Rail Operation**
- **Control Pin Fail-Safe Function**
- **Break-Before-Make Switching**
- **-40°C to +125°C Operating Temperature Range**
- **Available in Green TSSOP-16 and TQFN-2.5×3.5-16L Packages**

### APPLICATIONS

Battery Management Systems (BMS)  
Signal Multiplexing and Demultiplexing  
Diagnostics and Monitoring  
ADC and DAC System

# 5V, Bidirectional 4:1, SGM4523 2-Channel Multiplexer with Injection Current Control

## PACKAGE/ORDERING INFORMATION

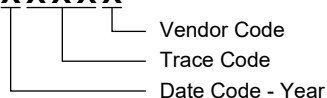
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4523	TSSOP-16	-40°C to +125°C	SGM4523XTS16G/TR	SGM4523 XTS16 XXXXX	Tape and Reel, 4000
	TQFN-2.5×3.5-16L	-40°C to +125°C	SGM4523XTRG16G/TR	1YXRG XXXXX	Tape and Reel, 8000

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

### TSSOP-16/TQFN-2.5×3.5-16L

**XXXXX**



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range, $V_{DD}$ .....	-0.5V to 6V
Logic Control Input Pin Voltage ( $\overline{EN}$ , A0, A1), $V_{SEL}$ or $V_{EN}$ .....	-0.5V to 6V
Source or Drain Voltage, $V_S$ or $V_D$ .....	-0.5V to ( $V_{DD} + 0.5V$ )
Continuous Current through Switch (Sx, Dx Pins), $I_S$ or $I_{D(CONT)}$ , -40°C to +125°C .....	-50mA to 50mA
Continuous Current through GND, $I_{GND}$ ....	-100mA to 100mA
Package Thermal Resistance	
TSSOP-16, $\theta_{JA}$ .....	130.8°C/W
TSSOP-16, $\theta_{JB}$ .....	88.2°C/W
TSSOP-16, $\theta_{JC}$ .....	53.6°C/W
TQFN-2.5×3.5-16L, $\theta_{JA}$ .....	63.8°C/W
TQFN-2.5×3.5-16L, $\theta_{JB}$ .....	25.4°C/W
TQFN-2.5×3.5-16L, $\theta_{JC(TOP)}$ .....	51.3°C/W
TQFN-2.5×3.5-16L, $\theta_{JC(BOT)}$ .....	7.3°C/W
Junction Temperature.....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility <sup>(1)(2)</sup>	
HBM.....	±4000V
CDM .....	±1000V

## NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

**RECOMMENDED OPERATING CONDITIONS**

Supply Voltage Range, $V_{DD}$ .....	1.62V to 5.5V
Signal Path Input/Output Voltage, $V_S$ or $V_D$ .....	0V to $V_{DD}$
Logic Control Input Pin Voltage ( $\overline{EN}$ , A0, A1), $V_{SEL}$ or $V_{EN}$ .....	0V to 5.5V
Continuous Current through Switch (Sx, Dx Pins), $I_S$ or $I_{D(CONT)}$ , -40°C to +125°C.....	-50mA to 50mA
Current per Input into Source or Drain Pins when Signal Voltage Exceeds Recommended Operating Voltage, $I_{OK}$ .....	-50mA to 50mA
Injected Current into Single Off Switch Input, $I_{INJ}$ .....	-50mA to 50mA
Total Injected Current into All Off Switch Inputs Combined, $I_{INJ\_ALL}$ .....	-100mA to 100mA
Operating Ambient Temperature Range .....	-40°C to +125°C

**OVERSTRESS CAUTION**

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

**ESD SENSITIVITY CAUTION**

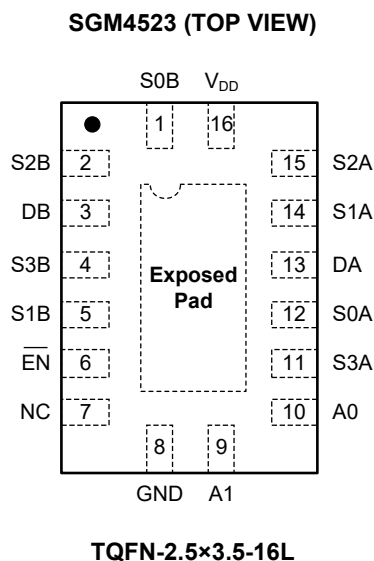
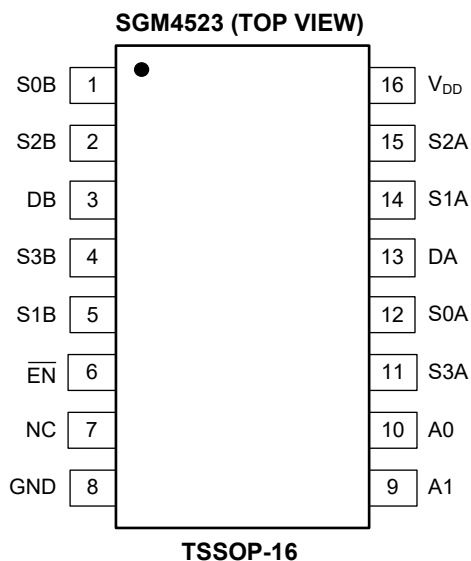
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

**DISCLAIMER**

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

# SGM4523 5V, Bidirectional 4:1, 2-Channel Multiplexer with Injection Current Control

## PIN CONFIGURATIONS



## PIN DESCRIPTION

PIN		NAME	FUNCTION
TSSOP-16	TQFN-2.5x3.5-16L		
1	1	S0B	Source Pin 0 of Mux B. Signal input or output path.
2	2	S2B	Source Pin 2 of Mux B. Signal input or output path.
3	3	DB	Drain Pin (Common Terminal) of Mux B. Signal input or output path.
4	4	S3B	Source Pin 3 of Mux B. Signal input or output path.
5	5	S1B	Source Pin 1 of Mux B. Signal input or output path.
6	6	$\overline{\text{EN}}$	Enable Control Input Pin (Active Low). When $\overline{\text{EN}}$ is set to high, common terminal is disconnected to any other signal ports and the switch is turned off.
7	7	NC	No Connection.
8	8	GND	Ground Pin.
9	9	A1	Digital Address A1 Pin.
10	10	A0	Digital Address A0 Pin.
11	11	S3A	Source Pin 3 of Mux A. Signal input or output path.
12	12	S0A	Source Pin 0 of Mux A. Signal input or output path.
13	13	DA	Drain Pin (Common Terminal) of Mux A. Signal input or output path.
14	14	S1A	Source Pin 1 of Mux A. Signal input or output path.
15	15	S2A	Source Pin 2 of Mux A. Signal input or output path.
16	16	$V_{\text{DD}}$	Power Supply Pin. It is recommended to connect a 0.1 $\mu\text{F}$ to 10 $\mu\text{F}$ capacitor between $V_{\text{DD}}$ and GND to get good power supply decoupling.
—	Exposed Pad	Exposed Pad	Exposed Pad. It can be connected to GND or be left floating.

FUNCTIONAL BLOCK DIAGRAM

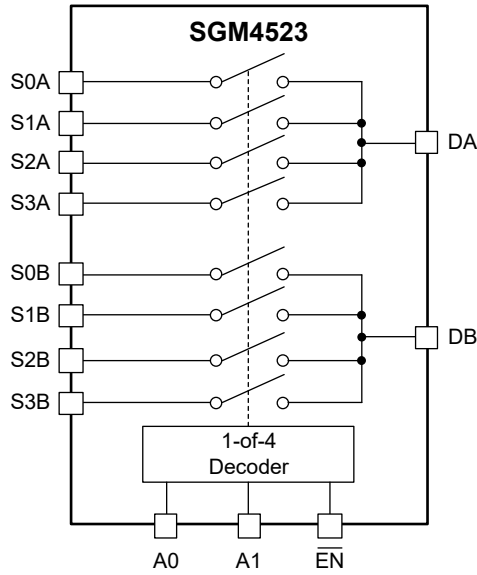


Figure 1. Block Diagram

FUNCTION TABLE

$\overline{\text{EN}}$	SELECT INPUTS		SELECTED SIGNAL PATH CONNECTED TO DRAIN (D) PIN
	A1	A0	
0	0	0	S0A to DA S0B to DB
0	0	1	S1A to DA S1B to DB
0	1	0	S2A to DA S2B to DB
0	1	1	S3A to DA S3B to DB
1	X	X	All Channels are OFF

NOTE: X = Don't care.

## ELECTRICAL CHARACTERISTICS

(At specified  $V_{DD} \pm 10\%$ , typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
On-Resistance	$R_{ON}$	$V_S = 0\text{V to } V_{DD}, I_{SD} = 0.5\text{mA},$ Test Circuit 1	$V_{DD} = 1.8\text{V}$	+25°C	950	1600	$\Omega$
				Full		1800	
			$V_{DD} = 2.5\text{V}$	+25°C	260	385	
				Full		420	
			$V_{DD} = 3.3\text{V}$	+25°C	150	210	
				Full		240	
			$V_{DD} = 5\text{V}$	+25°C	93	120	
				Full		150	
On-Resistance Matching between Inputs	$\Delta R_{ON}$	$V_S = 0\text{V to } V_{DD}, I_{SD} = 0.5\text{mA},$ Test Circuit 1	$V_{DD} = 1.8\text{V}$	+25°C	11	90	$\Omega$
				Full		95	
			$V_{DD} = 2.5\text{V}$	+25°C	2.5	18	
				Full		20	
			$V_{DD} = 3.3\text{V}$	+25°C	1.2	8.5	
				Full		10	
			$V_{DD} = 5\text{V}$	+25°C	1	6	
				Full		7	
On-Resistance Flatness	$R_{FLAT}$	$V_S = 0\text{V to } V_{DD}, I_{SD} = 0.5\text{mA},$ Test Circuit 1	$V_{DD} = 1.8\text{V}$	+25°C	825	1400	$\Omega$
				Full		1500	
			$V_{DD} = 2.5\text{V}$	25°C	175	270	
				Full		310	
			$V_{DD} = 3.3\text{V}$	+25°C	83	125	
				Full		130	
			$V_{DD} = 5\text{V}$	+25°C	40	60	
				Full		70	
Channel On Leakage Current	$I_{D(ON)}$ $I_{S(ON)}$	Switch On $V_D = V_S = 0.8 \times V_{DD}$ or $V_D = V_S = 0.2 \times V_{DD},$ Test Circuit 2	$V_{DD} = 1.8\text{V}$	Full	$\pm 10$	$\pm 800$	nA
			$V_{DD} = 2.5\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 3.3\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 5\text{V}$	Full	$\pm 10$	$\pm 800$	
Source Off Leakage Current	$I_{S(OFF)}$	Switch Off $V_D = 0.8 \times V_{DD}/ 0.2 \times V_{DD},$ $V_S = 0.2 \times V_{DD}/ 0.8 \times V_{DD},$ Test Circuit 3	$V_{DD} = 1.8\text{V}$	Full	$\pm 10$	$\pm 800$	nA
			$V_{DD} = 2.5\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 3.3\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 5\text{V}$	Full	$\pm 10$	$\pm 800$	
Drain Off Leakage Current (Common Drain Pin)	$I_{D(OFF)}$	Switch Off $V_D = 0.8 \times V_{DD}/ 0.2 \times V_{DD},$ $V_S = 0.2 \times V_{DD}/ 0.8 \times V_{DD},$ Test Circuit 3	$V_{DD} = 1.8\text{V}$	Full	$\pm 10$	$\pm 800$	nA
			$V_{DD} = 2.5\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 3.3\text{V}$	Full	$\pm 10$	$\pm 800$	
			$V_{DD} = 5\text{V}$	Full	$\pm 10$	$\pm 800$	
$V_{DD}$ Supply Current	$I_{DDH}$	Logic Inputs = $V_{DD}$	$V_{DD} = 1.8\text{V}$	Full	0.01	1	$\mu\text{A}$
			$V_{DD} = 2.5\text{V}$	Full	0.01	1	
			$V_{DD} = 3.3\text{V}$	Full	0.01	1	
			$V_{DD} = 5\text{V}$	Full	0.01	1	
$V_{DD}$ Supply Current	$I_{DDL}$	Logic Inputs = 0V	$V_{DD} = 1.8\text{V}$	Full	0.2	1	$\mu\text{A}$
			$V_{DD} = 2.5\text{V}$	Full	0.3	1	
			$V_{DD} = 3.3\text{V}$	Full	0.4	1	
			$V_{DD} = 5\text{V}$	Full	0.6	2	

**ELECTRICAL CHARACTERISTICS (continued)**(At specified  $V_{DD} \pm 10\%$ , typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX <sup>(1)</sup>	UNITS	
Source Off Capacitance	$C_{SOFF}$	$V_S = V_{DD} / 2, f = 1\text{MHz}$	$V_{DD} = 1.8\text{V}$	Full		8.5	15	pF
			$V_{DD} = 2.5\text{V}$	Full		8.5	15	
			$V_{DD} = 3.3\text{V}$	Full		8	15	
			$V_{DD} = 5\text{V}$	Full		7.8	15	
Drain Off Capacitance	$C_{DOFF}$	$V_S = V_{DD} / 2, f = 1\text{MHz}$	$V_{DD} = 1.8\text{V}$	Full		10.5	17	pF
			$V_{DD} = 2.5\text{V}$	Full		10.5	17	
			$V_{DD} = 3.3\text{V}$	Full		10.5	17	
			$V_{DD} = 5\text{V}$	Full		10	17	
On Capacitance	$C_{ON}$	$V_S = V_{DD} / 2, f = 1\text{MHz}$	$V_{DD} = 1.8\text{V}$	Full		22.5	30	pF
			$V_{DD} = 2.5\text{V}$	Full		22	30	
			$V_{DD} = 3.3\text{V}$	Full		22	30	
			$V_{DD} = 5\text{V}$	Full		21	30	

## NOTE:

1. Specified by design and characterization, not production tested.

## LOGIC AND DYNAMIC CHARACTERISTICS

(At specified  $V_{DD} \pm 10\%$ , typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
<b>Logic Inputs (<math>\overline{\text{EN}}</math>, A0, A1)</b>							
Input Logic High	$V_{IH}$	$V_{DD} = 1.8\text{V}$	Full	1.0		5.5	V
		$V_{DD} = 2.5\text{V}$	Full	1.1		5.5	
		$V_{DD} = 3.3\text{V}$	Full	1.15		5.5	
		$V_{DD} = 5\text{V}$	Full	1.25		5.5	
Input Logic Low	$V_{IL}$	$V_{DD} = 1.8\text{V}$	Full	0		0.55	V
		$V_{DD} = 2.5\text{V}$	Full	0		0.65	
		$V_{DD} = 3.3\text{V}$	Full	0		0.8	
		$V_{DD} = 5\text{V}$	Full	0		0.9	
Logic High Input Leakage Current	$I_{IH}$	$V_{\text{LOGIC}} = 1.8\text{V}$ or $V_{DD}$	Full		0.01	1	$\mu\text{A}$
Logic Low Input Leakage Current	$I_{IL\_AI}$	$V_{\text{LOGIC}} = 0\text{V}$ , $V_{DD} = 1.8\text{V}$ to $5\text{V}$	Full	-1	-0.01		$\mu\text{A}$
	$I_{IL\_EN}$	$V_{\text{LOGIC}} = 0\text{V}$	$V_{DD} = 1.8\text{V}$	Full	-1	-0.2	
			$V_{DD} = 2.5\text{V}$	Full	-1	-0.3	
			$V_{DD} = 3.3\text{V}$	Full	-1	-0.4	
		$V_{DD} = 5\text{V}$	Full	-2	-0.6		
Logic Input Capacitance	$C_{IN}$	$V_{\text{LOGIC}} = 0\text{V}$ , $1.8\text{V}$ or $V_{DD}$ , $f = 1\text{MHz}$	Full		6.5	10	pF
<b>Dynamic Characteristics</b>							
Charge Injection	$Q_{INJ}$	$V_S = V_{DD} / 2$ , $C_L = 100\text{pF}^{(1)}$ , Test Circuit 4	$V_{DD} = 1.8\text{V}$	+25°C		-2	pC
			$V_{DD} = 2.5\text{V}$	+25°C		-6	
			$V_{DD} = 3.3\text{V}$	+25°C		-10	
			$V_{DD} = 5\text{V}$	+25°C		-18	
Off-Isolation	$O_{ISO}$	$V_{BIAS} = V_{DD} / 2$ , $V_S = 200\text{mVpp}$ , $R_L = 50\Omega$ , $C_L = 12\text{pF}^{(1)}$ , $f = 100\text{kHz}$ , Test Circuit 5	$V_{DD} = 1.8\text{V}$	+25°C		-100	dB
			$V_{DD} = 2.5\text{V}$	+25°C		-100	
			$V_{DD} = 3.3\text{V}$	+25°C		-100	
			$V_{DD} = 5\text{V}$	+25°C		-100	
	$O_{ISO}$	$V_{BIAS} = V_{DD} / 2$ , $V_S = 200\text{mVpp}$ , $R_L = 50\Omega$ , $C_L = 12\text{pF}^{(1)}$ , $f = 1\text{MHz}$ , Test Circuit 5	$V_{DD} = 1.8\text{V}$	+25°C		-80	dB
			$V_{DD} = 2.5\text{V}$	+25°C		-80	
			$V_{DD} = 3.3\text{V}$	+25°C		-80	
			$V_{DD} = 5\text{V}$	+25°C		-80	
Channel-to-Channel Crosstalk	$X_{TALK}$	$V_{BIAS} = V_{DD} / 2$ , $V_S = 200\text{mVpp}$ , $R_L = 50\Omega$ , $C_L = 12\text{pF}^{(1)}$ , $f = 100\text{kHz}$ , Test Circuit 6	$V_{DD} = 1.8\text{V}$	+25°C		-95	dB
			$V_{DD} = 2.5\text{V}$	+25°C		-95	
			$V_{DD} = 3.3\text{V}$	+25°C		-95	
			$V_{DD} = 5\text{V}$	+25°C		-95	
	$X_{TALK}$	$V_{BIAS} = V_{DD} / 2$ , $V_S = 200\text{mVpp}$ , $R_L = 50\Omega$ , $C_L = 12\text{pF}^{(1)}$ , $f = 1\text{MHz}$ , Test Circuit 6	$V_{DD} = 1.8\text{V}$	+25°C		-75	dB
			$V_{DD} = 2.5\text{V}$	+25°C		-75	
			$V_{DD} = 3.3\text{V}$	+25°C		-75	
			$V_{DD} = 5\text{V}$	+25°C		-75	
-3dB Bandwidth	BW	$V_{BIAS} = V_{DD} / 2$ , $V_S = 200\text{mVpp}$ , $R_L = 50\Omega$ , $C_L = 12\text{pF}^{(1)}$ , Test Circuit 7	$V_{DD} = 1.8\text{V}$	+25°C		235	MHz
			$V_{DD} = 2.5\text{V}$	+25°C		210	
			$V_{DD} = 3.3\text{V}$	+25°C		210	
			$V_{DD} = 5\text{V}$	+25°C		210	

NOTE: 1.  $C_L$  = Load capacitance including jig and probe capacitance.

# 5V, Bidirectional 4:1, SGM4523 2-Channel Multiplexer with Injection Current Control

## TIMING CHARACTERISTICS

(At specified  $V_{DD} \pm 10\%$ , typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN <sup>(1)</sup>	TYP	MAX <sup>(1)</sup>	UNITS	
<b>Switching Characteristics</b>								
Propagation Delay Time	$t_{PD}$	$C_L = 50\text{pF}^{(2)}$ , Sx to D, D to Sx	$V_{DD} = 1.8\text{V}$	Full		20	35	ns
			$V_{DD} = 2.5\text{V}$	Full		13	25	
			$V_{DD} = 3.3\text{V}$	Full		9	20	
			$V_{DD} = 5\text{V}$	Full		6.5	17	
		$C_L = 15\text{pF}^{(2)}$ , $V_{DD} = 5\text{V}$	Full		3	12		
Transition-Time between Inputs	$t_{TRANS}^{(3)}$	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}^{(2)}$ , Ax to D, Ax to Sx, Test Circuit 8	$V_{DD} = 1.8\text{V}$	Full		130	165	ns
			$V_{DD} = 2.5\text{V}$	Full		65	100	
			$V_{DD} = 3.3\text{V}$	Full		45	75	
			$V_{DD} = 5\text{V}$	Full		32	60	
		$R_L = 10\text{k}\Omega$ , $C_L = 15\text{pF}^{(2)}$ , $V_{DD} = 5\text{V}$ , Test Circuit 8	Full		30	55		
Turn-On Time from Enable	$t_{ON\_EN}^{(4)}$	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}^{(2)}$ , $\overline{EN}$ to D, $\overline{EN}$ to Sx, Test Circuit 9	$V_{DD} = 1.8\text{V}$	Full		58	75	ns
			$V_{DD} = 2.5\text{V}$	Full		34	50	
			$V_{DD} = 3.3\text{V}$	Full		25	42	
			$V_{DD} = 5\text{V}$	Full		20	35	
		$R_L = 10\text{k}\Omega$ , $C_L = 15\text{pF}^{(2)}$ , $V_{DD} = 5\text{V}$ , Test Circuit 9	Full		18	45		
Turn-Off Time from Enable	$t_{OFF\_EN}^{(5)}$	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}^{(2)}$ , $\overline{EN}$ to D, $\overline{EN}$ to Sx, Test Circuit 9	$V_{DD} = 1.8\text{V}$	Full		105	145	ns
			$V_{DD} = 2.5\text{V}$	Full		60	100	
			$V_{DD} = 3.3\text{V}$	Full		35	70	
			$V_{DD} = 5\text{V}$	Full		20	45	
		$R_L = 10\text{k}\Omega$ , $C_L = 15\text{pF}^{(2)}$ , $V_{DD} = 5\text{V}$ , Test Circuit 9	Full		13	40		
Break-Before-Make Delay Time	$t_D$	$R_L = 10\text{k}\Omega$ , $C_L = 15\text{pF}^{(2)}$ , Sx to D, D to Sx, Test Circuit 10	$V_{DD} = 1.8\text{V}$	Full	1	29		ns
			$V_{DD} = 2.5\text{V}$	Full	0.5	17		
			$V_{DD} = 3.3\text{V}$	Full	0.5	13		
			$V_{DD} = 5\text{V}$	Full	0.5	9.5		

### NOTES:

- Specified by design and characterization, not production tested.
- $C_L$  = Load capacitance including jig and probe capacitance.
- If the input logic signal's high level amplitude is  $V_{IH}(\text{MIN})$  and low level amplitude is  $V_{IL}(\text{MAX})$ , the  $t_{TRANS}$  will be  $1.5\mu\text{s}$ .
- If the input logic signal's high level amplitude is  $V_{IH}(\text{MIN})$  and low level amplitude is  $V_{IL}(\text{MAX})$ , the  $t_{ON\_EN}$  will be  $1.5\mu\text{s}$ .
- If the input logic signal's high level amplitude is  $V_{IH}(\text{MIN})$  and low level amplitude is  $V_{IL}(\text{MAX})$ , the  $t_{OFF\_EN}$  will be  $0.5\mu\text{s}$ .

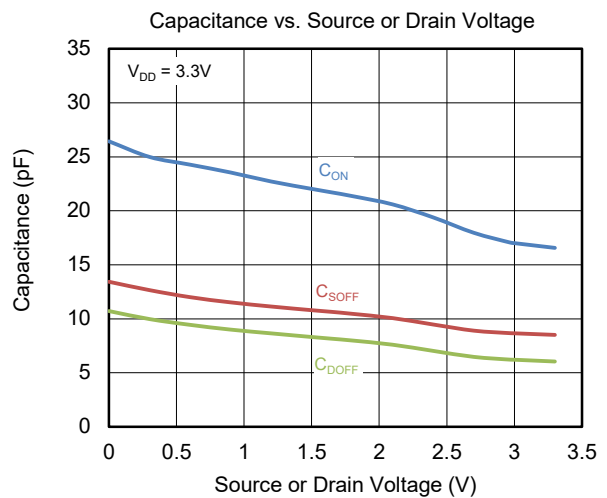
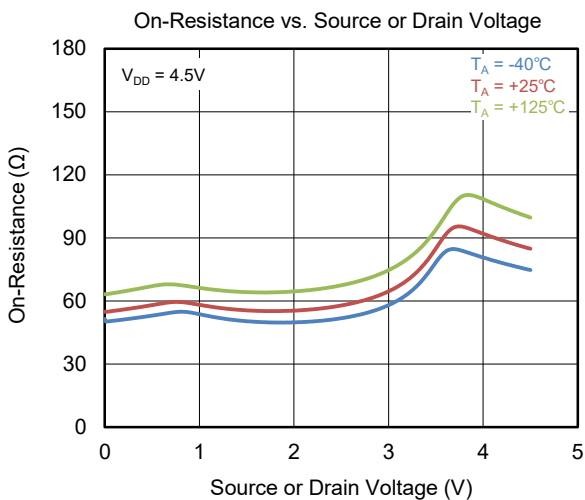
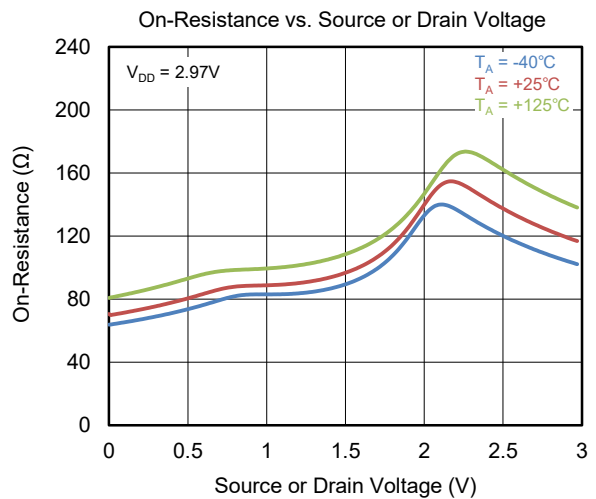
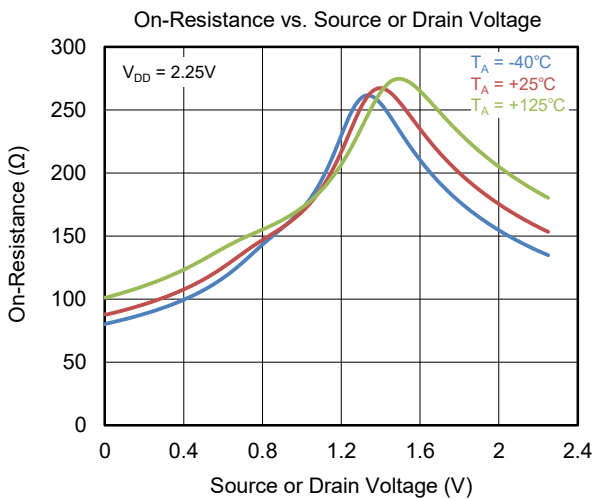
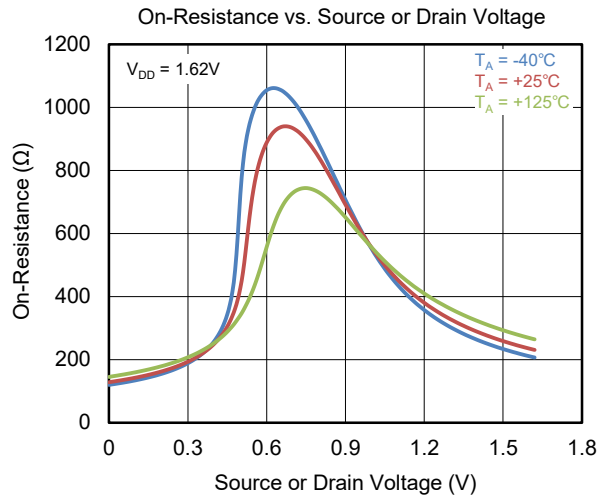
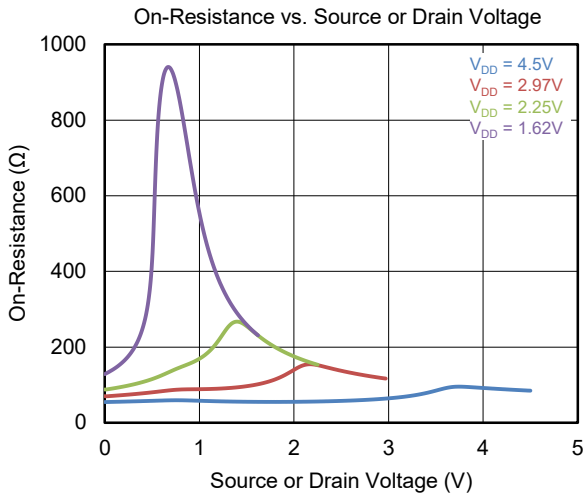
## INJECTION CURRENT COUPLING

(At specified  $V_{DD} \pm 10\%$ , typical values are at  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	
<b>Injection Current Coupling, Test Circuit 11</b>								
Maximum Shift of Output Voltage of Enabled Analog Input	$\Delta V_{OUT}$	$R_S \leq 3.9\text{k}\Omega$ , $I_{INJ} \leq 1\text{mA}$	$V_{DD} = 1.8\text{V}$	Full		0.01	1	mV
			$V_{DD} = 5\text{V}$	Full		0.01	0.5	
		$R_S \leq 3.9\text{k}\Omega$ , $I_{INJ} \leq 10\text{mA}$	$V_{DD} = 1.8\text{V}$	Full		0.01	1	
			$V_{DD} = 5\text{V}$	Full		0.01	0.5	
		$R_S \leq 20\text{k}\Omega$ , $I_{INJ} \leq 1\text{mA}$	$V_{DD} = 1.8\text{V}$	Full		0.01	1	
			$V_{DD} = 5\text{V}$	Full		0.01	0.5	
		$R_S \leq 20\text{k}\Omega$ , $I_{INJ} \leq 10\text{mA}$	$V_{DD} = 1.8\text{V}$	Full		0.01	1	
			$V_{DD} = 5\text{V}$	Full		0.01	0.5	

TYPICAL PERFORMANCE CHARACTERISTICS

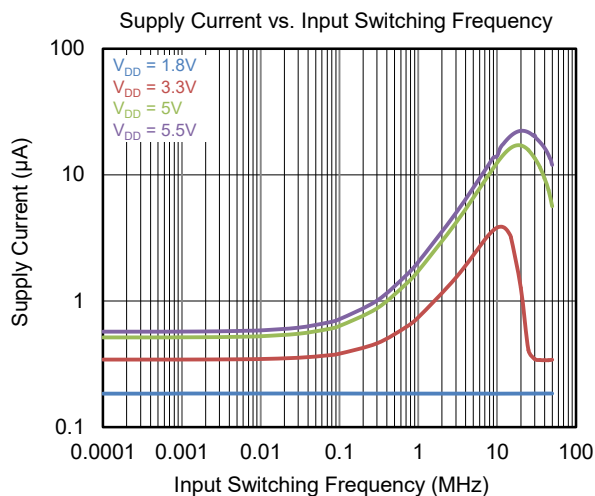
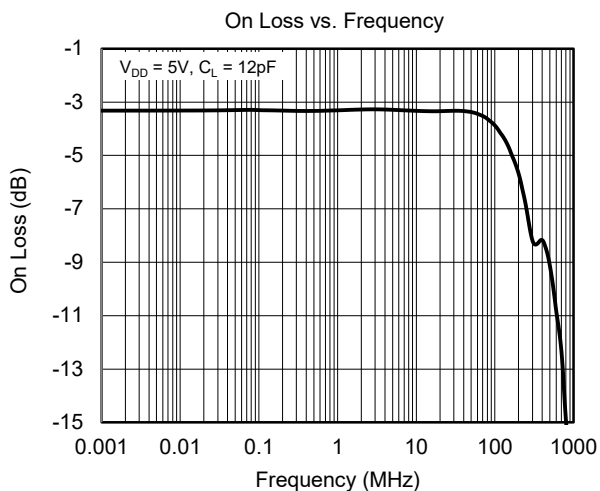
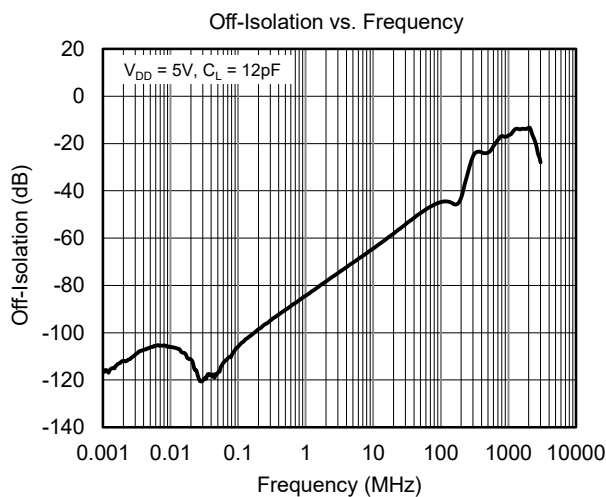
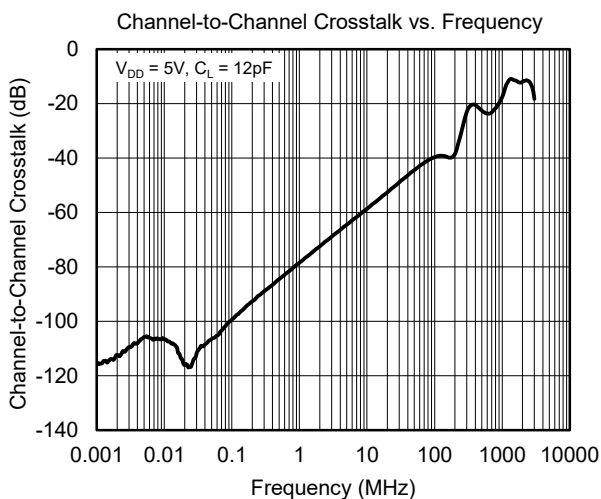
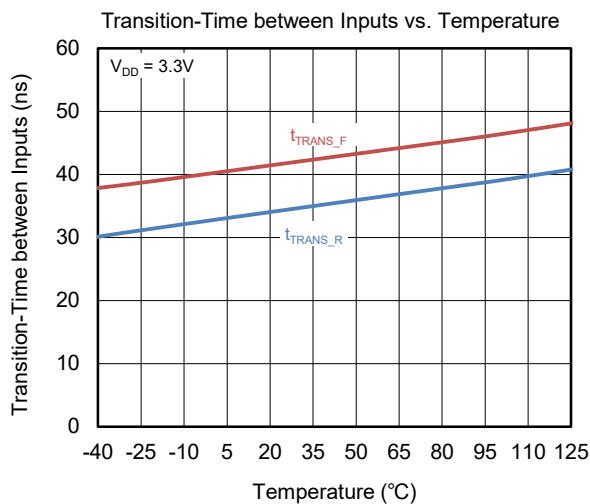
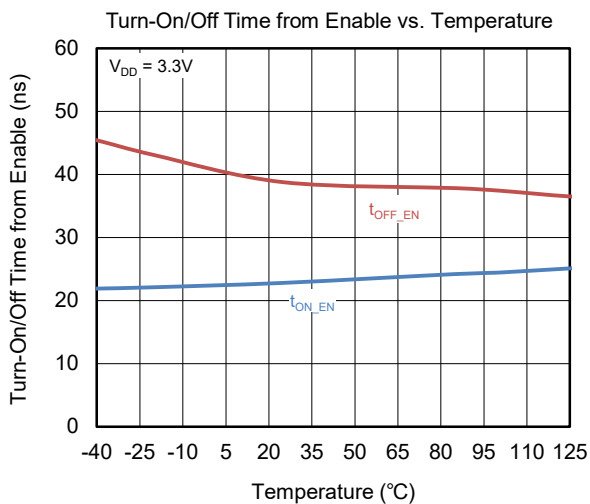
T<sub>A</sub> = +25°C, unless otherwise noted.



# SGM4523 5V, Bidirectional 4:1, 2-Channel Multiplexer with Injection Current Control

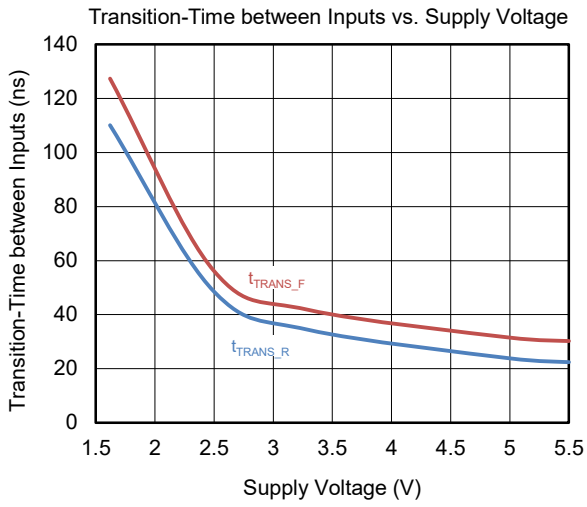
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A = +25^\circ\text{C}$ , unless otherwise noted.

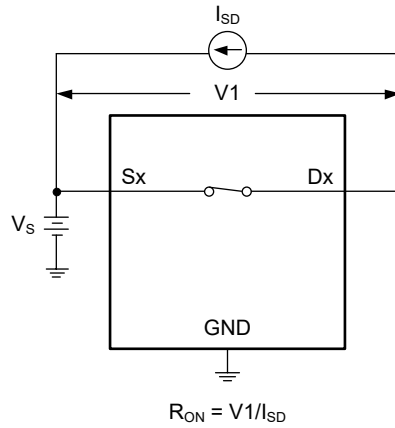


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

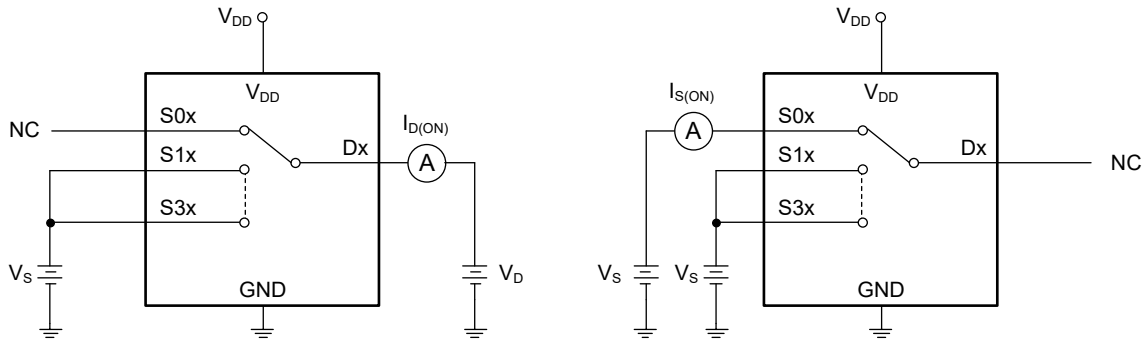
T<sub>A</sub> = +25°C, unless otherwise noted.



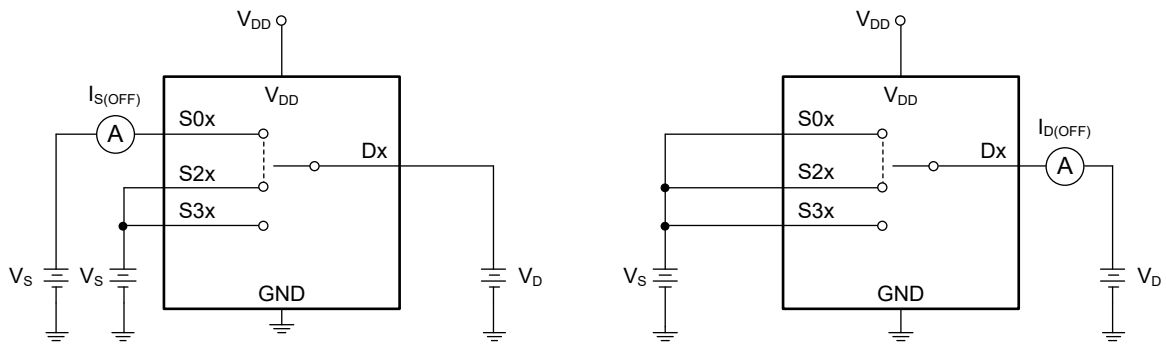
TEST CIRCUITS



Test Circuit 1. On-Resistance

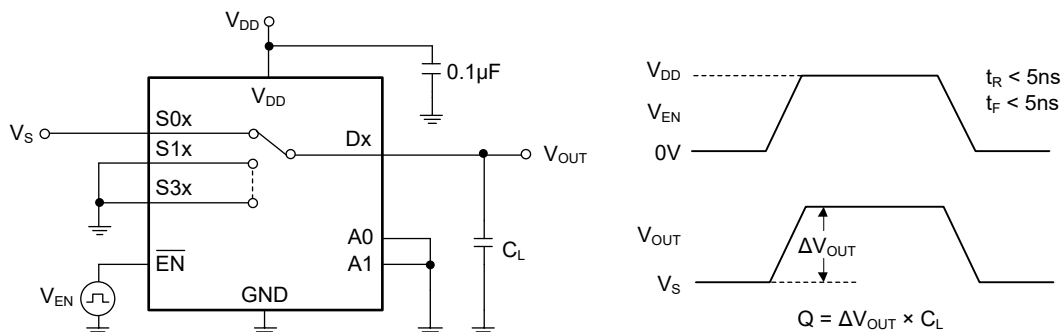


Test Circuit 2. On Leakage

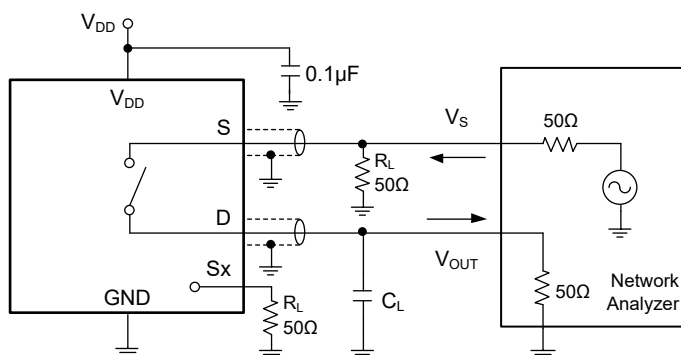


Test Circuit 3. Off Leakage

**TEST CIRCUITS (continued)**

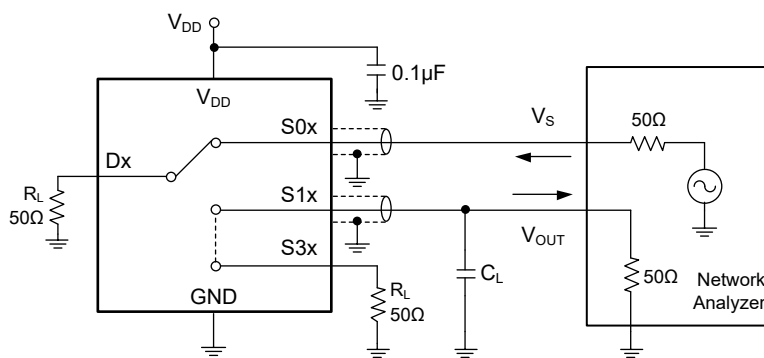


**Test Circuit 4. Charge Injection (Q)**



Off-Isolation =  $20\log(V_{OUT}/V_S)$

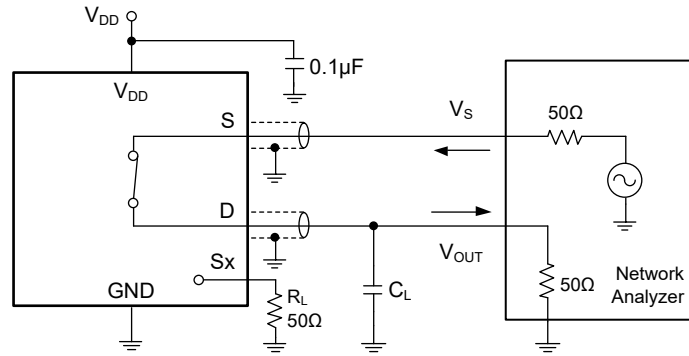
**Test Circuit 5. Off-Isolation**



Channel-to-Channel Crosstalk =  $20\log(V_{OUT}/V_S)$

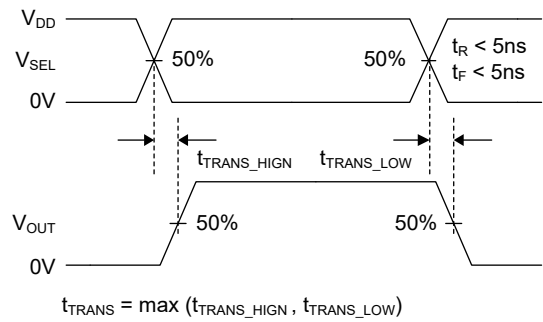
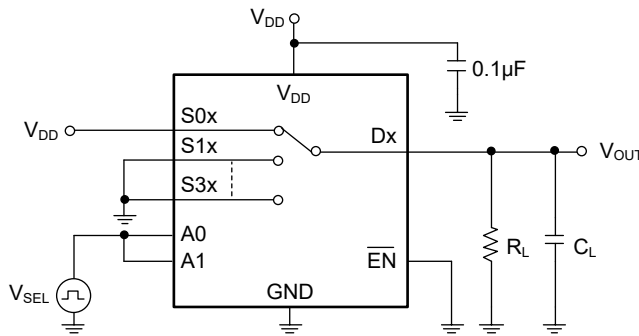
**Test Circuit 6. Channel-to-Channel Crosstalk**

**TEST CIRCUITS (continued)**

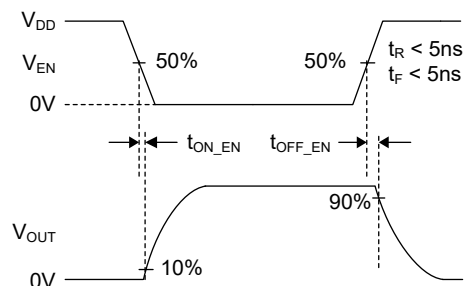
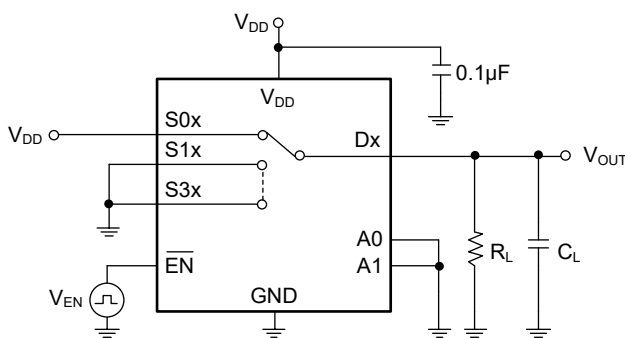


On Loss =  $20\log(V_{OUT}/V_S)$

**Test Circuit 7. On Loss**

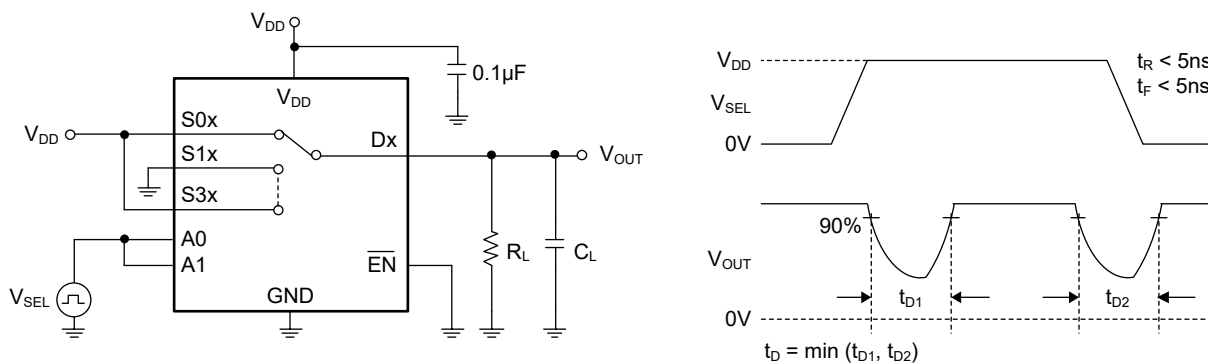


**Test Circuit 8. Transition Time ( $t_{TRANS}$ )**

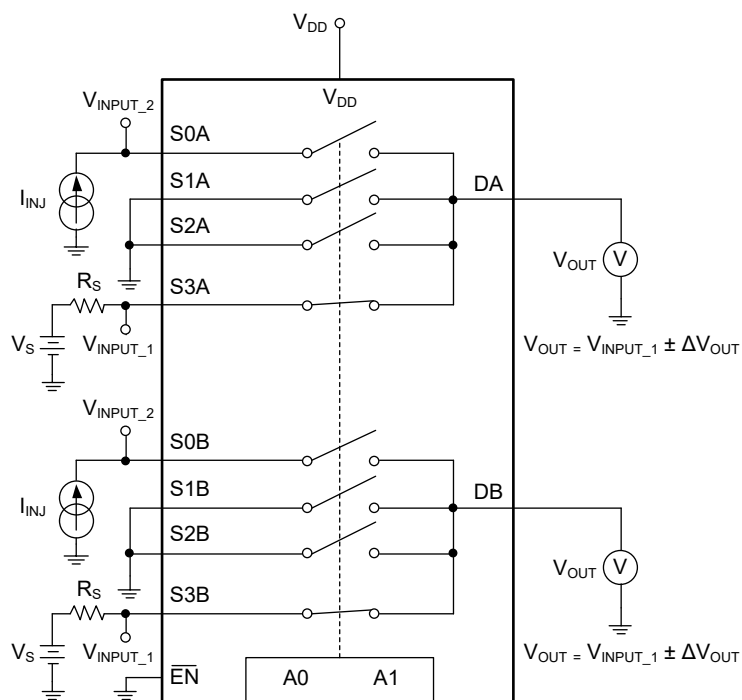


**Test Circuit 9. Switching Times ( $t_{ON}$ ,  $t_{OFF}$ )**

**TEST CIRCUITS (continued)**



**Test Circuit 10. Break-Before-Make Delay Time ( $t_D$ )**



NOTE: Any OFF Input  $V_{INPUT\_2} < GND$  or  $V_{INPUT\_2} > V_{DD}$

**Test Circuit 11. Injection Current**

## APPLICATION INFORMATION

The SGM4523 is a 4:1, 2-channel CMOS analog multiplexer and all signal paths support rail-to-rail operation. All control input pins are also designed with fail-safe function and operate up to 5.5V withstand voltage regardless of the supply voltage. This function can prevent reverse current injection to  $V_{DD}$  pin from control pins even though the voltage of control pins already exceeds the  $V_{DD}$  pin. All signal ports of the SGM4523 have injection current control circuits between the signal input and GND, which can inject current into GND to prevent back feeding into  $V_{DD}$  when the signal input exceeds  $V_{DD}$ .

Based on the above special features, the SGM4523 can be used to simplify circuit design and decrease overall system cost in applications.

### Logic Control

The logic control input pins include  $\overline{EN}$ , A0 and A1. The logic input thresholds of the SGM4523 are related to the power supply. The thresholds will increase as the power supply voltage increases. This feature allows the logic control inputs of the SGM4523 to be connected to processors with lower logic I/O rails and no additional level shifters are required.

### Fail-Safe Function

All control input pins ( $\overline{EN}$ , A0 and A1) of the SGM4523 are designed with fail-safe function and operate up to 5.5V withstand voltage regardless of the supply voltage. This special design eliminates the need for strict timing control for the SGM4523 between the  $V_{DD}$  pin and control input pins. All control pins are allowed to be powered on earlier than the power supply and without damage. The fail-safe function reduces the complexity of system circuit design. For instance, when  $V_{DD} = 0V$ , the fail-safe function allows the control pins of the SGM4523 to be connected to 5.5V. In this case, the switch is disabled because there is no power supply. Another application, when  $V_{DD} = 1.8V$ , the switch is enabled. The feature allows the control pins to be connected to interface with a logic level of another device up to 5.5V and without the need for additional level shifter.

### Enable Control

The SGM4523 has an enable control pin ( $\overline{EN}$ ). When the  $\overline{EN}$  pin is driven to high and power supply is normal, all the signal paths are disabled and the drain pin is open to any source pins. On the contrary, when the  $\overline{EN}$  pin is driven to low, one of the signal paths is closed according to the logic of address pins (A0 and A1).

### Injection Current Control

Injection current is defined as the current flowing into the input pin when the input voltage is higher than power supply ( $V_{DD} + \Delta V$ ) or lower than ground ( $V_{SS}$ ). Typical CMOS switches are designed with ESD diodes between the input pin and the  $V_{DD}/GND$  pin. These diodes will form a leakage path when the input voltage exceeds the power supply or below ground. This leakage may affect the reliability of the power system. Different applications determine that the injection current can come from different sources.

The current injected by switches or transient events is easy to occur in harsh environments of factory automation.

When the input signals are from various sensors or current sources, the injection current can also affect other self-contained systems.

### Injected Current Impact to Typical CMOS Switches

The unexpected injected current may affect the common terminal voltage in application. Typical CMOS switches adopt a parallel structure of NMOS and PMOS and have designed with ESD diodes at the input as shown in Figure 2. These ESD diodes have the function of clamping input voltage. When current is injected into a disabled signal path and the forward diode voltage of the ESD diode ( $V_F$ ) is higher than the PMOS threshold voltage ( $V_T$ ), the PMOS in the circuit will be turned ON from OFF and form a leakage path between source and drain on disabled signal path. This situation causes the drain voltage to be changed by the source voltage in disabled signal path and it is not expected in applications. The simplified architecture of typical CMOS switch and the associated injected current path are shown in Figure 2.



## APPLICATION INFORMATION (continued)

To simplify circuit design and avoid adding additional protection in the system, the SGM4523 is designed with an internal injection current control function. It allows signals on disabled signal channels to exceed the power supply voltage without affecting the enabled signal channel and typical CMOS switches do not have this feature. There is no need to add additional diodes and resistor networks to keep the input signals within the supply voltage in applications. In addition, there is no internal diode path from all pins except GND to the  $V_{DD}$  pin. This design eliminates the risk of damaging components connected to the supply pin or reverse current injection to the power supply. Figure 4 shows a design block diagram of injection current control circuit of the SGM4523.

Each source or drain pin ( $S_x$ ,  $D_x$ ) of the SGM4523 has completely independent injection current control circuit. It includes a control circuit and a FET, which is enabled and shunts unexpected current from the inputs to GND once over-voltage or current injection at the inputs

occurs. The prerequisite for enabling this current control circuit is that the input terminal ( $S_x$ ,  $D_x$ ) is disabled by the control pins and the injected current causes the voltage at the pin to be higher than  $V_{DD}$  or less than GND. Figure 5 shows injected current at input pin when over-voltage or current injection at the inputs occurs.

Each injection current circuit can handle a maximum rated current of 50mA and the SGM4523 can accept a maximum injection current of 100mA at any time. Assuming multiple source terminals are injected at the same time, the SGM4523 can only accept a total current of 100mA. If the current injected exceeds 100mA, the SGM4523 is at risk of damage. So a series current limiting resistor may be required and must be sized appropriately based on the system application. Figure 6 shows an application circuit of using a series current limiting resistors when over-voltage event occurs.

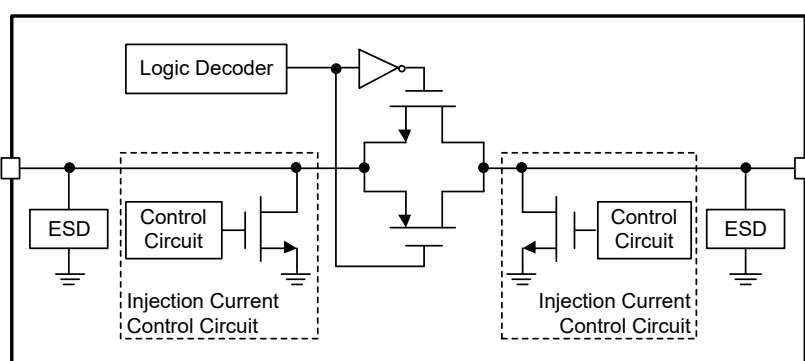


Figure 4. Design Block Diagram of Injection Current Control

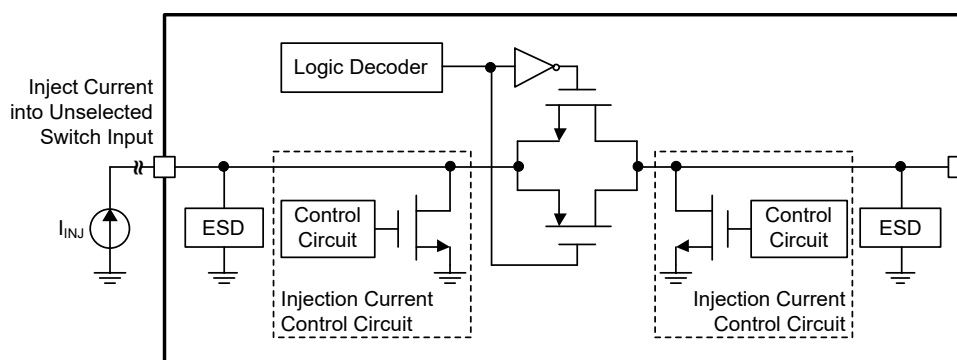


Figure 5. Injected Current at Input Pin

APPLICATION INFORMATION (continued)

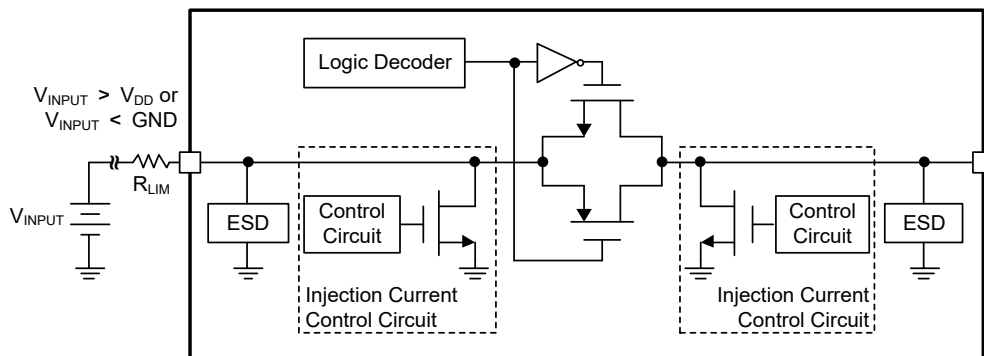


Figure 6. Over-Voltage Event with Series Resistor

Once the voltage at the source or drain pins exceeds  $V_{DD}$  or falls below GND, the FET is enabled for any disabled signal path and shunts unexpected current from the inputs to GND. In this scene, a series of resistors is required to limit the total current injected into the input to within 100mA. An example is as follow:

**SGM4523 is Powered and the Input Signal is Higher than  $V_{DD}$  ( $V_{DD} = 5V$ ,  $V_{INPUT} = 5.5V$ )**

For the typical CMOS switch with an internal ESD diode, when the input signal exceeds the  $V_{DD}$  pin, the internal ESD diode will be forward biased and the current injected into the power supply from the input. In this case, if the inputs have no additional protective devices, the power supply system may be at risk of damage. Even though the use of limiting resistors can reduce the risk to a certain extent, this risk cannot be completely eliminated due to the architecture of the typical CMOS switch. When the input voltage is too high and exceeds  $V_{DD}$ , the application circuit still requires a series of limiting resistors, because the injected current control circuit of the SGM4523 can only handle injection current less than 100mA. The current path of the SGM4523 is from inputs to GND and does not have the same problems as the current injected into the power rail.

In addition, the injection current control circuit of the SGM4523 can work well in both unselected and selected paths. It should be noted when the injection current occurs in the selected path, the injection current will also flow through the source to drain path not just flow into ground.

**Power Supply and Decoupling**

Power supply range of the  $V_{DD}$  pin is from 1.62V to 5.5V. Besides, the  $V_{DD}$  pin is not allowed to exceed the maximum absolute withstand voltage because over-voltage will cause damage to the SGM4523.

In general, the  $V_{DD}$  pin should be installed with a 0.1 $\mu$ F to 10 $\mu$ F ceramic capacitor to prevent power disturbance from other power supply components and the bypass capacitor should be placed as close as possible to the  $V_{DD}$  pin for the best power supply decoupling. Multiple capacitors with different capacitance values can also be placed to reject noise of different frequencies in applications with high requirements for noise. One end of this decoupling capacitor should be directly connected to the GND pin of the SGM4523 as short as possible in PCB layout design.

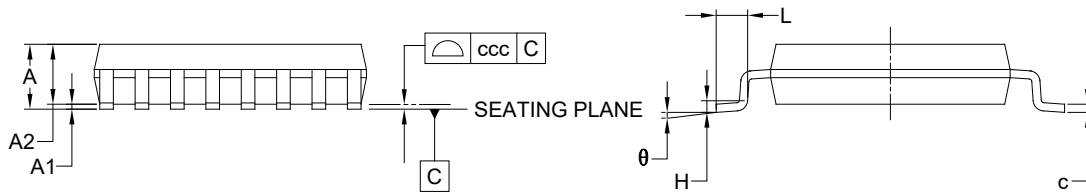
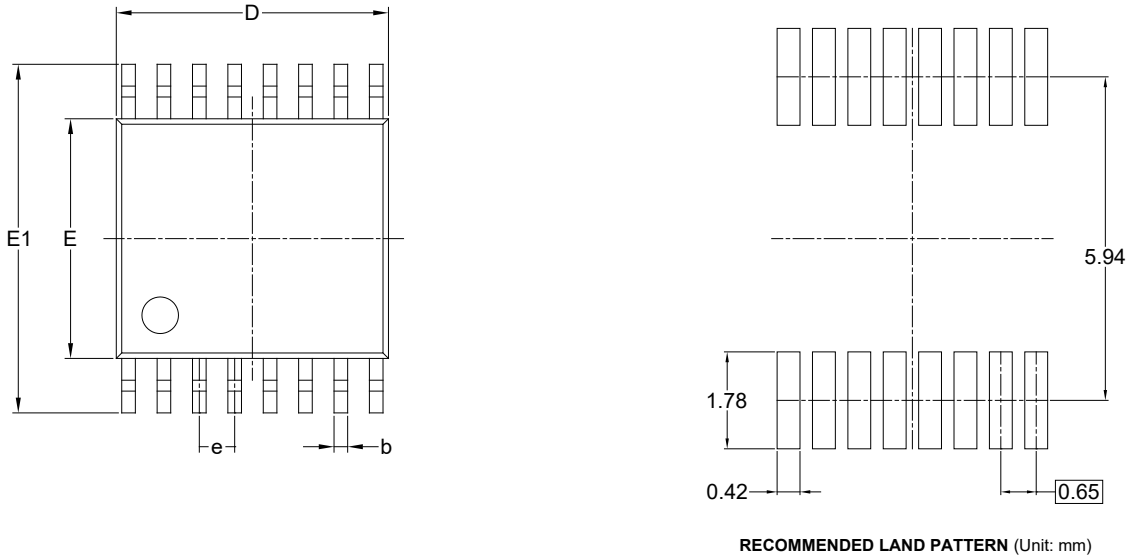
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (MAY 2026)	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



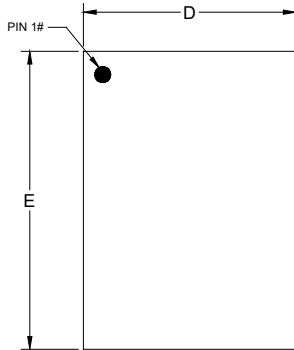
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:

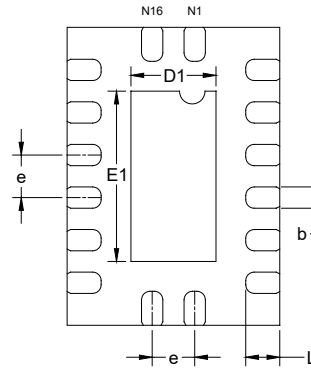
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

TQFN-2.5×3.5-16L



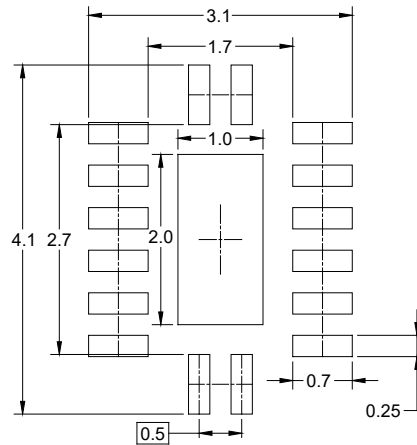
TOP VIEW



BOTTOM VIEW



SIDE VIEW



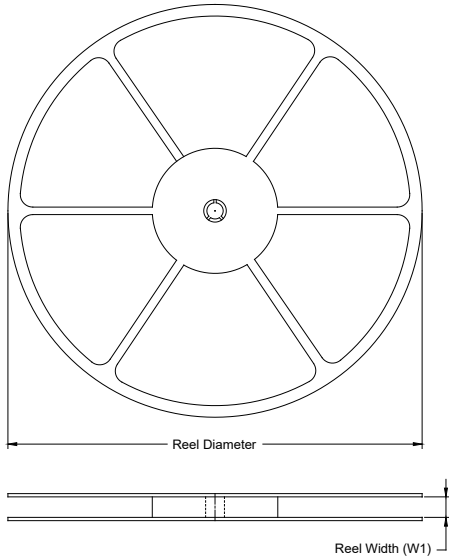
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203 REF		
b	0.20	0.25	0.30
D	2.40	2.50	2.60
D1	0.85	1.00	1.15
E	3.40	3.50	3.60
E1	1.85	2.00	2.15
e	0.45	0.50	0.55
L	0.30	0.40	0.50

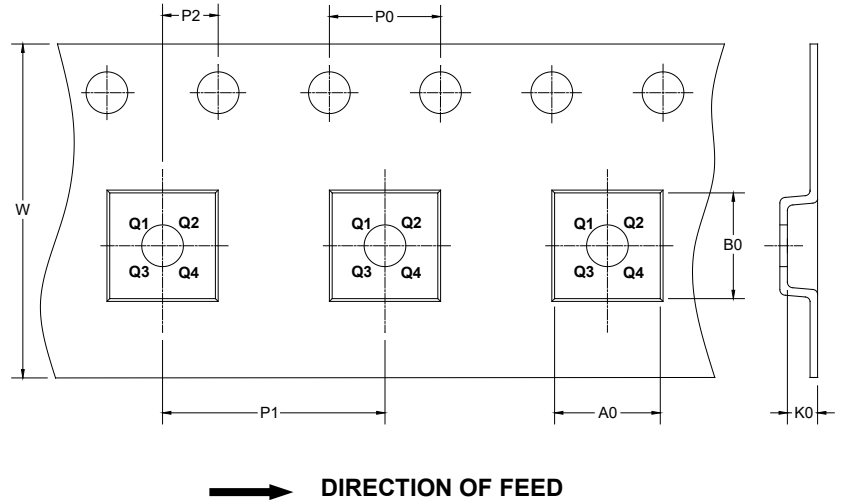
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

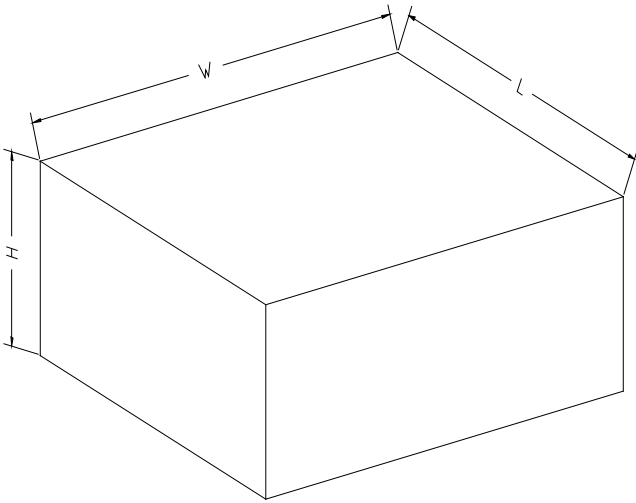
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-2.5×3.5-16L	13"	12.4	2.80	3.80	1.13	4.0	4.0	2.0	12.0	Q1

DD0001

# PACKAGE INFORMATION

## CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002