74AHC573
Octal Transparent D-Type Latch with 3-State Outputs

GENERAL DESCRIPTION

The 74AHC573 device is an octal transparent D-type latch with 3-state outputs. The supply voltage can accept any voltage from 2.0V to 5.5V.

The output enable $\overline{OE}$ input is active low. In this case, when latch enable LE input is taken high, the Q outputs follow the data D inputs. When LE input is taken low, the Q outputs are latched to retain the set-up data. When $\overline{OE}$ is high, all outputs are in high-impedance state.

The output enable $\overline{OE}$ input can make all outputs in high/low logic levels or high-impedance state, which has no influence on the inner working of the latches. When the outputs are in a high-impedance state, the latch can retain old data or enter new data.

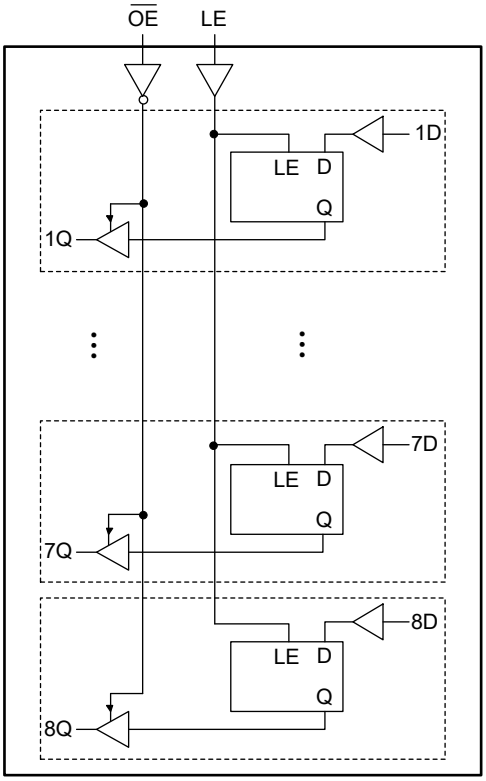
FEATURES

- **Wide Supply Voltage Range: 2.0V to 5.5V**
- **Input Accept Voltage Higher than the Supply Voltage**
- **+8mA/-8mA Output Current**
- **3-State Outputs Drive Bus Lines Directly**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-20 and TSSOP-20 Packages**

APPLICATIONS

Computing: Server, PC and Notebook
Network Switch
Telecom Infrastructure

LOGIC DIAGRAM



FUNCTION TABLE

INPUT			OUTPUT
$\overline{OE}$	LE	nD	nQ
L	H	H	H
L	H	L	L
L	L	*X*	Q_0
H	*X*	*X*	Z

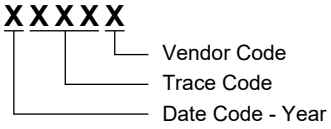
H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance State
X = Don't Care

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC573	SOIC-20	-40℃ to +125℃	74AHC573XS20G/TR	74AHC573XS20 XXXXX	Tape and Reel, 1500
	TSSOP-20	-40℃ to +125℃	74AHC573XTS20G/TR	08PXTS20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 7.0V
Input Voltage, V_I (2) ..... -0.5V to 7.0V
Output Voltage, V_O (2) ..... -0.5V to MIN (7.0V, V_{CC} + 0.5V)
Input Clamping Current, I_{IK} (V_I < 0V) ..... -20mA
Output Clamping Current, I_{OK} (V_O < 0V or V_O > V_{CC}) ... ±20mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}) ..... ±25mA
Continuous Current (V_{CC} or GND) ..... ±75mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 2.0V to 5.5V
Input Voltage, V_I ..... 0V to 5.5V
Output Voltage, V_O ..... 0V to V_{CC}
Output Current, I_O ..... ±8mA
Input Transition Rise or Fall Rate, Δt/ΔV ..... 100ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

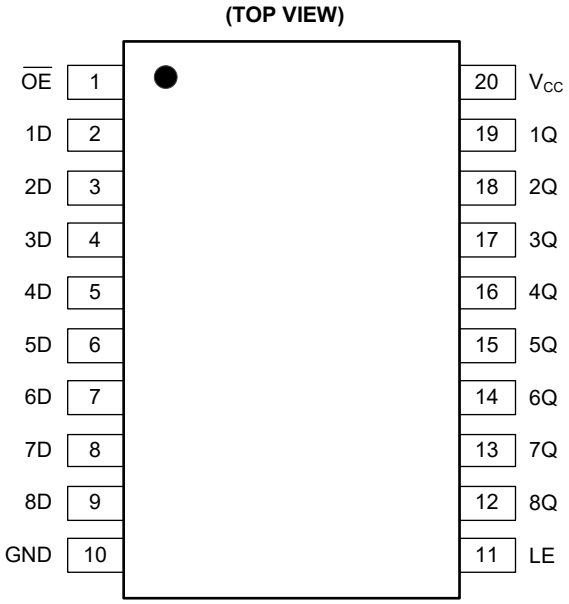
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable Input (Active Low).
2, 3, 4, 5, 6, 7, 8, 9	1D, 2D, 3D, 4D, 5D, 6D, 7D, 8D	Data Inputs.
19, 18, 17, 16, 15, 14, 13, 12	1Q, 2Q, 3Q, 4Q, 5Q, 6Q, 7Q, 8Q	Data Outputs.
11	LE	Latch Enable Input (Active High).
10	GND	Ground.
20	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		Full	1.50			V
		V_{CC} = 3.0V		Full	2.10			
		V_{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V		Full			0.50	V
		V_{CC} = 3.0V		Full			0.90	
		V_{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V_{OH}	$V_I = V_{IH}$	V_{CC} = 2.0V, I_{OH} = -50μA	Full	1.95	1.995		V
			V_{CC} = 3.0V, I_{OH} = -50μA	Full	2.95	2.995		
			V_{CC} = 4.5V, I_{OH} = -50μA	Full	4.45	4.495		
			V_{CC} = 3.0V, I_{OH} = -4mA	Full	2.60	2.820		
			V_{CC} = 4.5V, I_{OH} = -8mA	Full	4.00	4.240		
Low-Level Output Voltage	V_{OL}	$V_I = V_{IL}$	V_{CC} = 2.0V, I_{OL} = 50μA	Full		0.005	0.05	V
			V_{CC} = 3.0V, I_{OL} = 50μA	Full		0.005	0.05	
			V_{CC} = 4.5V, I_{OL} = 50μA	Full		0.005	0.05	
			V_{CC} = 3.0V, I_{OL} = 4mA	Full		0.160	0.44	
			V_{CC} = 4.5V, I_{OL} = 8mA	Full		0.260	0.44	
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND		Full		±0.1	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, $V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		Full		±0.1	±2	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, $V_I = V_{CC}$ or GND, I_O = 0A		Full		0.1	10	μA
Input Capacitance	C_I	V_{CC} = 5.0V, $V_I = V_{CC}$ or GND		+25℃		5		pF
Output Capacitance	C_O	V_{CC} = 5.0V, $V_O = V_{CC}$ or GND		+25℃		6		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	nD to nQ, C_L = 15pF	V_{CC} = 3.3V ± 0.3V	Full	1	6	14	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4	8.5	
		nD to nQ, C_L = 50pF	V_{CC} = 3.3V ± 0.3V	Full	1	6.5	18	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4.5	11	
		LE to nQ, C_L = 15pF	V_{CC} = 3.3V ± 0.3V	Full	1	6.5	15	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4.5	10	
		LE to nQ, C_L = 50pF	V_{CC} = 3.3V ± 0.3V	Full	1	7.5	19	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	5	12	
Enable Time (2)	t_{EN}	$\overline{OE}$ to nQ, C_L = 15pF	V_{CC} = 3.3V ± 0.3V	Full	1	6.5	14.5	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4	10	
		$\overline{OE}$ to nQ, C_L = 50pF	V_{CC} = 3.3V ± 0.3V	Full	1	7	18	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4.5	12	
Disable Time (2)	t_{DIS}	$\overline{OE}$ to nQ, C_L = 15pF	V_{CC} = 3.3V ± 0.3V	Full	1	7.5	14	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	3.5	10	
		$\overline{OE}$ to nQ, C_L = 50pF	V_{CC} = 3.3V ± 0.3V	Full	1	9.5	17.5	ns
			V_{CC} = 5.0V ± 0.5V	Full	1	4.5	12	
Pulse Duration	t_W	LE high	V_{CC} = 3.3V ± 0.3V	Full	5.5			ns
			V_{CC} = 5.0V ± 0.5V	Full	5.5			
Set-Up Time	t_{SU}	Data before LE ↓	V_{CC} = 3.3V ± 0.3V	Full	3.5			ns
			V_{CC} = 5.0V ± 0.5V	Full	3.5			
Hold Time	t_H	Data after LE ↓	V_{CC} = 3.3V ± 0.3V	Full	1.5			ns
			V_{CC} = 5.0V ± 0.5V	Full	1.5			
Channel-to-Channel Skew	t_{SKO}	V_{CC} = 3.3V ± 0.3V, C_L = 50pF		+25℃			1.5	ns
		V_{CC} = 5.0V ± 0.5V, C_L = 50pF		+25℃			1	
Power Dissipation Capacitance (3)	C_{PD}	No Load, f = 1MHz, V_{CC} = 5.0V		+25℃		7		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}. t_{EN} is the same as t_{PZL} and t_{PZH}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

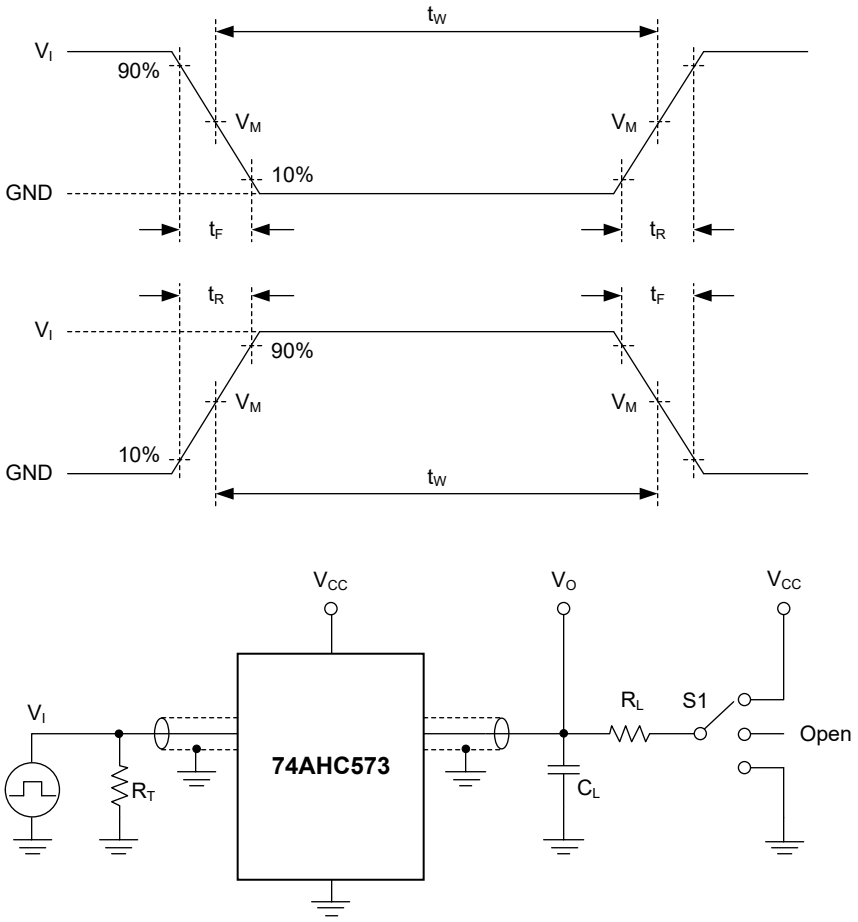
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

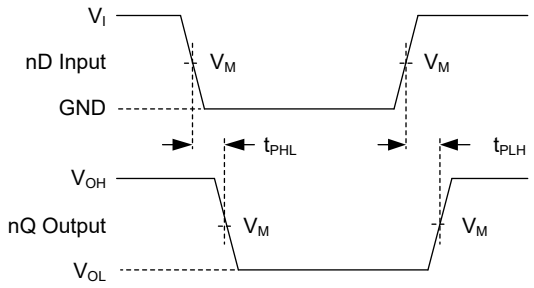
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

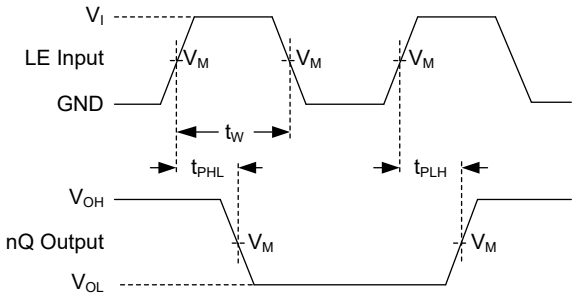
SUPPLY VOLTAGE	INPUT		LOAD		S1		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.0V to 5.5V	GND to V_{CC}	≤ 3.0ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS



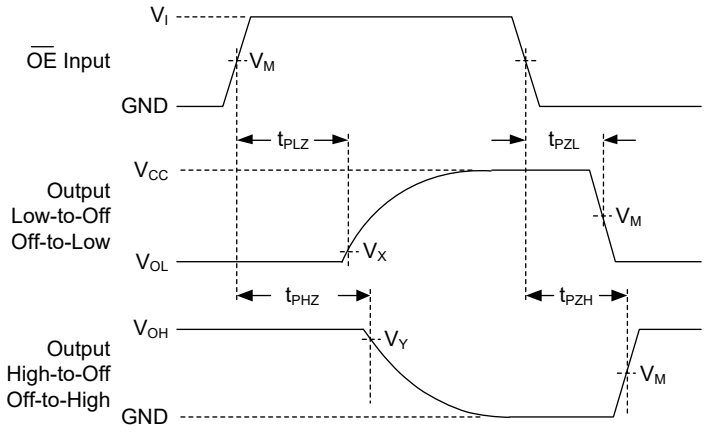
Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nD) to Output (nQ) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

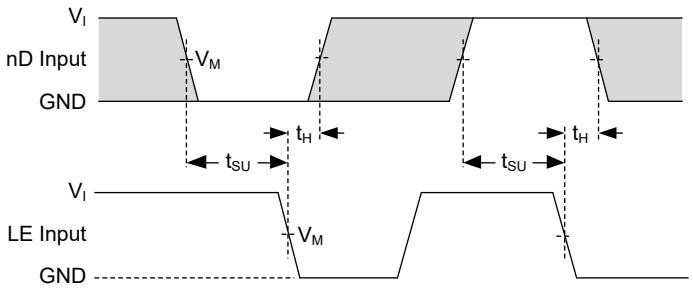
Figure 3. Latch Enable Input (LE) to Output (nQ) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and Disable Times

WAVEFORMS (continued)



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.
The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 5. Set-Up and Hold Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
2.0V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

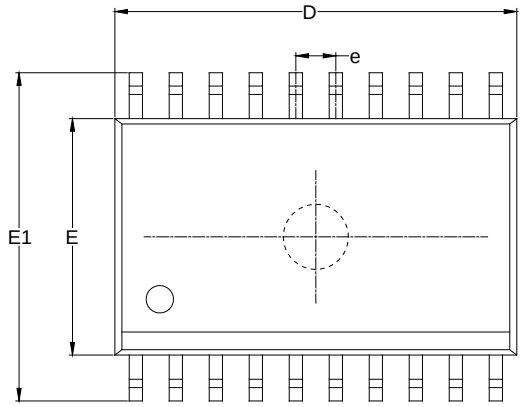
REVISION HISTORY

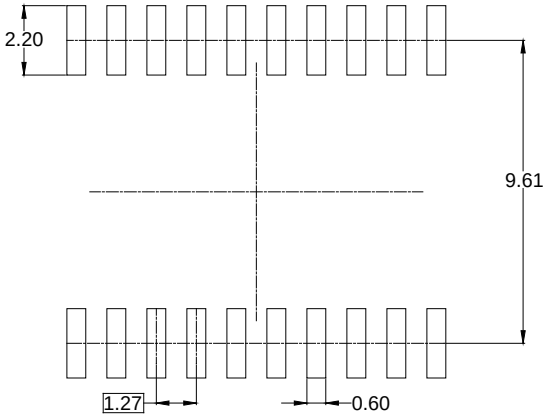
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data	All

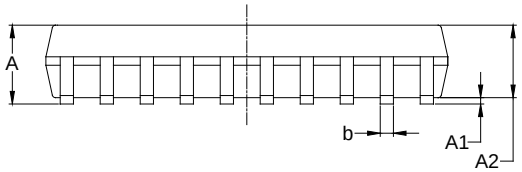
PACKAGE OUTLINE DIMENSIONS

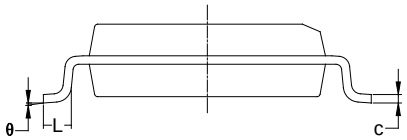
SOIC-20





RECOMMENDED LAND PATTERN (Unit: mm)



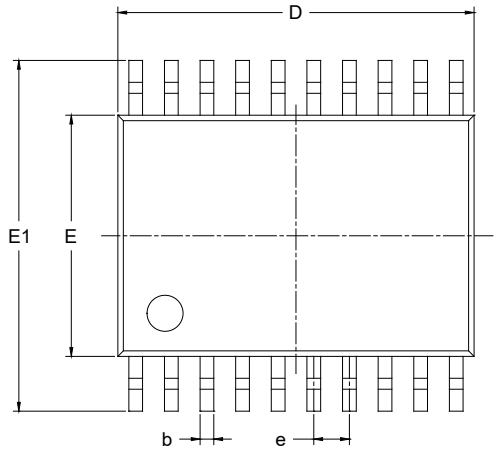


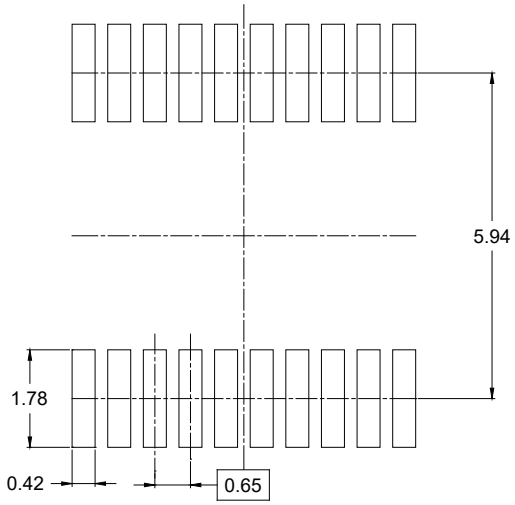
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

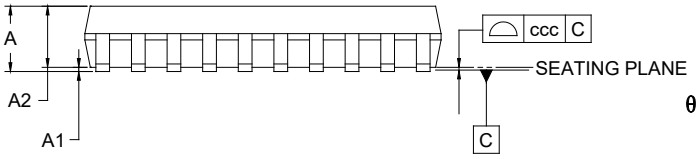
PACKAGE OUTLINE DIMENSIONS

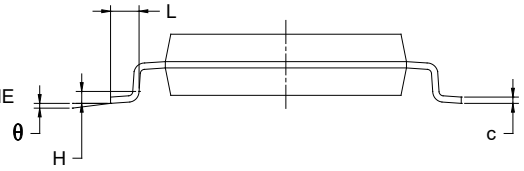
TSSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)



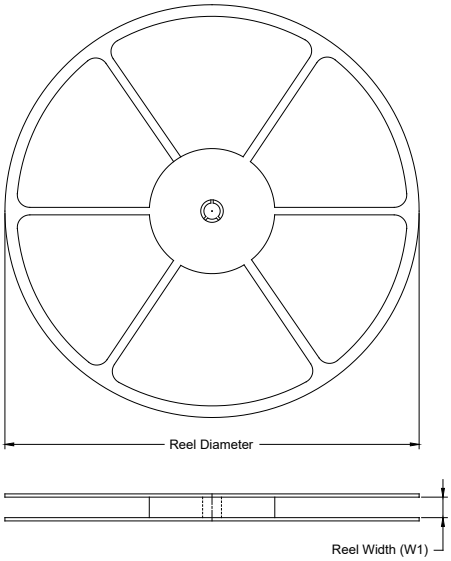


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

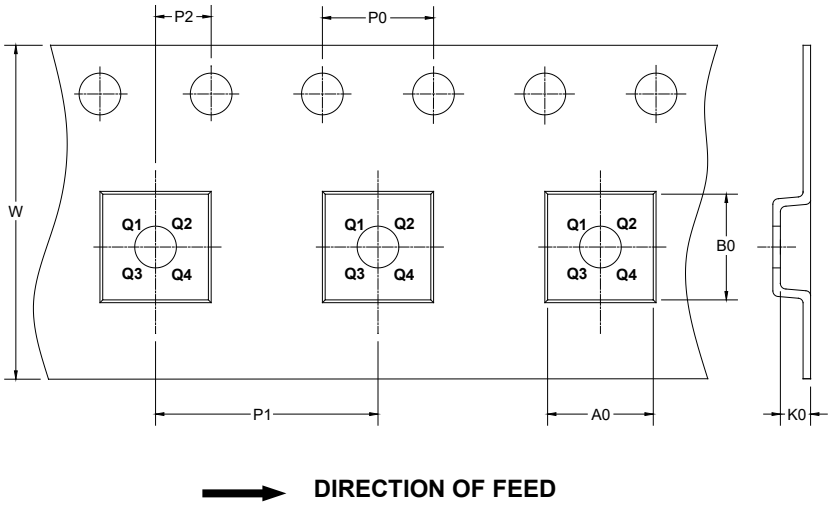
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



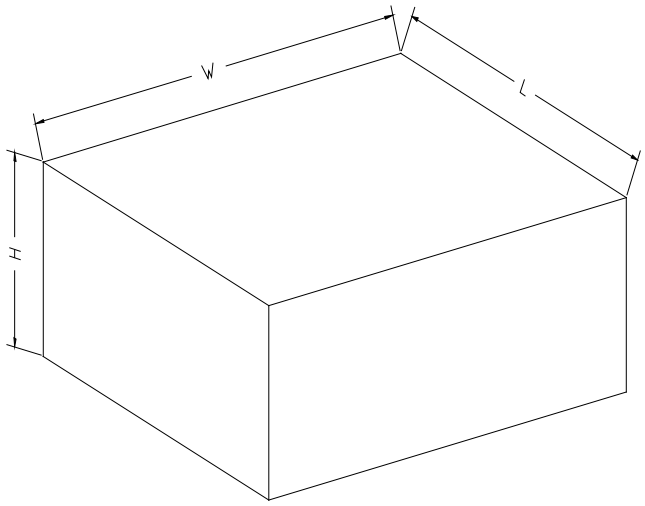
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-20	13″	24.4	10.90	13.30	3.00	4.0	12.0	2.0	24.0	Q1
TSSOP-20	13″	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002