SGM842

3-Channel, High-Side or Low-Side Measurement, Shunt and Bus Voltage Monitor with I²C- and SMBus-Compatible Interface

GENERAL DESCRIPTION

The SGM842 is a high accuracy, three-channel, power monitor with an I²C- and SMBus-compatible interface which can sense high-side or low-side current and bus voltage. It supports a wide common-mode voltage range from 0V to 30V. For more flexibly, the ADC conversion times and sample averaging modes are allowed to be programmed according to the requirements. Additionally, both critical and warning alerts are reported for each channel.

The SGM842 operates over an input voltage range of 2.7V to 5.5V and draws 1000μA (TYP) of supply current. It supports four programmable addresses.

The SGM842 is available in a Green TQFN-4×4-16L package and specified over a junction temperature range of -40℃ to +125℃.

FEATURES

- **2.7V to 5.5V Supply Voltage Range**
- **0V to 30V Senses Bus Voltages**
- **Report Shunt and Bus Voltage**
- **Low Gain Error: 0.25% (MAX)**
- **Low Input Offset Voltage: 80μV (MAX)**
- **Programmable Averaging and Conversion Times**
- **Programmable Alert and Warning Outputs**
- **4 Programmable Addresses**
- **Available in a Green TQFN-4×4-16L Package**

APPLICATIONS

Communication Equipment
Computers
Battery Chargers
Power Management
Test Equipment
Power Supplies

TYPICAL APPLICATION

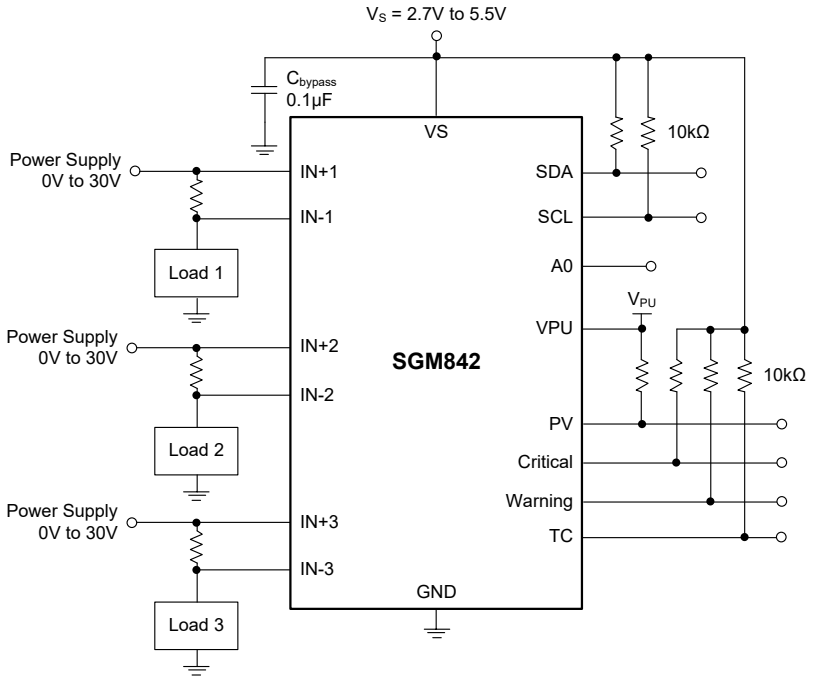


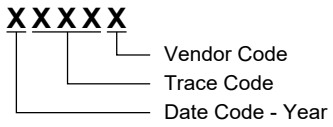
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM842	TQFN-4×4-16L	-40℃ to +125℃	SGM842XTQE16G/TR	SGM842 XTQE16 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Operating Supply Voltage, V_S 6V
Analog Inputs
Differential V_{IN+} - V_{IN-} ..... -30V to 30V
Common-Mode (V_{IN+} + V_{IN-})/2 ..... -0.3V to 30V
VPU 30V
Digital Outputs
Critical, Warning, Timing Control 6V
Power Valid 30V
Serial Bus
Data Line, SDA ..... GND - 0.3V to 6V
Clock Line, SCL ..... GND - 0.3V to V_S + 0.3V
Input Current into Any Pin 5mA
Open-Drain, Digital Output Current 10mA
Package Thermal Resistance
TQFN-4×4-16L, θ_{JA} ..... 37.3℃/W
TQFN-4×4-16L, θ_{JB} ..... 14.4℃/W
TQFN-4×4-16L, θ_{JC} ..... 30.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Supply Voltage, V_S ..... 2.7V to 5.5V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

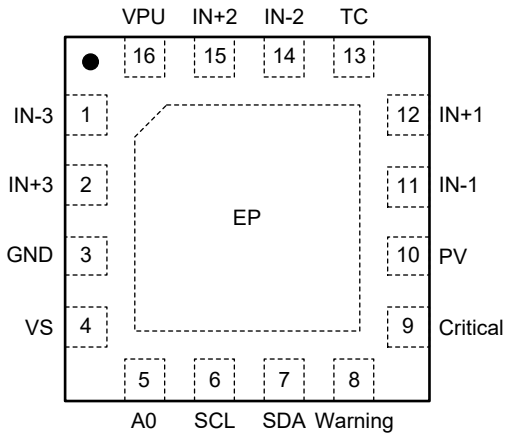
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-16L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IN-3	AI	Bus Voltage Input and Negative Shunt Voltage Input Pin of Channel 3. For high-side applications, connect it to the load side of the channel 3 sense resistor.
2	IN+3	AI	Positive Input of the Channel 3. For high-side applications, connect it to the supply side of the channel 3 sense resistor.
3	GND	A	Ground.
4	VS	A	Power Supply Pin.
5	A0	DI	Address Pin. Four options: GND, SCL, SDA, or VS with corresponding addresses.
6	SCL	DI	Open-Drain Clock Input Pin.
7	SDA	DI/DO	Open-Drain Data Input/Output Pin.
8	Warning	DO	The Warning Alert pin of Averaged Measurement. Open-drain output.
9	Critical	DO	The Critical Alert of Conversion-triggered. Open-drain output.
10	PV	DO	The Alert Pin of Power Valid. Open-drain output.
11	IN-1	AI	Bus Voltage Input and Negative Shunt Voltage Input Pin of Channel 1. For high-side applications, connect it to the load side of the channel 1 sense resistor.
12	IN+1	AI	Positive Input of the Channel 1. For high-side applications, connect it to the supply side of the channel 1 sense resistor.
13	TC	DO	The Alert Pin of Timing Control. Open-drain output.
14	IN-2	AI	Bus Voltage Input and Negative Shunt Voltage Input Pin of Channel 2. For high-side applications, connect it to the load side of the channel 2 sense resistor.
15	IN+2	AI	Positive Input of the Channel 2. For high-side applications, connect it to the supply side of the channel 2 sense resistor.
16	VPU	AI	Pull-up Power Supply. Apply for bias power valid output circuits.
Exposed Pad	EP	—	Exposed Pad.

NOTE: A: Analog, AI: analog input, DI: digital input, DO: digital output, DI/DO: digital input/digital output.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_S = 3.3V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} - V_{IN-}) = 0mV and V_{BUS} = V_{IN-} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input						
Shunt Voltage Input Range	V_{SHUNT}		-163.84		163.80	mV
Bus Voltage Input Range	V_{BUS}		0		30	V
Common-Mode Rejection	CMRR	V_{IN+} = 0V to 30V	102	124		dB
Shunt Offset Voltage, RTI (1)	V_{OS}			±40	±80	μV
		vs. temperature, T_A = -40℃ to +125℃		0.3	1	μV/℃
	PSRR	vs. power supply, V_S = 2.7V to 5.5V, V_{IN+} = 1V		15		μV/V
Bus Offset Voltage, RTI (1)	V_{OS}			±8	±30	mV
		vs. temperature, T_A = -40℃ to +125℃		200	400	μV/℃
	PSRR	vs. power supply, V_S = 2.7V to 5.5V, V_{IN+} = 1V		3		mV/V
Input Bias Current at IN+	I_{B+}			0.05		μA
Input Bias Current at IN-	I_{B-}			0.05||950		μA||kΩ
Input Leakage (3)		(IN+ pin) + (IN- pin), power-down mode		0.05	0.2	μA
DC Accuracy						
ADC Native Resolution				13		Bits
1 LSB Step Size		Shunt voltage		40		μV
		Bus voltage		8		mV
Shunt Voltage Gain Error				±0.02	±0.25	%
		vs. temperature, T_A = -40℃ to +125℃		10	50	ppm/℃
Bus Voltage Gain Error				±0.025	±0.28	%
		vs. temperature, T_A = -40℃ to +125℃		10	50	ppm/℃
Differential Nonlinearity				±0.7		LSB
ADC Conversion Time	t_{CT}	CT bit = 000		340	374	μs
		CT bit = 001		340	374	
		CT bit = 010		340	374	
		CT bit = 011		600	655	
		CT bit = 100		1.15	1.30	ms
		CT bit = 101		2.15	2.40	
		CT bit = 110		4.25	4.70	
		CT bit = 111		8.35	9.10	
SMBus						
SMBus Timeout (3)				28	35	ms
Digital Input/Output						
Input Capacitance	C_{IN}			4		pF
Leakage Input Current		V_{IN} = 0V to V_S		0.05	0.5	μA
High-Level Input Voltage	V_{IH}		0.7 × V_S		6	V
Low-Level Input Voltage	V_{IL}		0		0.3 × V_S	V
Low-Level Output Voltage	V_{OL}	SDA, critical, warning, PV, V_S > 2.7V, I_{OL} = 3mA		0.2	0.4	V
		TC, V_S > 2.7V, I_{OL} = 1.2mA		0.2	0.4	
		PV, V_S > 2.7V, I_{OL} = 3mA		0.3	0.5	
Hysteresis Voltage				500		mV

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_S = 3.3V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} - V_{IN-}) = 0mV and V_{BUS} = V_{IN-} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Quiescent Current	I_Q			1000	1400	μA
		Power-down (Shutdown) mode		2	2.4	
Power-On Reset Threshold	V_{POR}			2.2		V

NOTES:

1. RTI = Referred-to-input.
2. The leakage current that defined as the current flowing into the pin in this table is positive. And in the other input conditions, the negative leakage current may occur.
3. Once SCL keeps low for more than 28ms, the SMBus timeout of SGM842 will reset.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
SCL Operating Frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus Free Time between STOP and START Condition	t_{BUF}	1300		160		ns
Hold Time after Repeated START Condition (After this period, the first clock is generated.)	t_{HDSTA}	600		160		ns
Repeated START Condition Setup Time	t_{SUSTA}	600		160		ns
STOP Condition Setup Time	t_{SUSTO}	600		160		ns
Data Hold Time	t_{HDDAT}	0		0		ns
Data Valid Time	t_{VDDAT}		900		70	ns
Data Setup Time	t_{SUDAT}	100		10		ns
SCL Clock Low Period	t_{LOW}	1300		160		ns
SCL Clock High Period	t_{HIGH}	600		60		ns
Data Fall Time	t_{FDA}		500		80	ns
Clock Fall Time	t_{FCL}		300		40	ns
Clock Rise Time	t_R		300		40	ns
Clock/Data Rise Time for SCLK ≤ 100kHz	t_R		1000			ns

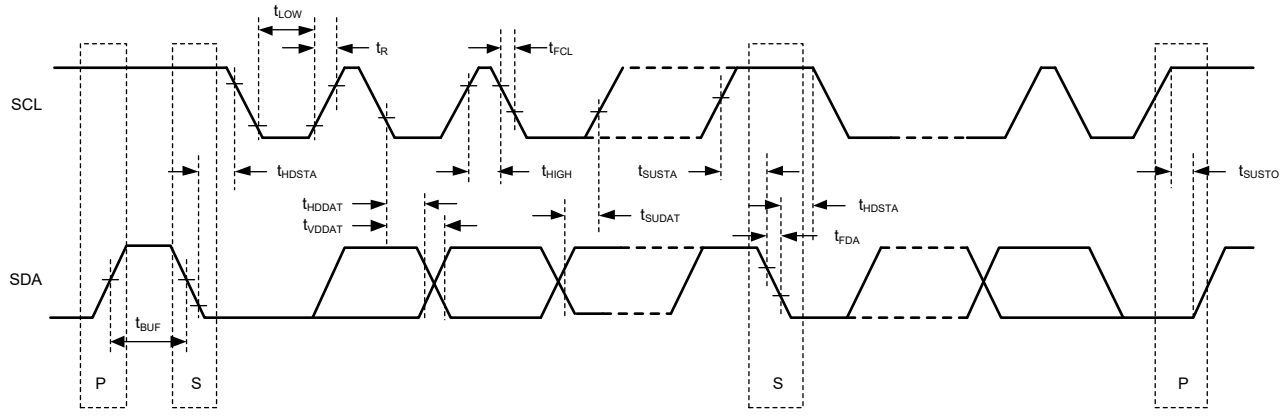
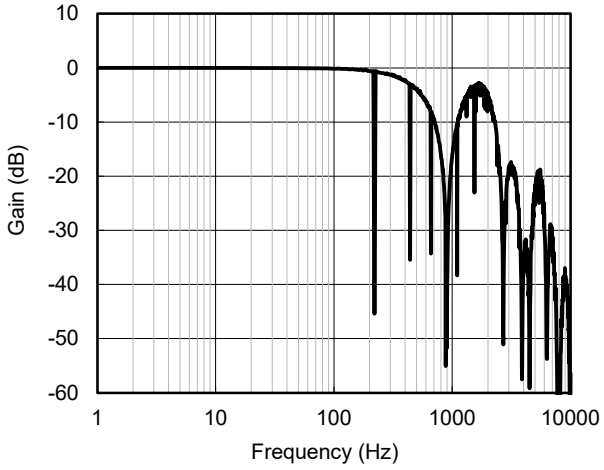


Figure 2. Bus Timing Diagram

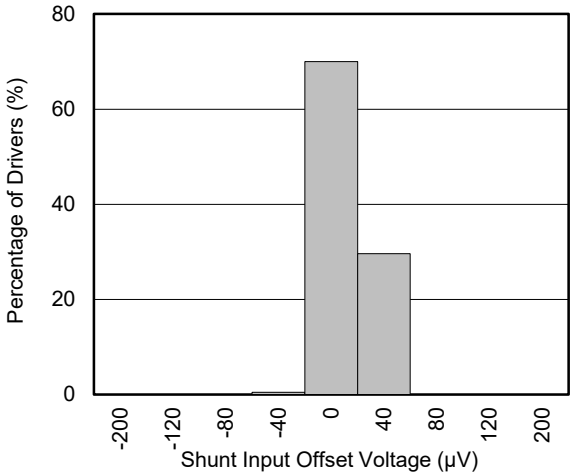
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_S = 3.3V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} - V_{IN-}) = 0mV and V_{BUS} = V_{IN-} = 12V, unless otherwise noted.

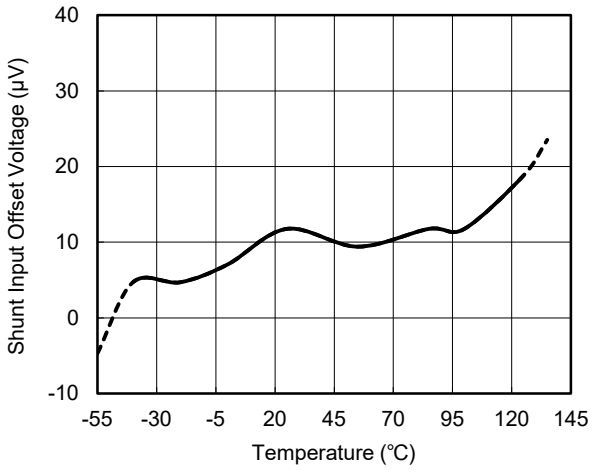
Shunt Frequency Response (3-Channel Shunt + Bus On)



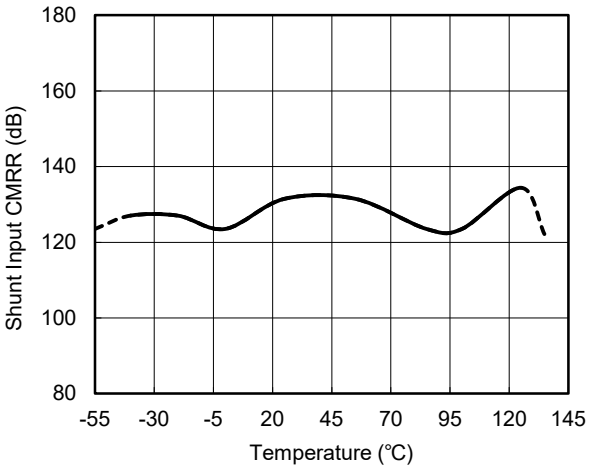
Shunt Input Offset Voltage Production Distribution



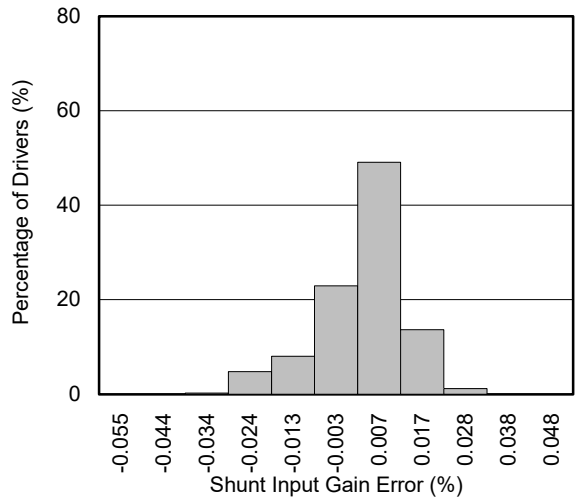
Shunt Input Offset Voltage vs. Temperature



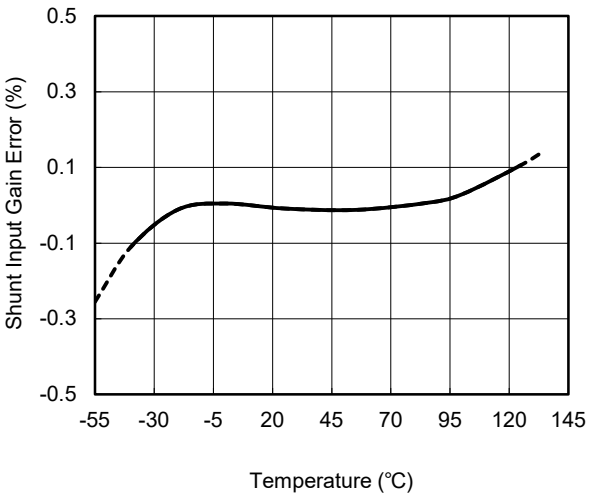
Shunt Input Common-Mode Rejection Ratio vs. Temperature



Shunt Input Gain Error Production Distribution



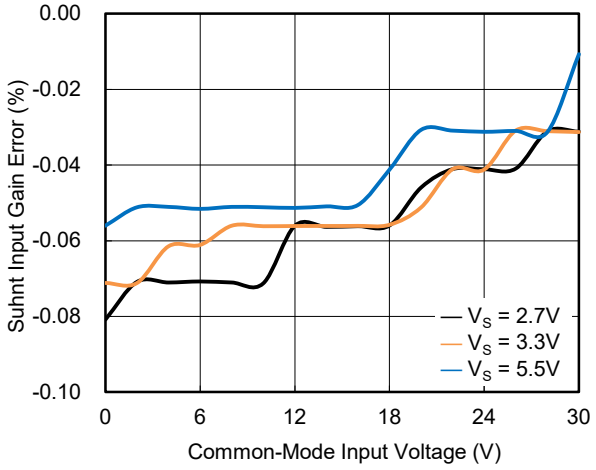
Shunt Input Gain Error vs. Temperature



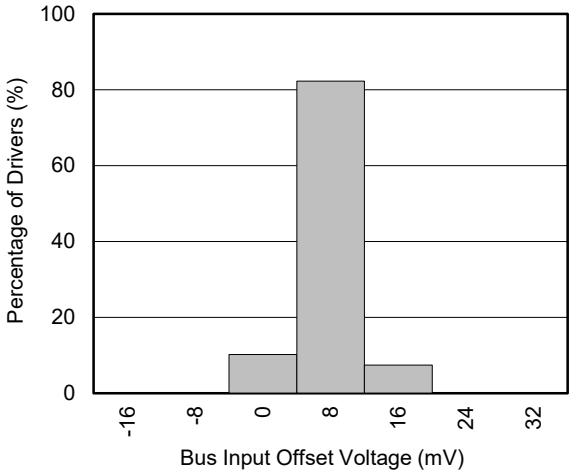
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} - V_{IN-}) = 0mV and V_{BUS} = V_{IN-} = 12V, unless otherwise noted.

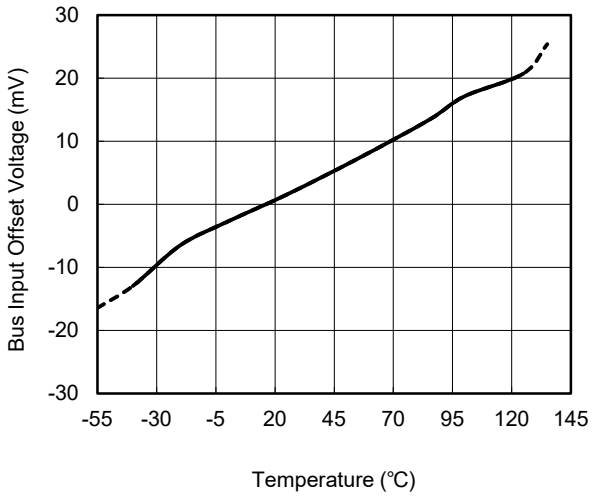
Shunt Input Gain Error vs. Common-Mode Input Voltage



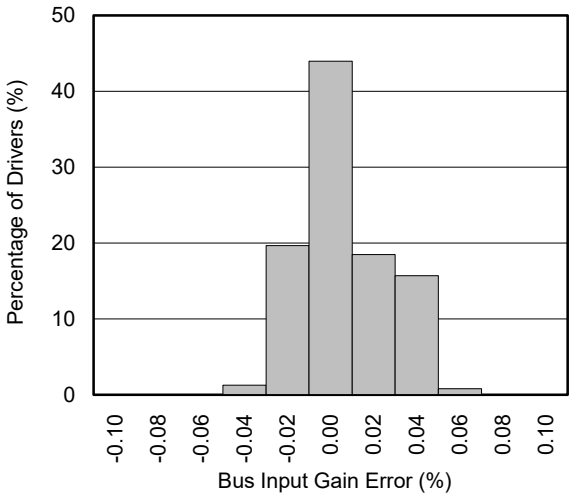
Bus Input Offset Voltage Production Distribution



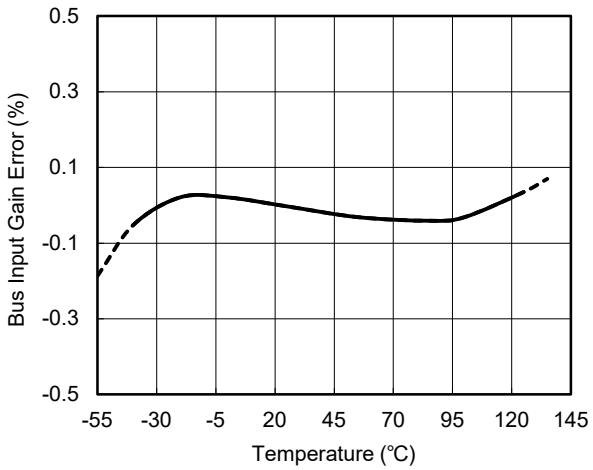
Bus Input Offset Voltage vs. Temperature



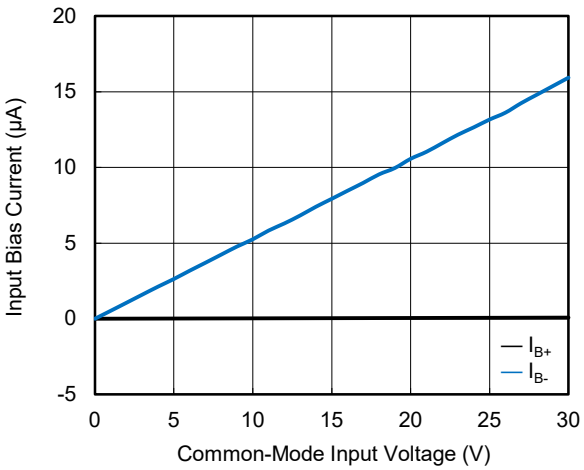
Bus Input Gain Error Production Distribution



Bus Input Gain Error vs. Temperature



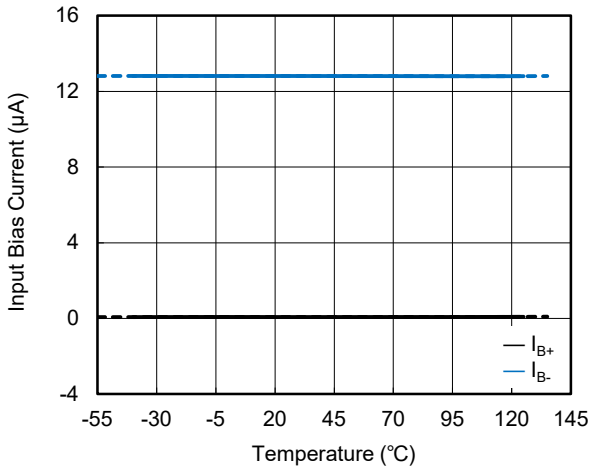
Input Bias Current vs. Common-Mode Voltage



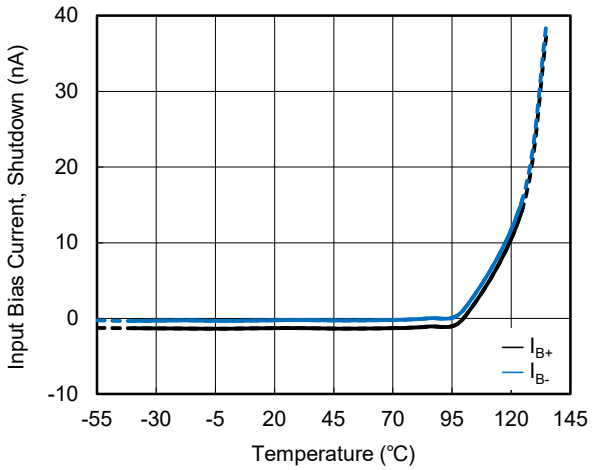
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_S = 3.3V, V_{IN+} = 12V, V_{SHUNT} = (V_{IN+} - V_{IN-}) = 0mV and V_{BUS} = V_{IN-} = 12V, unless otherwise noted.

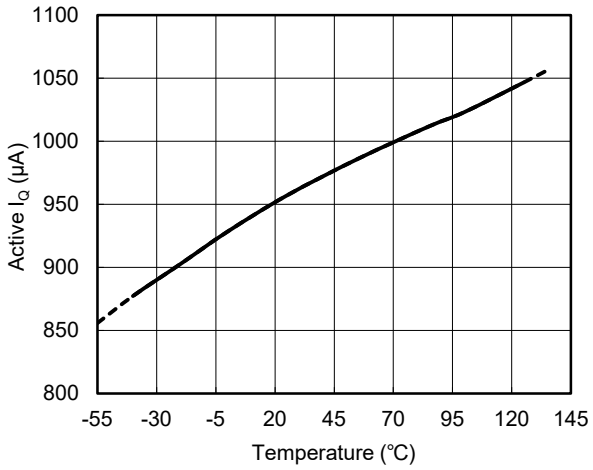
Input Bias Current vs. Temperature



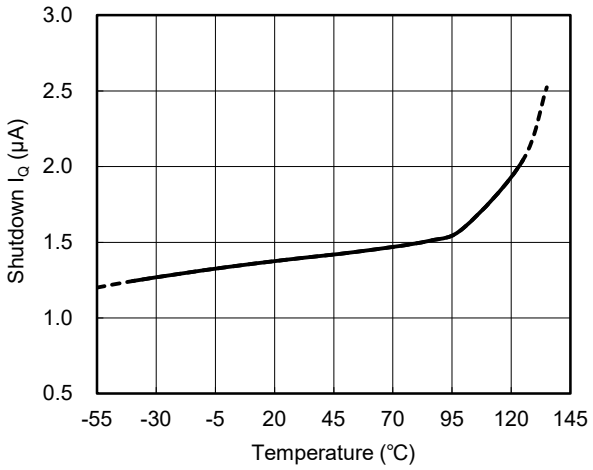
Input Bias Current vs. Temperature, Shutdown



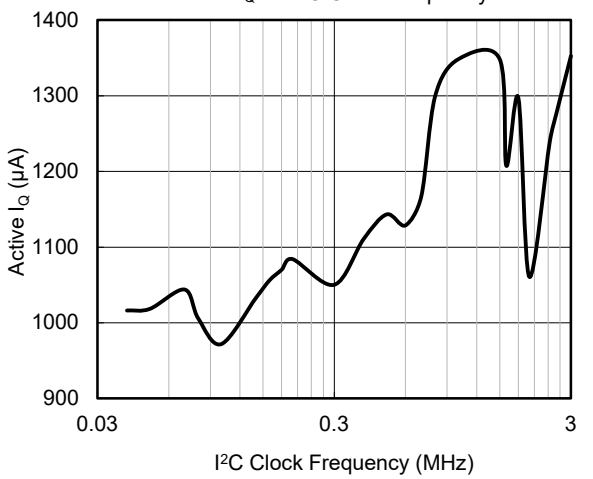
Active I_Q vs. Temperature



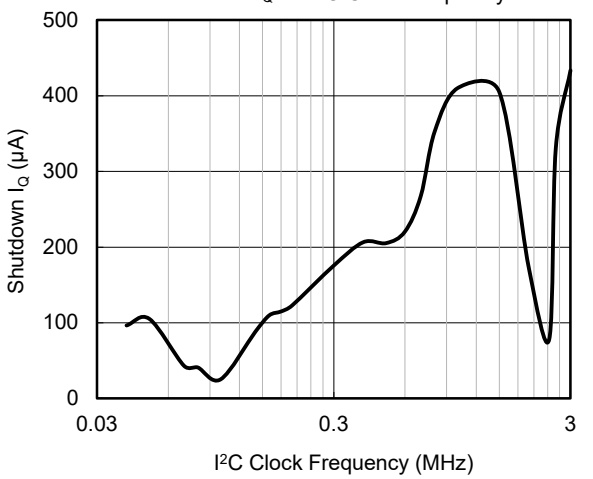
Shutdown I_Q vs. Temperature



Active I_Q vs. I^2C Clock Frequency



Shutdown I_Q vs. I^2C Clock Frequency



FUNCTIONAL BLOCK DIAGRAM

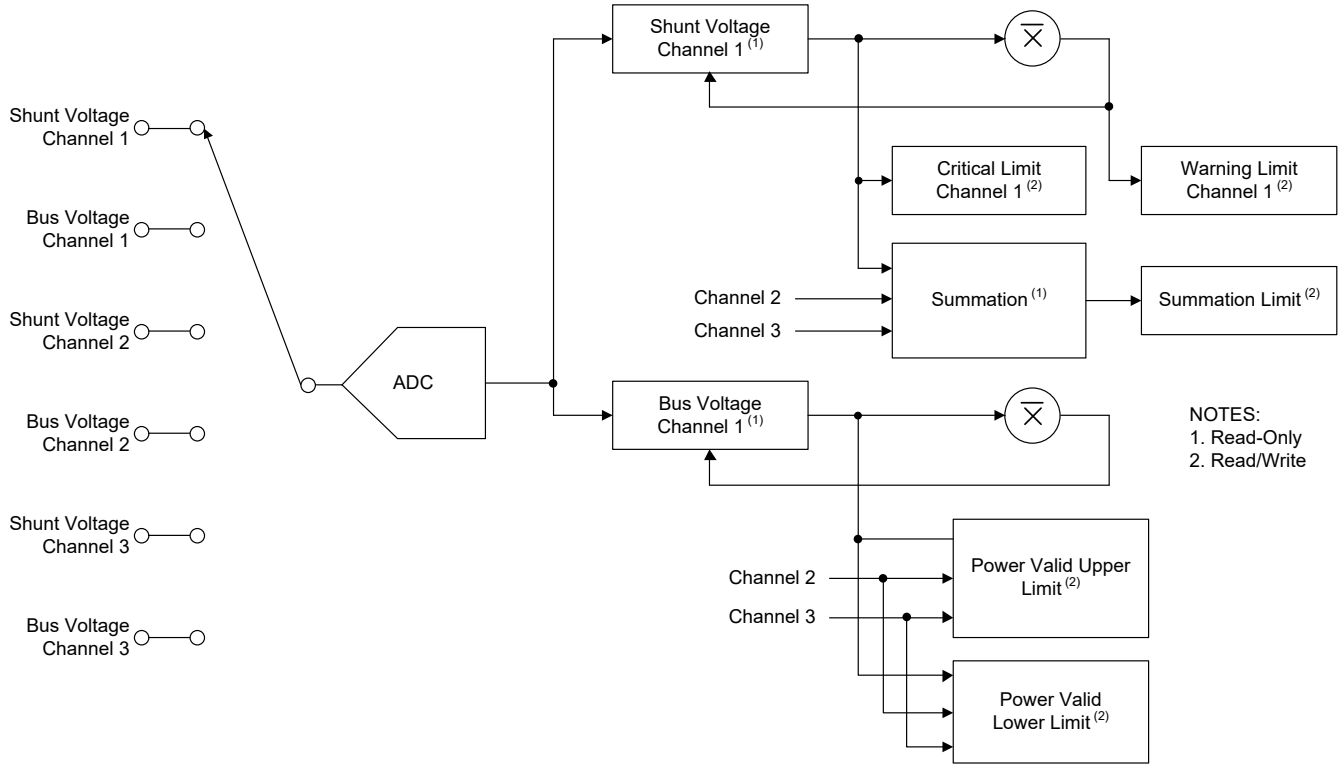


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM842 is a 13-bit shunt-voltage and bus-voltage monitor with I²C and SMBus compatible interface. The device senses both shunt and bus voltages, and provides total six digital results readings in the data registers for three rails to maintain compliance voltages. In addition, it provides programmable registers to flexibly configure the device such as operating modes, conversion and averaging times and multiple alert functions, including critical alert, warning alert, power-valid alert and timing control alert.

Basic ADC Functions

The SGM842 measures two voltages at the input terminals, namely the bus voltage on IN-x pin referred to GND pin and the shunt voltage on IN+x pin referred to IN-x pin (x = 1, 2 and 3.) In typical applications, a current sense resistor (shunt resistor) is connected to the IN+x and IN-x pins. When the power rail is connected to IN+ load current on the resistor, the shunt voltage developed is measured.

Since the power supply of the device, V_S is independent of the input voltage from IN+x (x = 1, 2 and 3), the power-up sequence does not need special attention. Therefore, the bus and shunt voltages can be applied to the input pins no matter when the device is powered on or powered off.

Continuous mode and triggered mode are two operating modes. For the default continuous mode, the SGM842 measures and converts the shunt voltage and the bus voltage sequentially. For the triggered mode, the SGM842 is triggered to perform a one-shot measurement/conversion by writing any of the triggered control modes to the Configuration Register. This action controls the device to perform a single measurement/conversion. Therefore, to trigger another single conversion, the Configuration Register must be written again, even though the operation mode does not change. To help coordinate one-shot or trigger conversions, the SGM842 provides a conversion ready flag bit, CVRF. The CVRF bit is set after all the measurements, conversions and averaging are completed. The CVRF bit clears under the conditions of writing to the Configuration Register or reading the Mask/Enable Register (0Fh).

For converting both the shunt voltage and bus voltage, the SGM842 can also be configured to convert only the shunt voltage or the bus voltage by setting the mode control bits in the Configuration Register. This design provides more application flexibility for the users.

Apart from the continuous and triggered modes, the power-down mode of the device can decrease the quiescent current and block current into the inputs. In this mode, the registers of the device can still be written and read. Until one of the active modes is written into the Configuration Register, the device stays in power-down mode.

Alert Monitoring

The SGM842 offers four alert functions to monitor potential faults and warnings, namely the critical alert, the warning alert, power-valid alert, and timing-control alert. The thresholds of triggering the alerts can be programmable through specific registers. In default power-up state, the registers are initialized according to the Register Maps. Therefore, any changes made to the alert thresholds from their default values will not be persistent after a power cycle. It is necessary to reprogram the user-defined alert configurations every time the power supply rail, V_S, turns on.

Critical Alert

The critical alert function is used to monitor whether there is exist the excessive current loading on the shunt resistors. If the measured shunt voltages of any channels exceed the limit set in every conversion time, the critical alert pin will be pulled to a low state, signaling a critical condition. To determine which specific channel has triggered the alert, users can examine the Mask/Enable Register and check the status of the critical alert flag indicator. A value of 1 for any of these bits indicates that the respective channel has exceeded its critical limit. The current limit of the critical alert is programmable in the registers.

In some specified cases, the SGM842 provides an option for users to report the alert of the exceeding summation of all currents from three channels. This selectable function calculates the cumulative sum of the shunt-voltage conversions for the register selected channels and then assesses whether this sum exceeds the configured limit. To ensure the summation limit is meaningful, it is recommended to use the same current sensing resistors on the IN+x and IN-x at different channels.

DETAILED DESCRIPTION (continued)

Warning Alert

The warning alert function is used to monitor whether the averaged current of each shunt voltage channel exceeds the configured warning alert limits. The average number is specified by the Configuration Register. If the average value exceeds the programmed limit, it indicates that the supply current is higher than the intended value and the warning alert pin will flip to low. By reading the Mask/Enable Register, the Mask/Enable Register can present the warning channel number.

Power-Valid (PV) Alert

The power-valid alert function is used to monitor whether the sensed three-channel bus voltages stay in the user-defined valid thresholds. It is available to define both the valid upper voltage limit and the lower limit. If the V_{BUS} of all the three channels are higher than the PV upper limit, the output state of power valid pin goes high. If at least one channel goes below lower limit, the output state of power valid pin flips to low, which takes low priority to the former·case.

Besides, if the PV pin output low, it indicates the input power is in an invalid condition. Otherwise, the input power is valid. Since the inner structure is an open-drain connection and the drain output is connected to VPU through a resistor, the high level can reach VPU. Besides, by adding an external pull-down resistor, the PV pin can be regulated to other user-defined range.

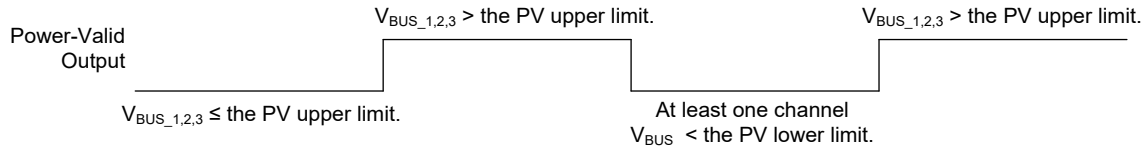
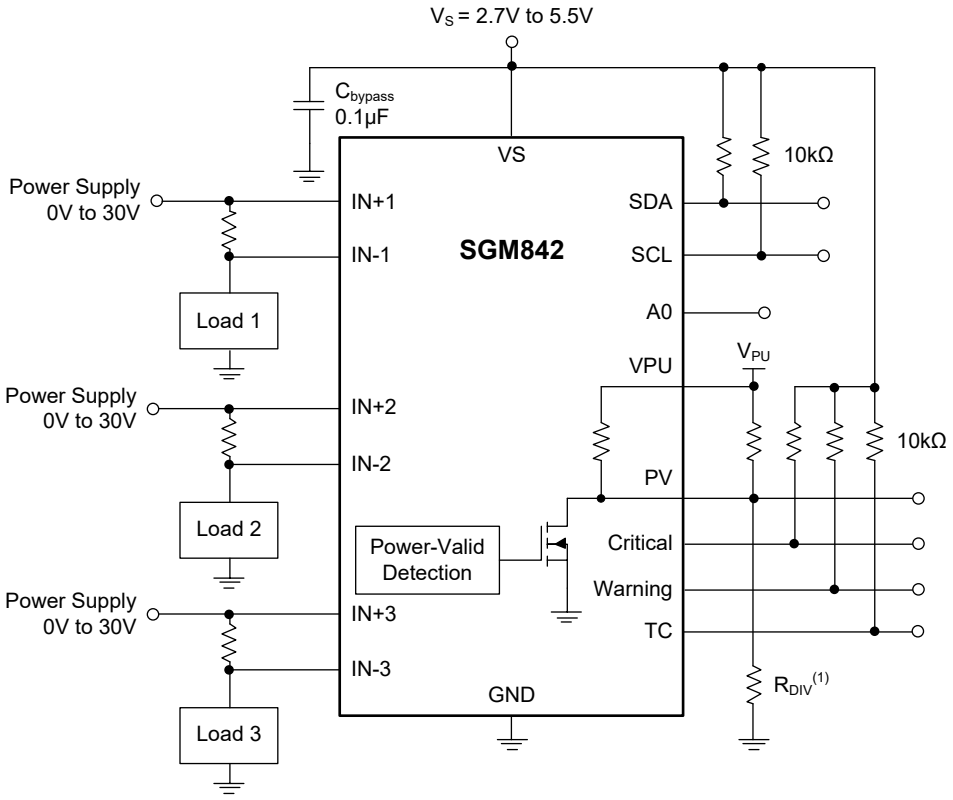


Figure 4. Power-Valid State Diagram



NOTE: 1. R_{DIV} can be used to level-shift the PV output high.

Figure 5. Power-Valid Output Structure

DETAILED DESCRIPTION (continued)

Timing-Control Alert (TC Alert)

The SGM842's timing-control alert function is designed to assist in verifying the correct sequencing of the power supply during startup or chip reset. When powered on or reset by the register, the SGM842 defaults to a continuous shunt-voltage and bus-voltage conversion mode. Internally, it starts comparing the bus voltage on channel 1 to determine when it reaches a threshold of 1.2V. Once capturing a 1.2V voltage on CH1, the SGM842 proceeds to monitor the bus voltage on CH2 for the same 1.2V threshold. However, if after four complete cycles of measuring all three channels' shunt and bus voltages, the SGM842 fails to detect a voltage of 1.2V or higher on channel 2, the TC alert pin is pulled low as an indication that the power on sequence is not valid. If the Configuration Register is written before the timing control alert function has completed its full sequence, it wi ll disable the alert functionality. Once disabled, the timing control alert will no longer be triggered until the next power cycle occurs or the RST bit is set again to issue a software reset.

As depicted in Figure 6 below, this verification sequence allows for approximately 29.9ms from the moment 1.2V is detected on channel 1 for a valid voltage to be established on channel 2. The possible states and transitions it undergoes based on the voltage levels detected on the bus voltages.

Software Reset

The SGM842 includes a software reset feature that allows for a system reset without the need to cycle power. To perform a software reset, set bit 15 (RST) of the Configuration Register. When this bit is set, all registers and settings are reset to their default state, except for the power-valid output state. This provides a convenient way to restore the SGM842 to its initial configuration without physically powering down and back up the device.

Upon issuing a software reset, the device retains the PV pin's output until the power-valid detection sequence is completed. Any reprogrammed limit registers are reset to their original values, ensuring that the initial power-valid thresholds are used to validate the power-valid conditions. This design ensures that the circuitry connected to the power-valid output remains uninterrupted during a software reset, as the PV pin's behavior is maintained until the detection sequence is completed.

Averaging Function

The SGM842 is equipped with three channels for monitoring up to three separate supply buses. However, when implementing multi-channel monitoring, there are challenges associated with the placement of shunt resistors. Ideally, shunt resistors should be positioned as closely as possible to their respective channel input pins. However, due to constraints in system layout and the presence of multiple power-supply rails, it may be necessary to locate one or more shunt resistors at a greater distance, leading to potentially increased measurement errors.

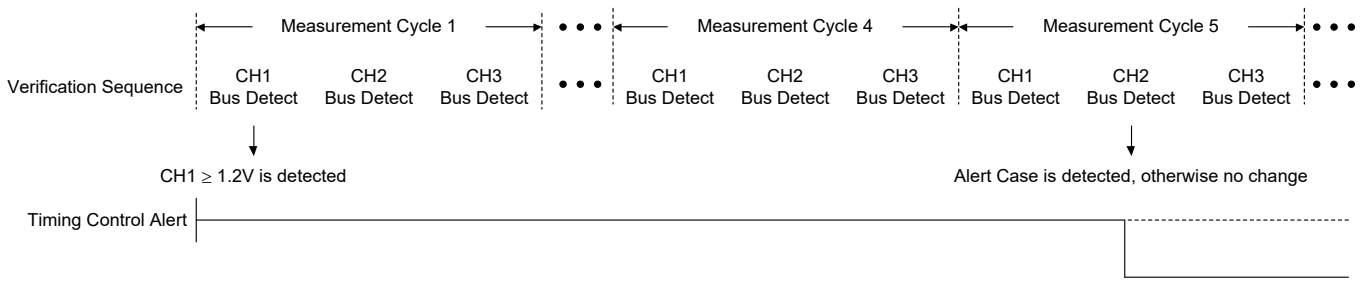


Figure 6. Timing Control State Diagram

DETAILED DESCRIPTION (continued)

The averaging feature of the SGM842 helps alleviate potential problems by lessening the significance of individual measurements in calculating the overall averaged signal value. As a result, it reduces the noise influence on the averaged output, effectively filtering the incoming signals.

The averaging function in Figure 7 works by capturing the shunt input signal on channel 1 and comparing it to the previous output value. The difference between the two is divided by a factor set by the averaging mode configuration (AVG[2:0] bits). This adjusted difference is then accumulated and added to the previous output value, resulting in a new average result updated in the register. As new measurements are taken, the process repeats. By increasing the averaging factor, the impact of individual measurements on the average is reduced, effectively filtering out noise from the averaged measurement value.

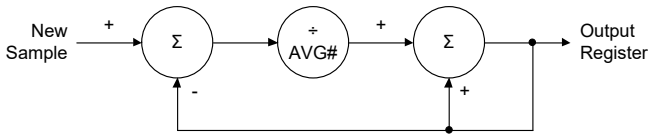


Figure 7. Averaging Function Block Diagram

Multiple Channel Monitoring

The SGM842 offers the channel enable option in the configuration register for single or dual channel(s) application. In default mode, all three channels are open and sense back six signals in the register.

Channel Configuration

During the power-up process, it is crucial to monitor all three channels. However, once the system achieves stability, it suffices to monitor only one channel. Consequently, in some specific applications, upon successful power-up, the remaining two channels can be disabled. This configuration enables the SGM842 to concentrate solely on monitoring the desired power-supply rail, thus optimizing its efficiency. Disabling unused channels also contributes to enhancing the system's response time by swiftly resuming sampling of the channel of interest. The SGM842 functions in a linear manner, monitoring enabled channels. By enabling a single channel and measuring only one signal, there is no extra delay between the end of present conversion and the next start of the new conversion.

Averaging and Conversion-Time Considerations

The averaging and conversion times are programmed by the Configuration Register. Six levels of conversion time from 340μs to 8.35ms are available. The programmable conversion and average times allow the device to match different time requirements in real applications.

For example, if the host requires the shunt voltage and bus voltage data of one channel every 13.908ms, the conversion time for shunt and bus voltage measurement can be set to 1.15ms, with the average time set to 4. With this configuration, the shunt and voltage values are updated approximately every 1.15ms with no influence on multiple times of averaging. Also, the conversion time for shunt and voltage measurement can be different, which allows the device to focus on one of the two voltages.

Suppose the system desires more conversion time for shunt voltage, an 8.35ms conversion time can be set for shunt voltage, with 1.15ms of conversion time for bus voltage and single conversion (average time set to ‘1’). With this configuration, the shunt and bus voltage values are updated approximately every 9.5ms.

There are trade-offs between the conversion and average times used. The averaging can filter the input signal, thus effectively improving the measurement accuracy. With more average times, the device would reduce the noise of the input signal more effectively.

Similarly, the conversion time also affects the measurement accuracy. A longer conversion time results in better measurement accuracy. Therefore, to achieve the highest measurement accuracy, use the longest conversion time with the most average times, provided that the time requirements of the system are met.

Figure 8 shows the relationship between noise and conversion time.

DETAILED DESCRIPTION (continued)

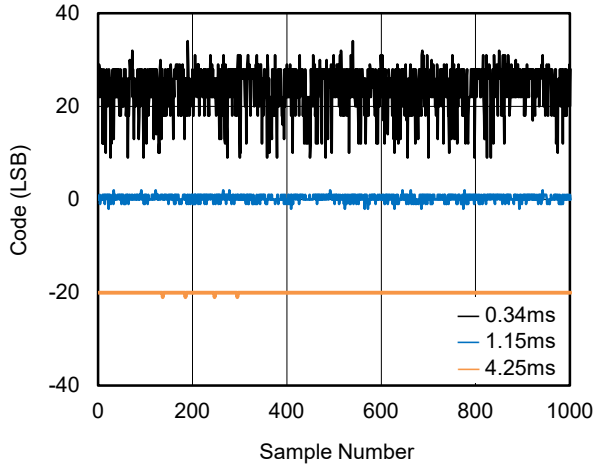


Figure 8. Noise vs. Conversion Time

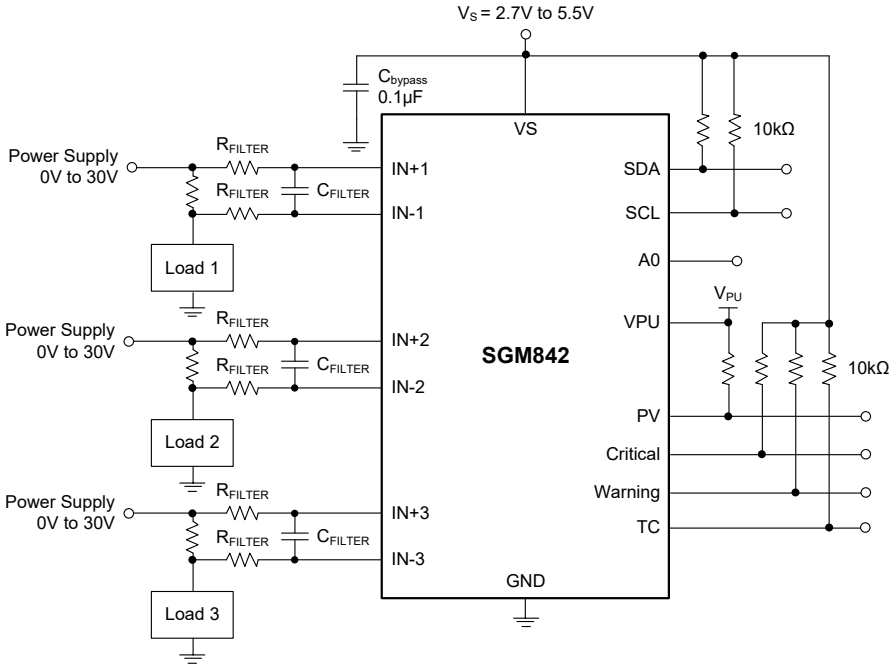
Filtering and Input Considerations

In real applications, the current measurement usually introduces undesirable noise. The SGM842 provides different noise filtering capabilities by configuring the conversion and average times independently in the Configuration Register. The conversion time for shunt and bus voltage can be set independently, while the average times are the same.

The ADC of SGM842 is a delta-sigma (Δ-Σ) structure with a 500kHz (±30%) typical sampling rate. The delta-sigma structure has good noise suppression capability. However, if there are transients at or near the sampling frequency (greater than 1MHz), it will affect the measurement accuracy which needs to be handled. By placing low-value resistors in series with a ceramic capacitor at the IN+ and IN- pins, these high frequency signals can be effectively filtered. Figure 9 shows the filter setup, where the recommended resistor value is less than 10Ω and the recommended capacitor value is between 0.1μF and 1μF. Both resistor values should be consistent to avoid offset due to I_{BIAS}.

Besides the transients, the input overload conditions should also be well addressed. The inputs of the device can tolerate 30V voltage. During a load short-circuit, the load current flows, and the shunt resistor increases sharply. When the short-circuit fault is removed, the parasitic inductance in the power loop could induce kickback voltages on the inputs which may exceed the voltage ratings. Such kickback voltages can be well suppressed using zener-type devices.

In some applications, an over-stress condition may occur as a result of an excessive dV/dt caused by events such as input hard short. The over-stress occurs due to the activation of the internal ESD protection with large available currents. The test results show that adding the 10Ω resistors at the inputs can sufficiently protect the devices from dV/dt induced fault event.



NOTE: R_{FLITER} < 10Ω, C_{FLITER} = 0.1μF to 1μF.

Figure 9. SGM842 with Input Filtering

PROGRAMMING

Bus Overview

The SGM842 provides compatibility with I²C and SMBus interfaces. I²C and SMBus are essentially compatible. In this manual, the I²C interface is used as an example, and the SMBus interface will only be mentioned unless there is a difference between the SMBus interface and the I²C interface. SCL and SDA connect the device to the bus, and they are both open-drain connections.

The device which can send the command to the target register is called master and the device which can be controlled by the master is called slave. The master device can generate the clock signal to the slave in order to control it with SCL and SDA lines.

Send a specific address to start the slave. The SDA signal will be pulled from high to low while SCL is still in high state. For the slaves connected to the bus, at the CLK rising edge, the slaves start to be addressed by the master, and followed by a READ or WRITE bit. For the ninth bit of the transmission signal, if SDA is pulled low, the slave acknowledges the transmission, in which case the slave is being addressed.

In one word, for the data transfer process, the initial signal will indicate a start state, and then followed by eight clock pulses and an acknowledge signal. However, the stability of SDA signal should be guaranteed when SCL is high, otherwise it will be mistaken for START or STOP mode. After the transmission completes, the signal of SDA will change from low to high when SCL is high. The device provides a 28ms timeout action logic on its interface to avoid the bus being locked up.

Serial Bus Address

For the definition of I²C communication, before sending data, the master device should address the specified slave device. There are seven bits for the address of the slave device and another one bit is for the command of reading or writing.

A0 is used to determine the address of the device. As shown in Table 1, if this pin is at different logic levels, the device will have different addresses. The device will sample the state of A0 pins before each communication, so it is necessary to ensure the stability of the states of A0 pin before any actions are taken on the interface.

Table 1. Address Pins and Slave Addresses

A0	Slave Address
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011

Serial Interface

On the I²C bus or SMBus, the SGM842 can be operated as a slave device, which is controlled by the master. When connecting to the bus, both SDA and SCL pins are connected through the topology of open-drain. In addition, in order to improve the performance of slave devices under the condition of input spikes and noise bus, filter and Schmitt flip-flop are adopted. Although the device has integrated tip suppression in the digital I/O lines, it is recommended that proper layout be used to minimize coupling in the communication lines. Noise in communication lines mainly comes from two sources: capacitive coupling generated at the signal edges between two communication lines, or switching noise generated by other parts of the system. Keeping lines parallel to ground when routing can reduce coupling effects between communication lines. In addition, shielded signal lines reduce the possibility of unintended noise coupling into digital I/O lines that could be misinterpreted as a START or STOP command.

There are two modes of transmission protocol: fast mode (1kHz to 400kHz) and high-speed mode (1kHz to 3.4MHz). MSB is the first bit to be transferred when transmitting a byte.

Writing to and Reading From the SGM842

In order to access the specified pointer register of SGM842, it is necessary to send the values of the desired pointer register after addressing the slave device. As already illustrated in Figure 9, the values of pointer register are required after each write command.

PROGRAMMING (continued)

The first byte written to a register is the address of the slave device, and R/$\overline{W}$ bit is low, then the device acknowledges receipt of a valid address. The second byte sent by the host is the address of the register to be written, which updates the register pointer to the desired register. The following two bytes are written to the register addressed by the register pointer, and the device then acknowledges receipt of each byte. Finally, the master generates a START or STOP condition to terminate data transfer (Figure 10).

If the master device desires to read the information of the specified register, a write command must be sent by the master at first to indicate which pointer register is needed. First, the slave address should be sent with the low state of R/$\overline{W}$, followed by the address of the pointer address (Figure 9). Second, the START command should be sent by the master, the slave address of the specified SGM842, and then followed with the high state of R/$\overline{W}$ to indicate a read command (Figure 11). The slave transmits the next byte, which is the most significant byte of the register indicated by the register pointer. For the condition of repeated reading, it is not required to send the bytes of pointer register again, unless the device is reset or the address of pointer register is altered by the write command.

High-Speed I²C Mode

The SGM842 also supports high-speed (HS) I²C mode whose data rate speeds up to 3.4MHz. To enable this mode, the master device sends a START condition. After the START, a master code is transmitted '00001XXX', followed by a mandatory Not Acknowledge (NACK) condition. Note that the master code is sent in Fast-mode or Standard-mode, which is at most 400kHz.

The three lowest bits of the master code are used to identify different I²C masters on the same bus. The user should guarantee that each master device has its unique identifier.

After the NACK condition, the high-speed transfer begins. At the master device side, the master device sends a REPEATED START condition followed by the slave address and the remaining data, the same as the frame in Fast-mode or Standard mode, just higher speed. At the slave device side, the SGM842 switches the internal circuit to support HS mode. To keep the bus in HS mode, the user should avoid using the STOP condition and use the REPEATED START condition instead. A STOP condition makes the SGM842 switch back to support Fast-mode or Standard-mode.

SMBus Alert Response

The SGM842 has the ability to respond to the SMBus alert response that has the ability to identify a quick fault for simple slaves. The master broadcasts the alert response slave address (0001100) and the R/$\overline{W}$ bit is high. The slave that generates the ALERT signal will send its own address through the bus after recognizing the alert response. The host can identify the slave that generates the alert after receiving the slave address (Figure 12).

The alert response is similar to the I²C broadcast call, which may cause multiple slave devices to respond at the same time, and the bus arbitration rules are applied at this time. The losing device will not generate an Acknowledge but continue to pull the Alert line low until it is the device's turn to complete the Acknowledge. Cleared Alert pin asserts again until alert event removes.

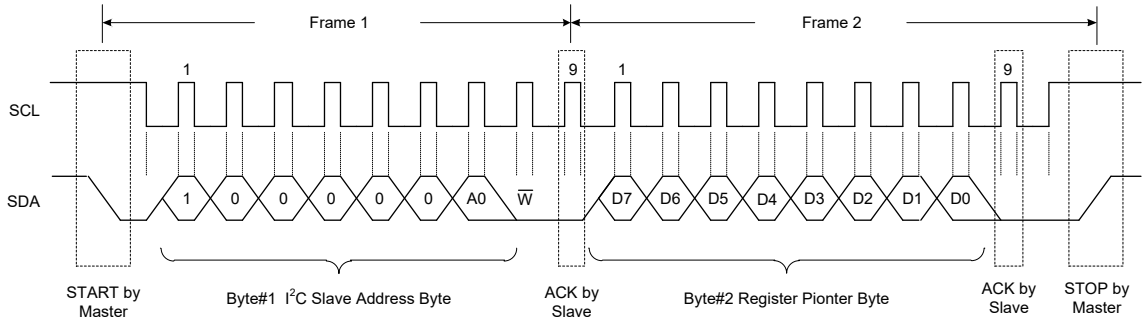


Figure 10. Typical Register Pointer Set

PROGRAMMING (continued)

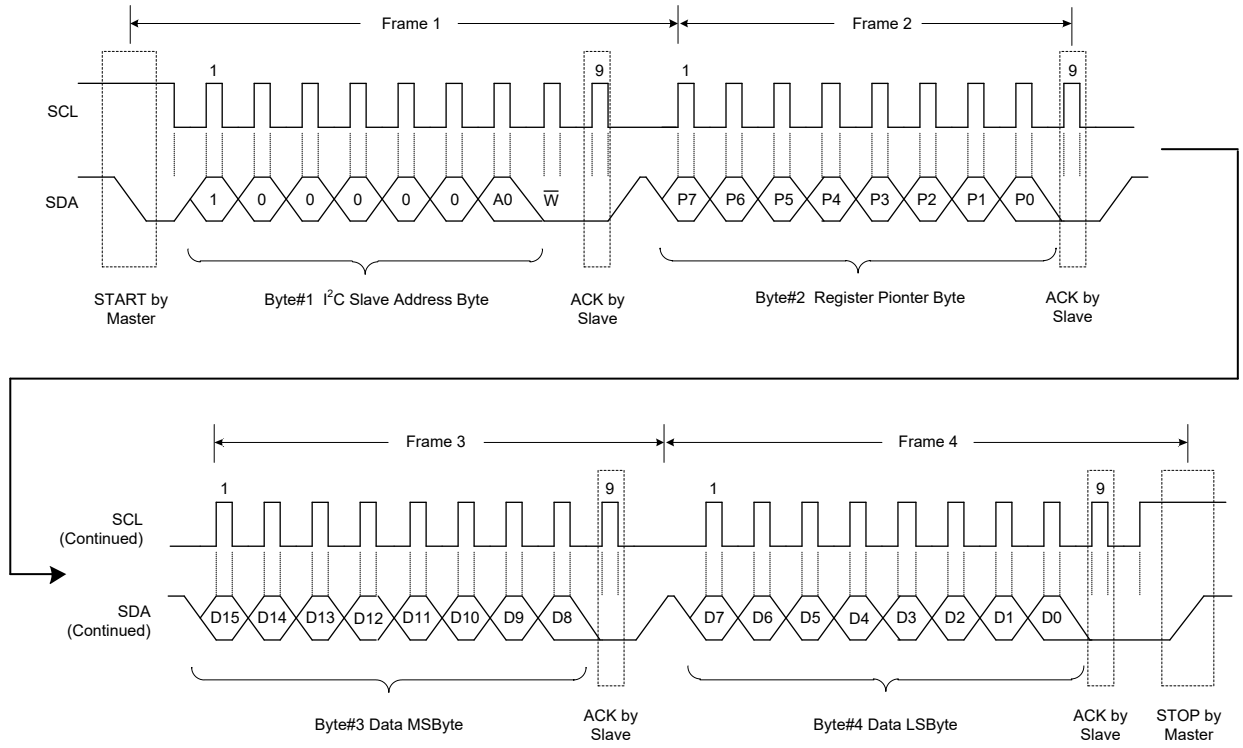


Figure 11. Register Write Word Format

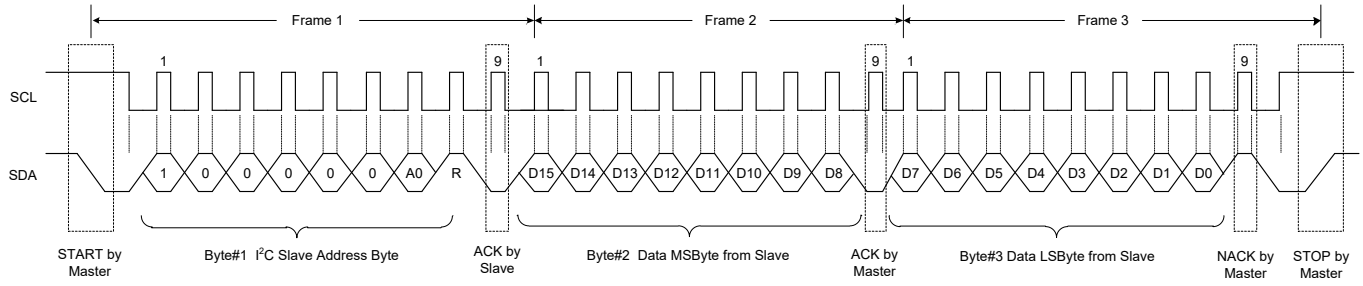


Figure 12. Register Read Word Format

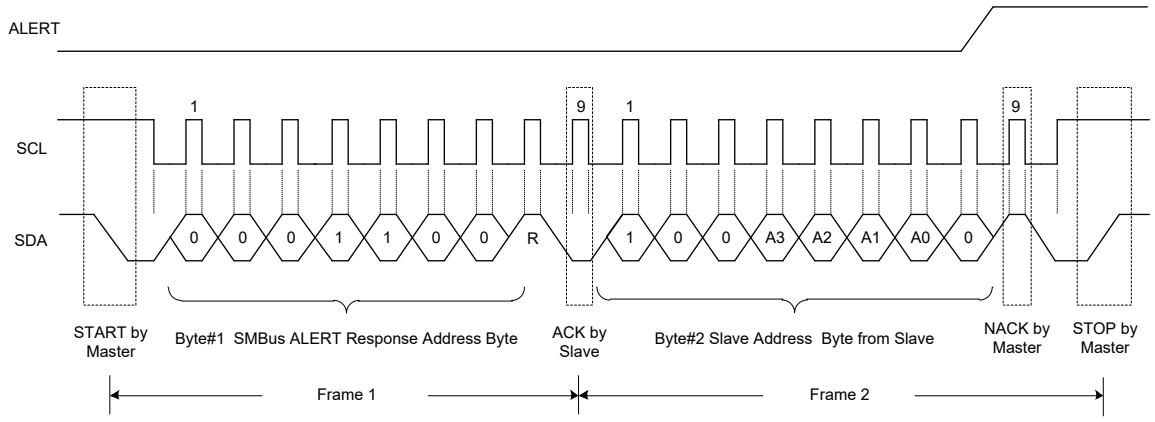


Figure 13. SMBus Alert Format

REGISTER MAPS

I²C Register Set Summary

The SGM842 uses multiple registers to hold configuration information, test results, threshold settings and status information. All device registers are 16 bits, 2 bytes, and communicate through the I²C interface.

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE
HEX			BINARY	HEX	
00	Configuration Register	Configure ADC averaging, conversion times and operating mode of shunt voltage and bus voltage, reset function.	01110001 00100111	7127	R/$\overline{W}$
01	Shunt Voltage 1 Register	Averaged shunt voltage value of channel 1.	00000000 00000000	0000	R
02	Bus Voltage 1 Register	Averaged bus voltage value of channel 1.	00000000 00000000	0000	R
03	Shunt Voltage 2 Register	Averaged shunt voltage value of channel 2.	00000000 00000000	0000	R
04	Bus Voltage 2 Register	Averaged bus voltage value of channel 2.	00000000 00000000	0000	R
05	Shunt Voltage 3 Register	Averaged shunt voltage value of channel 3.	00000000 00000000	0000	R
06	Bus Voltage 3 Register	Averaged bus voltage value of channel 3.	00000000 00000000	0000	R
07	Critical Alert Limit 1 Register	The threshold for each conversion value of Channel 1.	01111111 11111000	7FF8	R/$\overline{W}$
08	Warning Alert Limit 1 Register	The threshold for averaged measurement value of Channel 1.	01111111 11111000	7FF8	R/$\overline{W}$
09	Critical Alert Limit 2 Register	The threshold for each conversion value of Channel 2.	01111111 11111000	7FF8	R/$\overline{W}$
0A	Warning Alert Limit 2 Register	The threshold for averaged measurement value of Channel 2.	01111111 11111000	7FF8	R/$\overline{W}$
0B	Critical Alert Limit 3 Register	The threshold for each conversion value of Channel 3.	01111111 11111000	7FF8	R/$\overline{W}$
0C	Warning Alert Limit 3 Register	The threshold for averaged measurement value of Channel 3.	01111111 11111000	7FF8	R/$\overline{W}$
0D	Shunt-Voltage Sum Register	The sum measurement value of each selected shunt voltage conversions.	00000000 00000000	0000	R
0E	Shunt-Voltage Sum Limit Register	The threshold for the Shunt Voltage Sum register.	01111111 11111110	7FFE	R/$\overline{W}$
0F	Mask/Enable Register	Alert configuration and alert status indication. Summation control and status.	00000000 00000010	0002	R/$\overline{W}$
10	Power-Valid Upper Limit Register	The upper threshold for all bus voltage conversions.	00100111 00010000	2710	R/$\overline{W}$
11	Power-Valid Lower Limit Register	The lower threshold for all bus voltage conversions.	00100011 00101000	2328	R/$\overline{W}$
FE	Manufacturer ID Register	ID data of manufacturer.	01010100 01001001	5449	R
FF	Die ID Register	ID data of die.	00110010 00100000	3220	R

NOTE: 1. Type: R = Read-Only, R/$\overline{W}$ = Read/Write.

REGISTER MAPS (Continued)

00h: Configuration Register [reset = 7127h]

The Configuration Register is used to configure the operating mode of the three input channels. This register cannot only control the conversion time and averaging mode of both shunt and bus voltages, but also control what signals are selected to be measured.

The Configuration Register can be read without affecting device configuration and ongoing conversion. Writing to the Configuration Register suspends ongoing conversion until the write process is completed, and then the device will begin a new conversion process with the new configuration. The purpose is to avoid any uncertainty about the conditions under which a new conversion process will be started.

BITS	BIT NAME	RESET	TYPE	DESCRIPTION
D[15]	RST	0h	R/$\overline{W}$	Reset Bit. When this bit is set to 1, the system will be reset as the power-on reset. It means that all registers are set to their default values. This bit self-clears.
D[14]	CH1EN	7h	R/$\overline{W}$	Channel Enable Mode. Set each channel to be enabled or disabled independently. 0 = Channel disable 1 = Channel enable (default)
D[13]	CH2EN			
D[12]	CH3EN			
D[11:9]	AVG[2:0]	0h	R/$\overline{W}$	Averaging Mode. Determine the number of samples collected and averaged. 000 = 1 (default) 001 = 4 010 = 16 011 = 64 100 = 128 101 = 256 110 = 512 111 = 1024
D[8:6]	VBUSCT[2:0]	4h	R/$\overline{W}$	Bus Voltage Conversion Time. Set the conversion time for the bus voltage measurement. 000 = 340μs 001 = 340μs 010 = 340μs 011 = 600μs 100 = 1.15ms (default) 101 = 2.15ms 110 = 4.25ms 111 = 8.35ms
D[5:3]	VSHCT[2:0]	4h	R/$\overline{W}$	Shunt Voltage Conversion Time. Set the conversion time for the shunt voltage measurement. 000 = 340μs 001 = 340μs 010 = 340μs 011 = 600μs 100 = 1.15ms (default) 101 = 2.15ms 110 = 4.25ms 111 = 8.35ms
D[2:0]	MODE[2:0]	7h	R/$\overline{W}$	Operating Mode. Select the operation modes, continuous, one-shot (triggered) or power-down. These bits default to continuous shunt and bus measurement mode. 000 = Power-Down 001 = Shunt Voltage, One-Shot (Triggered) 010 = Bus Voltage, One-Shot (Triggered) 011 = Shunt and Bus, One-Shot (Triggered) 100 = Power-Down or Shutdown 101 = Shunt Voltage, Continuous 110 = Bus Voltage, Continuous 111 = Shunt and Bus, Continuous (Default)

REGISTER MAPS (Continued)

01h: Shunt Voltage Register 1 (reset = 00h)

This register is used to store the averaged shunt voltage reading, V_{SHUNT}, for channel 1. Positive numbers are directly displayed in binary format, while negative numbers are displayed in two's complement format. The two's complement of the negative number can be obtained by taking the binary complement.

For example: assuming V_{SHUNT} = -80mV:
Convert the absolute value (80mV) to a decimal integer in LSBs (80mV/40μV) = 2000
Convert this number to binary = 011 1110 1000 0000(last three bits are set to 0)
Complement the binary result = 100 0001 0111 1111
Add 1 to the complement to create the two's complement result = 100 0001 1000 0000
Extend the sign and create the 16-bit word: 1100 0001 1000 0000 = C180h

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	SD[11:0]	0h	R	Shunt-Voltage Data Bits for Channel 1.
D[2:0]	RESERVED	0h	R	Reserved.

02h: Bus Voltage Register 1 (reset = 00h)

This register is used to store the bus voltage reading, V_{BUS}, for channel 1. The register will display the averaged value if averaging enabled.

Full-scale range of bus voltage = 32.76V (decimal = 7FF8). LSB: 8mV. Do not apply more than 30V.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	BD[11:0]	0h	R	Bus-Voltage Data Bits for Channel 1.
D[2:0]	RESERVED	0h	R	Reserved.

03h: Shunt Voltage Register 2 (reset = 00h)

This register is used to store the shunt voltage reading, for channel 2. The register will display the averaged value if averaging enabled.

Full-scale range of shunt voltage = 163.8mV (decimal = 7FF8). LSB: 40μV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	SD[11:0]	0h	R	Shunt-Voltage Data Bits for Channel 2.
D[2:0]	RESERVED	0h	R	Reserved.

04h: Bus Voltage Register 2 (reset = 00h)

This register is used to store the bus voltage reading, for channel 2. The register will display the averaged value if averaging enabled.

Full-scale range of bus voltage = 32.76V (decimal = 7FF8). LSB: 8mV. Do not apply more than 30V.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	BD[11:0]	0h	R	Bus-Voltage Data Bits for Channel 2.
D[2:0]	RESERVED	0h	R	Reserved.

REGISTER MAPS (Continued)

05h: Shunt Voltage Register 3 (reset = 00h)

This register is used to store the shunt voltage reading, for channel 3. The register will display the averaged value if averaging enabled.

Full-scale range of shunt voltage = 163.8mV (decimal = 7FF8). LSB: 40μV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	SD[11:0]	0h	R	Shunt-Voltage Data Bits for Channel 3.
D[2:0]	RESERVED	0h	R	Reserved.

06h: Bus Voltage Register 3 (reset = 00h)

This register is used to store the bus voltage reading, for channel 3. The register will display the averaged value if averaging enabled.

Full-scale range of bus voltage = 32.76V (decimal = 7FF8). LSB: 8mV. Do not apply more than 30V.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = Positive number 1 = Negative number in two's complement format
D[14:3]	BD[11:0]	0h	R	Bus-Voltage Data Bits for Channel 3.
D[2:0]	RESERVED	0h	R	Reserved.

07h: Critical Alert Limit Register 1 (reset = 7FF8h)

This register is used to store the limit value for channel 1.When channel 1 completes every shunt voltage conversion, the value of this register will be compared to every shunt voltage to detect fast over-current events.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	C1L[12:0]	FFFh	R/$\overline{W}$	Critical-Alert-Limit Data Bits for Channel 1.
D[2:0]	RESERVED	0h	R	Reserved.

08h: Warning Alert Limit Register 1 (reset = 7FF8h)

This register is used to store the limit value for channel 1. When channel 1 completes averaged shunt voltage conversion, the value of this register will be compared to the averaged shunt voltage to detect a longer duration over-current event.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	W1L[12:0]	FFFh	R/$\overline{W}$	Warning-Alert-Limit Data Bits for Channel 1.
D[2:0]	RESERVED	0h	R	Reserved.

09h: Critical Alert Limit Register 2 (reset = 7FF8h)

This register is used to store the limit value for channel 2. When channel 2 completes every shunt voltage conversion, the value of this register will be compared to every shunt voltage to detect fast over-current events.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	C2L[12:0]	FFFh	R/$\overline{W}$	Critical-Alert-Limit Data Bits for Channel 2.
D[2:0]	RESERVED	0h	R	Reserved.

REGISTER MAPS (Continued)

0Ah: Warning Alert Limit Register 2 (reset = 7FF8h)

This register is used to store the limit value for channel 2. When channel 2 completes averaged shunt voltage conversion, the value of this register will be compared to the averaged shunt voltage to detect a longer duration over-current event.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	W2L[12:0]	FFFh	R/$\overline{W}$	Warning-Alert-Limit Data Bits for Channel 2.
D[2:0]	RESERVED	0h	R	Reserved.

0Bh: Critical Alert Limit Register 3 (reset = 7FF8h)

This register is used to store the limit value for channel 3. When channel 3 completes every shunt voltage conversion, the value of this register will be compared to every shunt voltage to detect fast over-current events.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	C3L[12:0]	FFFh	R/$\overline{W}$	Critical-Alert-Limit Data Bits Channel 3.
D[2:0]	RESERVED	0h	R	Reserved.

0Ch: Warning Alert Limit Register 3 (reset = 7FF8h)

This register is used to store the limit value for channel 3. When channel 3 completes averaged shunt voltage conversion, the value of this register will be compared to the averaged shunt voltage to detect a longer duration over-current event.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:3]	W3L[12:0]	FFFh	R/$\overline{W}$	Warning-Alert-Limit Data Bits Channel 3.
D[2:0]	RESERVED	0h	R	Reserved.

0Dh: Shunt-Voltage Sum Register (reset = 00h)

This register is used to store the sum of the single conversion shunt voltages of the selected channels. The summation control bits 12, 13, and 14 in the Mask/Enable register can select which channel is enabled.

This register is updated when all selected channels complete conversion. The LSB value of this register is 40μV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = positive number 1 = negative number in two's complement format
D[14:1]	SV[13:0]	0h	R	Shunt-Voltage Sum Data Bits
D[0]	RESERVED	0h	R	Reserved.

0Eh: Shunt-Voltage Sum-Limit Register (reset = 7FFEh)

This register is used to store the sum limit value that is compared to the Shunt-Voltage Sum register value after each completed cycle of all selected channels. The LSB value of this register is 40μV.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R/$\overline{W}$	Sign Bit. 0 = positive number 1 = negative number in two's complement format
D[14:1]	SVL[13:0]	3FFFh	R/$\overline{W}$	Shunt-Voltage Sum-Limit Data Bits.
D[0]	RESERVED	0h	R	Reserved.

REGISTER MAPS (Continued)

0Fh: Mask/Enable Register (reset = 0002h)

The Mask/Enable Register can choose different logic to control Critical alert and Warning alert pins, as well as how those pins function. Reading this register can clear any flag results present. Writing to this register cannot clear the flag results.

To eliminate uncertainty in the warning function setting and clear any set flag bits, read the Mask/Enable register before changing the warning function setting.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	RESERVED	0h	R/$\overline{W}$	Reserved.
D[14:12]	SCC[1:3]	0h	R/$\overline{W}$	Summation Channel Control Bits. If some bits are set to high, the corresponding channels shunt voltage measurement will be filled to the Shunt-Voltage Sum register. The selection of these bits does not impact the individual channel measurements itself. 0 = Disabled (default) 1 = Enabled
D[11]	WEN	0h	R/$\overline{W}$	Warning Alert Latch Enable. Configure the latch function of the Warning alert pin. 0 = Transparent (default) 1 = Latch enabled
D[10]	CEN	0h	R/$\overline{W}$	Critical Alert Latch Enable. Configure the latch function of the Critical alert pin. 0 = Transparent (default) 1 = Latch enabled
D[9:7]	CF[1:3]	0h	R	Critical-Alert Flag Indicator. These corresponding bit is set to 1 if the channel measurement exceeds the critical alert threshold, which also causes the Critical alert pin to be asserted. These bits can be read to make sure which channel causes the critical alert. These flag bits are cleared when the Mask/Enable register is read back.
D[6]	SF	0h	R	Summation-Alert Flag Indicator. The bit is set to 1 if the measurement in Shunt Voltage Sum register exceeds the threshold in Shunt-Voltage Sum-Limit register, which also causes the alert pin to be asserted. The Summation Alert Flag bit is cleared when the Mask/Enable register is read back.
D[5:3]	WF[1:3]	0h	R	Warning-Alert Flag Indicator. These corresponding bit is set to 1 if the channel averaged measurement exceeds the warning alert threshold, which also causes the warning alert pin to be asserted. These bits can be read to make sure which channel causes the warning alert. These flag bits are cleared when the Mask/Enable register is read back.
D[2]	PVF	0h	R	Power-Valid-Alert Flag Indicator. This bit indicates status of the power valid (PV) alert pin. This bit will not be cleared until the condition that causes the alert of PV pin to be asserted is removed.
D[1]	TCF	1h	R	Timing-Control-Alert Flag Indicator. This bit indicates status of the timing control (TC) alert pin. This bit will not be cleared after it has been asserted unless software resets or being power on again. The default state of the timing control alert flag is high.
D[0]	CVRF	0h	R	Conversion-Ready Flag.

REGISTER MAPS (Continued)

10h: Power-Valid Upper-Limit Register (reset = 2710h)

This register is used to determine the power-valid entering condition. When all bus-voltage channels exceed the value set in this register, the power-valid condition is met and the PV alert pin asserts high. If the bus measurements are not enabled, power-valid condition will not be monitored. The LSB value of this register is 8mV. Power-on reset value is 2710h = 10.000V.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = positive number 1 = negative number in two's complement format
D[14:3]	PVU[11:0]	4E2h	R/$\overline{W}$	Power-Valid Upper-Limit Data Bits.
D[2:0]	RESERVED	0h	R	Reserved.

11h: Power-Valid Lower-Limit Register (reset = 2328h]

When the power-valid conditions are met, the value stored in this register is used to determine if power-valid condition is no longer met. The PV alert pin pulls low when any bus-voltage channel drops below the value of this register. If the bus measurements are not enabled, power-valid condition will not be monitored. The LSB value of this register is 8mV. Power-on reset value is 2328h = 9.000V.

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15]	SIGN	0h	R	Sign Bit. 0 = positive number 1 = negative number in two's complement format
D[14:3]	PVL[11:0]	465h	R/$\overline{W}$	Power-Valid Lower-Limit Data Bits.
D[2:0]	RESERVED	0h	R	Reserved.

FEh: Manufacturer ID Register (reset = 5449h)

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:0]	ID[15:0]	5449h	R	Manufacturer ID Bits. Store the manufacturer identification bits.

FFh: Die ID Register (reset = 3220)

BITS	BIT NAME	POR	TYPE	DESCRIPTION
D[15:0]	DID[15:0]	3220h	R	Device ID Bits. Store the device identification bits.

APPLICATION INFORMATION

The SGM842 is a high accuracy, three-channel monitor with an I²C- and SMBus-compatible interface which can sense high-side or low-side current and bus voltage. It supports a wide common-mode voltage range from 0V to 30V. For more flexibility, the ADC conversion times and sample averaging modes are allowed to be programmed according to the requirements. Additionally, both critical and warning alerts are reported for each channel.

Typical Application

The SGM842 characterizes current by the voltage drop across the shunt resistor, and can also measure the bus voltage on the IN- pins. It has multiple programmable alert functions that respond to user-defined fault or conversion completion events .The device has four alert pins: Critical, Warning, PV, and TC. In addition, users can also customize the specific threshold that triggers alert.

Figure 14 illustrates the SGM842 as an over-current monitor. The bypass capacitors should be placed as close to input and GND pins of the device as possible to ensure the stability of the power supply.

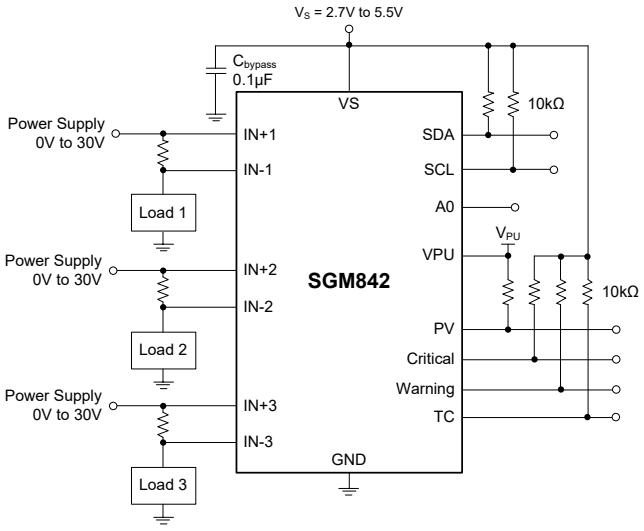


Figure 14. Using SGM842 as an Over-Current Sensor

Design Requirements

For this application, detailed design parameters are shown in Table 2. Set all other register to the default values.

Table 2. Design Parameters

Design Parameter	Design Result
V_S	5V
Pull-Up Resistors	10kΩ
V_{SHUNT}	-163.84mV to +163.8mV
Enabled Channel	CH1
Operating Mode	Shunt voltage, continuous
Average Setting	1
Critical Alert Limit	80mV
Critical Alert Limit Register Setting	7D0h

Detailed Design Procedure

Two conversion times are demonstrated under shunt-only single-channel condition. Figure 15 shows that the Critical alert pin responds to the shunt voltage over-limit when the threshold is set to 80mV, the conversion time (t_{CT}) is 1.15ms. Figure 16 shows the response of reducing the conversion time from 1.15ms to 600μs under the same conditions.

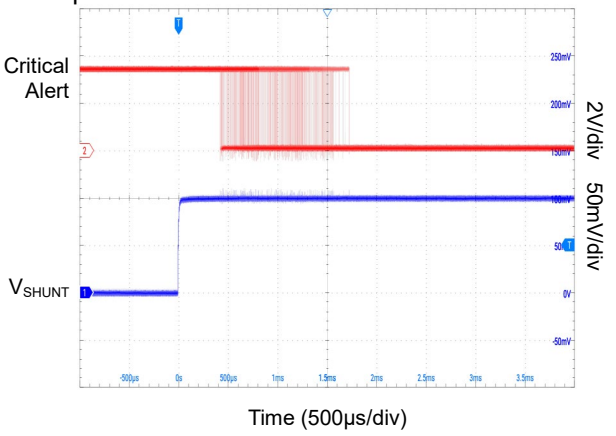


Figure 15. Critical Alert Response (t_{CT} = 1.15ms)

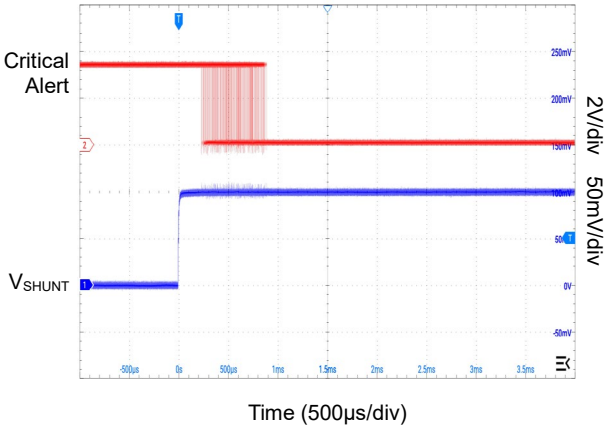


Figure 16. Critical Alert Response (t_{CT} = 600μs)

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The device can accurately measure the common-mode voltages applied to power supply terminals, which may be beyond its supply voltage V_S. For example, the device power supply voltage V_S is 5V, but the monitored load voltage can reach up to 30V. Whether the device is powered on or not, the input terminal of the device can withstand a voltage of 0V to 30V.

The bypass capacitors should be placed as close to input and GND pins of the device as possible to ensure the stability of the power supply. A bypass capacitor of 0.1μF is recommended. For noisy or high-impedance power supplies, add extra decoupling capacitors to filter out the noise.

Layout Guidelines

Current sense connections should be made using Kelvin or 4-wire connection between the input pins (IN+ and IN-) and the sensing resistor. These connection techniques avoid introducing additional impedance between the input pins. Considering that the resistance of the sensing resistor is very small, the additional high current-carrying impedance will result in considerable measurement errors.

REVISION HISTORY

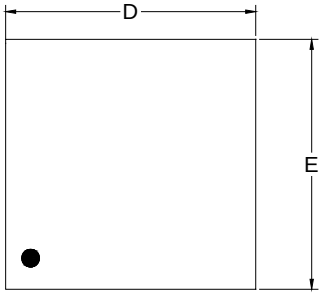
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JANUARY 2025 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	6

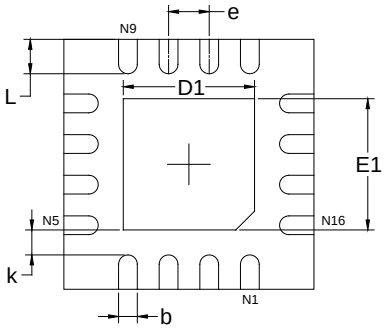
Changes from Original (NOVEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

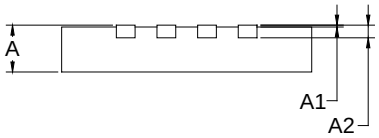
TQFN-4×4-16L



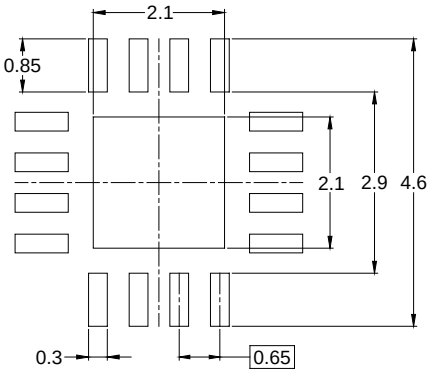
TOP VIEW



BOTTOM VIEW



SIDE VIEW



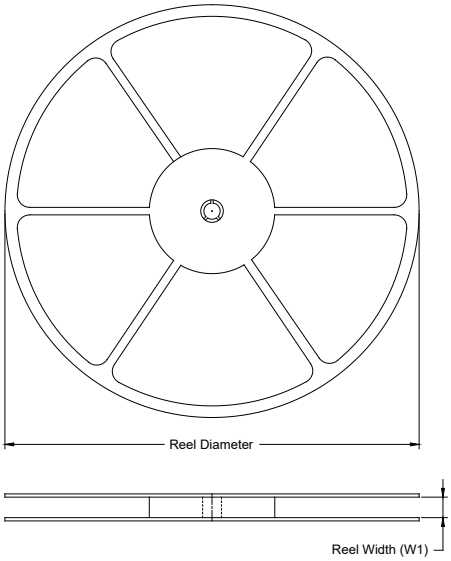
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.000	2.200	0.079	0.087
E	3.900	4.100	0.154	0.161
E1	2.000	2.200	0.079	0.087
k	0.200 MIN		0.008 MIN	
b	0.250	0.350	0.010	0.014
e	0.650 TYP		0.026 TYP	
L	0.450	0.650	0.018	0.026

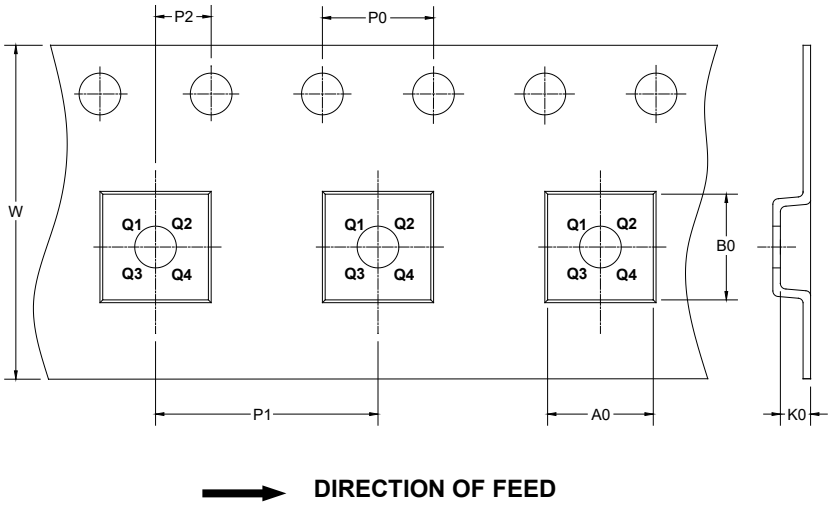
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



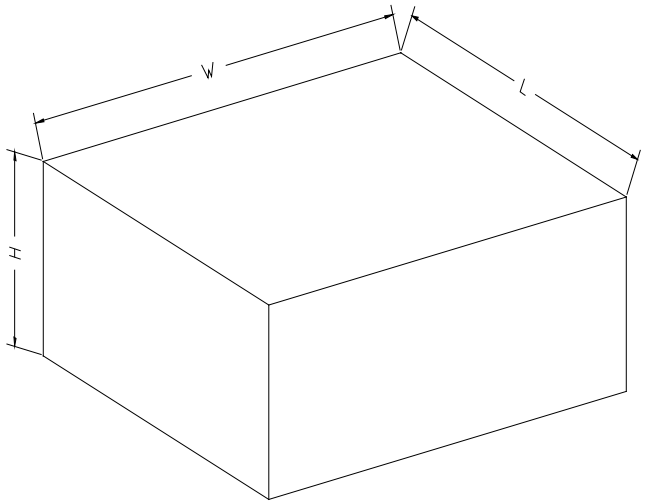
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-16L	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002