SGM821
Nano-Power System Timer with Watchdog Function

GENERAL DESCRIPTION

The SGM821 is an ultra-low power and programmable watchdog timer designed for system wake-up in duty-cycled and battery-powered applications.

The SGM821 with programmable interrupt timer consumes only 35nA (TYP) system current. Accordingly, the system can be placed in sleeping mode, consuming less power, and only returning to active mode when the device is interrupted. The SGM821 is ideal for wireless sensor applications or other applications with smaller batteries compared to the μC that typically costs micro-amps of total system current. The watchdog timer of the SGM821 can be programmed by an external resistor of 500Ω to 180kΩ. And it provides a corresponding time interval from 100ms to 8200s (TYP).

The SGM821 is available in Green SOT-23-6 and TDFN-2×2-6AL packages. It operates over a junction temperature range of -40℃ to +105℃.

FEATURES

- **Supply Voltage Range: 1.8V to 5.5V**
- **Low Current Consumption: 35nA (TYP)**
- **Programmable Watchdog Time: 100ms to 8200s (TYP)**
- **Manual Reset Input**
- **Available in Green SOT-23-6 and TDFN-2×2-6AL Packages**

APPLICATIONS

Low Power Systems
IoT
Tamper Detectors
Smart Home Controllers
Wireless Sensors

TYPICAL APPLICATION

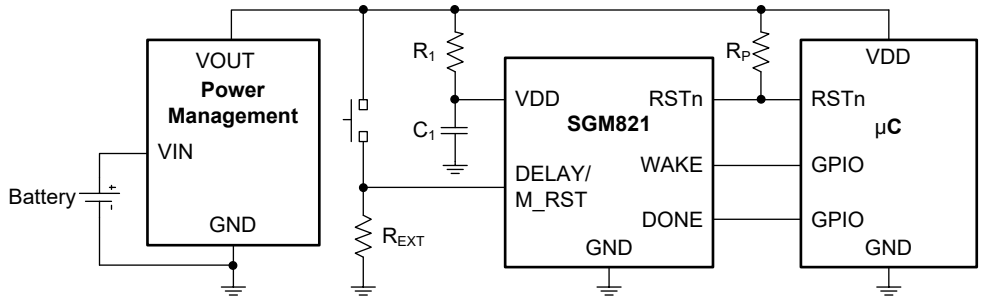


Figure 1. Simplified Application Schematic

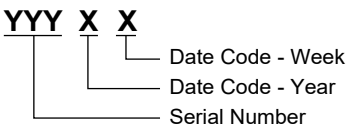
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM821	SOT-23-6	-40℃ to +105℃	SGM821GN6G/TR	RCEXX	Tape and Reel,3000
	TDFN-2×2-6AL	-40℃ to +105℃	SGM821GTDI6G/TR	RCF XXXX	Tape and Reel,3000

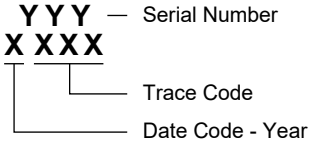
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code and Trace Code.

SOT-23-6



TDFN-2×2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.3V to 6V
Input Voltage at Any Pin (1) .....-0.3V to V_{CC} + 0.3V
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 215℃/W
TDFN-2×2-6AL, θ_{JA}..... 106℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC}.....1.8V to 5.5V
Operating Junction Temperature Range.....-40℃ to +105℃

NOTE:
1. The voltage between any two pins is not allowed to be greater than 6V.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

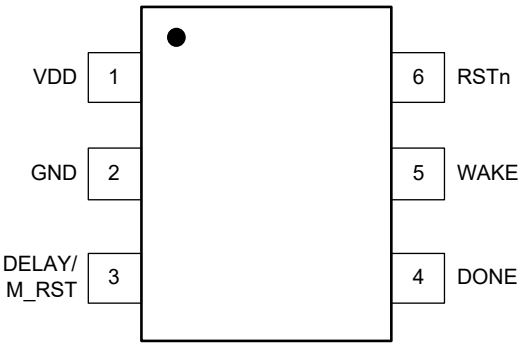
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

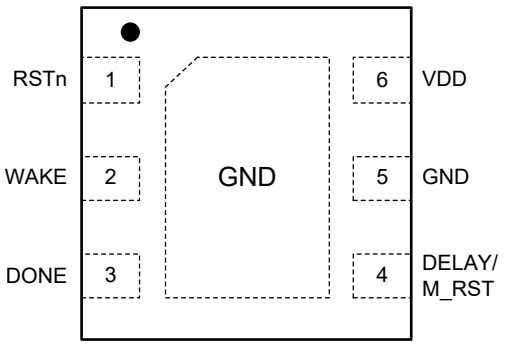
PIN CONFIGURATION

(TOP VIEW)



SOT-23-6

(TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SOT-23-6	TDFN-2×2-6AL			
1	6	VDD	P	Supply Voltage Pin.
2	5	GND	G	Ground.
3	4	DELAY/ M_RST	I	One-Time External Resistance Detection and Manual Reset Pin. Resistor connected between this pin and GND is used to set the watchdog timer. The allowable external resistance ranges from 500Ω to180kΩ. This pin is also used as an input manual reset pin, and pulling this pin up to VDD will issue an RSTn signal.
4	3	DONE	I	Logic Watchdog Input Pin. Digital signal sent by the external system, indicating that the WAKE signal is received. This pin is not allowed to be floating.
5	2	WAKE	O	Watchdog output (Push-Pull) Pin. A pulse signal is sent at the end of the programming time interval to wake up the external system.
6	1	RSTn	O	Reset Output (Open-Drain Output) Pin. Digital signal to RESET the external system. A pull-up resistor is required.
—	Exposed Pad	GND	—	Connect the thermal pad to a large-area ground plane. The exposed pad is internally connected to GND.

NOTE: I = Input, O = Output, G = Ground, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Current (1)	I_{DD}	Operation mode		35	50	nA
		Digital conversion of external resistance (R_{EXT} = 500Ω)		120	150	μA
Timer						
Time Interval Period	t_{IP}	Minimum time interval		100		ms
		Maximum time interval		8200		s
Resistance Detection Accuracy (2)		V_{CC} = 2.5V, excluding reliability test		±2.3		%
		V_{CC} = 2.5V, including reliability test		±4.3		
Resistance Detection Accuracy over Temperature		T_J = -40℃ to +105℃		90		ppm/℃
Resistance Detection Accuracy over Supply Voltage		V_{CC} = 1.8V to 5.5V		±0.02		%/V
Oscillator Accuracy		V_{CC} = 2.5V, excluding reliability test		±1.1		%
		V_{CC} = 2.5V, including reliability test		±2.1		
Oscillator Accuracy over Temperature		T_J = -40℃ to +105℃		210		ppm/℃
Oscillator Accuracy over Supply Voltage		V_{CC} = 1.8V to 5.5V		±0.1		%/V
DONE Pulse Width	t_{DONE}		100			ns
RSTn Pulse Width	t_{RSTn}			320		ms
WAKE Pulse Width	t_{WAKE}			20		ms
Time to Convert R_{EXT}	t_{R_EXT}			100	120	ms
Digital Logic Levels						
Logic High Threshold DONE Pin	V_{IH}		0.7 × V_{CC}			V
Logic Low Threshold DONE Pin	V_{IL}				0.3 × V_{CC}	V
Logic Output High Level WAKE Pin	V_{OH}	I_{OUT} = 100μA	V_{CC} - 0.3			V
		I_{OUT} = 1mA	V_{CC} - 0.7			
Logic Output Low Level WAKE Pin	V_{OL}	I_{OUT} = -100μA			0.3	V
		I_{OUT} = -1mA			0.7	
RSTn Logic Output Low Level	V_{OL_RSTn}	I_{OL} = -1mA			0.3	V
RSTn High Level Output Current	I_{OH_RSTn}	V_{OH_RSTn} = V_{CC}		1		nA
Logic High Threshold DELAY/M_RST Pin	V_{IHM_RST}		1.5			V

NOTES:

1. Current of load and pull-up resistor are not included.

2. This accuracy represents the error of different chip detection results when the external resistance is the same ideal resistance, excluding the error of the external resistance itself.

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DONE to RSTn or WAKE to DONE Delay	t_{DDONE}	Minimum delay (1)		100		ns
		Maximum delay (1)		t_{IP} - 20ms		ms
Debounce Manual Reset	t_{DB}			20		ms
Valid Manual Reset	t_{M_RST}			20		ms

NOTE: 1. From the falling edge of RSTn or the rising edge of WAKE.

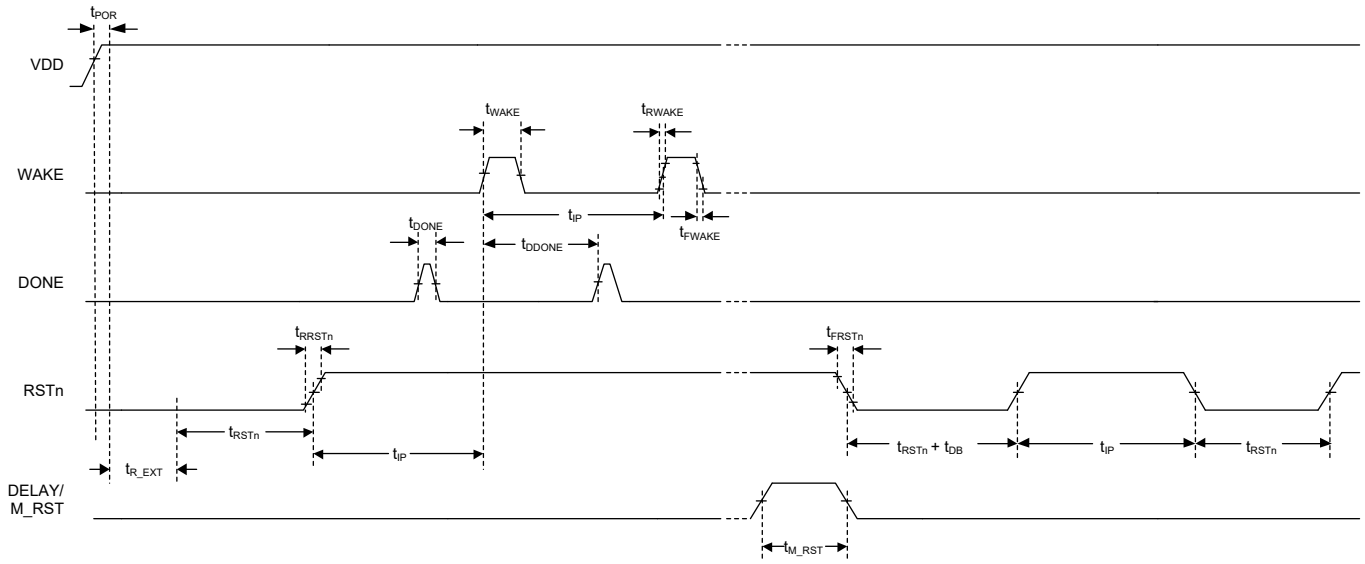
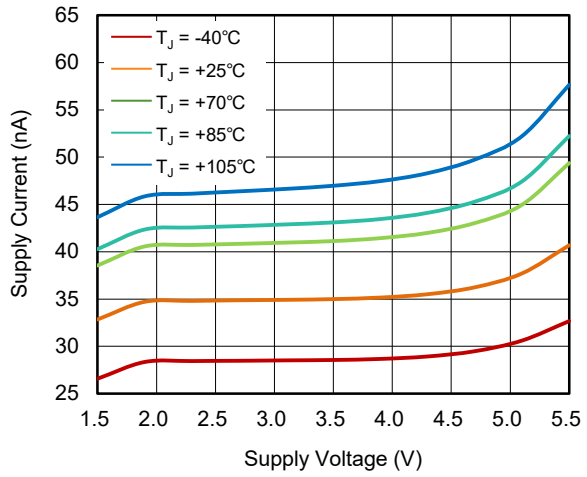


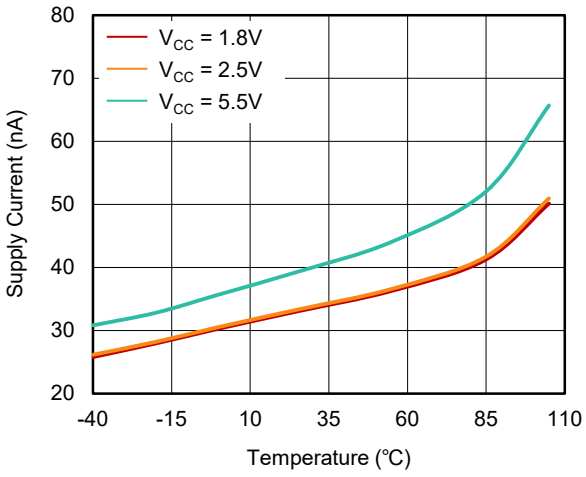
Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

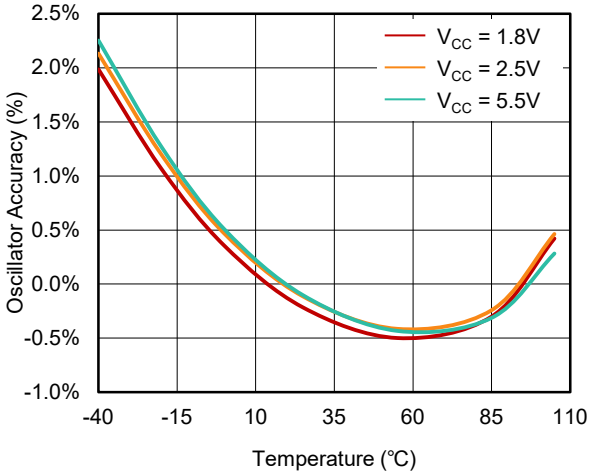
Supply Current vs. Supply Voltage



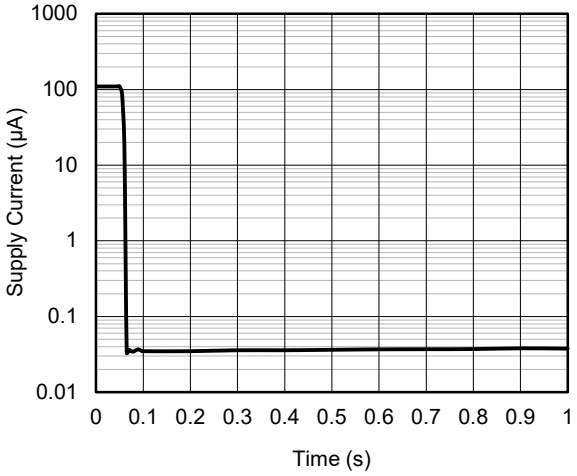
Supply Current vs. Temperature



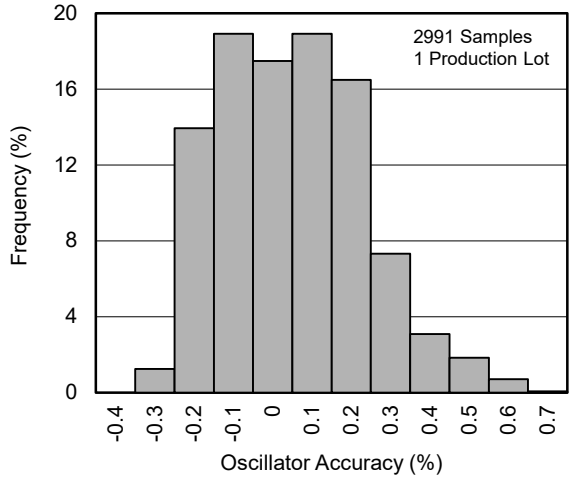
Oscillator Accuracy vs. Temperature



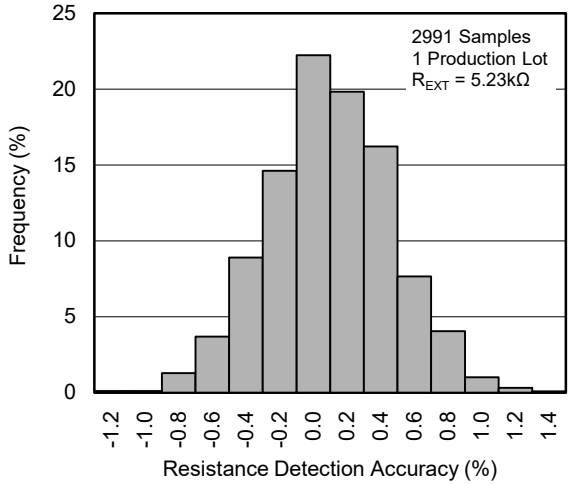
Supply Current vs. Time



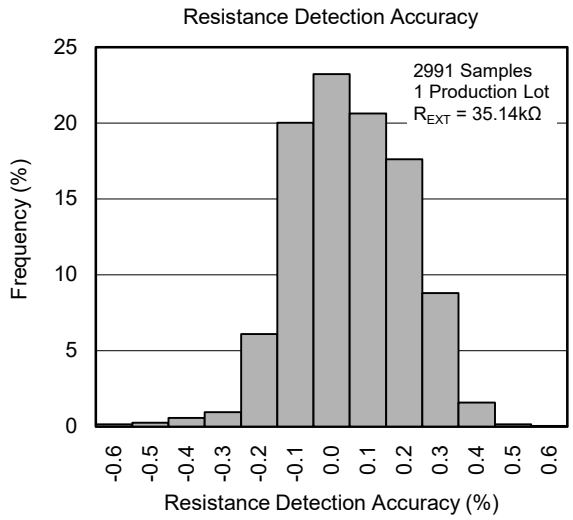
Oscillator Accuracy

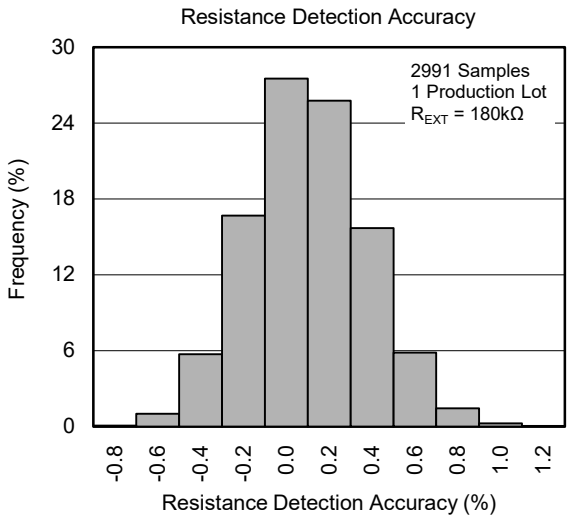


Resistance Detection Accuracy



TYPICAL PERFORMANCE CHARACTERISTICS (continued)





FUNCTIONAL BLOCK DIAGRAM

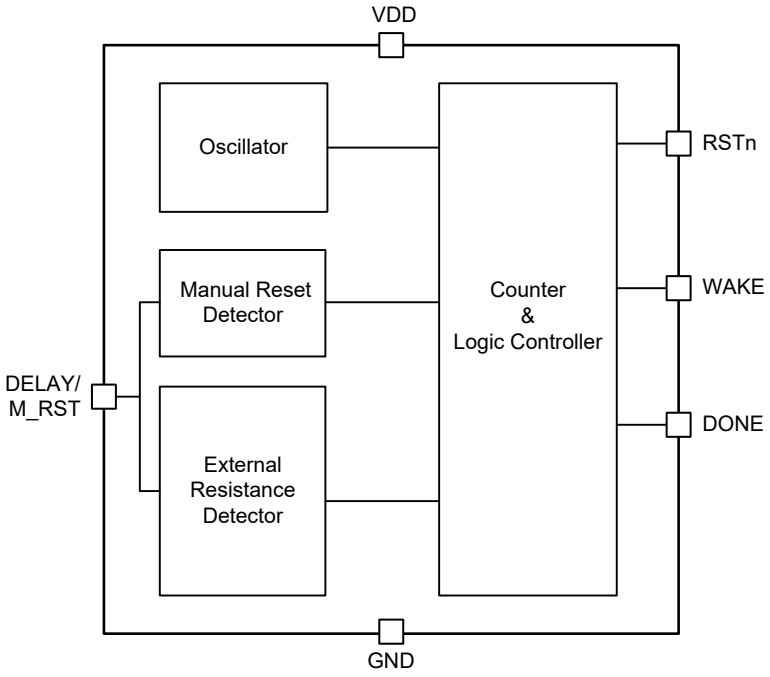


Figure 3. Functional Block Diagram

DETAILED DESCRIPTION

The SGM821 is a programmable wake-up watchdog timer with ultra-low power consumption. Besides, it provides a wide range of timing selections from 100ms to 8200s (TYP), which is ideal for most applications driven by interrupt.

At startup, the SGM821 sets the interrupt time interval by detecting the resistance of the external resistor connected between DELAY/M_RST pin and GND one time. After that, the resistance detection is disabled, and the watchdog function of SGM821 is realized through three pins: DONE, WAKE and RSTn. The SGM821 issues a programmed periodic WAKE pulse to a μC which is in sleeping or standby mode. And the μC must issue a DONE signal to the SGM821 within 20ms before the end of the current interrupt time interval. If a valid DONE is received, the SGM821 will issue a WAKE pulse at the beginning of next period. Otherwise, the RSTn signal will be asserted to reset the μC. Besides, the manual reset function is also supported by pulling the DELAY/M_RST pin to VDD.

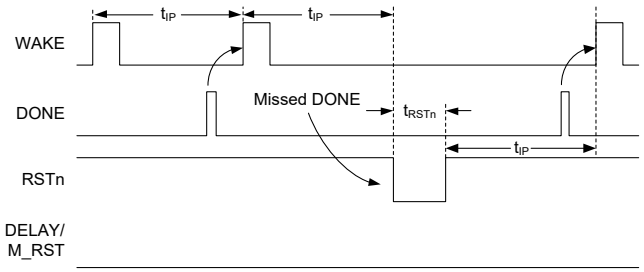


Figure 4. Watchdog

WAKE

The WAKE is an output signal that is normally low most of the time. When the programmed time interval starts, the SGM821 will sent out a WAKE pulse if a valid DONE has been received in the previous time interval. If DONE is not recognized in the previous time interval, the RSTn will assert and WAKE pulse will not be generated. At the beginning of the first cycle or after RSTn is deasserted, WAKE will not be generated and the SGM821 is waiting for a valid DONE in this new cycle. If a valid DONE is recognized, WAKE will be generated in the next time interval. Otherwise, RSTn will assert again.

DONE

The DONE is an input logic pin, and it is not allowed to be floating. After processing the WAKE signal successfully, the μC should give a positive DONE pulse. And the SGM821 will recognize the rising edge of the DONE pulse. It is recommended to set the pulse width larger than 100ns. Besides, the SGM821 only recognizes the first DONE signal when multiple DONE signals are sent within one time interval. Note that the DONE signal will not be recognized in the last 20ms of the current time interval.

If a valid DONE signal is recognized during the WAKE is still high, the WAKE will falls down as soon as possible.

RSTn

The SGM821 provides an open-drain output pin (RSTn) to meet different μC input voltage requirements. Therefore, a pull-up resistor is required to implement the reset interface between the SGM821 and the μC. To minimize current consumption, a 100kΩ pull-up resistor is recommended.

The RSTn signal keeps low during the POR and the reading of the R_{EXT}. After that, the SGM821 asserts periodic WAKE pulses in response to valid DONE pulses during normal operating mode. And RSTn will be triggered to be low in either of the following two cases:

1. If the DELAY/M_RST pin keeps high for at least 20ms (TYP) as a valid manual reset signal.

2. If the DONE is not received at least 20ms before the next WAKE rising edge (see Figure 4).

DETAILED DESCRIPTION (continued)

Startup and External Resistance Detection

At startup, the SGM821 set the time interval between two adjacent WAKE pulses (rising edges) by detecting the resistance of the external resistor (R_{EXT}) connected between DELAY/M_RST pin and GND one time. After that, the resistance detection is disabled unless the chip is restarted and powered on again. During this measurement time, the external resistance detection block is temporarily working, so the power consumption of the chip is temporarily high. After detecting, the external resistance detection block is powered off, the power consumption goes down. A counter starts working after POR, and it is timeout after t_{R_EXT} (100ms, TYP), which indicates the end of external resistance reading time. The power consumption of the chip during the resistance reading time is related to the external resistance, the smaller the resistance, the greater the power consumption. After the external resistance reading time (t_{R_EXT}), RSTn remains low for 320ms (TYP) and then goes high. After that, the SGM821 entering the normal operating mode. See Figure 5.

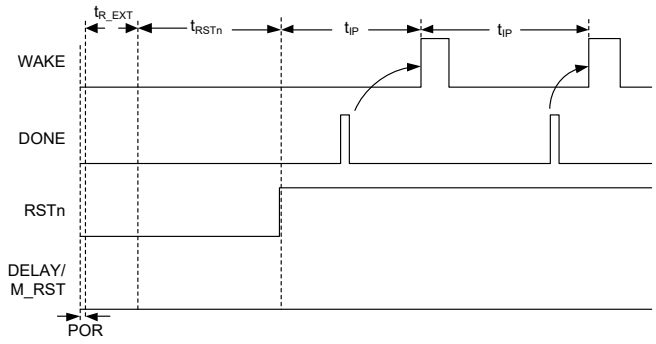


Figure 5. Startup

The recognizable range of external resistance is from 500Ω to 180kΩ. It is not allowed to connect a capacitance to DELAY/M_RST pin. And it is also recommended that the trace between the resistor on DELAY/M_RST pin and GND is as short as possible. Besides, other interfering signal should be kept far away for good detection. Section Time Interval Period Programming through External Resistance gives more information about the calculation of time interval configuration, and Section Time Interval Period Setting Error gives examples about the calculation of setting errors.

Manual Reset

DELAY/M_RST is a multiplex pin. After the POR and during the reading time of the external resistance, the resistance detection block is connected. And both of the resistance detection and manual reset function are enabled. After the reading of the external resistance, the resistance detection block is disabled, and DELAY/M_RST is only used as manual reset pin. The SGM821 provides a manual reset function with a de-bounce feature that is insensitive to the glitches on the DELAY/M_RST pin. If DELAY/M_RST is connected to VDD for at least t_{M_RST} (20ms, TYP), the SGM821 recognizes it as a manual reset condition. After that, the RSTn is asserted and remains low for t_{DB} + t_{RSTn}. The digital low status of the RSTn signal may be affected by an uncertainty of about ±5ms due to the asynchronous nature of the manual reset signal. And WAKE keeps low when RSTn is asserted.

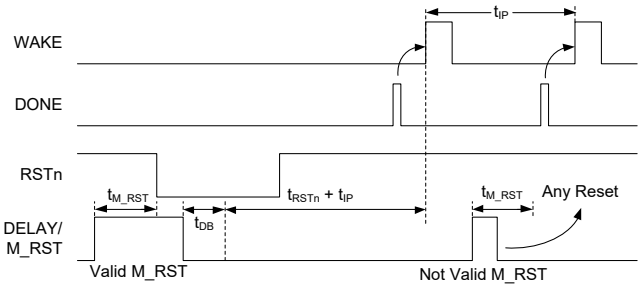


Figure 6. Manual Reset

DETAILED DESCRIPTION (continued)

Time Interval Period Programming through External Resistance

To set the time interval below 1 second, the external resistance R_{EXT} is selected according to Table 1.

Table 1. First 9 Time Intervals

t_{IP} (ms)	Resistance (kΩ)
100	0.5
200	1
300	1.5
400	2
500	2.5
600	3
700	3.5
800	4
900	4.5

To set the time interval over 1 second, the external resistance R_{EXT} is selected according to Equation 1.

$$R_{EXT} = 5.2 \times T^{0.3932} \quad (1)$$

Users can also calculate the time interval period through Equation 2 (the inverse function of Equation 1).

$$T = 0.0153 \times R_{EXT}{}^{2.543} \quad (2)$$

where:
T is the desired time interval in seconds,
R_{EXT} is the resistance value in kΩ.

Figure 9 is provided to facilitate customers to estimate the R_{EXT}.

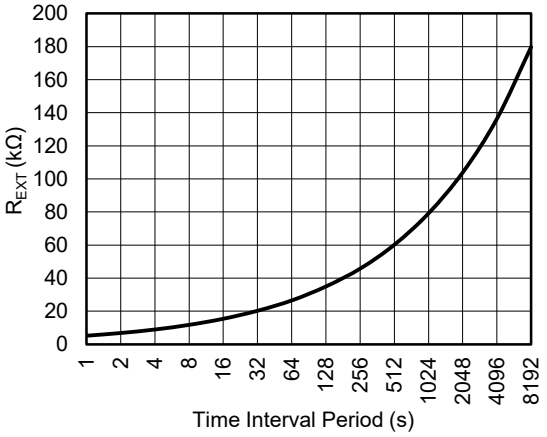


Figure 7. R_{EXT} vs. Time Interval Period

Time Interval Period Setting Error

The error of time interval period mainly consists of the following two parts: internal oscillator accuracy error and resistance detection error. It should be pointed out that this interval period setting error caused by the chip is discussed here, excluding the error caused by the external resistance. In order to reduce the error caused by external resistance, users should use high-precision resistance as much as possible. The examples below illustrate the procedure.

Example 1:
V_{CC} = 2.5V, T_J = +25℃, and the target time interval $t_{TARGET1}$ = 500ms. The required R_{EXT} is selected as 2.5kΩ according to Table 1.

Because the first 9 intervals are discrete intervals by multiples of 100ms, the resistance detecting tolerance is wide and can be neglect. The oscillator accuracy is ±1.1% (If reliability drift is included, the accuracy is 2.1%), So when R_{EXT} = 0.5kΩ, the actual time interval is:

$$500 \times (1-1.1\%) \le t_{IP}(ms) \le 500 \times (1+1.1\%)$$
$$494.5 \le t_{IP}(ms) \le 505.5 \quad (3)$$

Example 2：
V_{CC} = 2.5V, T_J = +25℃, and the target time interval $T_{TARGET2}$ = 120s. The required R_{EXT} is calculated as 34kΩ according to Equation 1.

The resistance detection accuracy according to the Electrical Characteristics table is ±2.3% approximately (If reliability drift is included, the accuracy is 4.3%), the approximate t_{IP} range excluding oscillator accuracy is:

$$0.0153 \times \left[34 \times (1-2.3\%)\right]^{2.543} \le t_{IP}(s)$$
$$\le 0.0153 \times \left[34 \times (1+2.3\%)\right]^{2.543}$$
$$113.1 \le t_{IP}(s) \le 127.2 \quad (4)$$

The oscillator accuracy is ±1.1%, so the final approximate t_{IP} range is:

$$113.1 \times (1-1.1\%) \le t_{IP}(s) \le 127.2 \times (1+1.1\%)$$
$$111.8 \le t_{IP}(s) \le 128.6 \quad (5)$$

APPLICATION INFORMATION

Power Supply Recommendations

The SGM821 requires a voltage supply within 1.8V and 5.5V. To immune the power supply noise, an RC low-pass filter is strongly recommended as Figure 1 shows. The recommended resistance value is 10Ω, and the ceramic X7R capacitor value is 1μF.

Layout

Because of the DELAY/M_RST pin is sensitive to parasitic capacitance when detecting the resistance, it is recommended that the trace between external resistor on the pin and GND track is as short as possible. To improve signal integrity on the WAKE and RSTn pins, it is also suggested to keep the trace length between the SGM821 and the μC short.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2025 – REV.A.2 to REV.A.3	**Page**
Updated Time Interval Period Setting Error section	10

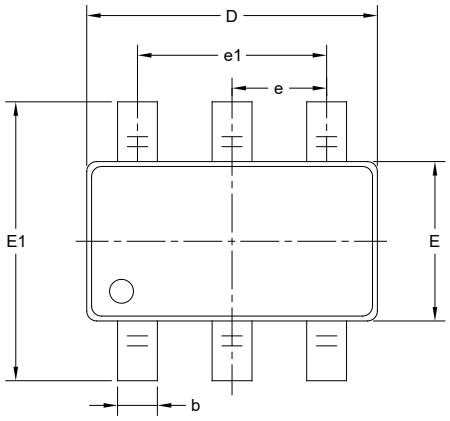
AUGUST 2024 – REV.A.1 to REV.A.2	**Page**
Updated Time Interval Period Programming through External Resistance section	10

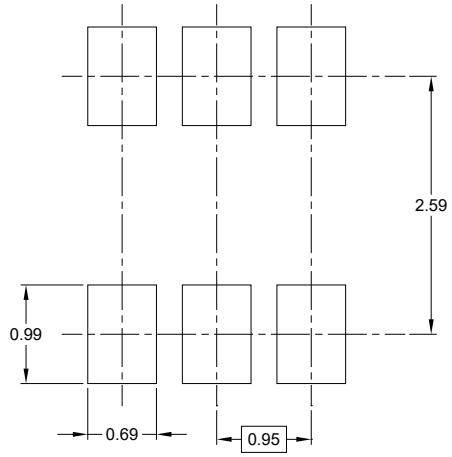
DECEMBER 2023 – REV.A to REV.A.1	**Page**
Changed Time Interval Period Setting Error section	10

Changes from Original (APRIL 2022) to REV.A	**Page**
Changed from product preview to production data	All

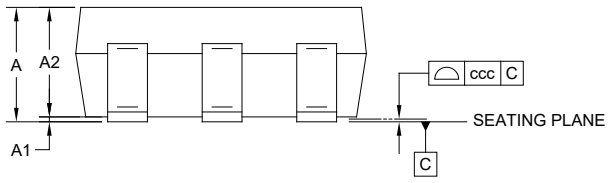
PACKAGE OUTLINE DIMENSIONS

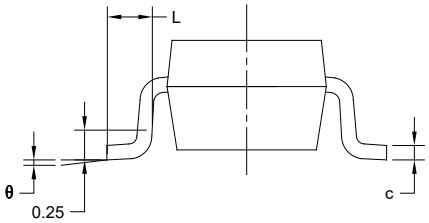
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



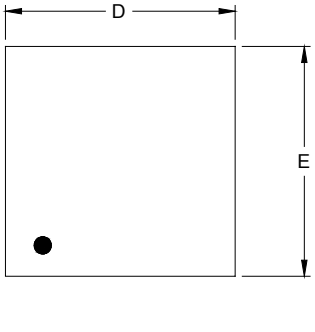


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

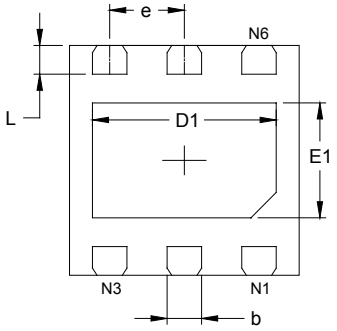
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

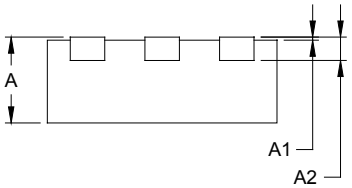
TDFN-2×2-6AL



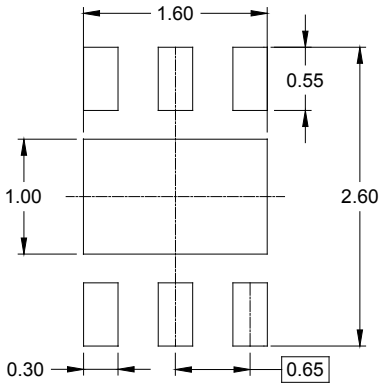
TOP VIEW



BOTTOM VIEW



SIDE VIEW

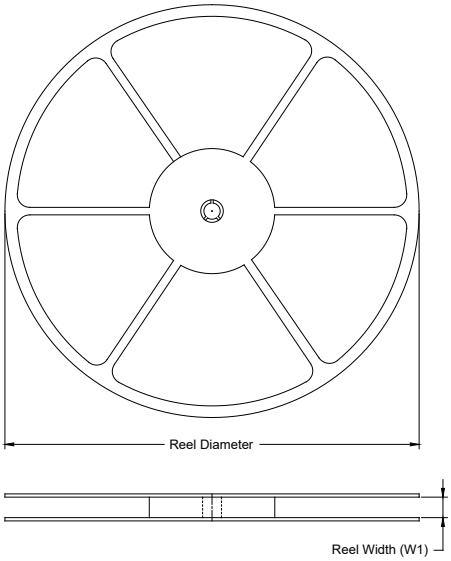


RECOMMENDED LAND PATTERN (Unit: mm)

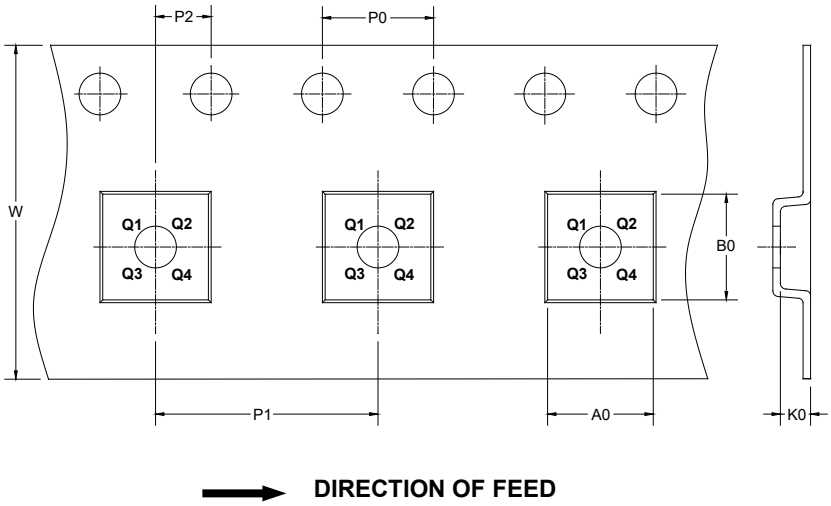
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



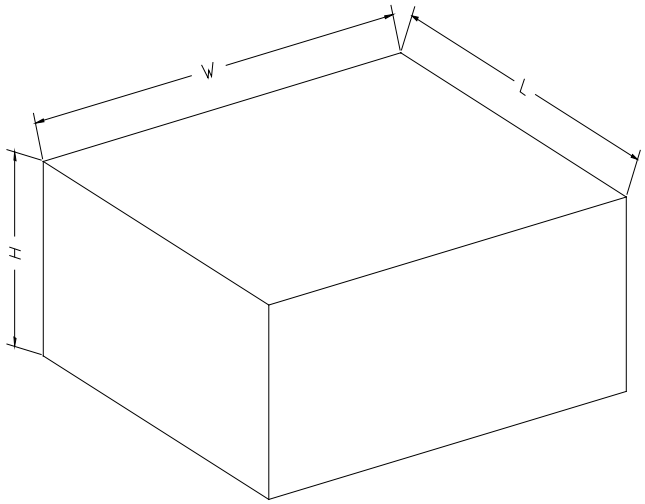
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002