74LV541AT Octal Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The 74LV541AT is an octal buffer/line driver with 3-state outputs, which can accept supply voltage range from 4.5V to 5.5V. The device is the best choice for driving bus lines or buffer memory address registers. The inputs and outputs are placed on opposite sides of the package, making it easier to print circuit board layout. The inputs are compatible with TTL voltage that enables them to be connected to bipolar outputs and 3.3V devices. In addition, the device can support translating from 3.3V to 5V voltage.

The device features 3-state control gate consisting of a two-input AND gate with active-low inputs. $\overline{OE}1$ and $\overline{OE}2$ are two output enable inputs. When $\overline{OE}1$ and $\overline{OE}2$ are low, data transmits from An inputs to the Yn outputs. When $\overline{OE}1$ or $\overline{OE}2$ is high, all outputs are in high-impedance state.

This device is highly suitable for partial power-down applications by using power-off leakage current (I_{OFF}) circuit. When the device is powered down, the outputs are disabled, and the current backflow can be prevented from passing through the device.

The 74LV541AT is available in Green TSSOP-20 and TQFN-3.5×4.5-20AL packages. It operates over an operating temperature range of -40°C to +125°C.

FUNCTION TABLE

	OUTPUT		
OE1	OE2	An	Yn
L	L	L	L
L	L	Н	Н
Н	X	X	Z
X	Н	X	Z

H = High Voltage Level

L = Low Voltage Level

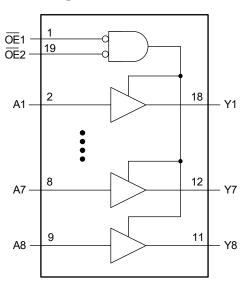
Z = High-Impedance State

X = Don't Care

FEATURES

- Supply Voltage Range: 4.5V to 5.5V
- Inputs Accept Voltages Higher than the Supply Voltage and up to 5.5V
- +16mA/-16mA Output Current
- Inputs are Compatible with TTL-Voltage
- All Ports Support Mixed-Mode Voltage Operation
- Support Partial Power-Down Mode
- -40°C to +125°C Operating Temperature Range
- Available in Green TSSOP-20 and TQFN-3.5×4.5-20AL Packages

LOGIC DIAGRAM

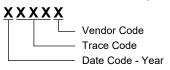


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LV541AT	TSSOP-20	-40°C to +125°C	74LV541ATXTS20G/TR	178XTS20 XXXXX	Tape and Reel, 4000
74LV54TAT	TQFN-3.5×4.5-20AL	-40°C to +125°C	74LV541ATXTVL20G/TR	177 XTVL20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} 0.5V to 7V
Input Voltage Range, V _I ⁽¹⁾ 0.5V to 7V
Output Voltage Range, V _O ⁽¹⁾
High-State or Low-State0.5V to MIN(7V, V _{CC} + 0.5V)
3-State or Power-Down Mode0.5V to 7V
Input Clamp Current, $I_{IK}(V_I < 0V)$ 20mA
Output Clamp Current, I _{OK} (V _O < 0V)50mA
Continuous Output Current, $I_O(V_O = 0V \text{ to } V_{CC})$ $\pm 35 \text{mA}$
Continuous Current through V _{CC} or GND±70mA
Junction Temperature ⁽²⁾ +150°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10s)+260°C
ESD Susceptibility (3) (4)
HBM±2000V
CDM±1000V

NOTES:

- 1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
- 3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
- 4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.
- 5. Unused input pins must be held at V_{CC} or GND to guarantee the device in normal operation.

RECOMMENDED OPERATING CONDITIONS

Operating Supply Voltage Range, V _{CC}	4.5V to 5.5V
Input Voltage Range, V _I ⁽⁵⁾	0V to 5.5V
Output Voltage Range, Vo	
High-State or Low-State	0V to V _{CC}
3-State or Power-Down Mode	0V to 5.5V
Output Current, Io	±16mA
Input Transition Rise or Fall Rate, $\Delta t/\Delta V$	
V _{CC} = 4.5V to 5.5V	20ns/V (MAX)
Operating Temperature Range	40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

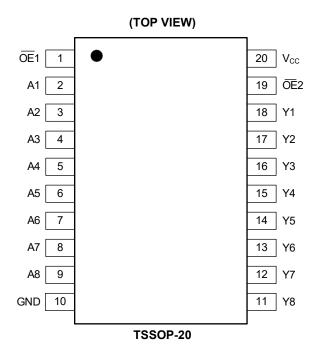
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

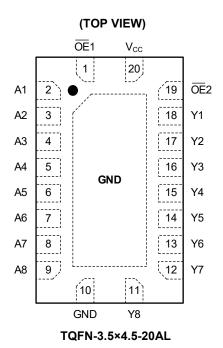
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.



PIN CONFIGURATIONS





PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 19	ŌĒ1, ŌĒ2	Output Enable Inputs (Active-Low).
2, 3, 4, 5, 6, 7, 8, 9	A1, A2, A3, A4, A5, A6, A7, A8	Data Inputs.
18, 17, 16, 15, 14, 13, 12, 11	Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8	Data Outputs.
10	GND	Ground.
20	V _{CC}	Supply Voltage.
Exposed Pad	GND	Connect it to GND internally. This pad is not an electrical connection point. TQFN-3.5×4.5-20AL package only.

ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS	
High-Level Input Voltage	V _{IH}	V _{CC} = 4.5V to 5.5V	Full	2			V	
Low-Level Input Voltage	V _{IL}	V _{CC} = 4.5V to 5.5V	Full			0.8	V	
High-Level Output Voltage	V _{OH}	V _{CC} = 4.5V, I _{OH} = -50μA	Full	4.4	4.49		V	
High-Level Output Voltage	V OH	V _{CC} = 4.5V, I _{OH} = -16mA	Full	3.8	4.27		V	
Low Lovel Output Voltage	Vol	$V_{CC} = 4.5V, I_{OL} = 50\mu A$	Full		0.01	0.1	V	
Low-Level Output Voltage V _{OL}		V _{CC} = 4.5V, I _{OL} = 16mA	Full		0.24	0.55		
Input Leakage Current	l _l	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	Full		±0.01	±1	μA	
Off-State Output Current	l _{OZ}	V_{CC} = 5.5V, V_{O} = V_{CC} or GND	Full		±0.01	±5	μA	
Power-Off Leakage Current	I _{OFF}	$V_{CC} = 0V$, V_I or $V_O = 0V$ to 5.5V	Full		±0.01	±5	μA	
Supply Current	I _{cc}	$V_{CC} = 5.5V$, $V_I = V_{CC}$ or GND, $I_O = 0A$	Full		0.06	20	μA	
Additional Supply Current	ΔI _{CC}	V_{CC} = 5.5V, one input at 3.4V, other inputs at V_{CC} or GND	Full		0.04	1.5	mA	
Input Capacitance	Cı	$V_{I} = V_{CC}$ or GND	+25°C		4		pF	

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40°C to +125°C, all typical values are measured at T_A = +25°C, V_{CC} = 5V ± 0.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Dranagation Dalay (2)	4	An to Yn	C _L = 15pF	Full	0.5	5.5	8.7	200
Propagation Delay (2)	t _{PD}	An to th	C _L = 50pF	Full	0.5	6.0	9.8	ns
Enable Time (2)		OF: As Vis	C _L = 15pF	Full	0.5	7.5	11.7	
Enable Time Y	t _{EN}	OEn to Yn	C _L = 50pF	Full	0.5	8.0	13.4	ns
Disable Time (2)		OF: As Vis	C _L = 15pF	Full	0.5	5.5	8.9	
Disable Time (2)	t _{DIS}	OEn to Yn	C _L = 50pF	Full	1.0	7.5	11.0	ns
Channel-to-Channel Skew Time	t _{sko}			+25°C		160		ns
Power Dissipation Capacitance (3)	C_PD	Outputs enabled	, C _L = 50pF, f = 10MHz	+25°C		14		pF

NOTES:

- 1. Specified by design and characterization, not production tested.
- 2. t_{PD} is the same as t_{PLH} and t_{PHL} , t_{DIS} is the same as t_{PLZ} and t_{PHZ} , t_{EN} is the same as t_{PZL} and t_{PZH} .
- 3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$

where:

 f_i = input frequency in MHz.

f_o = output frequency in MHz.

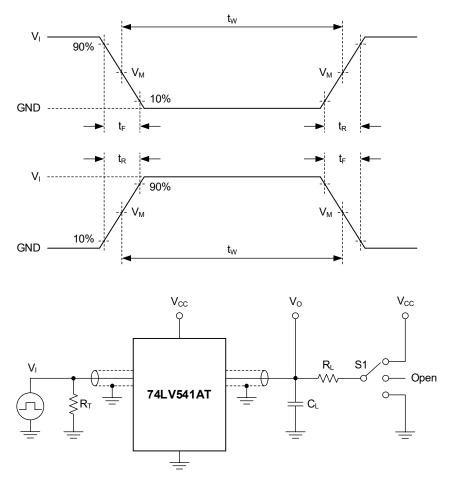
C_L = output load capacitance in pF.

V_{CC} = supply voltage in Volts.

N = number of inputs switching.

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

 R_T : Termination resistance (equals to output impedance Z_0 of the pulse generator).

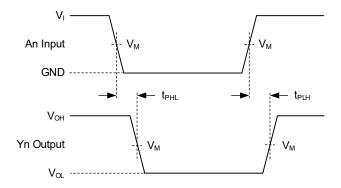
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INF	TUT	LO	AD		S1 POSITION	
V _{cc}	Vı	t _R , t _F	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
4.5V to 5.5V	V _{CC}	≤ 2.5ns	15pF, 50pF	1kΩ	Open	V _{CC}	GND

WAVEFORMS

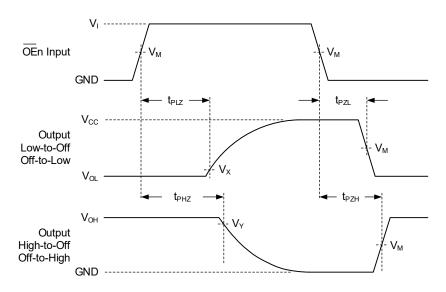


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (An) to Output (Yn) Propagation Delay Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE				OUTPUT	
V _{CC}	Vı	V _M ⁽¹⁾	V _M	V _X	V _Y
4.5V to 5.5V	V _{cc}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.3V	V _{OH} - 0.3V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

74LV541AT

Octal Buffer/Line Driver with 3-State Outputs

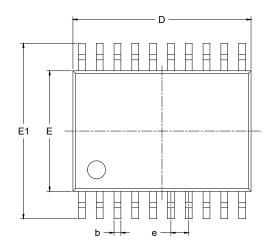
REVISION HISTORY

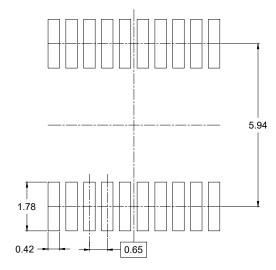
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2024) to REV.A

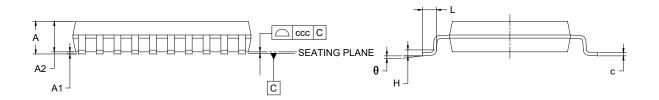
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PACKAGE OUTLINE DIMENSIONS TSSOP-20





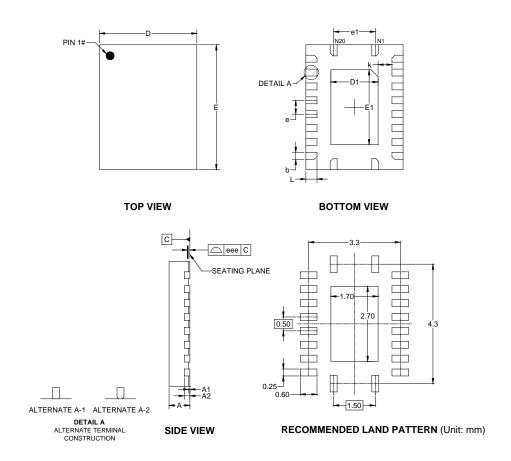
RECOMMENDED LAND PATTERN (Unit: mm)



Cymahal	Dimensions In Millimeters					
Symbol	MIN	NOM	MAX			
Α	-	-	1.200			
A1	0.050	-	0.150			
A2	0.800	-	1.050			
b	0.190	-	0.300			
С	0.090	-	0.200			
D	6.400	-	6.600			
E	4.300	-	4.500			
E1	6.200 - 6.600					
е	0.650 BSC					
L	0.450	-	0.750			
Н	0.250 TYP					
θ	0°	-	8°			
ccc		0.100				

- 1. Body dimensions do not include mode flash or protrusion.
- This drawing is subject to change without notice.
 Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS TQFN-3.5×4.5-20AL



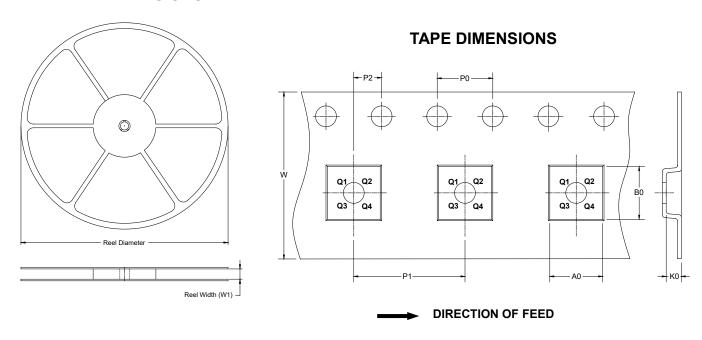
Comple of	Dimensions In Millimeters					
Symbol	MIN	NOM	MAX			
А	0.700	-	0.800			
A1	0.000	-	0.050			
A2	0.203 REF					
b	0.200	-	0.300			
D	3.400	-	3.600			
D1	1.600	-	1.800			
Е	4.400	-	4.600			
E1	2.600 - 2.800					
е	0.500 BSC					
e1	1.500 BSC					
L	0.300	-	0.500			
k	0.500 REF					
eee		0.080				

NOTE: This drawing is subject to change without notice.



TAPE AND REEL INFORMATION

REEL DIMENSIONS

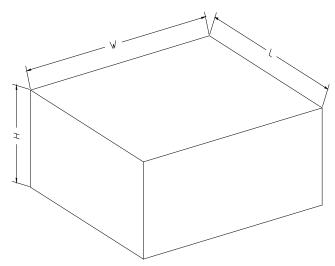


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20	13"	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1
TQFN-3.5×4.5-20AL	13"	12.4	3.80	4.80	1.10	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
13″	386	280	370	5	DD0002