SGM42685
45V, 1.5A Stepper Driver with Integrated Current Sense, 1/256 Microstepping and Advance Decay Mode

GENERAL DESCRIPTION

The SGM42685 is a stepper motor driver with power supply voltage up to 45V, available for various applications such as consumer, industrial, and medical equipment. Due to the fully integrated of power MOSFETs and current sense circuits, as well as the implementation of microstepping indexer and current regulator internally, only a small number of peripheral circuits are required to drive a stepper motor. The SGM42685 provides peak current driving capabilities of 1.5A.

The SGM42685 adopts a built-in current sense architecture, which ensures high current accuracy while eliminating external sampling resistors. The integrated indexer can reach up to 256 micro-steps, so as to achieve smooth and low noise driving effects. In addition to the traditional slow and mixed decay modes, the internal current regulator offers advanced smart tune ripple control to achieve smaller current ripple.

Universal STEP, DIR, and ENABLE interfaces are provided to control the motion of the stepper motor. By pulling down the nSLEEP pin, the driver can enter sleep mode to obtain ultra-low standby current. Protection functions are integrated such as under-voltage, short-circuit, over-current, and over-temperature, which is indicated through the nFAULT pin.

The SGM42685 is available in a Green TSSOP-24 (Exposed Pad) package.

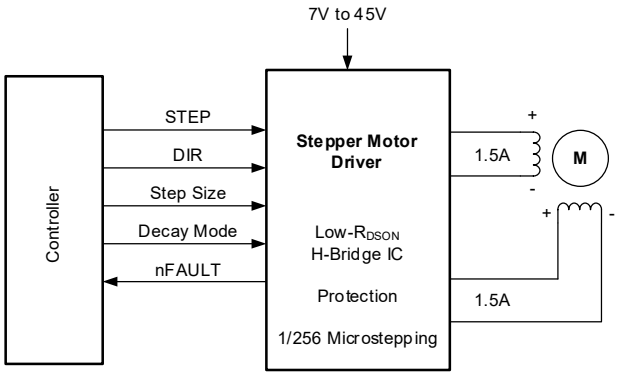
APPLICATIONS

ATMs
3D/Laser Beam Printers
Stage Lighting Equipment
Multi-Function Printers/Scanners
Textile and Sewing Machines
Office and Home Automation
Factory Automation and Robotics

FEATURES

- **Fully Integrated Stepper Motor Driver**
  - **Two Power MOSFET H-Bridge**
  - **Internal Current Sense Circuit**
- **Up to 1/256 Microstepping Indexer**
- **Slow, Mixed, Smart Tune Ripple Control**
- **Operating Supply Voltage Range: 7V to 45V**
- **Low On-Resistance: 900mΩ HS + LS at 24V, +25℃**
- **High Current Capacity for each Winding**
  - **1.5A Full-Scale, 1A RMS Output**
- **Configurable Current Scale through TRQ Pin**
  - **100%, 75%, 50%**
- **Support 1.8V, 3.3V, 5.0V Logic Inputs**
- **Low Current Sleep Mode: 1μA (TYP)**
- **Protection Features**
  - **VM Under-Voltage Lockout (UVLO)**
  - **Charge Pump Under-Voltage (CPUV)**
  - **Over-Current Protection (OCP)**
  - **Thermal Shutdown (TSD)**
  - **Fault Condition Output (nFAULT)**
- **Available in a Green TSSOP-24 (Exposed Pad) Package**

SIMPLIFIED SCHEMATIC

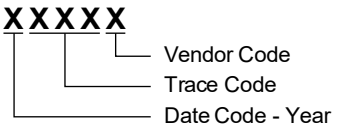


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42685	TSSOP-24 (Exposed Pad)	-40℃ to +125℃	SGM42685XPTS24G/TR	SGM42685 XPTS24 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_M ..... -0.3V to 50V
Charge Pump Voltage, VCP, CPH..... -0.3V to V_M + 5.5V
Charge Pump Negative Switching Pin, CPL ..... -0.3V to 5.5V
Internal Regulator Voltage, DVDD ..... -0.3V to 5.5V
Control Pin Voltage, ENABLE, STEP, DIR, nFAULT, DECAY, M0, M1, TRQ, nSLEEP..... -0.3V to 5.5V
nFAULT Open-Drain Output Current .....0mA to 10mA
Current Limit Input Pin Voltage, RREF ..... -0.3V to 6V
Phase Node Voltage (Continuous), AOUT1, AOUT2, BOUT1, BOUT2..... -0.7V to V_M + 0.7V
Package Thermal Resistance
TSSOP-24 (Exposed Pad), θ_{JA} ..... 28.4℃/W
TSSOP-24 (Exposed Pad), θ_{JB} ..... 9.1℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (TOP)}$ ..... 22℃/W
TSSOP-24 (Exposed Pad), $\theta_{JC\ (BOT)}$ ..... 1.8℃/W
Junction Temperature .....+150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage for Normal (DC) Operation, V_M ..... 7V to 45V
Logic-Level Input Voltage, V_I ..... 0V to 5.3V
Applied Step Signal (STEP), f_{PWM}.....0kHz to 400kHz
Motor Full-Scale Current, I_{MAX} ..... 0A to 1.5A
Motor RMS Current, I_{RMS} ..... 0A to 1A
Operating Ambient Temperature Range ..... -40℃ to +125℃
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

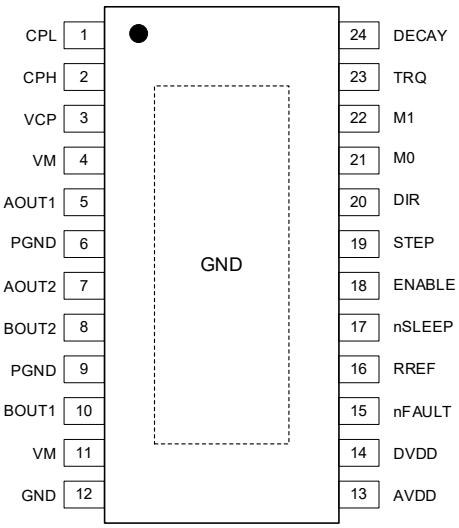
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-24 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	CPL	Charge Pump Flying Capacitor. An X7R, 0.022μF capacitor is used between CPH and CPL pins.
2	CPH	
3	VCP	Gate Drive Voltage of the High-side Switches. Decouple with a 0.22μF ceramic capacitor to VM pin.
4, 11	VM	Power Supply Pin. Connect to the motor power supply (7V to 45V).
5	AOUT1	Bridge A Output 1.
6, 9	PGND	Power Ground.
7	AOUT2	Bridge A Output 2.
8	BOUT2	Bridge B Output 2.
10	BOUT1	Bridge B Output 1.
12	GND	Ground Reference.
13	AVDD	Internal Regulator. Bypass to GND with an X5R or X7R, 0.47μF, 6.3V ceramic capacitor.
14	DVDD	Logic Supply Voltage. Connect an X7R, 0.47μF to 1μF, 6.3V or 10V rated ceramic capacitor to GND.
15	nFAULT	Fault Indication. Pulled logic low with fault condition, open-drain output requires an external pull-up resistor.
16	RREF	Current Limit Analog Input. Connect resistor to ground to set full-scale regulation current.
17	nSLEEP	Sleep Mode Input. Active-low sleep mode logic input with weak internal pull-down. Apply high to enable device, and low to enter in the low-power sleep mode.
18	ENABLE	Enable Pin. Active-high enable logic input with internal pull-down resistor.
19	STEP	Step Logic Input. Rising edge causes the microstepping indexer to move one step. It has a weak internal pull-down.
20	DIR	Direction Input Pin. Control the direction of stepping. It has a weak internal pull-down.
21	M0	Micro-Step Mode Selection Logic Input. M0 and M1 are logic inputs to set the step size. It has a weak internal pull-down and an internal pull-up to DVDD.
22	M1	
23	TRQ	Current-Scaling Control. Scale the output current tri-level. It has a weak internal pull-down and an internal pull-up to DVDD.
24	DECAY	Decay Mode Select. It has an internal pull-up to DVDD.
Exposed Pad	GND	Thermal Pad. Connect to system ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_M = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies (VM, DVDD, AVDD)						
Motor Power Supply Voltage	V_M	Normal (DC) operation	7		45	V
VM Operating Supply Current	I_{VM}	ENABLE = high, nSLEEP = high, no motor load		6.5	10	mA
VM Sleep Mode Supply Current	I_{VMQ}	nSLEEP = low		1	10	μA
Time to Enter Sleep Mode	t_{SLEEP}	nSLEEP = low to sleep mode	130			μs
Wake-Up Time	t_{WAKE}	nSLEEP = high to output transition		1	1.3	ms
Turn-On Time	t_{ON}	$V_M > V_{UVLO}$ to output transition		1	1.3	ms
Internal Regulator Voltage	V_{DVDD}	No external load	4.7	5	5.2	V
	V_{AVDD}	No external load	4.7	5	5.2	V
Charge Pump (VCP, CPH, CPL)						
CP Operating Voltage	V_{CP}			V_M + 4.5		V
Charge Pump Switching Frequency	f_{CP}	$V_M > V_{UVLO}$, nSLEEP = high		155		kHz
Logic-Level Inputs (STEP, DIR, ENABLE, nSLEEP)						
Input Logic-Low Voltage	V_{IL}		0		0.4	V
Input Logic-High Voltage	V_{IH}		1.6		5.3	V
Input Hysteresis	V_{HYS}			150		mV
Input Low Current	I_{IL}	V_{IN} = 0V	-1		1	μA
Input High Current	I_{IH}	V_{IN} = 5V			100	μA
Tri-Level Inputs (M0, TRQ)						
Input Logic-Low Voltage	V_{I1}	Tied to GND	0		0.5	V
Input Hi-Z Voltage	V_{I2}	Hi-Z		1		V
Input Logic-High Voltage	V_{I3}	Tied to DVDD	1.8		5.3	V
Output Pull-Up Current	I_O			10		μA
Quad-Level Inputs (M1)						
Input Logic-Low Voltage	V_{I1}	Tied to GND	0		0.5	V
	V_{I2}	330kΩ ± 5% to GND		1.1		V
Input Hi-Z Voltage	V_{I3}	Hi-Z		1.8		V
Input Logic-High Voltage	V_{I4}	Tied to DVDD	3		5.3	V
Output Pull-Up Current	I_{IL}			10		μA
Multi-Level Inputs (DECAY)						
Multi-Level Input Voltage	V_{I1}	Tied to GND, initial accuracy, T_J = +25℃	0		0.12	V
	V_{I2}	Can set with 1% 15kΩ to GND, initial accuracy, T_J = +25℃	0.22		0.4	V
	V_{I3}	Can set with 1% 45kΩ to GND, initial accuracy, T_J = +25℃	0.65		1.04	V
	V_{I4}	Can set with 1% 80kΩ to GND, initial accuracy, T_J = +25℃	1.48		1.55	V
	V_{I5}	Tied to DVDD, initial accuracy, T_J = +25℃	3		5.3	V
Control Outputs (nFAULT)						
Output Low Voltage	V_{OL}	I_O = 5mA			0.5	V
Output High Leakage	I_{OH}	V_M = 24V	-1		1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are at T_J = +25℃, V_M = 24V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Motor Driver Outputs (xOUTx)						
High-side FET On-Resistance	R_{DSON_H}	V_M = 24V, I_O = 0.5A		450	800	mΩ
Low-side FET On-Resistance	R_{DSON_L}	V_M = 24V, I_O = 0.5A		450	800	mΩ
Output Rise Time	t_R	V_M = 24V, I_O = 0.5A, between 10% and 90%		20		ns
PWM Current Control (RREF)						
RREF Transimpedance Gain	A_{RREF}			30		kAΩ
RREF Voltage	V_{RREF}	R_{REF} = 18kΩ to 132kΩ	1.162	1.232	1.273	V
PWM Off-Time	t_{OFF}			24		μs
Equivalent Capacitance on RREF	C_{RREF}				10	pF
PWM Blanking Time	t_{BLANK}			2		μs
Current Trip Accuracy	ΔI_{TRIP}	I_{RREF} = 1.5A, 1% reference resistor, 10% to 20% current setting, T_J = +25℃	-20%		20%	
		I_{RREF} = 1.5A, 1% reference resistor, 20% to 63% current setting, T_J = +25℃	-12.5%		12.5%	
		I_{RREF} = 1.5A, 1% reference resistor, 71% to 100% current setting, T_J = +25℃	-7.5%		7.5%	
Protection Circuits						
VM UVLO Lockout	V_{UVLO}	Falling	5.6	5.9	6.1	V
		Rising	6.2	6.5	6.7	
Under-Voltage Hysteresis	V_{UVLO_HYS}			600		mV
Charge Pump Under-Voltage	V_{CPUV}	VCP falling, CPUV report		V_M + 2		V
Over-Current Protection	I_{OCP}	Current through any FET		2		A
Over-Current Deglitch Time	t_{OCP}			2		μs
Over-Current Retry Time	t_{RETRY}			4		ms
Thermal Shutdown	T_{SD}	Die temperature T_J		165		℃
Thermal Shutdown Hysteresis	T_{HYS}	Die temperature T_J		40		℃

INDEXER TIMING REQUIREMENTS

(T_J = +25℃, V_M = 24V, unless otherwise noted.)

SYMBOL	FUNCTION	MIN	MAX	UNITS
f_{STEP}	Step frequency.		400	kHz
t_{WH_STEP}	Pulse duration, STEP high.	1.25		μs
t_{WL_STEP}	Pulse duration, STEP low.	1.25		μs
$t_{SU\_DIR, Mx}$	Set-up time, DIR or MODEx to STEP rising.	250		ns
$t_{H\_DIR, Mx}$	Hold time, DIR or MODEx to STEP rising.	250		ns

NOTE: STEP input can be up to 400kHz, but system bandwidth is limited by the motor load.

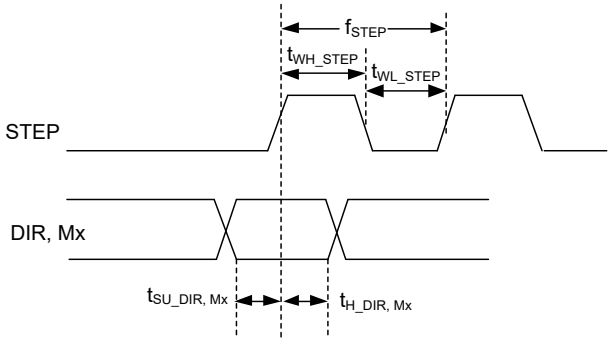
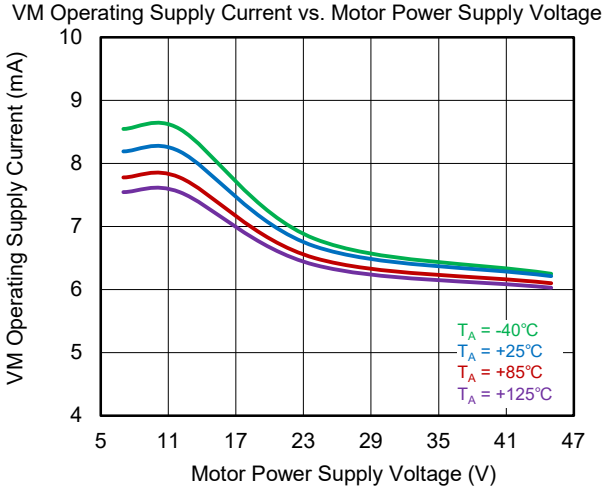


Figure 1. Timing Diagram

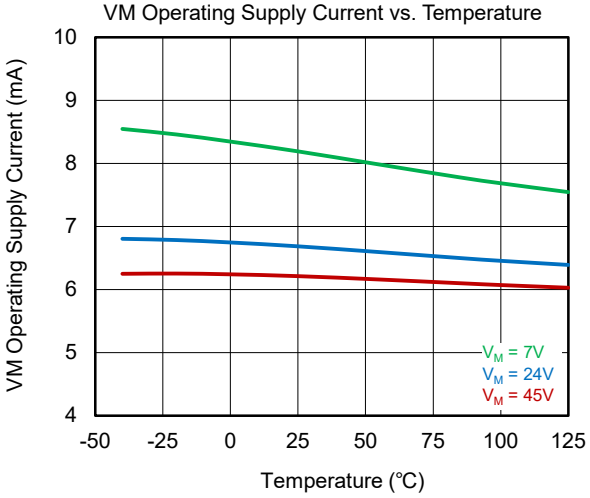
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

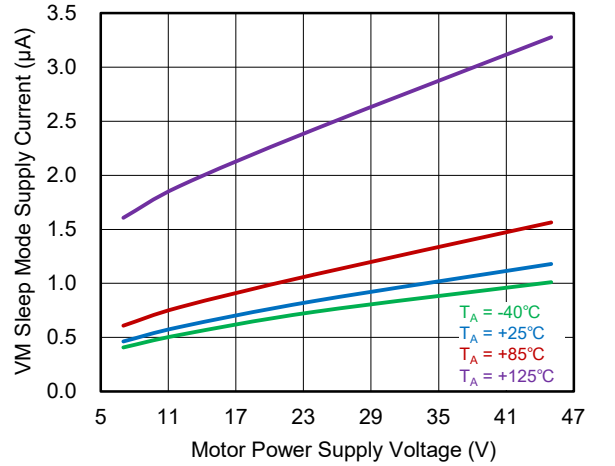
VM Operating Supply Current vs. Motor Power Supply Voltage



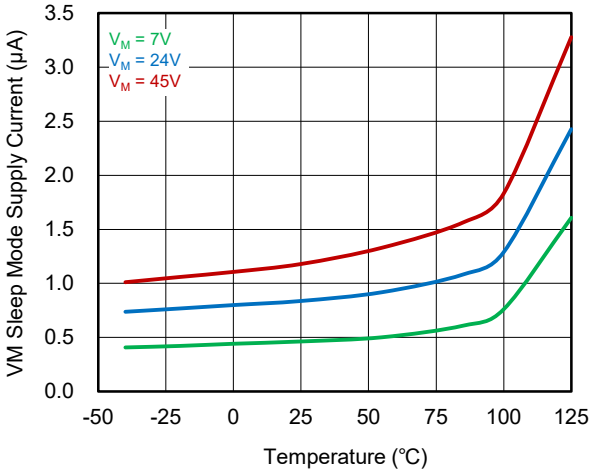
VM Operating Supply Current vs. Temperature



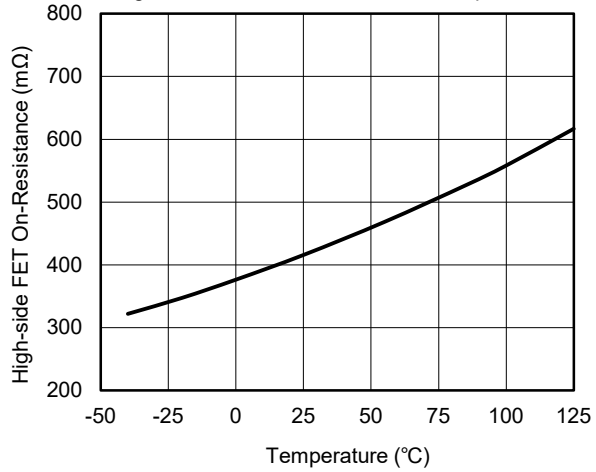
VM Sleep Mode Supply Current vs. Motor Power Supply Voltage



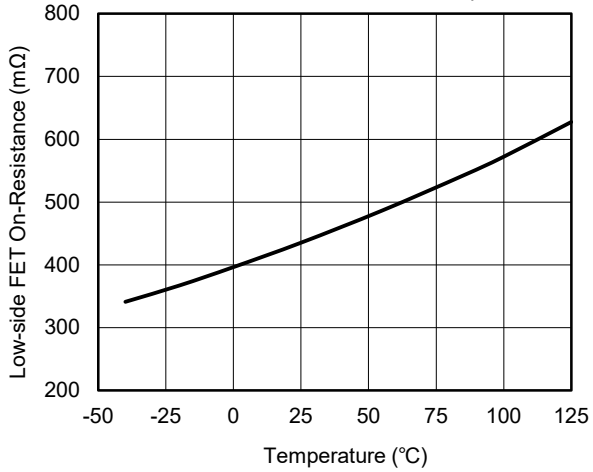
VM Sleep Mode Supply Current vs. Temperature



High-side FET On-Resistance vs. Temperature



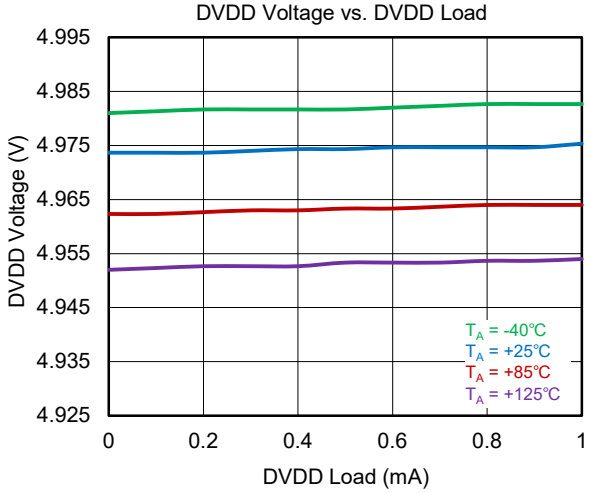
Low-side FET On-Resistance vs. Temperature



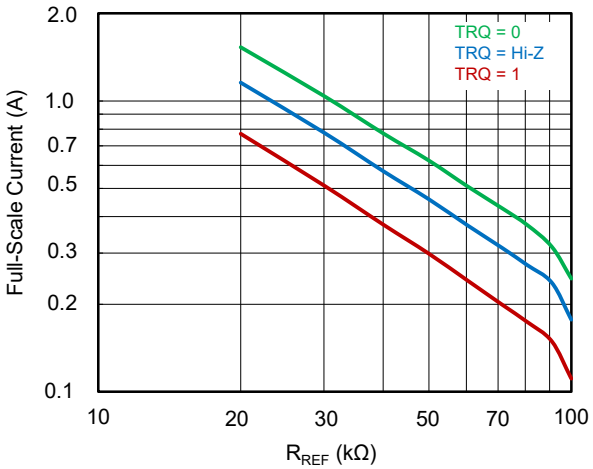
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

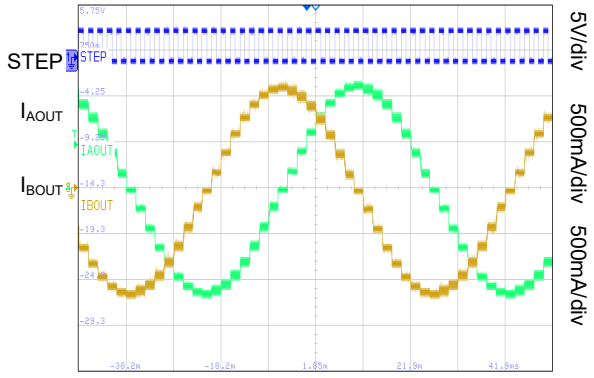
DVDD Voltage vs. DVDD Load



Full-Scale Current vs. R_{REF}

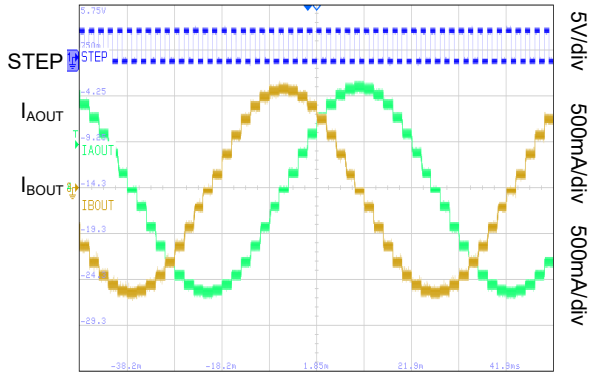


1/8 Microstepping with Slow-Mixed Decay



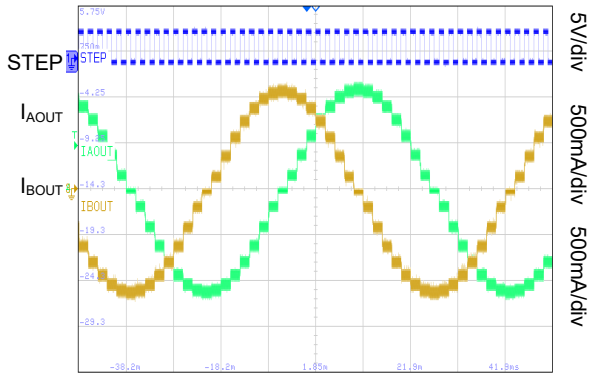
Time (10ms/div)

1/8 Microstepping with Mixed-Mixed Decay (30% Fast)



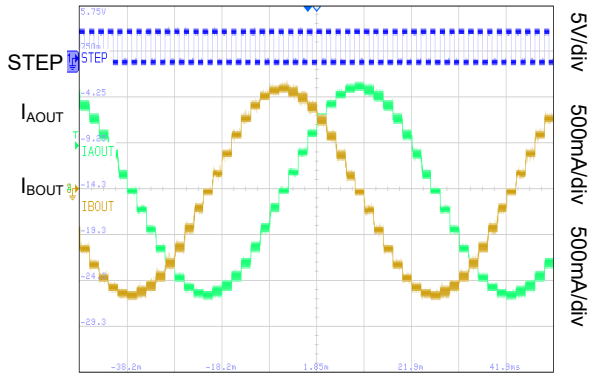
Time (10ms/div)

1/8 Microstepping with Mixed-Mixed Decay (60% Fast)



Time (10ms/div)

1/8 Microstepping with Auto Tune Ripple Control



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

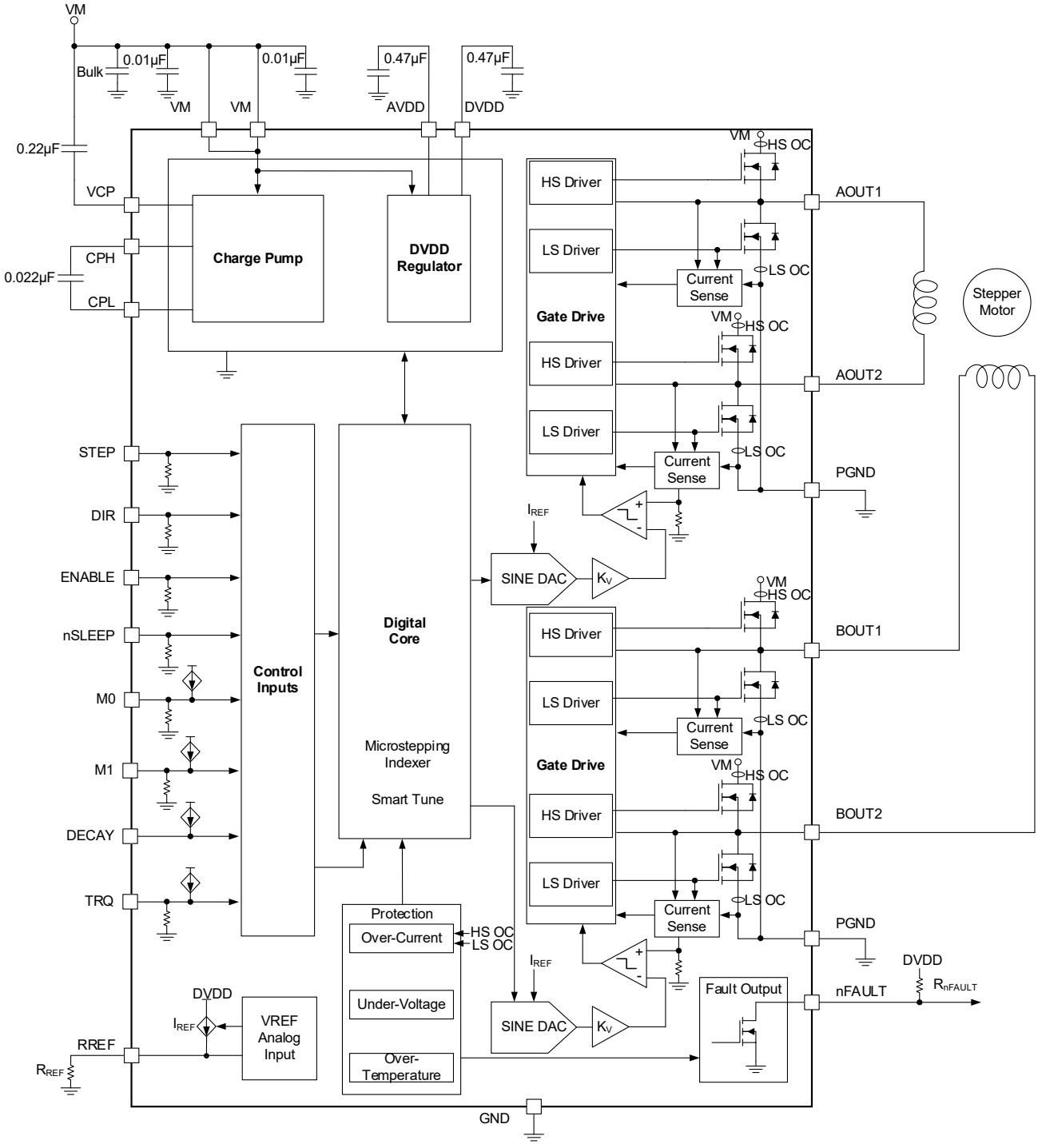


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM42685 is a highly integrated bipolar stepper motor driver offering compact solution size with high efficiency and minimal number of external components. It includes two N-MOSFET H-bridges for driving the motor windings with current sense and current regulation circuitry and a microstepping indexer. It can be powered with a supply voltage in the 7V to 45V range. The SGM42685 can provide up to 1.5A full-scale current and 1A RMS current for each winding. The actual full-scale and safe RMS currents are de-rated based on the device temperature that is affected by the ambient temperature, device cooling, running frequency and supply voltage. The sleep mode (low power) can be used to save power when the system does not actively drive the motor.

There is no need for external power sense resistors due to the integrated current sensing architecture used in the SGM42685. This feature eliminates the need for external resistors and removes their losses from the system. The set point for regulating the output current is controlled by the resistor connected to the RREF pin.

The simple and conventional STEP/DIR interface is used for control of the motor direction and step rate. The integrated indexer can provide accurate microstepping with no need for external current controller. Full step, 1/2 step, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, and 1/256 microstepping are available. Moreover, in addition to the standard half stepping, a non-circular half stepping mode is included that can be used to boost the torque at higher RPM.

Several decay modes are available and can be chosen for current regulation by configuring the DECAY pin voltages. During a slow decay, the winding current is circulated through the lower bridge MOSFETs to decay, while in fast decay, the bridge applies a reverse voltage to accelerate the current decay. Combinations of slow and fast decays are used to define several decay modes current regulation schemes including slow-mixed, mixed-decay (30% or 60% fast), smart tune ripple control. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune ripple control mode automatically adjusts the decay segments for optimal current regulation performance and compensate for motor parameter variations and aging effects.

A list of recommended external components for use with the SGM42685 is provided in Table 1.

Table 1. SGM42685 Suggested External Component Values

Peripheral	PIN 1	PIN 2	Recommended Value
C_{VM1}	VM	GND	Two parallel X7R, 0.01μF ceramic capacitors rated for operating at VM voltage
C_{VM2}	VM	GND	A bulk capacitor rated for operating at VM voltage
C_{CP}	VCP	VM	X7R, 0.22μF, 16V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022μF ceramic capacitor rated for operating at VM voltage
C_{AVDD}	AVDD	GND	X5R or X7R, 0.47μF, 6.3V ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47μF to 1μF, 6.3V ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	> 4.7kΩ resistor (10kΩ typical) NOTE: 1. VCC is the pull-up voltage for nFAULT open-drain output. DVDD may be used as VCC.
R_{REF}	RREF	GND	Resistor to set I_{TRIP} current.

DETAILED DESCRIPTION (continued)

Stepper Motor Driver Current Ratings

For a stepper motor driver usually the output current peak, RMS and full-scale ratings are specified. For the SGM42685, these ratings are described as follows.

Peak Current Rating

The driver peak current is usually limited by the over-current protection trip threshold (I_{OCP}). Such peaks usually occur during current transients with very low duty cycle in a current pulse, for example, due to charging of a capacitance. The minimum I_{OCP} threshold usually specifies the rated peak current of the stepper motor driver.

RMS Current Rating

The RMS current is limited by the maximum operation temperature of the device junction. Thermal performance of the system may increase or decrease the effective maximum RMS current. The junction temperature depends on the MOSFETs R_{DSON}, rise and fall times of the output pulses, PWM frequency, device quiescent current, heat removal performance of the system and ambient temperature. The specified RMS values are given for a typical system operating at +25℃. The rated RMS current is 1A for the SGM42685 per bridge.

Full-Scale Current Rating

The full-scale current is the peak of the quasi-sinusoid current waveform during microstepping and rotation. Like a sinusoid current, the peak and RMS values are not independent and the full-scale current is almost $\sqrt{2}$ times the rated RMS value ($I_{FS} \approx 1.41 \times I_{RMS}$). Therefore, the peak current is effectively limited by the thermal performance as well. The rated full-scale current is 1.5A for the SGM42685 per bridge.

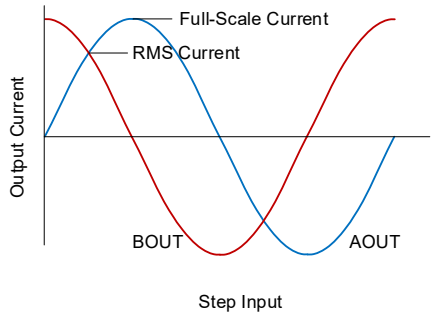


Figure 3. Full-Scale and RMS Current

Full-Bridge Drivers

Each driver has two N-channel full H-bridges (A and B) that drive the two windings (A and B) of the bipolar stepper motor respectively. The structure of each full bridge is shown in Figure 4 for winding A as example.

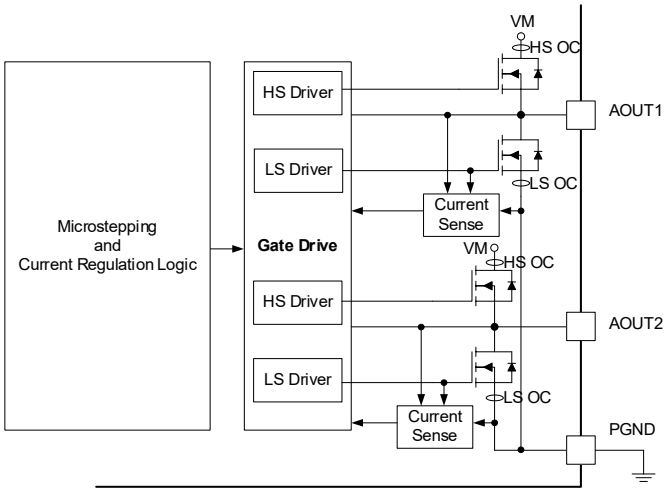


Figure 4. Full-Bridge Driver Block Diagram

DETAILED DESCRIPTION (continued)

Microstepping Indexer

Several stepping modes can be applied with the indexer integrated in the SGM42685. The Mode pins (M0 and M1) are biased to select the stepping mode as given in Table 2. Stepping modes can be changed on the fly.

Table 2. Using Mode Pins (M0 and M1) to Configure Microstepping

M0	M1	STEP MODE
0	0	Full step with 71% current
0	1	1/2 step
0	Hi-Z	1/32 step
1	0	1/16 step
1	1	1/4 step
1	Hi-Z	1/256 step
Hi-Z	0	1/8 step
Hi-Z	1	Non-circular 1/2 step
Hi-Z	330kΩ to GND	1/64 step
Hi-Z	Hi-Z	1/128 step

In Table 3, the winding currents (as percentage of the full-scale) and the electrical angles in each indexer state are listed for full step (71% current), 1/2 step, 1/4 step and 1/8 step operation modes. Table 4 lists the non-circular half-step mode. The currents and electrical angles for higher stepping resolutions (1/16, 1/32, 1/64, 1/128 and 1/256) can be extended similarly from Table 3. The AOUT and BOUT currents in this table are approximate sine and cosine functions of the electrical angle respectively. Winding current is positive when flowing from terminal 1 to terminal 2 (xOUT1 to xOUT2).

With every rising edge of the STEP input, the indexer advances to its next state shown in the table when the DIR input is high. If the DIR is set to logic low, the sequence is reversed. The step size is set by M0 and M1 inputs and may be changed on the fly during stepping.

The indexer resets to home state at 45° electrical angle after power-up, under-voltage lockout, or exit from sleep mode.

Table 3. Output Currents and Electrical Rotor Angle for Each Indexer Stepping State (for DIR = High)

Indexer State				AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1/8 Step	1/4 Step	1/2 Step	Full Step 71%			
1	1	1		0%	100%	0.00
2				20%	98%	11.25
3	2			38%	92%	22.50
4				56%	83%	33.75
5	3	2	1	71%	71%	45.00
6				83%	56%	56.25
7	4			92%	38%	67.50
8				98%	20%	78.75
9	5	3		100%	0%	90.00
10				98%	-20%	101.25
11	6			92%	-38%	112.50
12				83%	-56%	123.75
13	7	4	2	71%	-71%	135.00

DETAILED DESCRIPTION (continued)

Indexer State				AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1/8 Step	1/4 Step	1/2 Step	Full Step 71%			
14				56%	-83%	146.25
15	8			38%	-92%	157.50
16				20%	-98%	168.75
17	9	5		0%	-100%	180.00
18				-20%	-98%	191.25
19	10			-38%	-92%	202.50
20				-56%	-83%	213.75
21	11	6	3	-71%	-71%	225.00
22				-83%	-56%	236.25
23	12			-92%	-38%	247.50
24				-98%	-20%	258.75
25	13	7		-100%	0%	270.00
26				-98%	20%	281.25
27	14			-92%	38%	292.50
28				-83%	56%	303.75
29	15	8	4	-71%	71%	315.00
30				-56%	83%	326.25
31	16			-38%	92%	337.50
32				-20%	98%	348.75

Similarly, Table 4 lists the parameters for the non-circular 1/2 step mode. This mode uses more power compared to the normal (circular) 1/2 step, but produces higher torque (usually needed for higher motor speeds).

Table 4. Output Currents and Electrical Angle for Indexer Steps in Non-Circular 1/2 Step Mode (for DIR = High)

Indexer State Non-Circular 1/2 Step Mode	AOUT Current (% Full-Scale)	BOUT Current (% Full-Scale)	Electrical Angle (Degrees)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	-100	135
5	0	-100	180
6	-100	-100	225
7	-100	0	270
8	-100	100	315

DETAILED DESCRIPTION (continued)

R_{REF} Control for Full-Scale Current Adjustment

Set the current magnitude by connecting a suitable resistor between RREF and GND. The current flowing through the resistor serves as a reference to scale the global current. Current adjustment is also available for applications that need to set motor current based on the motor loading and speed. A DAC output from MCU may be used to set the reference current on R_{REF} for adjusting the full-scale current as shown in Figure 5. A PWM output signal along with a low-pass filter may also be used to set the reference current on R_{REF} as shown in Figure 6.

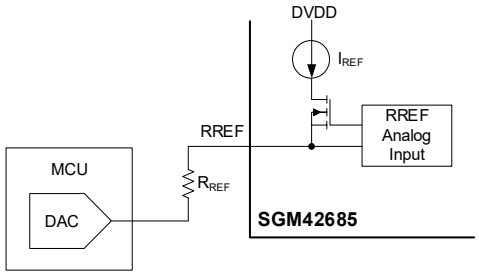


Figure 5. Control of the RREF Voltage with a DAC

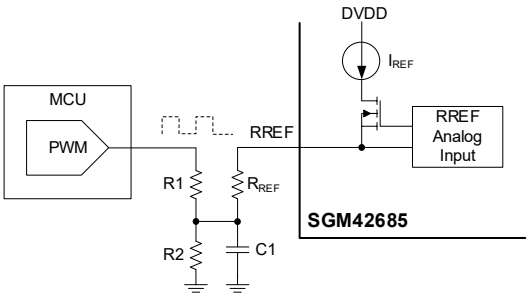


Figure 6. Control of the RREF with a PWM Output and an LPF

Current Regulation

An adjustable, off-time control PWM current regulation scheme is used to control the motor winding currents as shown in Figure 7. With activation of the H-bridge, the current rises with a rate determined by the VM voltage, winding inductance, and the back-EMF induced by rotor rotation. In each PWM cycle, the bridge is active for at least t_{BLANK} time. The PWM pulse is on until t_{DRIVE} where the current exceeds the I_{TRIP} regulation threshold and then the decay (current drop) begins and continuous during the t_{OFF} time. For SGM42685, t_{OFF} is a fixed value. The chip obtains sampling current through a built-in circuit. Based on the comparison result between the actual current and I_{TRIP}, the driving state of the H-bridge is determined. When each step arrives, the I_{TRIP} level is updated with a quantized sine (or cosine) waveform. The full-scale value of this reference current is set by the R_{REF}. The current can be further scaled by setting the TRQ pin as shown in Table 5. The product of the full-scale regulation current (I_{FS}) and the A_{RREF} is 30kAΩ for SGM42685. Full-scale current is calculated as follow:

$$I_{FS}(A) = A_{RREF}(kA\Omega)/R_{REF}(k\Omega) \times TRQ(100\%)$$

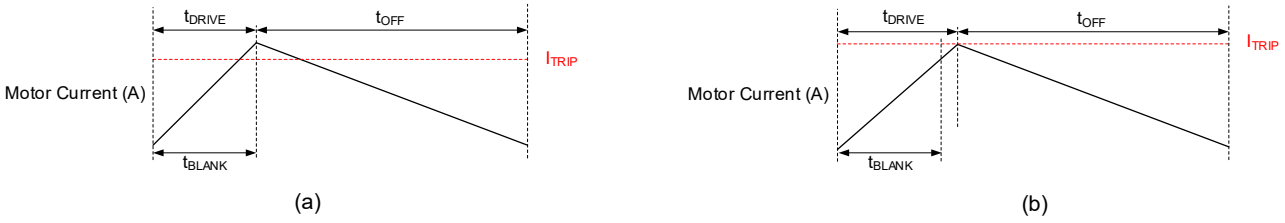


Figure 7. Bridge Output PWM Current Chopping Waveform (Simplified Decay Current is Shown)

DETAILED DESCRIPTION (continued)

Table 5. Torque DAC Settings

TRQ	Current Scalar (TRQ)
0	100%
Hi-Z	75%
1	50%

PWM Off-Time

The PWM off-time (t_{OFF}) of the chip is a constant value, approximately 24μs. Decay mode will not affect the t_{OFF}.

Blanking Time

At the beginning of each PWM cycle, the H-bridge begins driving current into the motor winding. In order to obtain a stable and reliable trigger signal, t_{BLANK} is usually set as the blanking time. After the t_{BLANK} has passed, the driver will perform the corresponding action based on the output state of the internal comparator. For small inductance or large supply voltage, the current in the motor coil will rise rapidly, even if the I_{TRIP} and current comparator have been triggered, the driver will not immediately enter the decay state, but at least continue to t_{BLANK} the on-time. For SGM42685, t_{BLANK} is a fixed value of about 2μs. After t_{BLANK}, the drive switches to either fast decay or slow decay according to the current decay mode.

PWM Decay Modes

During PWM off-time, the H-bridge current begins to decay either in fast rate or slow as shown in Figure 8. In the fast decay, when the current exceeds the I_{TRIP} threshold, the bridge applies a reverse voltage by turning the opposite switches and forcing the current to reverse its direction. Bridge is deactivated before the current reversal. In the slow decay mode, the lower switches are both turned on to freewheel the winding current. In this mode, a near zero voltage is applied to the winding to decay the current. In a mixed decay, the off-time initially begins with fast decay that lasts for a fixed time (t_{FAST}) and then a slow decay phase for the remainder of t_{OFF} time.

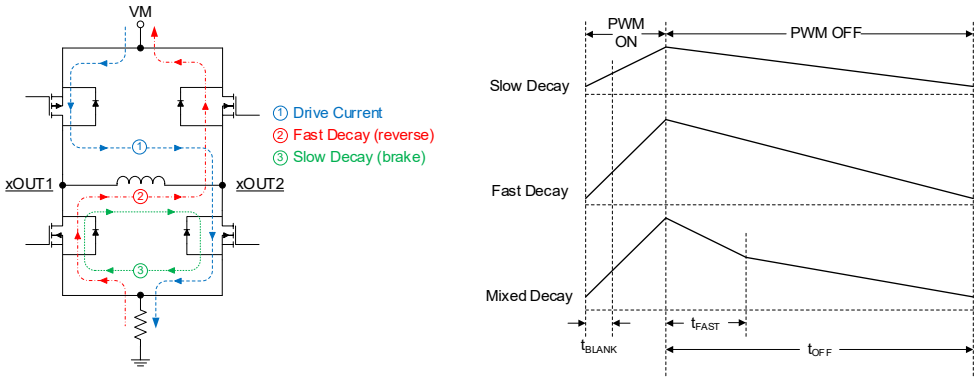


Figure 8. Slow, Fast and Mixed Decay Current Chopping Modes

By combining the slow and fast decays based on different criteria, 5 decay mode options are available in the SGM42685 as listed in Table 6. Decay mode is set by the DECAY pin and can be changed on the fly. As shown in Figure 9 with two phases, based on the increasing or decreasing of the current reference (I_{TRIP}) in the next step, the bridge can be in increasing steps (INC) or decreasing steps (DEC) state.

DETAILED DESCRIPTION (continued)

Decay Modes

Select the SGM42685 decay modes by setting the multi-level DECAY pin voltage, as shown in Table 6. When the DECAY pin voltage changes, the new configuration of decay mode works immediately.

Table 6. Decay Mode Settings

DECAY	Increasing Steps	Decreasing Steps
GND	Slow Decay	Mixed Decay: 30% Fast
15kΩ to GND	Mixed Decay: 30% Fast	Mixed Decay: 30% Fast
45kΩ to GND	Mixed Decay: 60% Fast	Mixed Decay: 60% Fast
80kΩ to GND	Smart Tune Ripple Control	Smart Tune Ripple Control
DVDD	Slow Decay	Slow Decay

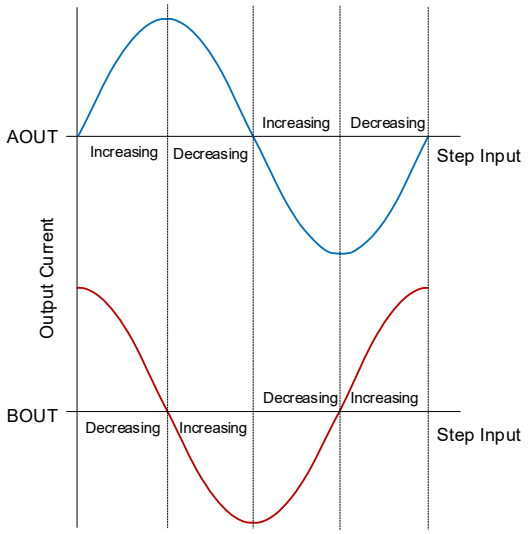


Figure 9. Definition of Bridge Increasing (INC) and Decreasing (DEC) Step Phases

The slow decay has the lowest current ripple for a given t_{OFF} time. However, during the current decreasing phases, it may take a long time to reach the new I_{TRIP} level due to the slow current drop rate.

An important case occurs when the speed is very low (slow stepping) and the back-EMF is almost zero. The current rises sharply during the blank time in such condition. The high peak current may require several off-time extensions to bring the current below I_{TRIP} or it may even result in loss of regulation. Therefore, slow decay may not be an appropriate choice to regulate the current at low speeds and more intense decay modes are needed.

DETAILED DESCRIPTION (continued)

Slow-Slow (DECAY = 1)

In the slow-slow decay mode, slow decay is used for both increase or decrease phases. The current regulation during INC and DEC phases are shown in Figure 10.

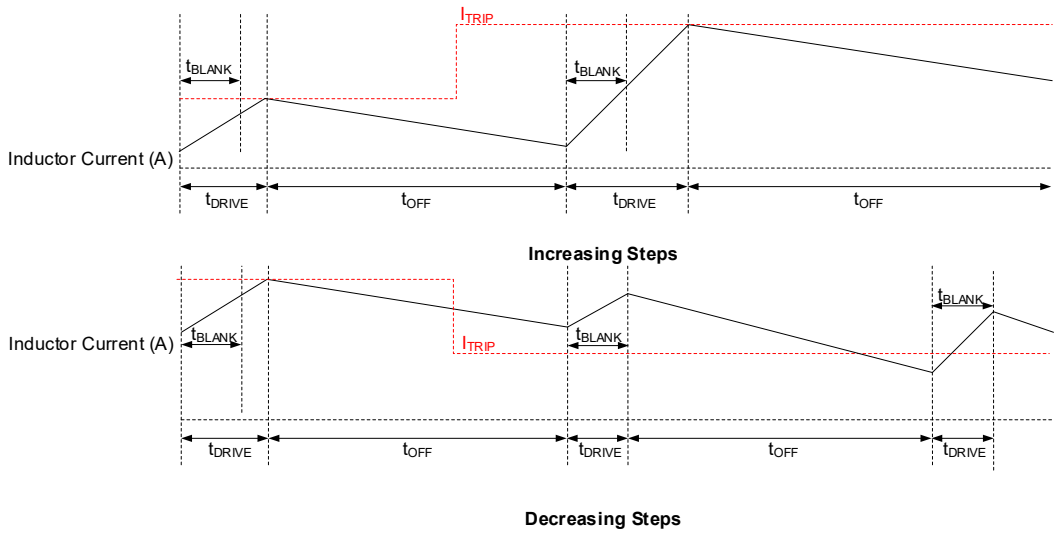


Figure 10. Current Regulation with Slow-Slow Decay Mode (Slow for both INC and DEC Phases)

Slow-Mixed (DECAY = 0)

In this mode, mixed decay is only used in the decreasing current phase and slow decay is used for increasing phase. The current ripple in the INC phases is small (slow decay), but in the DEC phases, the ripple is larger (but still less than pure fast decay ripple). With mixed decay, the current settling to the new I_{TRIP} level during DEC phase is faster than slow decay. See Figure 11 for the current regulation waveforms during INC and DEC phases for this decay mode.

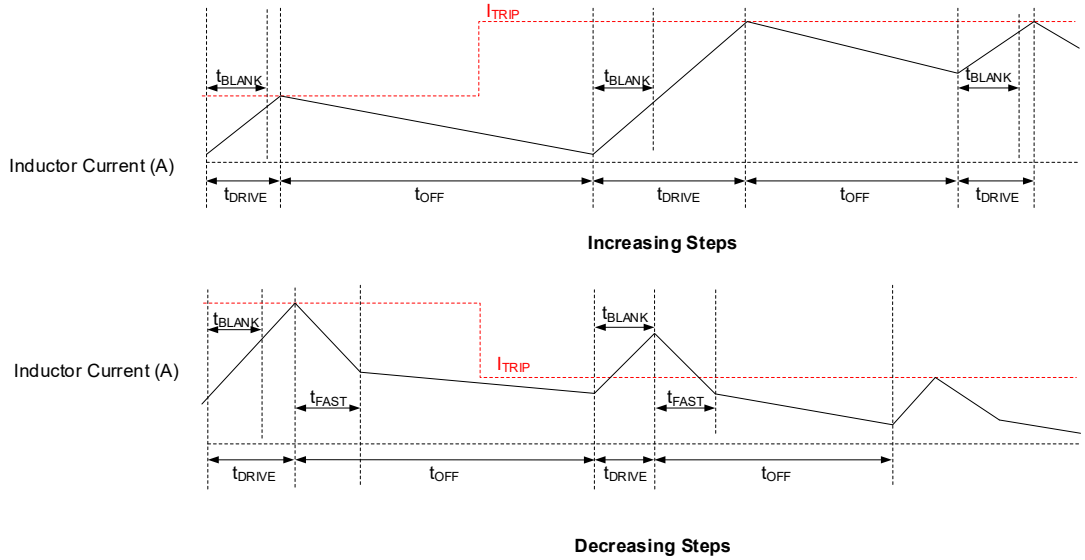


Figure 11. Current Regulation with Slow-Mixed Decay Mode: Slow for INC Phase and Mixed for DEC Phase

DETAILED DESCRIPTION (continued)

Mixed-Mixed Modes (DECAY = 15kΩ or 45kΩ to GND)

In these two modes, mixed decay is used for both increasing and decreasing current steps. If DECAY connects a 15kΩ resistor to GND, t_{FAST} is set to 30% of the t_{OFF} period and if DECAY connects a 45kΩ resistor to GND, t_{FAST} is set to 60% of the t_{OFF}. The current ripple is larger compared to slow decay, but still less than pure fast decay in both INC and DEC phases. Figure 12 shows the current regulation waveforms during INC and DEC phases for the mixed-mixed decay modes.

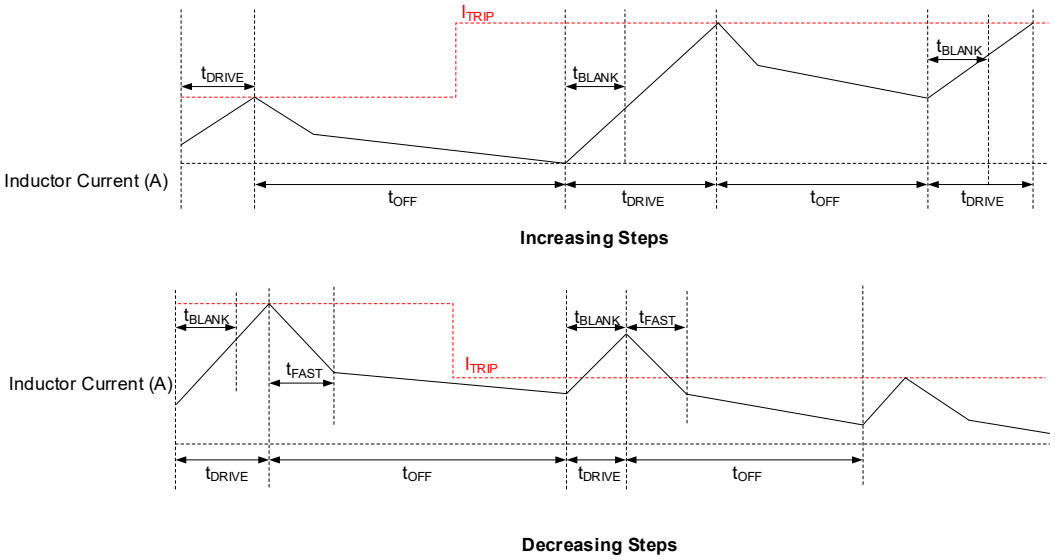


Figure 12. Current Regulation with Mixed-Mixed Decay Mode: Mixed for both INC and DEC Phases

Smart Tune Ripple Control Mode (DECAY = 80kΩ to GND)

In the smart tune ripple control mode, besides the I_{TRIP} upper-level comparator for the current rising, an I_{TRIP} lower-level comparator is also used for current falling. In this smart mode, the decay switches between slow and mixed decay. When t_{DRIVE} is larger than t_{BLANK}, the chopper maintains a slow decay time of t_{OFF} after t_{DRIVE}. When the t_{BLANK} is equal to t_{DRIVE} or step changes during DEC phase, the chopper will insert a fast decay period until the current drops to I_{TRIP} again.

The smart tune ripple control makes it possible to quickly adjust the current to the target value and reduces power consumption.

See Figure 13 for an illustration of smart tune ripple control decay mode and the current regulation waveforms.

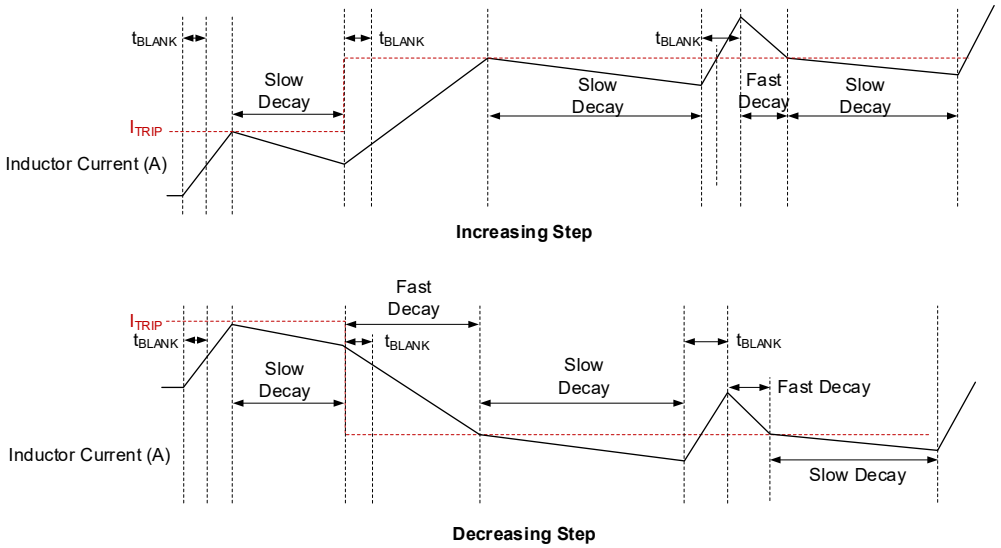


Figure 13. Smart Tune Ripple Control Decay Mode Current Waveforms during INC and DEC Phases

DETAILED DESCRIPTION (continued)

Charge Pump

The high-side N-channel power MOSFETs require a gate-drive voltage higher than the VM supply voltage. A charge pump is integrated to generate this supply voltage and its output is available on the VCP pin. A filter capacitor should be connected externally between VM and VCP pins and another ceramic capacitor is needed between CPL and CPH pins for pump operation. The structure of the charge pump is shown in Figure 14.

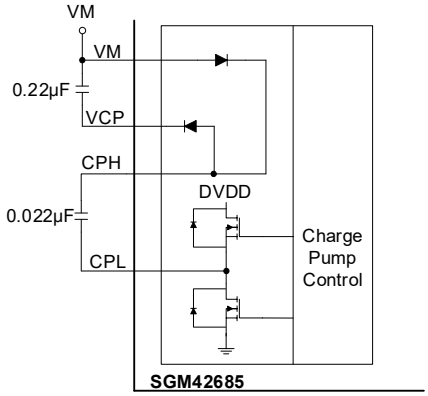


Figure 14. Integrated Charge Pump Block Diagram

Integrated DVDD Regulator

The SGM42685 includes a linear voltage regulator that provides a 5V (nominal) reference voltage on the DVDD output as shown in Figure 15. The maximum load on this pin is limited to 2mA and if this limit is exceeded, the output will drop significantly. Bypass the DVDD to GND with a ceramic capacitor.

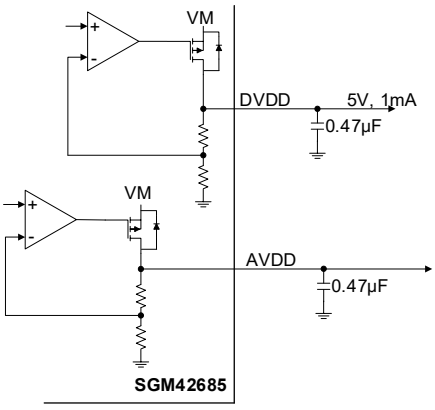


Figure 15. Linear Voltage Regulator Block Diagram

If a digital input (like, M0, M1, DECAY, or TRQ) needs a permanent pull up, it is preferred to use DVDD output for better power saving in sleep mode. When VM voltage is removed, the regulator is disabled and no current flows in the internal pull-down resistors.

Note that the nSLEEP pin must not be pulled up to DVDD, otherwise the device cannot exit the sleep mode.

DETAILED DESCRIPTION (continued)

Logic and Multi-Level Input Pins

The block diagram of the two-level logic inputs (ENABLE, STEP, DIR and nSLEEP) is also shown in Figure 16.

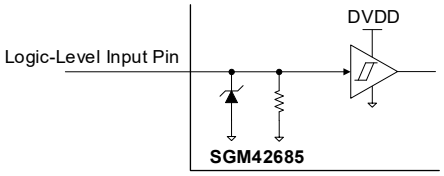


Figure 16. Internal Structure of the Two-Level (Logic) Input Pins

The SGM42685 uses multi-level inputs for configuring its operation. The block diagram of the tri-level inputs (M0 and TRQ) are shown in Figure 17.

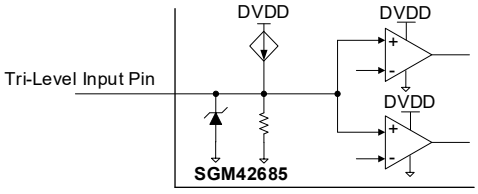


Figure 17. Internal Structure of the Tri-Level Input Pins

The quad-level input structure of the M1 pin is shown in Figure 18.

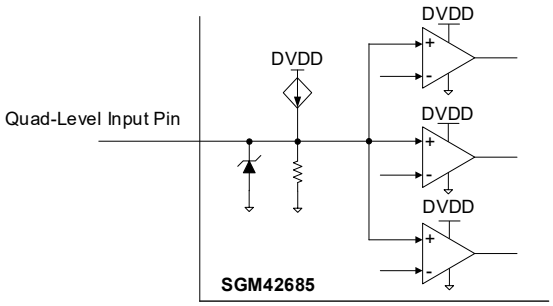


Figure 18. Internal Structure of the Quad-Level Input Pins

The five-level input structure of the DECAY pin is shown in Figure 19.

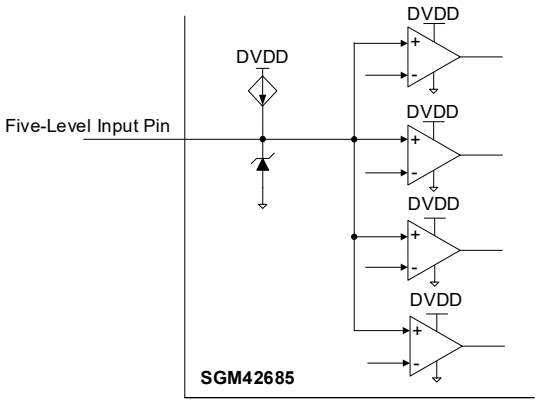


Figure 19. Internal Structure of the Five-Level Input Pins

DETAILED DESCRIPTION (continued)

nFAULT Output

The nFAULT is an open-drain output that is pulled low when a fault is detected. It should be pulled up to a 5V (like DVDD) or 3.3V supply voltage as shown in Figure 20. After power-up, nFAULT is released to go high.

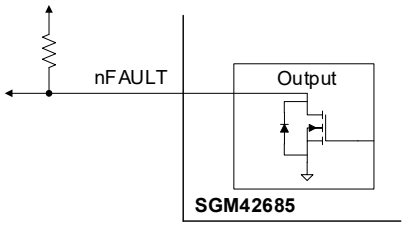


Figure 20. The nFAULT Output

Faults and Protections

The SGM42685 has a complete set of protection features to protect it against faults including VM supply under-voltage, VCP under-voltage, output over-current, and junction over-temperature. A summary of the fault conditions and the resulting protection functions is provided in Table 7. Each item is explained in the following sections.

Table 7. SGM42685 Faults and Protections Summary

Fault	Condition	Configuration	Report	H-Bridge	Charge Pump	Indexer	Logic Circuitry	Recovery
VM Under-Voltage (UVLO)	$V_M < V_{UVLO}$	-	nFAULT	Disabled	Disabled	Disabled	Resets and V_{DVDD} falls below 3.9V	Automatic when $V_M > V_{UVLO}$
VCP Under-Voltage (CPUV)	$VCP < V_{CPUV}$	-	nFAULT	Disabled	Operating	Operating	Operating	Automatic when $VCP > V_{CPUV}$
Over-Current (OCP)	$I_{OUT1} > I_{OCP}$ or $I_{OUT2} > I_{OCP}$	ENABLE = 1	nFAULT	Disabled	Operating	Operating	Operating	Auto-retry after t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	-	nFAULT	Disabled	Disabled	Operating	Operating	Normal operation resumes and the nFAULT is released when the TSD condition is removed.

VM Under-Voltage Lockout (UVLO)

If the VM supply voltage drops below the UVLO falling threshold, all outputs, charge pump and logic circuit will be disabled, and nFAULT goes low. Device will recover and nFAULT is released like a new power-up when the VM voltage exceeds the UVLO rising threshold.

Charge Pump Under-Voltage Lockout (CPUV)

If the VCP voltage drops below the CPUV falling threshold, all outputs are disabled and nFAULT is pulled low. The charge pump and logic circuits continue operation. The outputs will resume operation and nFAULT is released when VCP exceeds the CPUV rising threshold and returns to its normal range.

Over-Current Protection (OCP)

Over-current protection is implemented by an analog circuit that senses the MOSFET currents and stops the gate pulses if the current limit is exceeded. If after t_{OCP} time, the current is still high, all MOSFETs in that bridge will be disabled and nFAULT is asserted. The charge pump continues to operate. After a t_{RETRY} wait time, the bridge in the OCP condition is re-enabled for normal operation and nFAULT is released. If the OC condition persists, the bridge output is disabled and nFAULT is asserted until another retry.

Thermal Protection and Shutdown (TSD)

To prevent overheating damage to the device, an over-temperature shutdown protection is implemented in the device. If the die temperature (T_J) exceeds the T_{SD} limit, all H-bridge MOSFETs are turned off and nFAULT is asserted. The charge pump is disabled and logic circuits continue operation. Normal operation resumes and the nFAULT is released when the TSD condition is removed.

DETAILED DESCRIPTION (continued)

Functional Modes

The SGM42685 can be in different functional conditions as summarized in Table 8 and explained below.

Table 8. Summary of the Device Functional Modes

Condition		Configuration	H-Bridges	DVDD Regulator	Charge Pump	Indexer	Logic
Sleep Mode	7V < V_M < 45V	nSLEEP = 0	Disabled	Disabled	Disabled	Disabled	Disabled
Disabled	7V < V_M < 45V	nSLEEP = 1 ENABLE = 0	Disabled	Operating	Operating	Operating	Operating
Run (Active)	7V < V_M < 45V	nSLEEP = 1 ENABLE = 1	Operating	Operating	Operating	Operating	Operating

Sleep Mode (nSLEEP = 0)

This state is controlled by the nSLEEP input. When the nSLEEP input is pulled low for at least t_{SLEEP} time, the SGM42685 enter low-power mode in which both bridges and the charge pump are disabled. By pulling the nSLEEP high and after t_{WAKE} time, the device exits sleep mode. During the t_{WAKE} time, the inputs are ignored.

Disable Mode (nSLEEP = 1, ENABLE = 0)

The ENABLE input is used to enable or disable the bridges. If ENABLE = 0, the outputs go to Hi-Z state.

Run Mode (nSLEEP = 1, ENABLE = 1)

With $V_M \geq V_{UVLO}$, if nSLEEP = 1 and ENABLE is set to 1 state, the device will be activated and enters the run mode. The inputs are ignored for the t_{WAKE} time after the two conditions are both valid.

APPLICATION INFORMATION

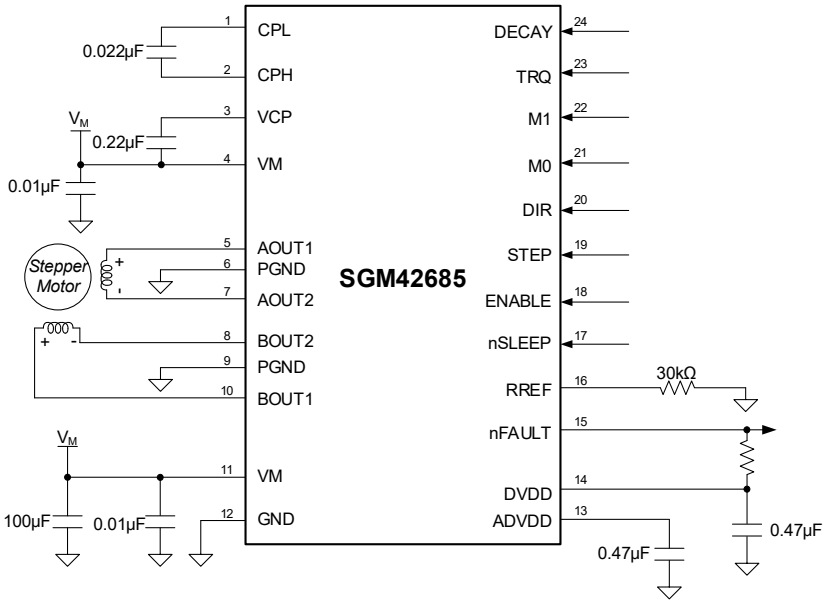


Figure 21. Typical Application Schematic

Configurations of the SGM42685 are explained in the following design examples.

Design Requirements

A list of design parameters for a typical motor drive system with the SGM42685 are provided in Table 9 as example.

Table 9. Design Parameters

Design Parameter	Reference	Example Value
Supply Voltage	V_M	24V
Motor Winding Resistance	R_L	2.6Ω/phase
Motor Winding Inductance	L_L	1.4mH/phase
Motor Full Step Angle	θ_{STEP}	1.8°/step
Target Microstepping Level	n_m	1/8 step
Target Motor Speed	v	120rpm
Target Full-Scale Current	I_{FS}	1A

Stepper Motor Speed

The motor speed and microstepping requirements are the first parameters to consider in configuration of the stepper motor driver. If the application requires a constant speed, STEP pin must receive square pulses with f_{STEP} frequency.

Note that if the target speed is set too high, the motor may not be able to follow the STEP and won't spin, so, it is important to make sure the motor and load can support that speed with the available torque/power.

Equation 1 can be used to calculate the required f_{STEP} frequency for driving the stepper motor at speed (v) based on the microstepping level (n_m) and the motor full step angle (θ_{STEP}):

$$f_{STEP}\left(steps/s\right)=\frac{v\left(rpm\right)\times 360\left(°/rot\right)}{\theta_{STEP}\left(°/step\right)\times n_m\left(steps/micro\text{-}step\right)\times 60\left(s/min\right)} \quad (1)$$

θ_{STEP} is a stepper motor parameter that is specified in its datasheet or on the motor body.

The microstepping level (n_m) is set by the MODE pins (M0 and M1) based on the list in Table 2. By choosing a finer microstepping value, smoother and quieter motor motion is achieved, but at the cost of increased switching losses and higher required f_{STEP} frequency for the same motor speed.

APPLICATION INFORMATION (continued)

For example, to get the a target speed of 120rpm for a 1.8°/step motor with 1/8 microstepping the required step pulse frequency is:

$$f_{STEP} = \frac{120(rpm) \times 360(°/rot)}{1.8(°/step) \times 1/8(steps/micro\text{-}step) \times 60(s/min)} = 3200Pluse/sec$$

Power Supply Considerations

The SGM42685 stepper driver is designed to operate from 7V to 45V supply voltage on their VM pins and can drive stepper motors with the same voltage rating. Each VM pin must be decoupled with at least one 0.01μF ceramic capacitor. These capacitors must be placed as close as possible to each VM pins and its adjacent PGND pin. A bulk capacitor should also be used between VM and PGND return near the device to limit voltage ripple on the VM and stabilize the supply line.

Bulk Capacitance Selection for Motor Drivers

Using local bulk capacitors near the motor driver is necessary even though they increase the size and cost of the system. This capacitor is selected based on several factors including the following:

• The required peak current of the system
• The power supply internal capacitance and its sourcing capability
• The parasitic supply line inductance between the source and motor driver
• The system maximum acceptable voltage ripple

If other motor types are used (like brushed or brushless DC) the selection can be different and motor braking method should also be considered.

The parasitic inductance of the supply line limits the rate of the current change. It can result in large voltage variations if the load current has sharp changes. The local bulk capacitance keeps the VM voltage stable by providing or absorbing the difference between sharp motor driver current variations and the available slow changing current through the supply line. This capacitor should be large enough to provide or absorb the difference and limit the voltage rise or fall within the acceptable ripple range.

Even though datasheets usually recommend a wide range for this capacitor, a system-level testing is highly recommended to find the proper bulk capacitance. The bulk capacitor voltage rating must be chosen sufficiently above the VM operating voltage, because with motor loads, the energy transfer is sometimes rapidly reversed from the motor to the supply bus that charges the capacitor. The transient voltage can be significantly above the supply voltage. Selection of a higher voltage rating for the capacitor also improves the capacitor reliability by reducing the stress on its dielectric and mitigating its aging effects.

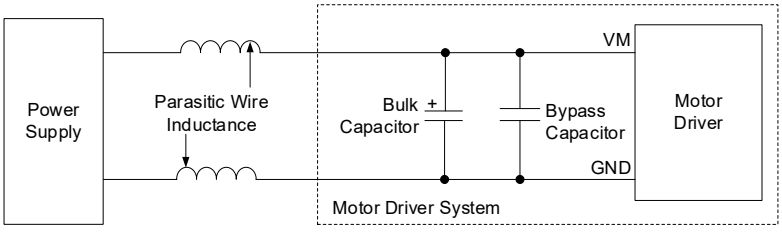


Figure 22. A Typical Motor Drive System with External Power Supply

APPLICATION INFORMATION (continued)

Layout Considerations

PCB layout has a significant impact on the performance of the drive system. The conductors must be sufficiently sized to carry large currents. Wide PGND planes are recommended for stable operation and better cooling.

The VM supply pins must be bypassed to their adjacent PGND pins using 0.01μF low-ESR ceramic capacitors with sufficient voltage rating with thick traces. PGND pins share large ground planes. The electrolytic bulk capacitor must be placed near the device on the VM and PGND traces as well.

Also, a low-ESR ceramic capacitor (0.022μF recommended) rated for VM voltage should be placed as charge pump flying capacitor between and close to the CPL and CPH pins. Same capacitor with 16V rating must be connected between and close to the VM and VCP pins for decoupling.

To bypass DVDD regulator output, it is recommended to use a low-ESR 0.47μF/6.3V capacitor between and as close as possible to the DVDD and GND pins.

The thermal PAD must be connected to system ground planes. This pad serves as a heat sinking path as well.

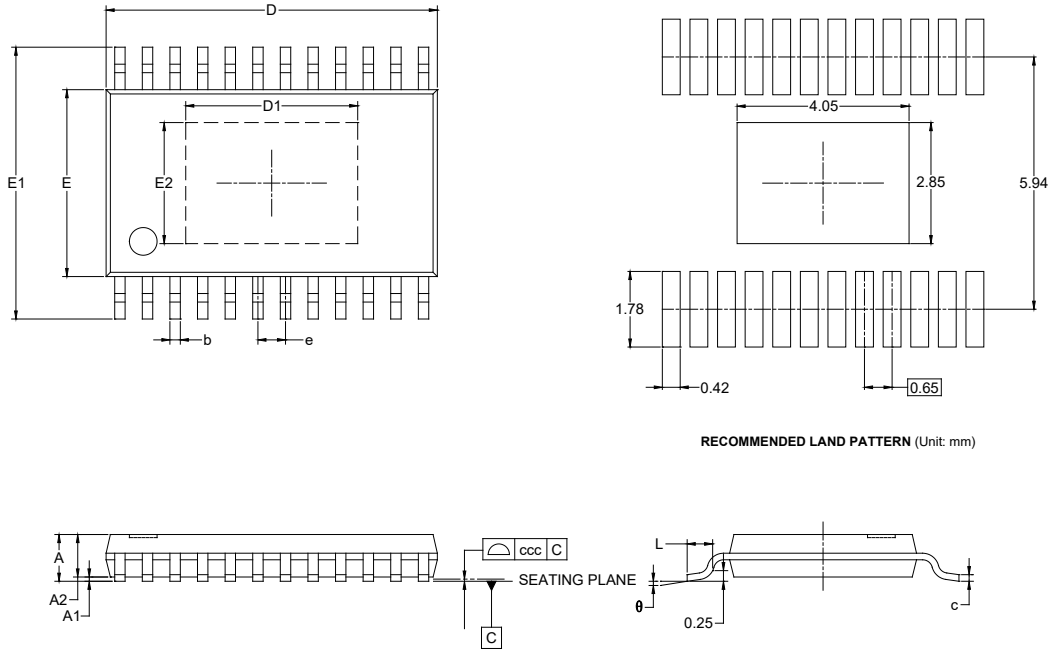
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (OCTOBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TSSOP-24 (Exposed Pad)

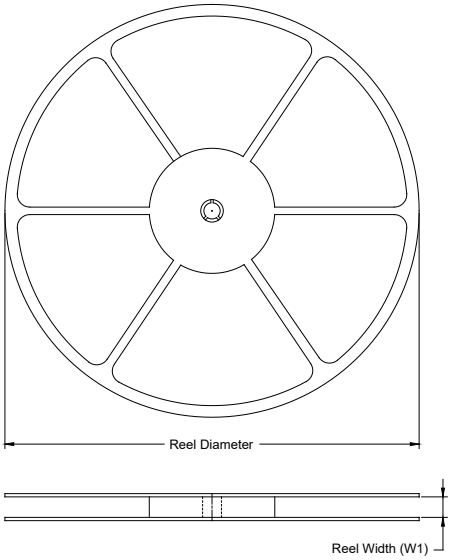


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	1.000 REF		
b	0.190	-	0.300
c	0.090	-	0.200
D	7.700	-	7.900
D1	3.850	-	4.250
E	4.300	-	4.500
E1	6.200	-	6.600
E2	2.650	-	3.050
e	0.650 BSC		
L	0.450	-	0.750
θ	0°	-	8°
ccc	0.100		

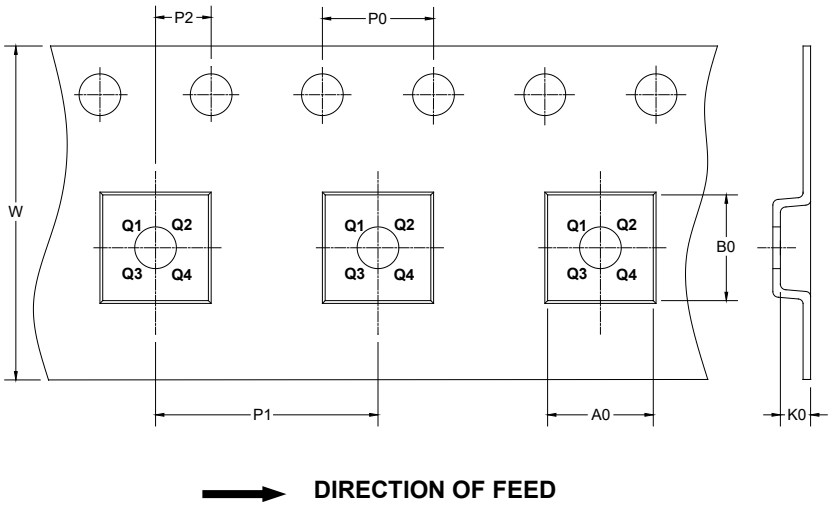
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



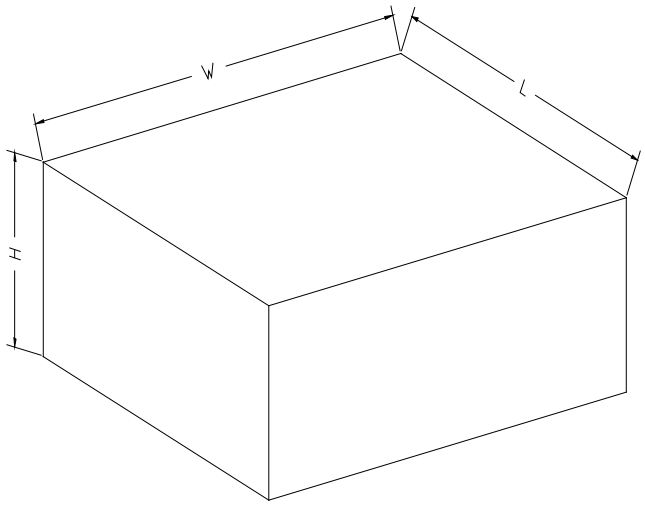
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-24 (Exposed Pad)	13"	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002