SGM3840
Triple-Output 1A AMOLED Display Power Supply

GENERAL DESCRIPTION

The SGM3840 is designed for powering AMOLED displays which require V_{ELVDD}, V_{ELVSS} and V_{AVDD}. The device integrates two Boost converters, VO1 for V_{ELVDD} and VO3 for V_{AVDD}, and a dual-phase inverting Buck-Boost converter VO2 for V_{ELVSS}. Output voltages of all the three converters can be programmed in digital steps through the digital interface control pin (SWIRE).

The SGM3840 is available in a Green WLCSP-2.37×2.37-36B package.

FEATURES

- **2.5V to 4.8V Input Supply Voltage Range**
- **Synchronous Boost Converter (VO1 = ELVDD)**
  - **4.6V to 5.0V Output Voltage with 100mV Steps**
  - **4.6V Default Output Voltage**
  - **0.7% Accuracy at 4.6V**
  - **Output Voltage Sensing Pin for Path Loss Compensation (FBS)**
- **Synchronous Inverting Buck-Boost Converter (VO2 = ELVSS)**
  - **-7.0V to -0.8V Output Voltage with 100mV Steps**
  - **-3.0V Default Output Voltage**
  - **1% Accuracy at -3V**
- **ELVDD-ELVSS Combined Output Current Capability (V_{VO1} = 4.6V)**
  - **1A @ V_{IN} = 2.5V, V_{VO2} = -3V**
  - **1A @ V_{IN} = 2.6V, V_{VO2} = -4V**
  - **1A @ V_{IN} = 2.8V, V_{VO2} = -5V**
  - **1A @ V_{IN} = 3.1V, V_{VO2} = -6V**
- **Synchronous Boost Converter (AVDD)**
  - **5.5V to 7.9V Output Voltage with 100mV Steps**
  - **7.3V Default Output Voltage**
  - **0.8% Accuracy at 7.3V**
  - **150mA Output Current Capability**
- **V_{IN} and V_{OUT} Bi-Directional Isolation**
- **Short Circuit Protection (SCP)**
- **Overload Protection**
- **Thermal Shutdown**
- **V_{ELVSS} Start-Up Delay: 6ms**
- **Short Circuit and OLP Detection Time: 0.7ms**
- **Available in a Green WLCSP-2.37×2.37-36B Package**

APPLICATIONS

Smartphones & Tablets
Active Matrix OLED Displays

TYPICAL APPLICATION

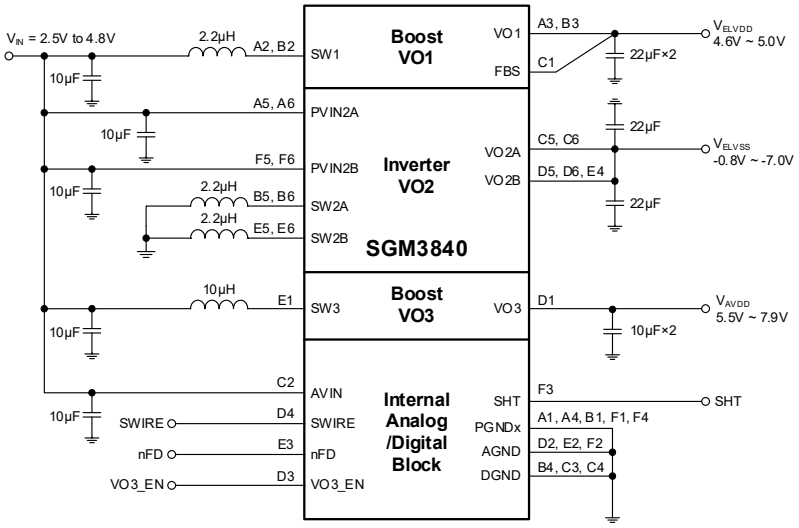


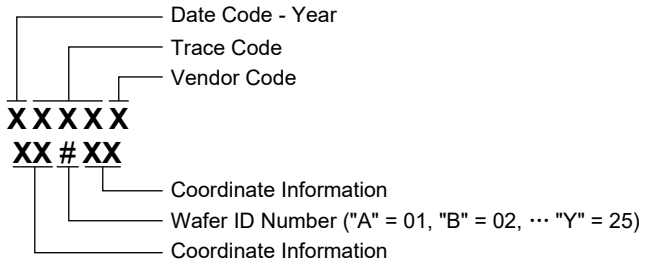
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3840	WLCSP-2.37×2.37-36B	-40℃ to +85℃	SGM3840YG/TR	17B XXXXX XX#XX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to Ground Pin)

PVIN2A, PVIN2B, AVIN, VO3_EN, SWIRE, nFD, VO1, FBS, SHT ..... -0.3V to 6V

SW1 ..... -0.3V to 6V

SW3, VO3 ..... -0.3V to 9V

VO2A, VO2B ..... -8V to 0.3V

SW2A, SW2B ..... -8.5V to 6V

Package Thermal Resistance

WLCSP-2.37×2.37-36B, θ_{JA} ..... 37℃/W

WLCSP-2.37×2.37-36B, θ_{JB} ..... 7.1℃/W

WLCSP-2.37×2.37-36B, θ_{JC} ..... 12.2℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 2000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +85℃

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

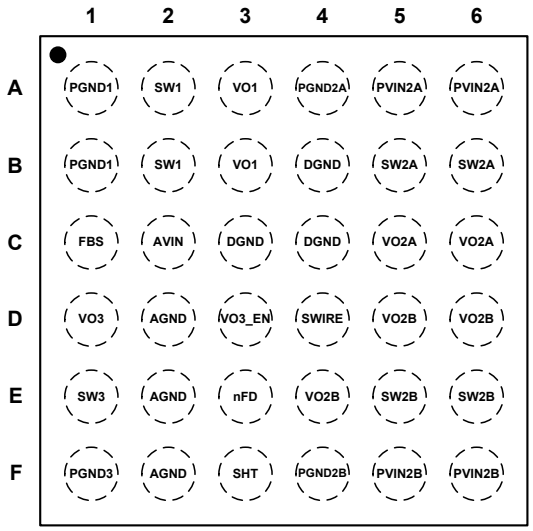
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.37×2.37-36B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1, B1	PGND1	G	VO1 Boost Converter Power Ground.
C1	FBS	I	VO1 Boost Converter Output Sense Input. It should be connected to VO1 pin or to the far-end VO1 output capacitor.
D1	VO3	O	VO3 Boost Converter Output.
E1	SW3	I	VO3 Boost Converter Switching Node.
F1	PGND3	G	VO3 Boost Converter Power Ground.
A2, B2	SW1	I	VO1 Boost Converter Switching Node.
C2	AVIN	I	Analog Input Pin.
D2, E2, F2	AGND	G	Analog Ground Pin.
A3, B3	VO1	O	VO1 Boost Converter Output.
C3	DGND	G	Digital Ground Pin.
D3	VO3_EN	I	VO3 Boost Converter Enable Pin.
E3	nFD	I	Output Discharge Enable/Disable During Shutdown. Logic low level enables the discharge and logic high level disables the discharge.
F3	SHT	O	Fault Protection (SCP, UVLO) Status Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
A4	PGND2A	G	Power Ground Pin.
B4, C4	DGND	G	Digital Ground Pin.
D4	SWIRE	I	VO1/VO2 Converter Enable Pin.
E4	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
F4	PGND2B	G	Power Ground Pin.
A5	PVIN2A	I	VO2 Inverting Buck-Boost Converter A Power Supply Input Pin.
B5	SW2A	I	VO2 Inverting Buck-Boost Converter A Switching Node.
C5	VO2A	O	VO2 Inverting Buck-Boost Converter A Output Pin.
D5	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
E5	SW2B	I	VO2 Inverting Buck-Boost Converter B Switching Node.
F5	PVIN2B	I	VO2 Inverting Buck-Boost Converter B Power Supply Input Pin.
A6	PVIN2A	I	VO2 Inverting Buck-Boost Converter A Power Supply Input Pin.
B6	SW2A	I	VO2 Inverting Buck-Boost Converter A Switching Node.
C6	VO2A	O	VO2 Inverting Buck-Boost Converter A Output Pin.
D6	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
E6	SW2B	I	VO2 Inverting Buck-Boost Converter B Switching Node.
F6	PVIN2B	I	VO2 Inverting Buck-Boost Converter B Power Supply Input Pin.

NOTE: I: input, O: output, I/O: input or output, G: ground.

ELECTRICAL CHARACTERISTICS

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE} = V_{VO3_EN} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -3V, V_{VO3} = 7.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current and Thermal Protection						
Input Voltage Range	V_{IN}		2.5		4.8	V
Shutdown Current into PVIN, AVIN	I_{SD}	V_{SWIRE} = V_{VO3_EN} = GND		0.5	1.6	μA
Quiescent Current into PVIN, AVIN	I_{QON}	V_{IN} = 3.7V, no load, V_{SWIRE} = V_{VO3_EN} = high		3.5		mA
Under-Voltage Lockout Threshold (AVIN)	V_{IT-}	V_{IN} falling	2	2.08	2.15	V
	V_{IT+}	V_{IN} rising	2.2	2.33	2.4	V
Thermal Shutdown Temperature	T_{SD}	Junction temperature rising		145		℃
		Junction temperature falling		135		℃
Logic Signals (VO3_EN, SWIRE, nFD)						
Logic High Level Voltage	V_H	V_{IN} = 2.5V to 4.8V	0.93			V
Logic Low Level Voltage	V_L	V_{IN} = 2.5V to 4.8V			0.4	V
Pull-Down Resistor of VO3_EN	R_{DOWN1}			660		kΩ
Pull-Down Resistor of SWIRE	R_{DOWN2}			2.6		MΩ
Logic Signal (SHT)						
Pull-Up Resistor to AVIN	R_{UP}			390		kΩ
Pull-Down Current	I_{DOWN}	V_{IN} = 3.7V, output short, V_{SHT} = 1V		6.7		mA
Boost Converter (V_{VO1} = V_{ELVDD})						
Positive Output 1 Voltage	V_{VO1}	4.6V to 5.0V with 0.1V/step, default 4.6V, T_J = -40℃ to +85℃	4.6	4.6	5.0	V
Positive Output 1 Voltage Accuracy		V_{VO1} = 4.6V, no load	-0.4		0.4	%
		V_{VO1} = 4.6V, no load, T_J = -40℃ to +85℃	-0.7		0.7	
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 200mA		80		mΩ
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 200mA		100		
SW1 Switch Current Limit	I_{SW1}	Inductor valley current	1.95	2.45	2.85	A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA	1.3	1.45	1.65	MHz
Output Current Capability	I_{VO1}	V_{IN} = 2.5V to 4.8V	1000			mA
Short Circuit Threshold in Operation	$V_{VO1(SCP)}$	Percentage of nominal V_{VO1}		83.5		%
Threshold of Output Sense with VO1	V_{TVO1}	V_{VO1} - V_{FBS} increasing		565		mV
Threshold of Output Sense with FBS	V_{TFBS}	V_{VO1} - V_{FBS} decreasing		420		mV
VO1 and FBS Leakage, No Discharge	I_{LEAK_VO1}	V_{nFD} = V_{IN}, V_{SWIRE} = GND		0.7	2	μA
Pull-Down Resistance of FBS	R_{FBS}			5.3		MΩ
VO1 Discharge Resistance	$R_{VO1(DCG)}$	V_{SWIRE} = GND, I_{VO1} = 20mA		65		Ω
VO1 Discharge Time	t_{DVO1}	V_{SWIRE} = GND		5		ms
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 2.7V to 4.5V		±0.002		%/V
Line Regulation	$VO1_{LINEREG}$	No load, V_{IN} = 2.7V to 4.5V		±0.002		%/V
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1_VO2} = 0 to 150mA		10		mV_{PP}
Load Regulation	$VO1_{LOADREG}$	1mA ≤ I_{VO1} ≤ 1A		±0.05		%/A

ELECTRICAL CHARACTERISTICS (continued)

(At T_J = +25℃, V_{IN} = 3.7V, V_{SWIRE} = V_{VO3_EN} = V_{IN}, V_{VO1} = 4.6V, V_{VO2} = -3V, V_{VO3} = 7.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck-Boost Converter (V_{VO2} = V_{ELVSS})						
Negative Output Voltage Range	V_{VO2}	-7.0V to -0.8V with 0.1V/step, default -3.0V, T_J = -40℃ to +85℃	-7.0	-3.0	-0.8	V
Negative Output Voltage Accuracy		V_{VO2} = -3V, no load, T_J = -40℃ to +85℃	-30		30	mV
SW2 MOSFET On-Resistance-Phase A	$R_{DS(ON)A1}$	I_{DS} = 200mA		150		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase A	$R_{DS(ON)A2}$	I_{DS} = 200mA		95		
SW2 MOSFET On-Resistance-Phase B	$R_{DS(ON)B1}$	I_{DS} = 200mA		150		mΩ
SW2 MOSFET Rectifier On-Resistance-Phase B	$R_{DS(ON)B2}$	I_{DS} = 200mA		95		
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA	1.05	1.2	1.35	MHz
Output Current Capability	I_{VO2}	V_{IN} = 2.5V to 4.8V, V_{VO2} = -3V	1000			mA
		V_{IN} = 3.1V to 4.8V, V_{VO2} = -6V	1000			mA
SW2 Switch Current Limit-Phase A	I_{SW2A}	Inductor peak current		3.65		A
SW2 Switch Current Limit-Phase B	I_{SW2B}	Inductor peak current		3.65		A
Average Load Current Threshold with Dual-Phase	$I_{RMSA\&B}$	Load current rising		360		mA
Average Load Current Threshold with Phase A Only	I_{RMSA}	Load current falling		150		mA
Short Circuit Threshold in Operation	$V_{VO2(SCP)}$	Percentage of nominal V_{VO2}		80		%
VO2 Discharge Resistance	$R_{VO2(DCG)}$	V_{SWIRE} = GND, I_{VO2} = 20mA		25		Ω
VO2 Discharge Time	t_{DVO2}	V_{SWIRE} = GND		3		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}	V_{nFD} = V_{IN}, V_{SWIRE} = GND		0.8	2.2	μA
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 2.7V to 4.5V		±0.002		%/V
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO1_VO2} = 0 to 150mA		10		mV_{PP}
Load Regulation	$VO2_{LOADREG}$	1mA ≤ I_{VO2} ≤ 1A		±0.05		%/A
Boost Converter (V_{VO3} = V_{AVDD})						
Positive Output 2 Voltage Range	V_{VO3}	5.5V to 7.9V with 0.1V/step, default 7.3V, T_J = -40℃ to +85℃	5.5	7.3	7.9	V
Positive Output 2 Voltage Accuracy		V_{VO3} = 7.3V, no load, T_J = -40℃ to +85℃	-0.8		0.8	%
SW3 MOSFET On-Resistance	$R_{DS(ON)31}$	I_{DS} = 200mA		325		mΩ
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)32}$	I_{DS} = 200mA		485		
SW3 Switch Current Limit	I_{SW3}	Inductor peak current	0.85	1.3	1.75	A
SW3 Switching Frequency	f_{SW3}	I_{VO3} = 30mA	1.3	1.45	1.65	MHz
Output Current Capability	I_{VO3}	V_{IN} = 2.7V to 4.8V	150			mA
Short Circuit Threshold in Operation	$V_{VO3(SCP)}$	Percentage of nominal V_{VO3}		84.5		%
VO3 Leakage, No Discharge	I_{LEAK_VO3}	V_{nFD} = V_{IN}, V_{VO3_EN} = GND		2.2	3.5	μA
VO3 Discharge Resistance	$R_{VO3(DCG)}$	V_{VO3_EN} = GND, I_{VO3} = 20mA		50		Ω
VO3 Discharge Time	t_{DVO3}	V_{VO3_EN} = GND		2		ms
Line Regulation	$VO3_{LINEREG}$	I_{VO3} = 30mA, V_{IN} = 2.7V to 4.5V		±0.01		%/V
Output Voltage Ripple	$VO3_{RIPPLE}$	I_{VO3} = 0 to 100mA		10		mV_{PP}
Load Regulation	$VO3_{LOADREG}$	1mA ≤ I_{VO3} ≤ 150mA		±0.01		%/A

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short Circuit Timer					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$	1.8	2.1	2.4	ms
VO1 Short Circuit Detection Time in Operation		0.6	0.7	0.8	
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$	5.5	6.4	7.2	
VO2 Short Circuit Detection Time in Operation		0.6	0.7	0.8	
VO3 Short Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$		2.6		
VO3 Short Circuit Detection Time in Operation		0.6	0.7	0.8	
Power Sequence					
VO1 Start-Up Time	t_{SS1}		3.2		ms
VO2 Start-Up Time	t_{SS2}		1.5		
VO2 Start-Up Time Delay after VO1	t_{DELAY}		2.7		
SWIRE Interface					
Initialization Time	t_{INIT}		350	450	μs
Shutdown Time Period	t_{OFF}	35	55	80	
Pulse High Level Time Period	t_{HIGH}	2	10	20	
Pulse Low Level Time Period	t_{LOW}	2	10	20	
Data Storage/Accept Time Period	t_{STORE}	35	55	80	

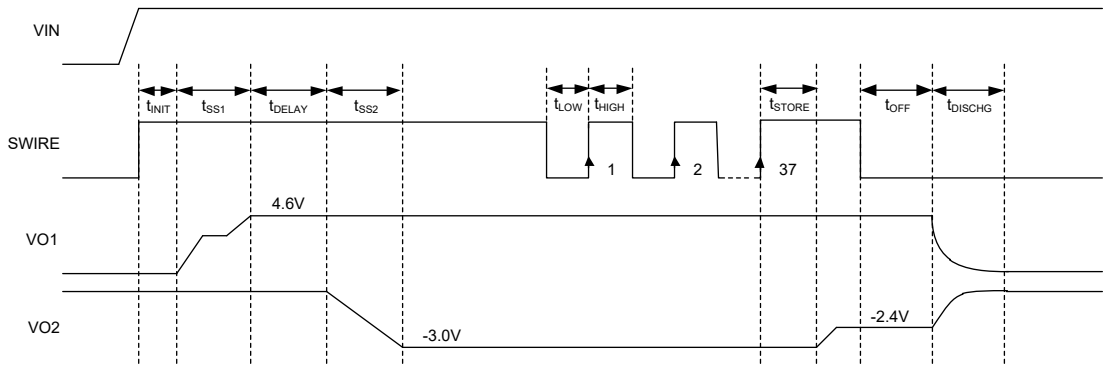
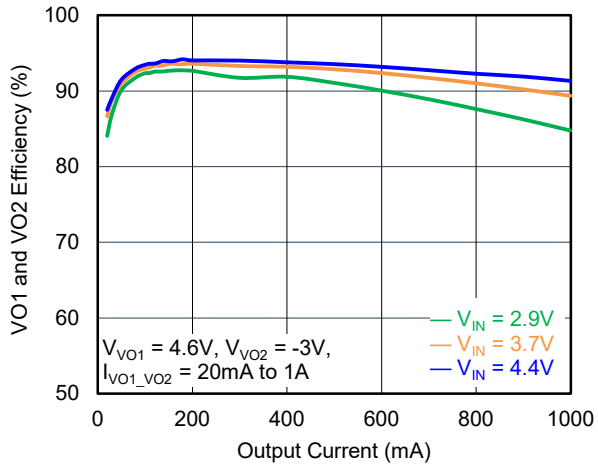


Figure 2. Timing Diagram

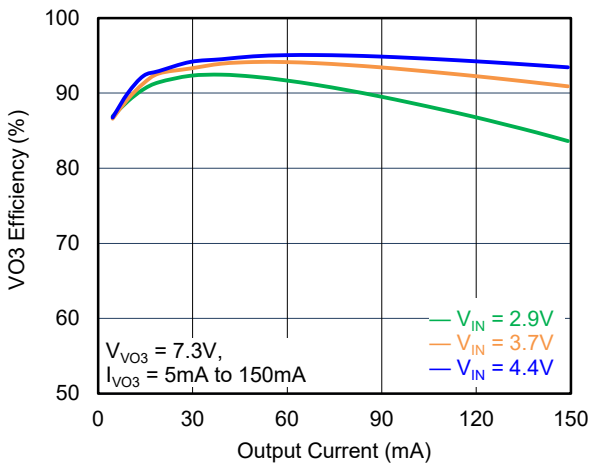
Figure 3. V_{ELVSS} Transition Time Control

TYPICAL PERFORMANCE CHARACTERISTICS

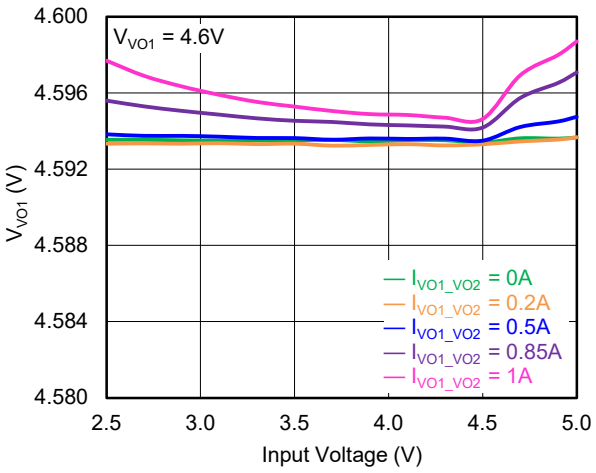
VO1 and VO2 Combined Efficiency vs. Output Current



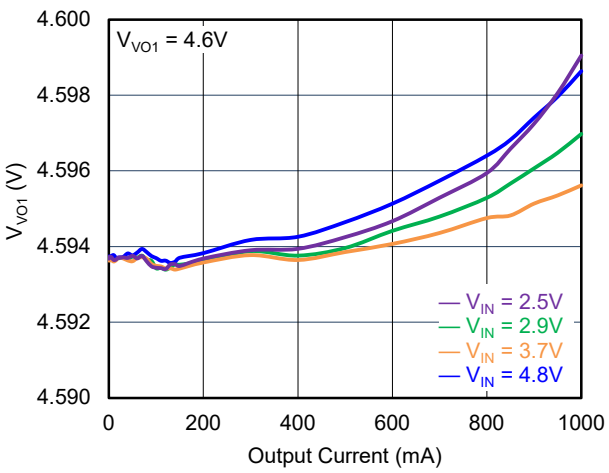
VO3 Efficiency vs. Output Current



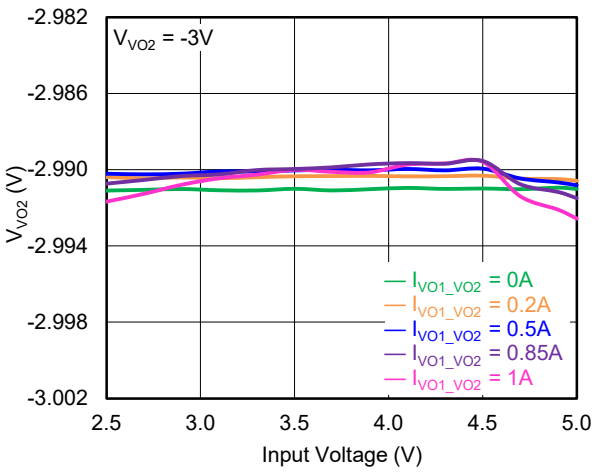
VO1 Line Regulation



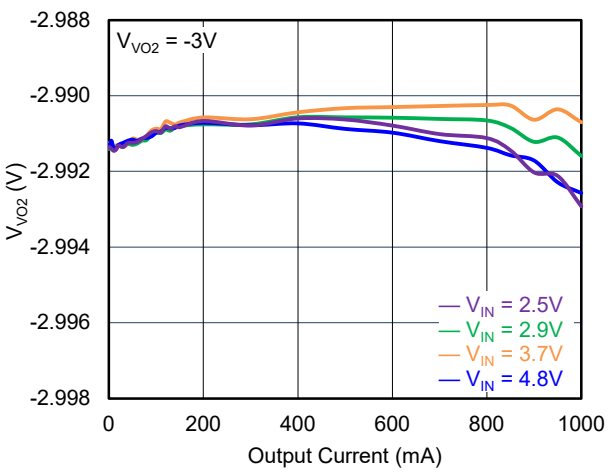
VO1 Load Regulation



VO2 Line Regulation

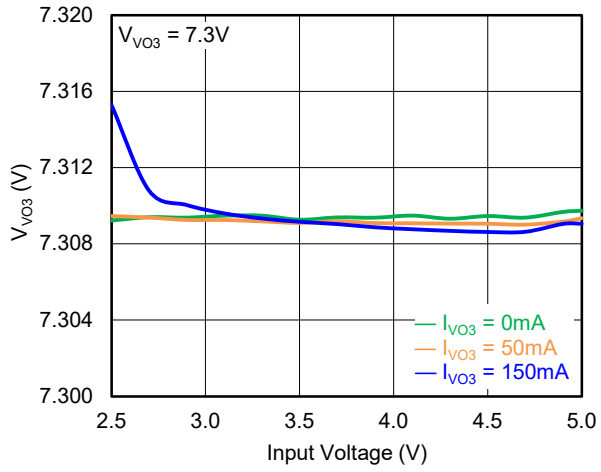


VO2 Load Regulation

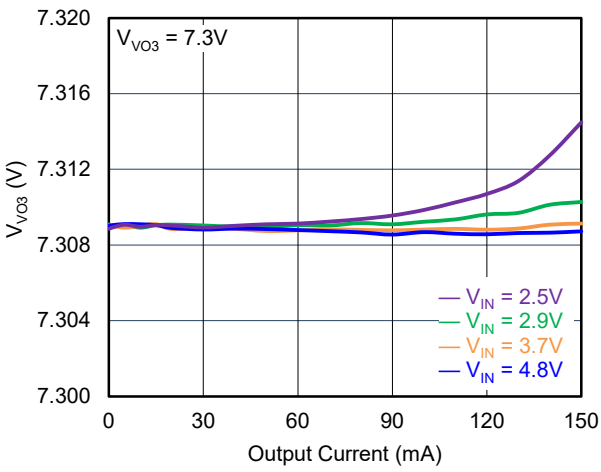


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

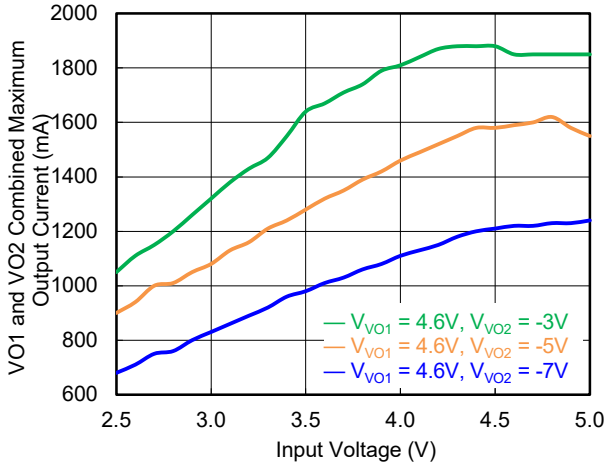
VO3 Line Regulation



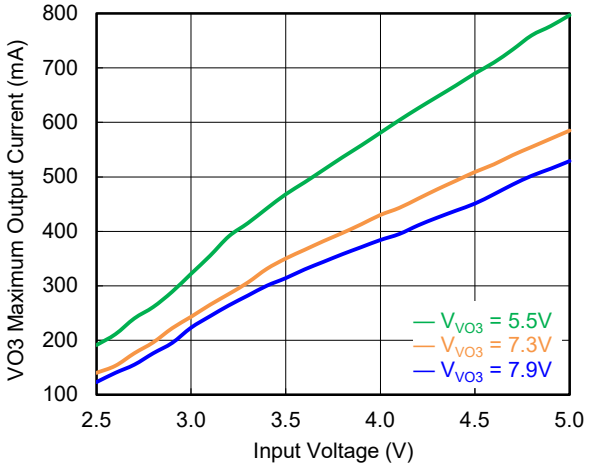
VO3 Load Regulation



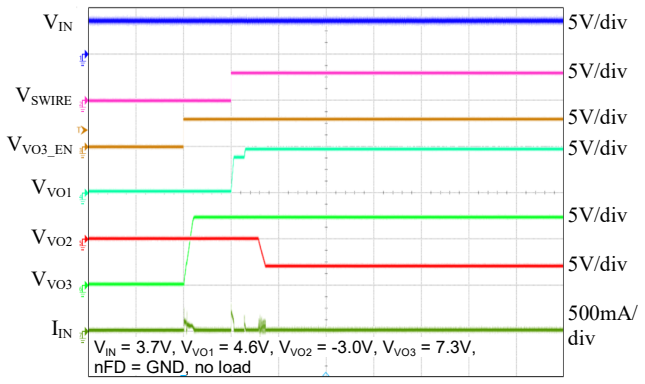
VO1 and VO2 Combined Maximum Output Current vs. Input Voltage



VO3 Maximum Output Current vs. Input Voltage

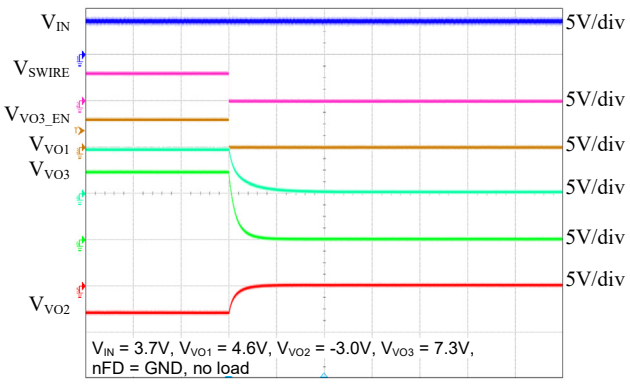


Start-Up Sequence



Time (10ms/div)

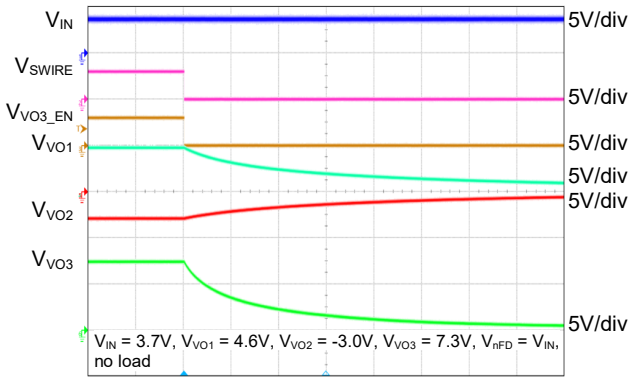
Shutdown Sequence Discharge = ON



Time (5ms/div)

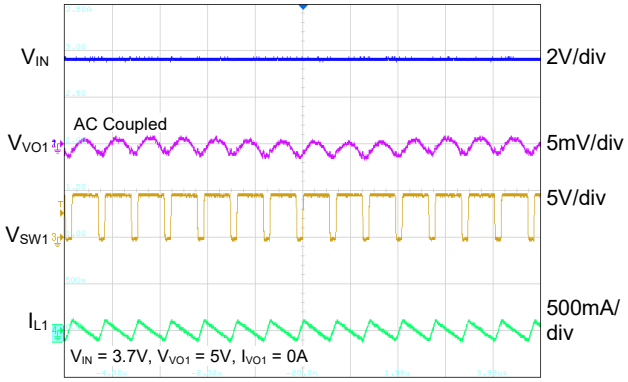
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Shutdown Sequence Discharge = OFF



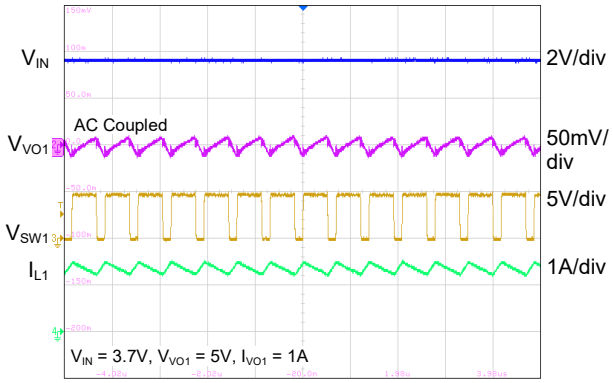
Time (5s/div)

VO1 Output Ripple at No Load



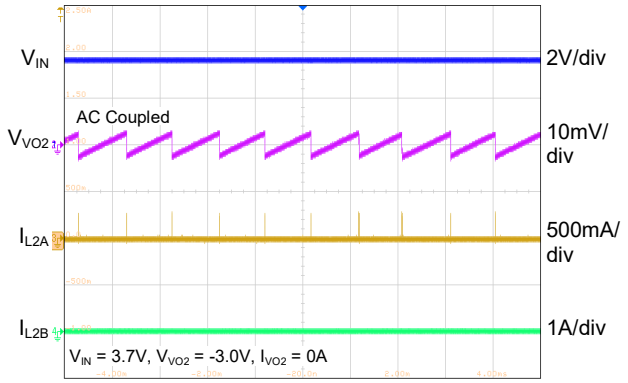
Time (1μs/div)

VO1 Output Ripple at Full Load



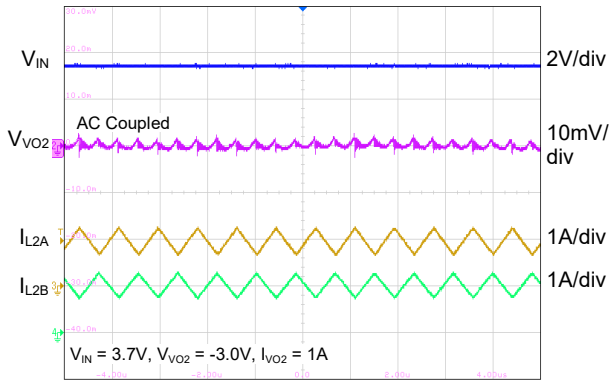
Time (1μs/div)

VO2 Output Ripple at No Load



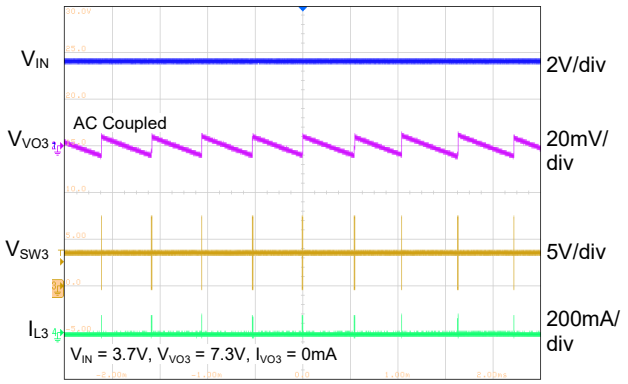
Time (1ms/div)

VO2 Output Ripple at Full Load



Time (1μs/div)

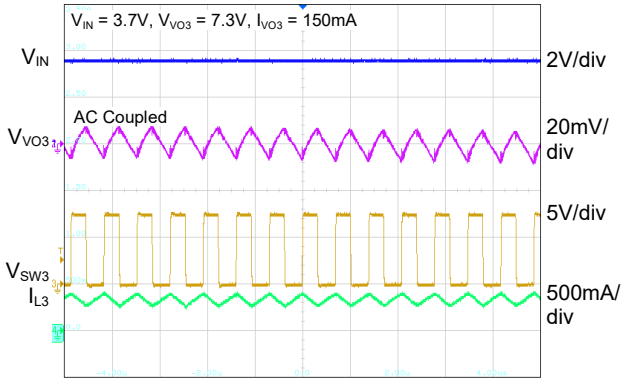
VO3 Output Ripple at No Load



Time (500μs/div)

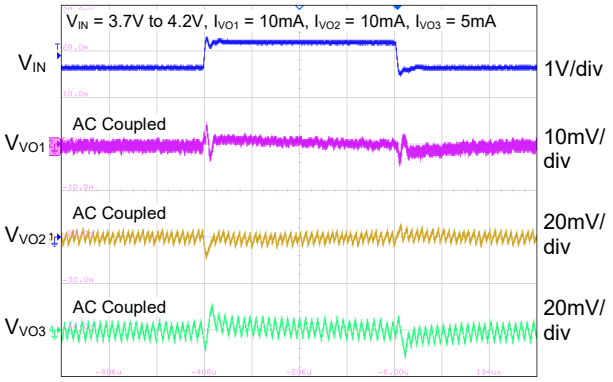
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO3 Output Ripple at Full Load



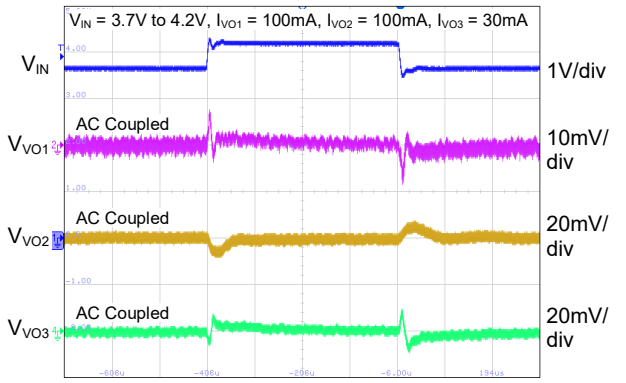
Time (1μs/div)

Line Transient at Light Load



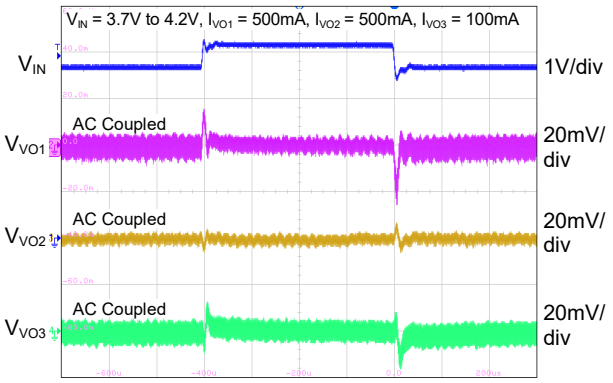
Time (100μs/div)

Line Transient at Moderate Load



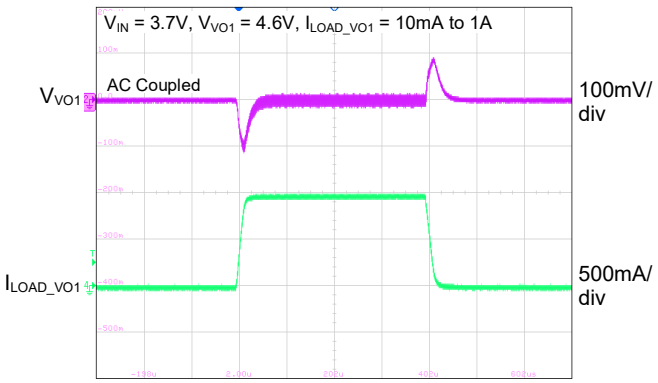
Time (100μs/div)

Line Transient at Heavy Load



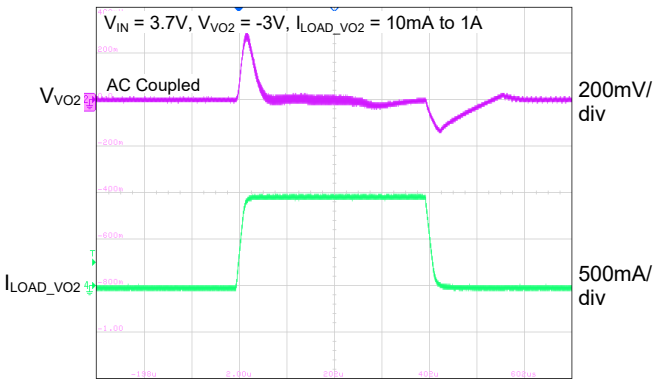
Time (100μs/div)

VO1 Load Transient



Time (100μs/div)

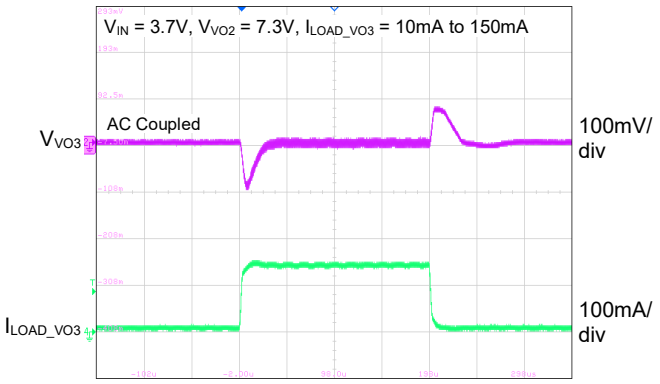
VO2 Load Transient



Time (100μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO3 Load Transient



Time (50μs/div)

FUNCTIONAL BLOCK DIAGRAM

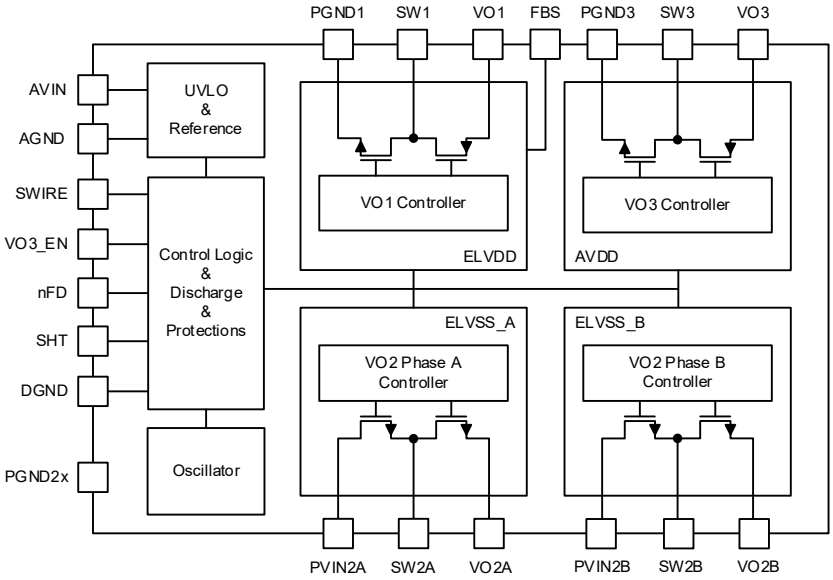


Figure 4. Functional Block Diagram

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended Component Selection

Converter	Component	Value	Total Number	Electrical Spec	Part Number	Manufacturer
ELVDD	C_{IN1}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO1}	22μF	2	X5R, 6.3V, 0603	GRM188R60J226MEA0	Murata
	L_{VO1}	2.2μH	1	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
ELVSS	C_{PVIN2A} C_{PVIN2B}	10μF	2	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO2A} C_{VO2B}	22μF	2	X5R, 10V, 0603	GRM187R61A226ME15	Murata
	L_{VO2A} L_{VO2B}	2.2μH	2	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
AVDD	C_{IN3}	10μF	1	X5R, 6.3V, 0402	GRM155R60J106ME05	Murata
	C_{VO3}	10μF	2	X5R, 16V, 0603	GRM188R61C106KAAL	Murata
	L_{VO3}	10μH	1	1.3A, 390mΩ, 252012	SDEM25201B-100MS	Cyntec

DETAILED DESCRIPTION

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down all the outputs when the junction temperature exceeds +145℃ (TYP), and restarts with the same programmed voltages and sequences when the temperature decreases to +135℃ (TYP).

Boost Converter VO1 (ELVDD)

The Boost converter VO1 operates with a valley-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO1 output voltage can be programmed between 4.6V and 5.0V (default 4.6V) with 100mV steps (see Table 2).

The output sense pin (FBS) is always connected to the positive pin of output capacitor for the highest output voltage accuracy. The wide hysteresis voltage makes the device suitable for large path loss applications. Additionally, the Boost converter can sense the output voltage with the VO1 pin, when the FBS pin is floating or connected to ground or connected as close to the VO1 pin as possible.

The output of VO1 is fully isolated in shutdown mode.

Inverting Buck-Boost Converter VO2 (ELVSS)

The inverting Buck-Boost converter VO2 operates with a peak-current-mode topology and dual-phase fixed 1.2MHz (TYP) frequency. The VO2 output voltage can be programmed between -7.0V and -0.8V (default -3.0V) with 100mV steps (see Table 2).

When the load current exceeds 360mA, both phase A and phase B of the inverting Buck-Boost converter work. And only phase A works when the load current decreases to 150mA for reducing the switching loss.

The output of VO2 is fully isolated in shutdown mode.

Boost Converter VO3 (AVDD)

The Boost converter VO3 operates with a peak-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO3 output voltage can be programmed between 5.5V and 7.9V (default 7.3V) with 100mV steps (see Table 2).

The output of VO3 is fully isolated in shutdown mode.

Output Current Capacity

The device operates with an input voltage range of 2.5V to 4.8V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 2.5V and 4.8V. To achieve full performance, a stable and noise-free input source is needed. Once the distance between input source and SGM3840 is a bit long, additional capacitors are suggested to place as close to the device as possible. Please refer to the typical application circuit for the suggested input capacitance.

SGMICRO has patented circuits to solve the spike problem of V_{ELVDD} due to mode switching when the input voltage rises close to or higher than the programmed V_{ELVDD}.

Fault Protection Status (SHT)

The SHT is an interface to indicate a fault protection (SCP, UVLO) status. SHT is internally pulled up to AVIN through a 390kΩ resistor, and it will be pulled down to AGND when fault protection (SCP or UVLO) occurs.

DETAILED DESCRIPTION (continued)

Digital Interface (SWIRE Pin)

The positive output voltages V_{ELVDD}, V_{AVDD} and the negative output voltage V_{ELVSS} can be programmed through the SWIRE digital interface with 100mV steps.

Figure 2 shows an example for SGM3840 programming V_{ELVSS} to -2.4V. The SWIRE pin can be used as a standard enable pin if programming is not required.

The device starts with its default values (green marked values in Table 2) if enabled. The SWIRE interface counts the rising edges to set the corresponding values as shown in Table 2. The device utilizes a volatile memory to store the settings.

Table 2. Programming Table

Rising Edges	VO2 (V_{ELVSS})	Rising Edges	VO2 (V_{ELVSS})	Rising Edges	VO3 (V_{AVDD})	Rising Edges	Outputs Discharge	Rising Edges	VO2 (V_{ELVSS})
0/no pulse	-3.0V	27	-3.4V	0/no pulse	7.3V	0/no pulse	controlled by nFD pin	93	-7.0V
1	-6.0V	28	-3.3V	54	5.5V	79	ON	94	-6.9V
2	-5.9V	29	-3.2V	55	5.6V	80	OFF	95	-6.8V
3	-5.8V	30	-3.1V	56	5.7V			96	-6.7V
4	-5.7V	31	-3.0V	57	5.8V	Rising Edges	VO2 Transition Time	97	-6.6V
5	-5.6V	32	-2.9V	58	5.9V	0/no pulse	12ms	98	-6.5V
6	-5.5V	33	-2.8V	59	6.0V	81	fast	99	-6.4V
7	-5.4V	34	-2.7V	60	6.1V	82	12ms	100	-6.3V
8	-5.3V	35	-2.6V	61	6.2V			101	-6.2V
9	-5.2V	36	-2.5V	62	6.3V	Rising Edges	VO1 (V_{ELVDD})	102	-6.1V
10	-5.1V	37	-2.4V	63	6.4V	0/no pulse	4.6V		
11	-5.0V	38	-2.3V	64	6.5V	83	4.6V		
12	-4.9V	39	-2.2V	65	6.6V	84	4.7V		
13	-4.8V	40	-2.1V	66	6.7V	85	4.8V		
14	-4.7V	41	-2.0V	67	6.8V	86	4.9V		
15	-4.6V	42	-1.9V	68	6.9V	87	5.0V		
16	-4.5V	43	-1.8V	69	7.0V				
17	-4.4V	44	-1.7V	70	7.1V				
18	-4.3V	45	-1.6V	71	7.2V				
19	-4.2V	46	-1.5V	72	7.3V				
20	-4.1V	47	-1.4V	73	7.4V				
21	-4.0V	48	-1.3V	74	7.5V				
22	-3.9V	49	-1.2V	75	7.6V				
23	-3.8V	50	-1.1V	76	7.7V				
24	-3.7V	51	-1.0V	77	7.8V				
25	-3.6V	52	-0.9V	78	7.9V				
26	-3.5V	53	-0.8V						

DETAILED DESCRIPTION (continued)

Soft-Start, Discharge, Start-Up and Timing Shutdown

The built-in soft-start function is adopted to limit the inrush current.

The output discharge function can be controlled by both nFD pin and SWIRE interface, where SWIRE interface has the higher priority. The discharge function follows the connection status of nFD pin until SWIRE pulse 79 or 80 is applied. In this case, if nFD = low or high impedance, all outputs are discharged when the device is shutdown. Once SWIRE counts 79 (discharge function ON) or 80 (discharge function OFF) pulses, the function follows the SWIRE and the nFD pin does not function. Only power resetting can reset the output discharge, and then output discharge is controlled by nFD pin.

Toggling SWIRE high or with relevant pulses enables the VO1 Boost converter. VO1 starts with a 0.2A soft-start current limit until it rises to the programmed voltage. Then the full current limit is active (2.45A, TYP).

6ms after toggling SWIRE high, the VO2 converter starts switching phase A (VO2A) with a 0.55A current limit until the VO2 rises to the default voltage (-3V). Then the full current limit is active (3.65A per phase, TYP).

Toggling VO3_EN high starts the VO3 Boost converter. Before VO3 rises to the default value (7.3V), it rises linearly for 1.5ms with a 0.35A current limit. Then the full current limit is active (1.2A, TYP).

Overload and Short Circuit Protection (SCP)

The built-in short circuit protection (SCP) prevents the device from damage. If any of the three outputs (VO1, VO2 and VO3) is shorted to the ground or VO1 and VO2 are shorted together, the SGM3840 will trigger the function.

When a short or an overload occurs, all the three converters stop switching, the outputs are shut down and latched.

Only resetting the power supply or pulling VO3_EN and SWIRE low at the same time for more than t_{OFF} can restart the device.

A SCP or overload occurs if any of the following events happens:

- V_{ELVDD} is not in regulation 2.1ms after V_{ELVDD} is enabled (SWIRE = high for longer than 2.1ms) then all converters shut down.
- V_{ELVSS} is not in regulation 6.4ms after V_{ELVSS} is enabled (SWIRE = high for longer than 12ms) then all converters shut down.
- V_{AVDD} protection is enabled when the soft-start is completed.
- V_{ELVDD} falls below 83.5% of the programmed output voltage longer than 0.7ms then all converters shut down.
- V_{ELVSS} rises above 80% of the programmed output voltage longer than 0.7ms then all converters shut down.
- V_{AVDD} falls below 84.5% of the programmed output voltage longer than 0.7ms then all converters shut down.

Device Reset

- Power resetting resets the device to default settings.
- Short circuit and overload protection reset all settings except for discharge controlled by SWIRE.
- Pulling SWIRE low for t_{OFF} then V_{ELVDD} and V_{ELVSS} are reset to default values of 4.6V and -3.0V, respectively.
- Pulling SWIRE low for t_{OFF} then V_{ELVSS} transition time is reset to default value of 12ms.
- Pulling VO3_EN and SWIRE low at the same time for t_{OFF} resets the SCP or overloading latch-up.

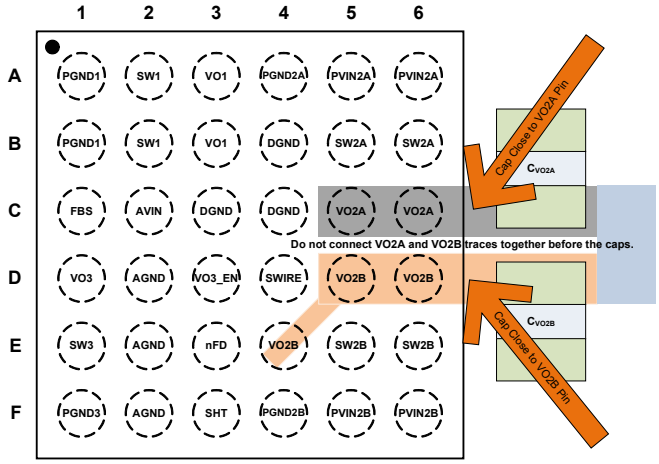
DETAILED DESCRIPTION (continued)

Layout Guideline

AMOLED displays are sensitive to quality of power supplies. A good PCB layout is quite important to reduce the ripple and to enhance the line and load transients, as well as to achieve better noise, better EMI and loop stability.

It is recommended to follow the below PCB layout guidelines:

• A common ground plane between AGND and PGND can minimize ground shifts.
• Traces of switching nodes (SW1, SW2A, SW2B and SW3) should be short and wide.
• Place input and output capacitors as close as possible to the related pins.
• Use short and wide traces to connect the input and output capacitors to the related pins.
• A common ground plane is between the ground pins of input capacitors and output capacitors.
• AVIN requires an independent input capacitor.
• Do not connect VO2A and VO2B traces together before connecting the output capacitors.
• Must put the VO2A and VO2B capacitors close to the VO2A and VO2B pins.



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

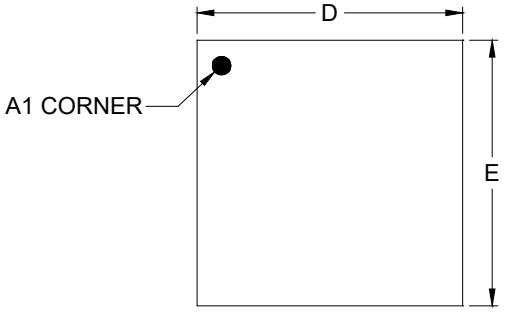
AUGUST 2025 – REV.A.1 to REV.A.2	Page
Added Layout Guideline	17

JANUARY 2025 – REV.A to REV.A.1	Page
Changed Figure 4	13

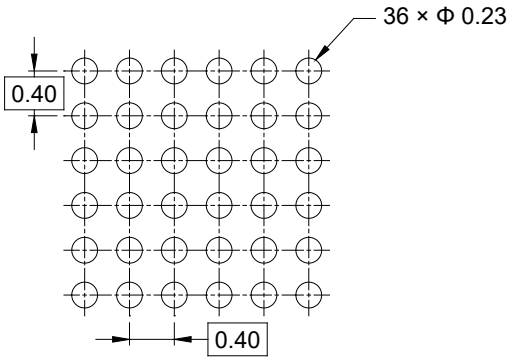
Changes from Original to REV.A (AUGUST 2024)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

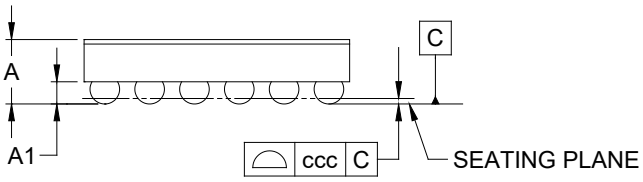
WLCSP-2.37×2.37-36B



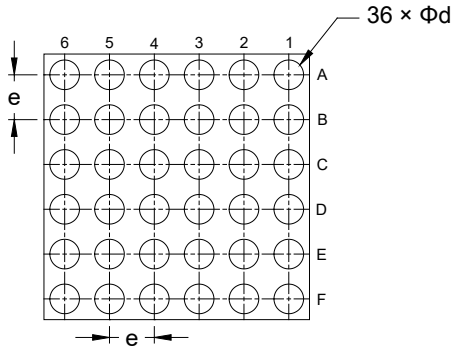
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



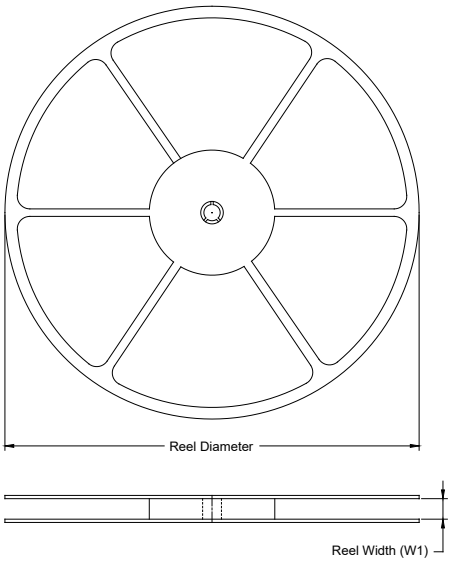
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.620
A1	0.178	-	0.218
D	2.340	-	2.400
E	2.340	-	2.400
d	0.234	-	0.294
e	0.400 BSC		
ccc	0.050		

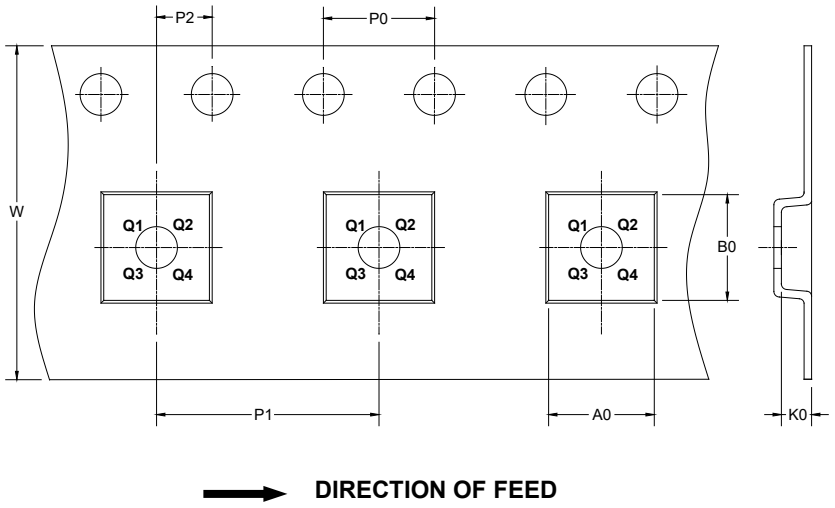
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



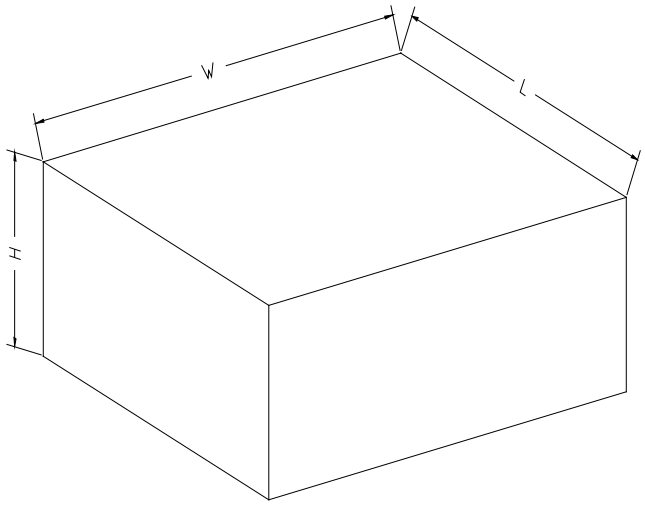
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.37×2.37-36B	7"	9.5	2.55	2.55	0.80	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002