74LVC1G32
Single 2-Input OR Gate

GENERAL DESCRIPTION

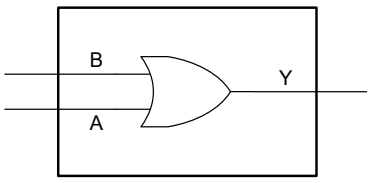
The 74LVC1G32 is a single 2-input OR gate that is designed for 1.65V to 5.5V V_{CC} operation. Both 3.3V and 5V devices can drive inputs, enabling this device to operate as translator in a mixed 3.3V and 5V system environment. All inputs support Schmitt-trigger action, which allows the circuit to tolerate slower input rise and fall times. The device also features the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

The device is capable of holding high output drive while low static power dissipation can be maintained over supply voltage operating range. This device is highly suitable for partial power-down applications by using power-off leakage current (I_{OFF}) circuit. When the device is powered down, the output is disabled, and the current backflow can be prevented from passing through the device.

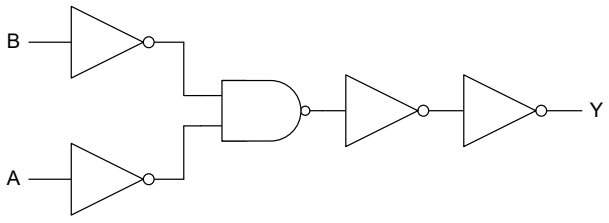
FEATURES

- **Wide Supply Voltage Range: 1.65V to 5.5V**
- **Inputs Accept Voltages up to 5.5V**
- **+32mA/-32mA Output Current**
- **CMOS Low Power Dissipation**
- **High Noise Immunity**
- **Direct Interface with TTL Levels**
- **Latch-Up Performance Exceeds 250mA**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SC70-5, SOT-23-5 and XTDFN-0.8×0.8-4AL Packages**

LOGIC SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUT		OUTPUT
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	H

$Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$

H = High Voltage Level

L = Low Voltage Level

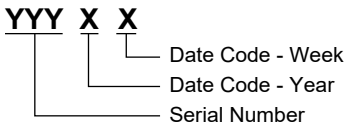
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC1G32	SC70-5	-40℃ to +125℃	74LVC1G32XC5G/TR	R57XX	Tape and Reel, 3000
	SOT-23-5	-40℃ to +125℃	74LVC1G32XN5G/TR	MEYXX	Tape and Reel, 3000
	XTDFN-0.8×0.8-4AL	-40℃ to +125℃	74LVC1G32XXGO4G/TR	1X	Tape and Reel, 10000

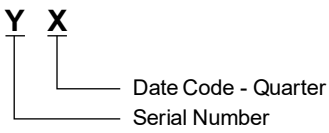
MARKING INFORMATION

NOTE: XX = Date Code. X = Date Code.

SC70-5/SOT-23-5



XTDFN-0.8×0.8-4AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 6.5V
Input Voltage Range, V_I (2) ..... -0.5V to 6.5V
Output Voltage Range, V_O (2)
Active Mode ..... -0.5V to MIN(6.5V, V_{CC} + 0.5V)
Power-Down Mode (V_{CC} = 0V)..... -0.5V to 6.5V
Input Clamp Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamp Current, I_{OK} (V_O < 0V) .....-50mA
Continuous Output Current, I_O (V_O = 0V to V_{CC})..... ±50mA
Continuous Current through V_{CC} or GND..... ±50mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} .....1.65V to 5.5V
Input Voltage Range, V_I.....0V to 5.5V
Output Voltage Range, V_O
Active Mode ..... 0V to V_{CC}
Power-Down Mode (V_{CC} = 0V).....0V to 5.5V
Output Current, I_O ..... ±32mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.65V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 5.5V ..... 10ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

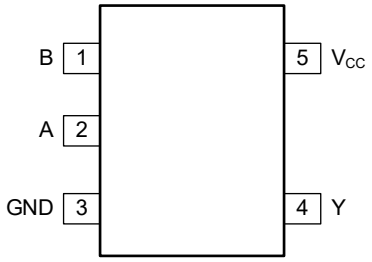
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

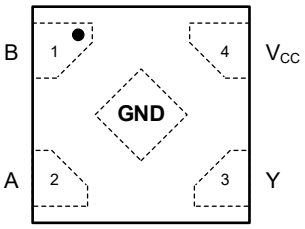
PIN CONFIGURATIONS

(TOP VIEW)



SC70-5/SOT-23-5

(TOP VIEW)



XTDFN-0.8×0.8-4AL

PIN DESCRIPTION

PIN		NAME	FUNCTION
SC70-5/SOT-23-5	XTDFN-0.8×0.8-4AL		
1, 2	1, 2	B, A	Data Inputs.
3	Exposed Pad	GND	Ground.
4	3	Y	Data Output.
5	4	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	Full	0.68 × V_{CC}			V
		V_{CC} = 2.3V to 2.7V	Full	1.7			
		V_{CC} = 2.7V to 3.6V	Full	2.0			
		V_{CC} = 4.5V to 5.5V	Full	0.7 × V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V	Full			0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V	Full			0.7	
		V_{CC} = 2.7V to 3.6V	Full			0.8	
		V_{CC} = 4.5V to 5.5V	Full			0.3 × V_{CC}	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 5.5V, I_O = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.01		V
		V_{CC} = 1.65V, I_O = -4mA	Full	1.43	1.55		
		V_{CC} = 2.3V, I_O = -8mA	Full	2.02	2.18		
		V_{CC} = 2.7V, I_O = -12mA	Full	2.38	2.56		
		V_{CC} = 3.0V, I_O = -24mA	Full	2.52	2.74		
		V_{CC} = 4.5V, I_O = -32mA	Full	4.00	4.22		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65V to 5.5V, I_O = 100μA	Full		0.01	0.05	V
		V_{CC} = 1.65V, I_O = 4mA	Full		0.10	0.22	
		V_{CC} = 2.3V, I_O = 8mA	Full		0.12	0.28	
		V_{CC} = 2.7V, I_O = 12mA	Full		0.16	0.34	
		V_{CC} = 3.0V, I_O = 24mA	Full		0.30	0.56	
		V_{CC} = 4.5V, I_O = 32mA	Full		0.32	0.60	
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND	Full		±0.01	±1	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 5.5V	Full		±0.01	±1	μA
Supply Current	I_{CC}	V_{CC} = 1.65V to 5.5V, V_I = 5.5V or GND, I_O = 0A	Full		0.01	1	μA
Additional Supply Current	ΔI_{CC}	Per pin, V_{CC} = 2.3V to 5.5V, V_I = V_{CC} - 0.6V, I_O = 0A	Full		0.05	10	μA
Input Capacitance	C_I	V_{CC} = 3.3V, V_I = GND to V_{CC}	+25℃		3.5		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit, see Figure 2 for waveforms. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃ and V_{CC} = 1.8V, 2.5V, 2.7V, 3.3V and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	A, B to Y, see Figure 2	V_{CC} = 1.65V to 1.95V	Full	0.1	7.2	15.5	ns
			V_{CC} = 2.3V to 2.7V	Full	0.5	3.9	8.5	
			V_{CC} = 2.7V	Full	0.5	3.5	7.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	3.2	6.5	
			V_{CC} = 4.5V to 5.5V	Full	0.1	2.7	5.0	
Power Dissipation Capacitance (3)	C_{PD}	V_{CC} = 3.3V, V_I = GND to V_{CC}		+25℃		18.0		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

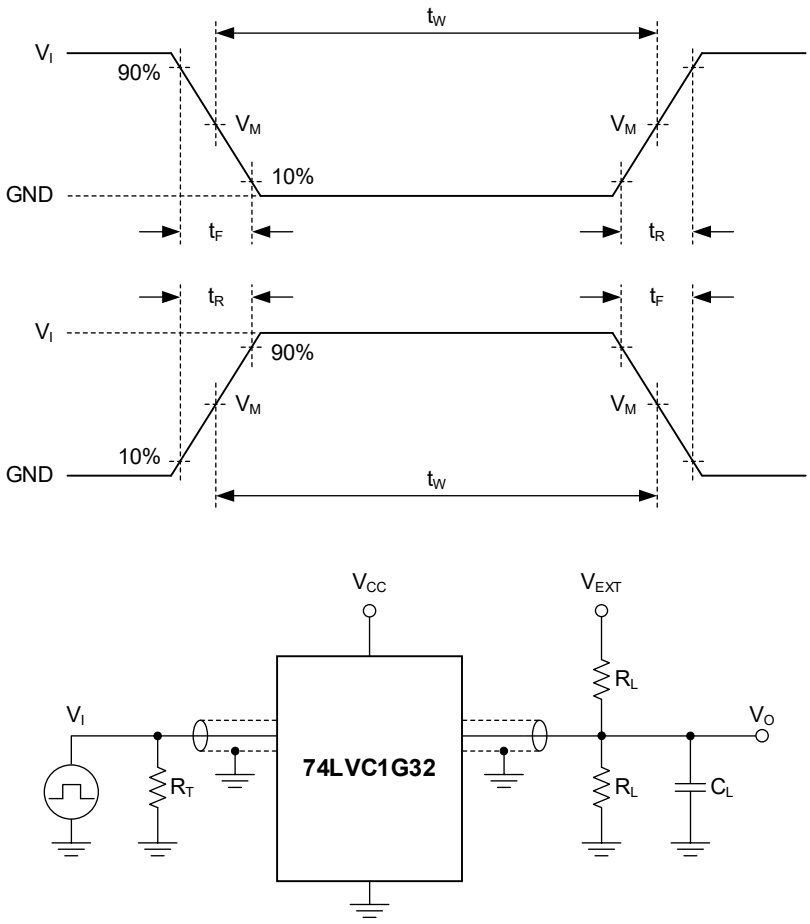
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

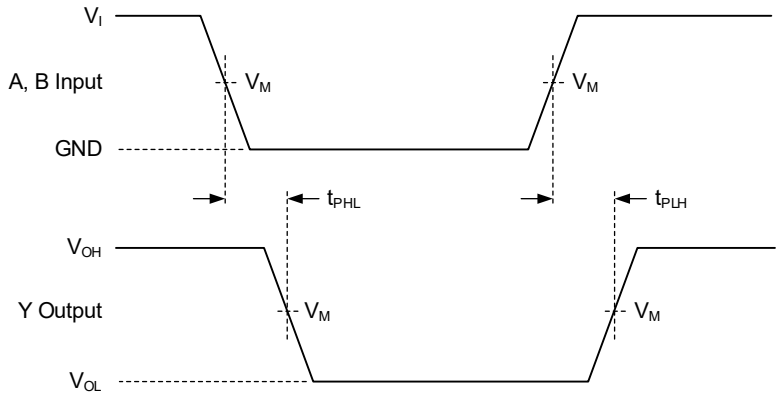
V_{EXT}: External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open
4.5V to 5.5V	V_{CC}	≤ 2.5ns	50pF	500Ω	Open

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input A, B to Output Y Propagation Delays

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.65V to 1.95V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	2.7V	1.5V	1.5V
3.0V to 3.6V	2.7V	1.5V	1.5V
4.5V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MARCH 2024 – REV.A.2 to REV.A.3	Page
Added XTDFN-0.8×0.8-4AL package	All

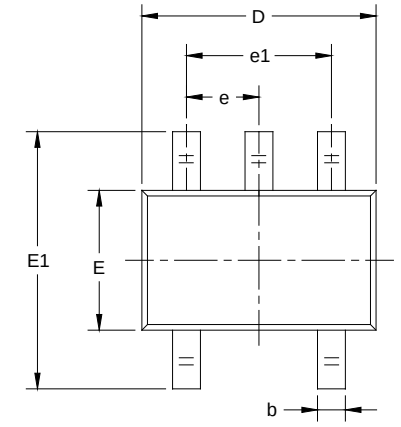
JULY 2022 – REV.A.1 to REV.A.2	Page
Updated Electrical Characteristics section	4
Added SOT-23-5 package	All

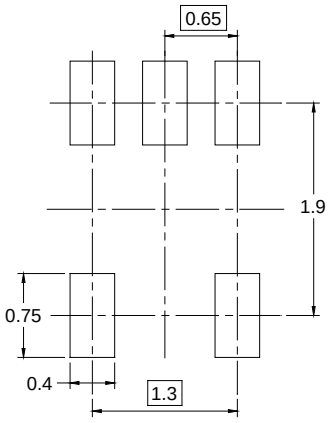
NOVEMBER 2021 – REV.A to REV.A.1	Page
Updated Dynamic Characteristics section	5
Added note of Table 2	7

Changes from Original (FEBRUARY 2021) to REV.A	Page
Changed from product preview to production data	All

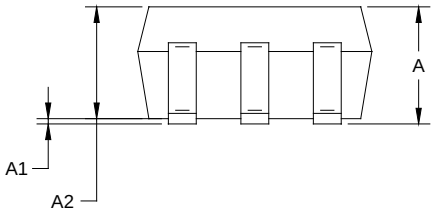
PACKAGE OUTLINE DIMENSIONS

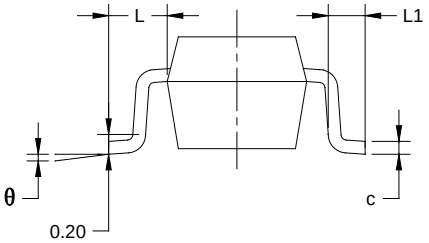
SC70-5





RECOMMENDED LAND PATTERN (Unit: mm)



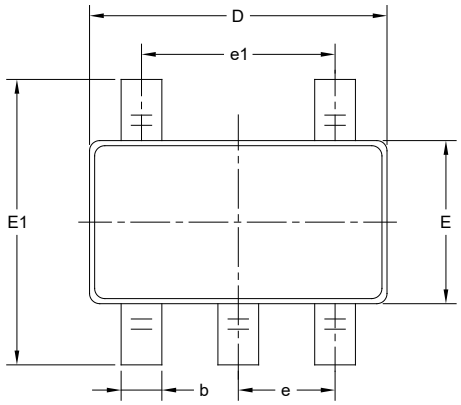


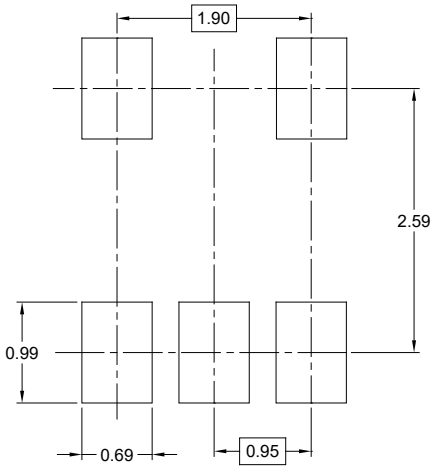
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.220	0.003	0.009
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.65 TYP		0.026 TYP	
e1	1.300 BSC		0.051 BSC	
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

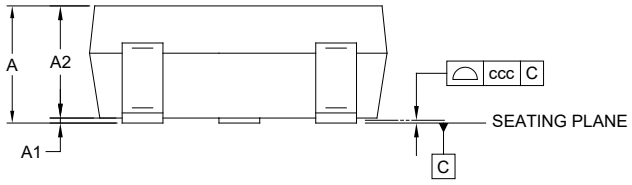
PACKAGE OUTLINE DIMENSIONS

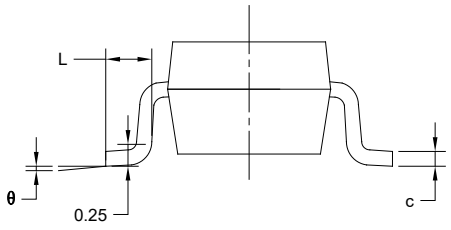
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



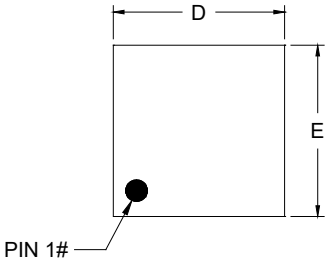


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

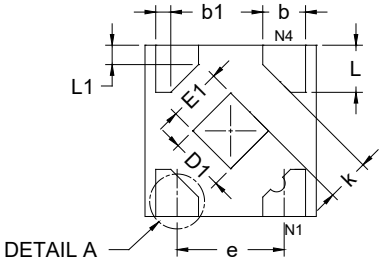
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

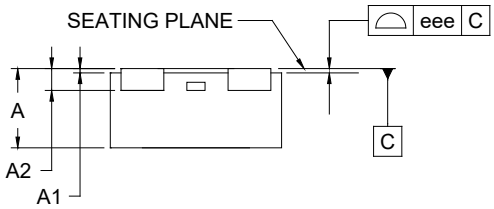
XTDFN-0.8×0.8-4AL



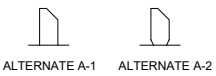
TOP VIEW



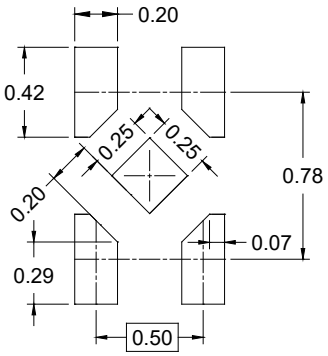
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



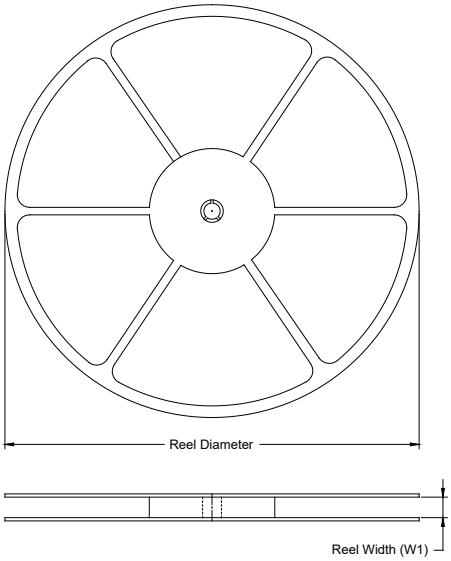
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.320	-	0.400
A1	0.000	-	0.050
A2	0.102 REF		
b	0.150	-	0.250
b1	0.070 REF		
D	0.700	-	0.900
E	0.700	-	0.900
D1	0.150	-	0.350
E1	0.150	-	0.350
L	0.170	-	0.270
L1	0.090 REF		
e	0.500 BSC		
k	0.200 REF		
eee	0.050		

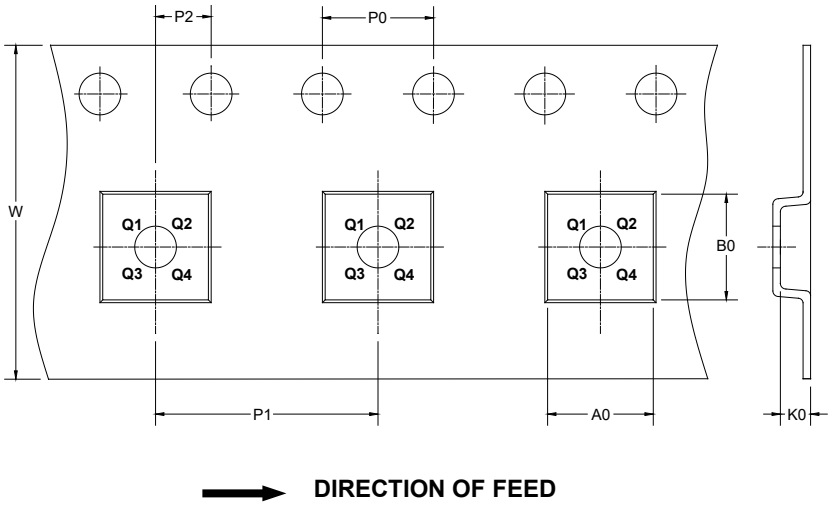
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



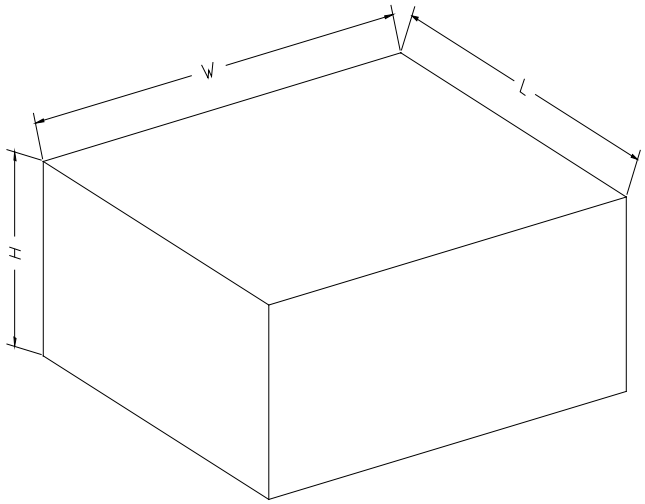
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-5	7″	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
XTDFN-0.8×0.8-4AL	7"	9.5	0.94	0.94	0.50	4.0	2.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002