SGM260321
High-Integration PMIC with 3 Bucks, 2 LDOs and Load Switch

GENERAL DESCRIPTION

The SGM260321 is a highly integrated multi-channel power management device. It supports a variety of microcontrollers, solid-state drive (SSD) applications. It consists of three Buck converters and two LDOs that deliver several output voltages. Buck1 can be set as a load switch. All outputs are highly configurable through the I^2C interface. The device has several default configurations which are programmed in the factory. System level sequencing, output voltage, switching frequency, start-up time, soft-start time, sleep and DPSLP modes, operating modes, and other settings can all be configured.

SGM260321 supplies 4 configurable GPIOs for system hardware control requirements. These GPIOs can be set for a variety of functions. Four input functions are EXT_PG, DVS control, SYS_EN, LSW (load switch mode) LDO control, and four output functions are EXT_EN, nRESET, nIRQ, SYSMON.

A number of protection features are provided in the device including under-voltage/over-voltage protection, short-circuit, over-current and over-temperature shutdown.

The SGM260321 is available in a Green WLCSP-2.42×2.82-36B package.

APPLICATIONS

Solid-State Drives
FPGA
Microcontroller Applications
Personal Navigation Devices

FEATURES

- **Input Voltage Range: 2.7V to 5.5V**
- **Advanced PMIC:**
  - **Buck1:**
    4A Maximum Output Current Capability,
    Configurable Bypass Function
    0.6V (1) to 2.991V Programmable, 9.375mV/Step
    0.8V (1) to 3.9875V Programmable, 12.5mV/Step
  - **Buck2:**
    3A Maximum Output Current Capability
    0.6V to 2.991V Programmable, 9.375mV/Step
    0.8V to 3.9875V Programmable, 12.5mV/Step
  - **Buck3:**
    3A Maximum Output Current Capability
    0.8V to 3.9875V Programmable, 12.5mV/Step
  - **LDO1/LDO2:**
    300mA Maximum Output Current Capability
    0.6V to 2.991V Programmable, 9.375mV/Step
    0.8V to 3.9875V Programmable, 12.5mV/Step
- **Flexible Configurable**
  - **Output Voltage**
  - **Soft-Start Time**
  - **Start-Up Sequence**
  - **Switching Frequency**
  - **Current Limit**
  - **Status Reporting and Controllability via I^2C Interface**
  - **4 Programmable GPIOs**
  - **Seamless Sequencing of External Supplies**
  - **Multiple Sleep Modes**
- **I^2C Interface: 1MHz (MAX)**
- **Input OV/UV Protection**
- **Output OV/UV Protection**
- **Thermal Shutdown Protection**
- **Available in a Green WLCSP-2.42×2.82-36B Package**

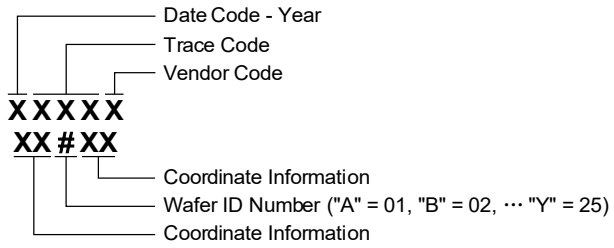
NOTE: 1. The Buck1 is optimized for large duty cycle applications, so a minimum output voltage of 1.7V is recommended for Buck1.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM260321-003	WLCSP-2.42×2.82-36B	-40℃ to +125℃	SGM260321-003XG/TR	SGM 260321-3 XXXXX XX#XX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines “Green” to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

All I/O and Power Pins Except AGND, PGNDx.... -0.3V to 6V
Any PGND referenced to AGND..... -0.3V to 0.3V
SW_Bx to PGNDx..... -1V to 6V
FB_Bx to PGNDx..... -0.3V to 6V
LDOx to AGND ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-2.42×2.82-36B, θ_{JA}..... 43.8℃/W
WLCSP-2.42×2.82-36B, θ_{JB}..... 12.5℃/W
WLCSP-2.42×2.82-36B, θ_{JC}..... 10.2℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (1) (2)
HBM.....±2000V
CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{IN}.....2.7V to 5.5V
Operating Junction Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

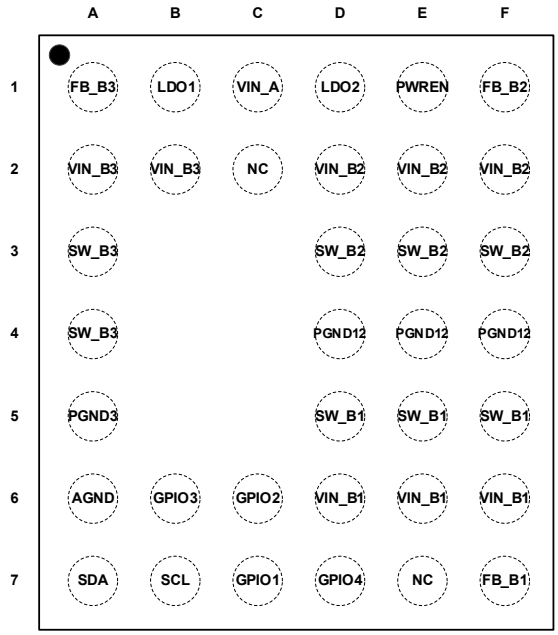
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.42×2.82-36B

PIN DESCRIPTION

PIN	NAME	FUNCTION	
E1	PWREN	Power Enable Digital Input. Control the device in power-on/DPSLP mode. Detailed operation modes are described in the DPSLP state section. Ensure input voltage compliance with logic level specifications in the Electrical Characteristics.	
A6	AGND	Analog Ground. AGND is the ground reference for the IC's analog circuitry and LDOx. It must be connected to the PGNDx pins, ensuring that no high-current paths flow through this connection.	
D4, E4, F4	PGND12	Power Ground of Buck1/Buck2.	The PGNDx pins serve as the power ground connections for the Buck converters and are directly linked to the low-side FETs. Buck1 and Buck2 share pins D4, E4, and F4 (PGND12), while Buck3 uses pin A5 (PGND3).
A5	PGND3	Power Ground of Buck3.	
C1	VIN_A	Analog VIN Supply and Power Input of LDO1/LDO2. Require a 2.2μF ceramic capacitor directly connected to AGND on the top PCB layer.	
D6, E6, F6	VIN_B1	VIN Power Input of Buck1.	Each VIN_Bx requires direct connection to its corresponding PGNDx pin through a 10μF bypass capacitor on the top PCB layer.
D2, E2, F2	VIN_B2	VIN Power Input of Buck2.	
A2, B2	VIN_B3	VIN Power Input of Buck3.	
D5, E5, F5	SW_B1	Switch Pin of Buck1.	Buck converter switch nodes requiring direct top-layer connection to inductors.
D3, E3, F3	SW_B2	Switch Pin of Buck2.	
A3, A4	SW_B3	Switch Pin of Buck3.	
F7	FB_B1	Feedback of Buck1.	Buck regulator feedback pins requiring Kelvin connections to output capacitors.
F1	FB_B2	Feedback of Buck2.	
A1	FB_B3	Feedback of Buck3.	
B1	LDO1	Output of LDO1.	LDOx outputs requiring 1μF bypass capacitors to AGND.
D1	LDO2	Output of LDO2.	
C7	GPIO1	Configurable General Purpose I/O (Open-Drain or Push-Pull).	Four programmable pins assigned specific functions through CMI configurations. Four input functions are EXT_PG, DVS control, SYS_EN, and LSW LDO control, and four output functions are EXT_EN, nRESET, nIRQ, SYSMON.
C6	GPIO2		
B6	GPIO3		
D7	GPIO4		
A7	SDA	I^2C Data Input and Output.	Standard I^2C interface pins for digital communication.
B7	SCL	I^2C Clock Input.	
C2, E7	NC	No Connection.	

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital I/O						
PWREN Input High Voltage	V_{IH_PWREN}		1.2			V
PWREN Input Low Voltage	V_{IL_PWREN}				0.4	V
GPIO Input High Voltage	V_{IH_GPIO}		1.2			V
GPIO Input Low Voltage	V_{IL_GPIO}				0.4	V
GPIO Leakage Current	I_{LKG_GPIO}	Output = 5V, T_J = -40℃ to +125℃			1	μA
GPIO Output High Voltage	V_{OH_GPIO}	I_{OH} = 10mA, T_J = -40℃ to +125℃	V_{IN_A} - 0.35			V
GPIO Output Low Voltage	V_{OL_GPIO}	I_{OL} = 10mA, T_J = -40℃ to +125℃			0.35	V
System Control						
Input Supply Voltage Range	V_{IN_A}	VIN_A referenced to AGND	2.7		5.5	V
VIN_A Under-Voltage Threshold	V_{UV}	Falling	2.5	2.6	2.7	V
VIN_A Under-Voltage Hysteresis	V_{UV_HYS}		100			mV
System Monitor Programmable Range	V_{SYSMON}	VIN_A	2.7		4.2	V
VIN_A Over-Voltage Threshold	V_{OV}	Rising, VIN_OV_SEL = 1		3.8		V
		Rising, VIN_OV_SEL = 0		5.7		
VIN_A Over-Voltage Hysteresis	V_{OV_HYS}	VIN_OV_SEL = 1, T_J = -40℃ to +125℃	100	200	300	mV
		VIN_OV_SEL = 0, T_J = -40℃ to +125℃	200	300	400	
Operating Supply Current	I_Q	All regulators disabled		18		μA
		All regulators enabled but no load		250		μA
Thermal Shutdown (1)	T_{SD}	Temperature rising		155		℃
Thermal Shutdown Hysteresis (1)	T_{HYS}			30		℃
Start-Up Delay after Initial V_{IN_A}	t_{D_START}			1000		μs
VIN_A Deglitch Time UV (1)	t_{DEG_UV}	Falling, enter UV		5		μs
		Rising, exit UV		100		
Transition Time from DPSLP State to Active State	t_{D_A}	Time from PWREN pin low to high transition to time when the first regulator turns on with minimum turn-on delay configuration		0.7	1	ms
Transition Time from Sleep to Active State (1)	t_{S_A}	Time from I^2C command to clear sleep mode to time when the first regulator turns on with minimum turn-on delay configuration		250		μs
Time to First Power Rail Turn-Off (1)	t_{OFF}	Time from turn-off event to when the first power rail turns off with minimum turn-off delay configuration		120		μs
Start-Up Delay Time (1)	t_{D_SU}	x_ON_DLY[1:0] = 00		0		ms
		x_ON_DLY[1:0] = 01		0.25		
		x_ON_DLY[1:0] = 10		0.5		
		x_ON_DLY[1:0] = 11		1.0		
Turn-Off Delay Programmable Range (1)	t_{D_OFF}	Configurable in 0.25ms steps	0		7.75	ms
nRESET Programmable Range (1)	t_{nRESET}	Configurable to 20ms, 40ms, 60ms or 100ms	20		100	ms

NOTE: 1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Buck1						
Input Operating Voltage Range	V_{IN_B1}		2.7		5.5	V
Output Voltage Programming Range 1 (1)	$V_{OUT\_B1\_R1}$	Configurable in 9.375mV steps	0.6		2.991	V
Output Voltage Programming Range 2 (1)	$V_{OUT\_B1\_R2}$	Configurable in 12.5mV steps	0.8		3.9875	V
Standby Supply Current	I_{Q_B1}	No switch, V_{OUT_B1} = 103% set point, T_J = -40℃ to +125℃		30	60	μA
Output Voltage Accuracy	ΔV_{OUT_B1}	V_{OUT_B1} = default CMI voltage, continuous PWM mode	-1		1	%
		V_{OUT_B1} = default CMI voltage, PSM mode (1)	-2		2	%
Power Good Threshold	V_{PG_B1}	V_{OUT_B1} rising	89.5	92	94.5	$\%V_{NOM}$
Power Good Hysteresis	$V_{PG\_HYS\_B1}$			3		$\%V_{NOM}$
Over-Voltage Fault Threshold	V_{OV_B1}	V_{OUT_B1} rising	107	110	113.5	$\%V_{NOM}$
Over-Voltage Fault Hysteresis	$V_{OV\_HYS\_B1}$			3		$\%V_{NOM}$
Switching Frequency	f_{OSC1}	T_J = -40℃ to +125℃	-5%	1.125/ 2.25	5%	MHz
Soft-Start Period	t_{SS_B1}	BUCK_SS = 0, 10% to 90% of V_{NOM}		500	750	μs
Current Limit, Cycle-by-Cycle (Accuracy is only valid for register default setting, B1_ILIM_SET[1:0] = 00)	I_{LIM_B1}	B1_ILIM_SET[1:0] = 00	4.8	5.6	6.3	A
		B1_ILIM_SET[1:0] = 01	4.1	4.8	5.5	
		B1_ILIM_SET[1:0] = 10	2.9	3.8	4.7	
		B1_ILIM_SET[1:0] = 11	1.8	3.0	4.3	
Current Limit, Warning		Compared to current limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	$R_{DSON\_B1\_P}$	I_{SW} = -1A		35		mΩ
NMOS On-Resistance	$R_{DSON\_B1\_N}$	I_{SW} = 1A		13		mΩ
Dynamic Voltage Scaling Rate (1)				3		mV/μs
Output Pull-Down Resistance (1)	R_{PD_B1}	Enabled when regulator disabled		4.4	8.75	Ω
Buck1 - Bypass Mode (V_{IN_B1} = 3.3V)						
Input Voltage for Bypass Mode	V_{IN_B1}		2.7	3.3	5.5	V
PMOS On-Resistance	$R_{DSON\_BY1\_P}$	I_{SW_B1} = -1A		35		mΩ
PMOS Current Limit, Warning		Compared to current limit, cycle-by-cycle	67.5	75	82.5	%
PMOS Current Limit Shutdown (Shut down after deglitch time and stay off for off-time)	I_{LIM_BY1}	B1_ILIM_SET[1:0] = 00	4.8	5.6	6.3	A
		B1_ILIM_SET[1:0] = 01	4.1	4.8	5.5	
		B1_ILIM_SET[1:0] = 10	2.9	3.8	4.7	
		B1_ILIM_SET[1:0] = 11	1.8	3.0	4.3	
Internal PMOS Current Shutdown Deglitch Time (1)	t_{DEG_BY1}			5		μs
Internal PMOS Current Shutdown Off-Time (Retry Time) (1)	t_{OFF_BY1}			10		ms
Internal PMOS Soft-Start (1)	t_{SS_BY1}	C_{OUT} = 66μF		500		μs

NOTE: 1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Buck2/3						
Input Operating Voltage Range	V_{IN_Bx}		2.7		5.5	V
Buck2 Output Voltage Range 1 (1)	$V_{OUT\_B2\_R1}$	Configurable in 9.375mV steps	0.6		2.991	V
Buck2 Output Voltage Range 2 (1)	$V_{OUT\_B2\_R2}$	Configurable in 12.5mV steps	0.8		3.9875	V
Buck3 Output Voltage Range (1)	V_{OUT_B3}	Configurable in 12.5mV steps	0.8		3.9875	V
Standby Supply Current	I_{Q_Bx}	No switch, V_{OUT_Bx} = 103% set point, T_J = -40℃ to +125℃		30	60	μA
Output Voltage Accuracy	ΔV_{OUT_Bx}	V_{OUT_Bx} = default CMI voltage, continuous PWM mode	-1		1	%
		V_{OUT_Bx} = default CMI voltage, PSM (1)	-2		2	%
Power Good Threshold	V_{PG_Bx}	V_{OUT_Bx} rising	90	93	96	$\%V_{NOM}$
Power Good Hysteresis	$V_{PG\_HYS\_Bx}$			3		$\%V_{NOM}$
Over-Voltage Fault Threshold	V_{OV_Bx}	V_{OUT_Bx} rising	107.5	110.5	114	$\%V_{NOM}$
Over-Voltage Fault Hysteresis	$V_{OV\_HYS\_Bx}$			3		$\%V_{NOM}$
Switching Frequency	f_{OSCx}	T_J = -40℃ to +125℃	-5%	1.125/ 2.25	5%	MHz
Soft-Start Period	t_{SS_Bx}	BUCK_SS = 0, 10% to 90% of V_{NOM}		500	750	μs
Buck2 Current Limit, Cycle-by-Cycle (Accuracy is only valid for register default setting, B2_ILIM_SET[1:0] = 00)	I_{LIM_B2}	B2_ILIM_SET[1:0] = 00	3.4	4.2	5.0	A
		B2_ILIM_SET[1:0] = 01	2.9	3.6	4.4	
		B2_ILIM_SET[1:0] = 10	2.3	3.0	3.8	
		B2_ILIM_SET[1:0] = 11	1.7	2.5	3.3	
Buck3 Current Limit, Cycle-by-Cycle (Accuracy is only valid for register default setting, B3_ILIM_SET[1:0] = 01)	I_{LIM_B3}	B3_ILIM_SET[1:0] = 00	3.1	4.0	4.8	A
		B3_ILIM_SET[1:0] = 01	2.6	3.4	4.2	
		B3_ILIM_SET[1:0] = 10	2.1	2.8	3.6	
		B3_ILIM_SET[1:0] = 11	1.6	2.3	2.9	
Current Limit, Warning		Compared to current limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	$R_{DSON\_Bx\_P}$	I_{SW_Bx} = -1A		80		mΩ
NMOS On-Resistance	$R_{DSON\_Bx\_N}$	I_{SW_Bx} = 1A		55		mΩ
Dynamic Voltage Scaling Rate (1)				3		mV/μs
Output Pull-Down Resistance (1)	R_{PD_Bx}	Enabled when regulator disabled		6.6	13	Ω

NOTE: 1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO1/2							
Operating Voltage Range	V_{IN_A}			2.7		5.5	V
Output Voltage Range 1 (1)	$V_{OUT\_LDOx\_R1}$	Configurable in 9.375mV steps		0.6		2.991	V
Output Voltage Range 2 (1)	$V_{OUT\_LDOx\_R2}$	Configurable in 12.5mV steps		0.8		3.9875	V
Output Current	I_{OUT_LDOx}				300		mA
Output Voltage Accuracy	ΔV_{OUT_LDOx}	I_{OUT_LDOx} = 5mA, T_J = -40℃ to +125℃		-1		1	%
Power Supply Rejection Ratio (1)	PSRR	I_{OUT_LDOx} = 20mA, V_{OUT_LDOx} = 1.8V	f = 1kHz		52		dB
			f = 10kHz		32		dB
			f = 2.25MHz		51		dB
Supply Current	I_{Q_LDOx}	Regulator enabled, no load			34	50	μA
Soft-Start Time	t_{SS_LDOx}	10% to 90% of V_{NOM}			300	430	μs
Power Good Threshold	V_{PG_LDOx}	V_{OUT_LDOx} rising		87	90.5	95	$\%V_{NOM}$
Power Good Hysteresis	$V_{PG\_HYS\_LDOx}$				4		$\%V_{NOM}$
Over-Voltage Fault Threshold	V_{OV_LDOx}	V_{OUT_LDOx} rising		105	110	115	$\%V_{NOM}$
Over-Voltage Fault Hysteresis	$V_{OV\_HYS\_LDOx}$				3		$\%V_{NOM}$
Discharge Resistance (1)	R_{DIS_LDOx}				50	125	Ω
Dropout Voltage	V_{DROP_LDOx}	I_{OUT_LDOx} = 220mA, V_{OUT_LDOx} = 2.7V				150	mV
Output Current Limit	I_{LIM_LDOx}	LDOx_ILIM_SET[1:0] = 00		80	155	230	mA
		LDOx_ILIM_SET[1:0] = 01		180	245	310	
		LDOx_ILIM_SET[1:0] = 10		300	365	430	
		LDOx_ILIM_SET[1:0] = 11		400	460	520	
LDO1/2 Load Switch Mode - Bypass Mode							
Operating Voltage Range LDO1/2	V_{IN_A}			2.7		5.5	V
PMOS On-Resistance	$R_{DSON\_LDOx\_P}$				320		mΩ
Supply Current	I_{Q_LDOx}	Load switch enabled, no load			42	60	μA
Output Current Limit	I_{LIM_LDOx}	LDOx_ILIM_SET[1:0] = 00		80	155	230	mA
		LDOx_ILIM_SET[1:0] = 01		180	245	310	
		LDOx_ILIM_SET[1:0] = 10		300	365	430	
		LDOx_ILIM_SET[1:0] = 11		400	460	520	
Internal PMOS Current Shutdown Deglitch Time (1)	$t_{DEG\_SD\_LDOx}$				5		μs
Internal PMOS Current Shutdown Off Time (Retry Time) (1)	t_{OFF_LDOx}				10		ms
Internal PMOS Soft-Start (1)		Only used with 3.3V input, C_{OUT} = 1μF			10		mV/μs

NOTE: 1. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.3V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C Interface						
SCL Clock Frequency	f_{SCL}		0		1000	kHz
SCL, SDA Input Low Voltage	V_{IL}				0.4	V
SCL, SDA Input High Voltage	V_{IH}		1.25			V
SDA Leakage Current	I_L	V_{SDA} = 5V			1	μA
SDA Output Low Voltage	V_{OL}	I_{OL} = 5mA			0.35	V
SCL Low Period	t_{LOW}		0.5			μs
SCL High Period	t_{HIGH}		0.26			μs
SDA Data Setup Time	t_{SU_DAT}		50			ns
SDA Data Hold Time	t_{HD_DAT}		0			ns
Start Setup Time	t_{SU_STA}	For start condition	260			ns
Stop Setup Time	t_{SU_STO}	For stop condition	260			ns
Capacitance on SCL or SDA Pin	C				10	pF
SCL/SDA Rise/Fall Time	t_R/t_F	Device requirement			120	ns

I²C TIMING DIAGRAM

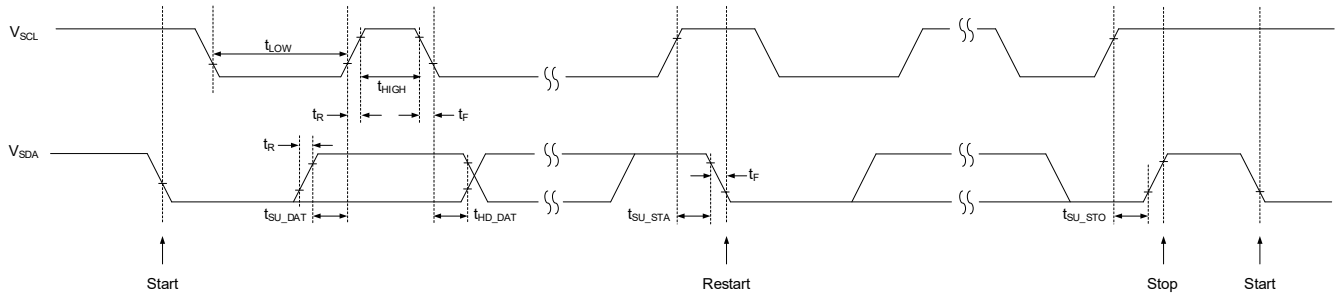
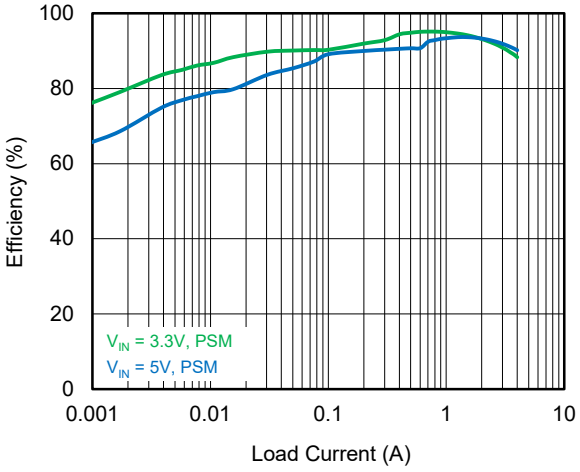


Figure 1. I²C Timing Diagram

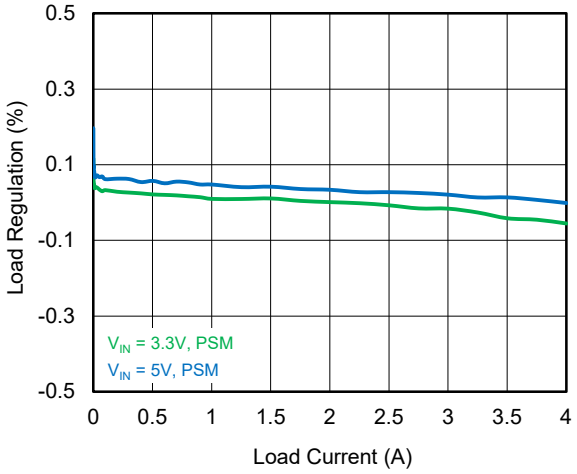
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{IN} = 3.3V, f = 2.25MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

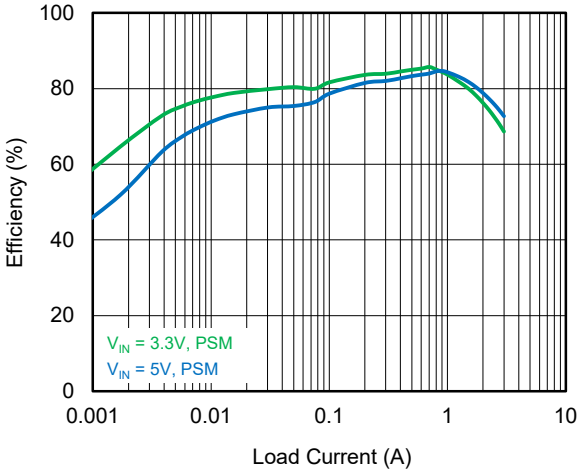
Efficiency vs. Load Current (V_{OUT_B1} = 2.5V)



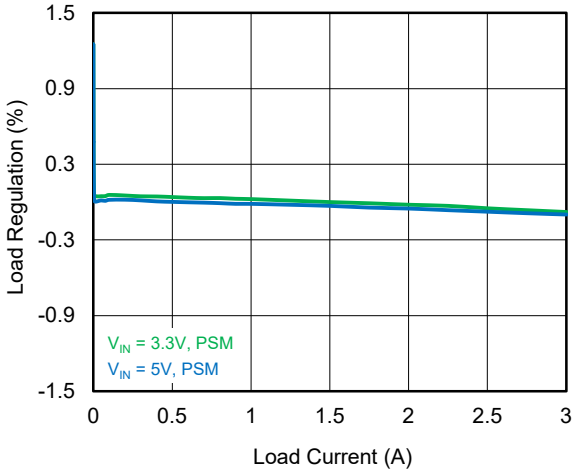
Load Regulation (V_{OUT_B1} = 2.5V)



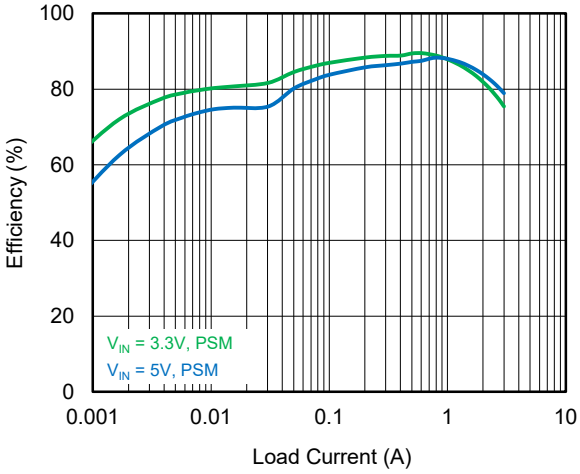
Efficiency vs. Load Current (V_{OUT_B2} = 0.8V)



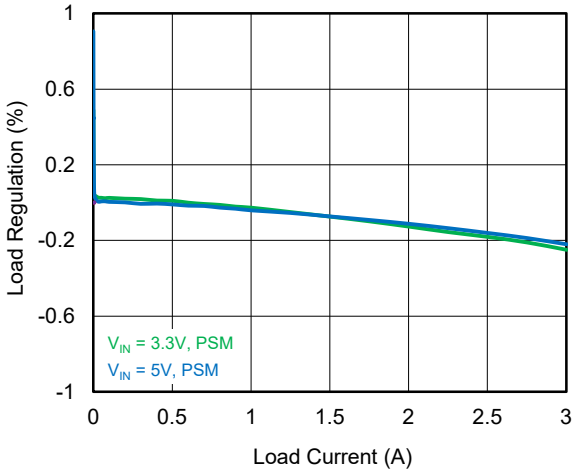
Load Regulation (V_{OUT_B2} = 0.8V)



Efficiency vs. Load Current (V_{OUT_B3} = 1.2V)



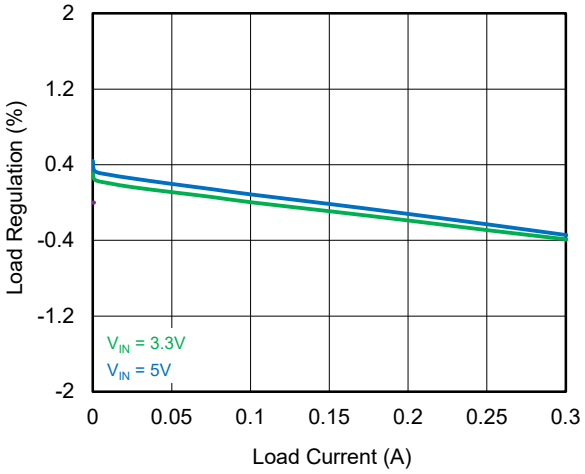
Load Regulation (V_{OUT_B3} = 1.2V)



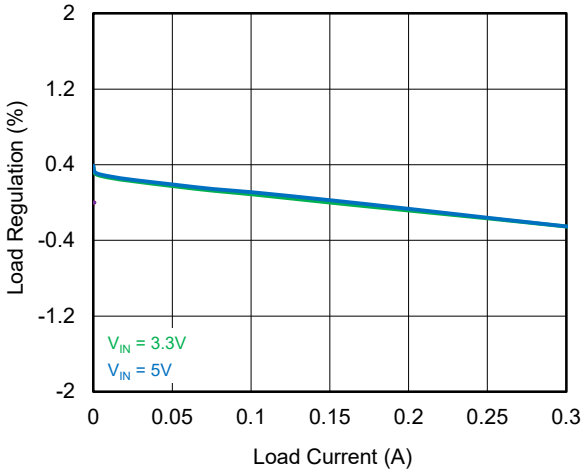
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN} = 3.3V, f = 2.25MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

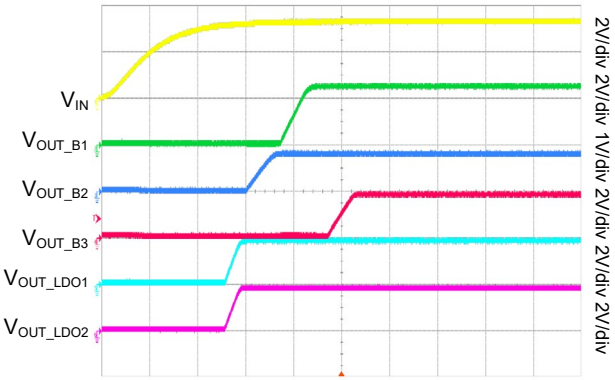
Load Regulation (V_{OUT_LDO1} = 1.8V)



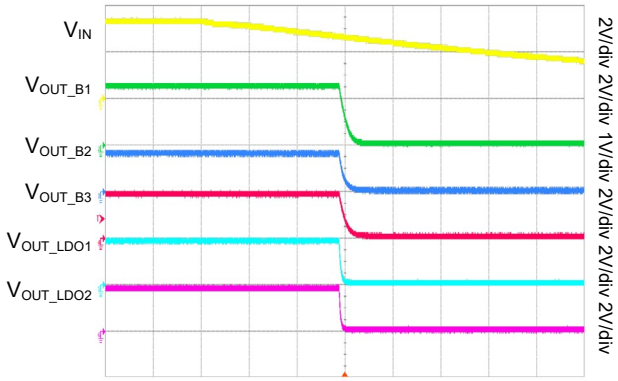
Load Regulation (V_{OUT_LDO2} = 1.8V)



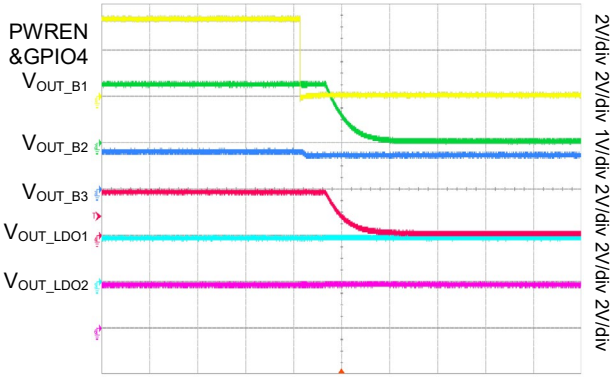
CMI 003 Power-Up Sequence (GPIO3 = High)



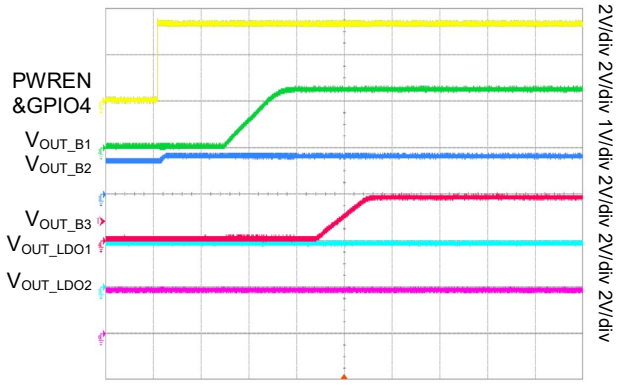
CMI 003 Power-Down Sequence (GPIO3 = High)



CMI 003 Enter PS4 with PWREN and GPIO4



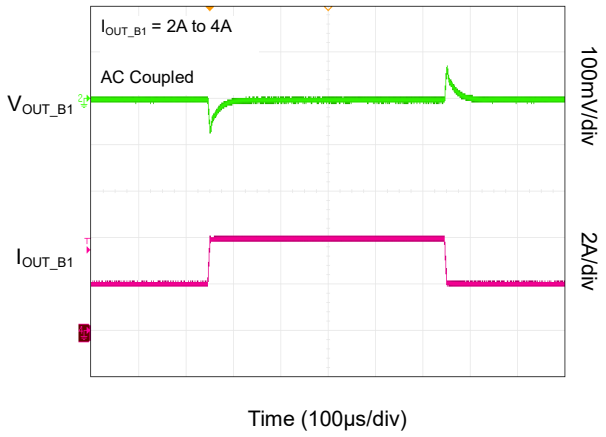
CMI 003 Exit PS4 with PWREN and GPIO4



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

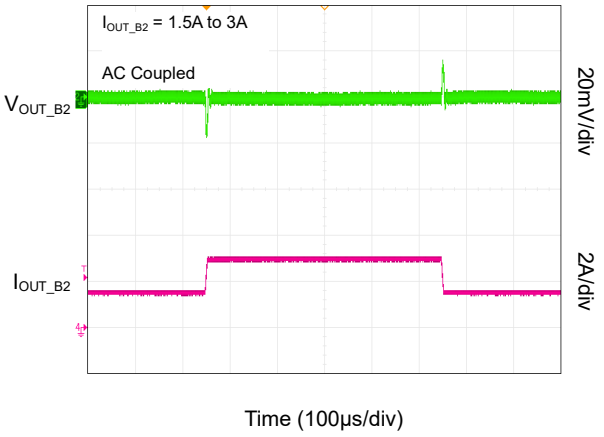
T_J = +25℃, V_{IN} = 3.3V, f = 2.25MHz, L = 0.47μH (DCR = 7.3mΩ), unless otherwise noted.

Load Transient (V_{OUT_B1} = 2.5V)



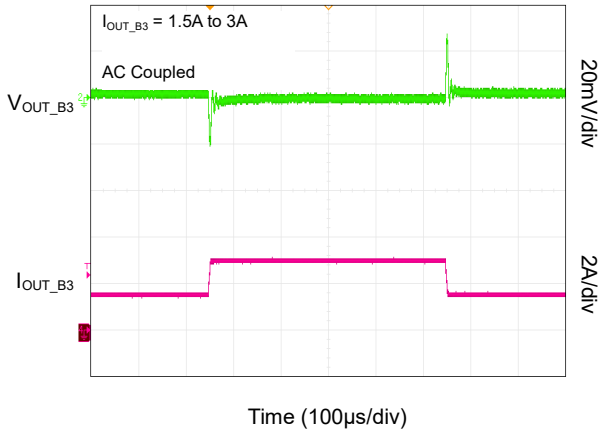
Time (100μs/div)

Load Transient (V_{OUT_B2} = 0.8V)



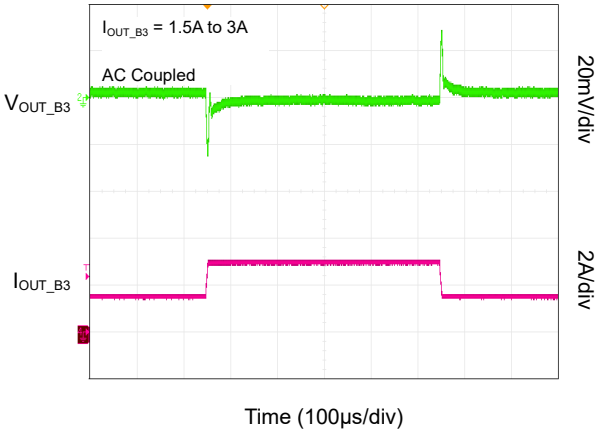
Time (100μs/div)

Load Transient (V_{OUT_B3} = 1.2V)



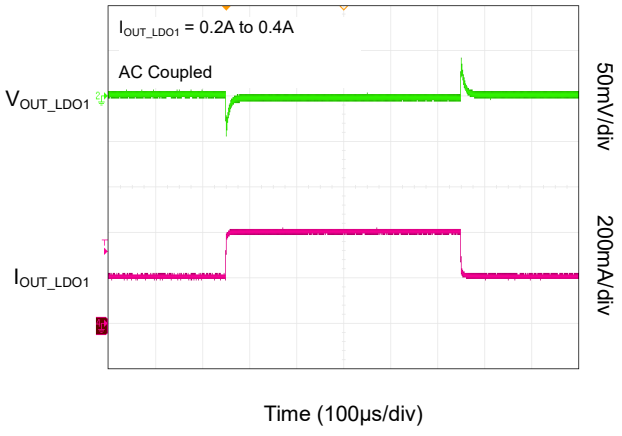
Time (100μs/div)

Load Transient (V_{OUT_B3} = 1.8V)



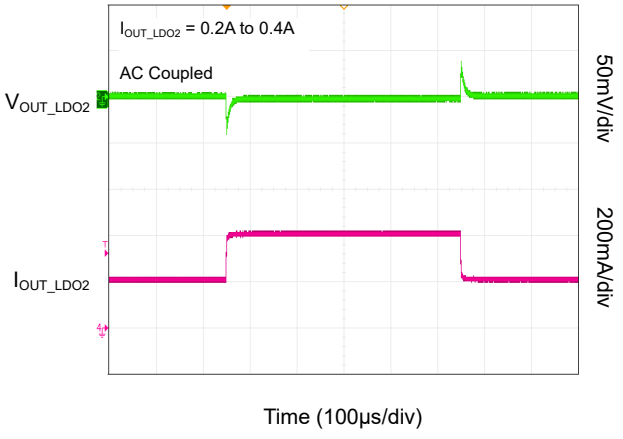
Time (100μs/div)

Load Transient (V_{OUT_LDO1} = 1.8V)



Time (100μs/div)

Load Transient (V_{OUT_LDO2} = 1.8V)



Time (100μs/div)

TYPICAL APPLICATION CIRCUIT

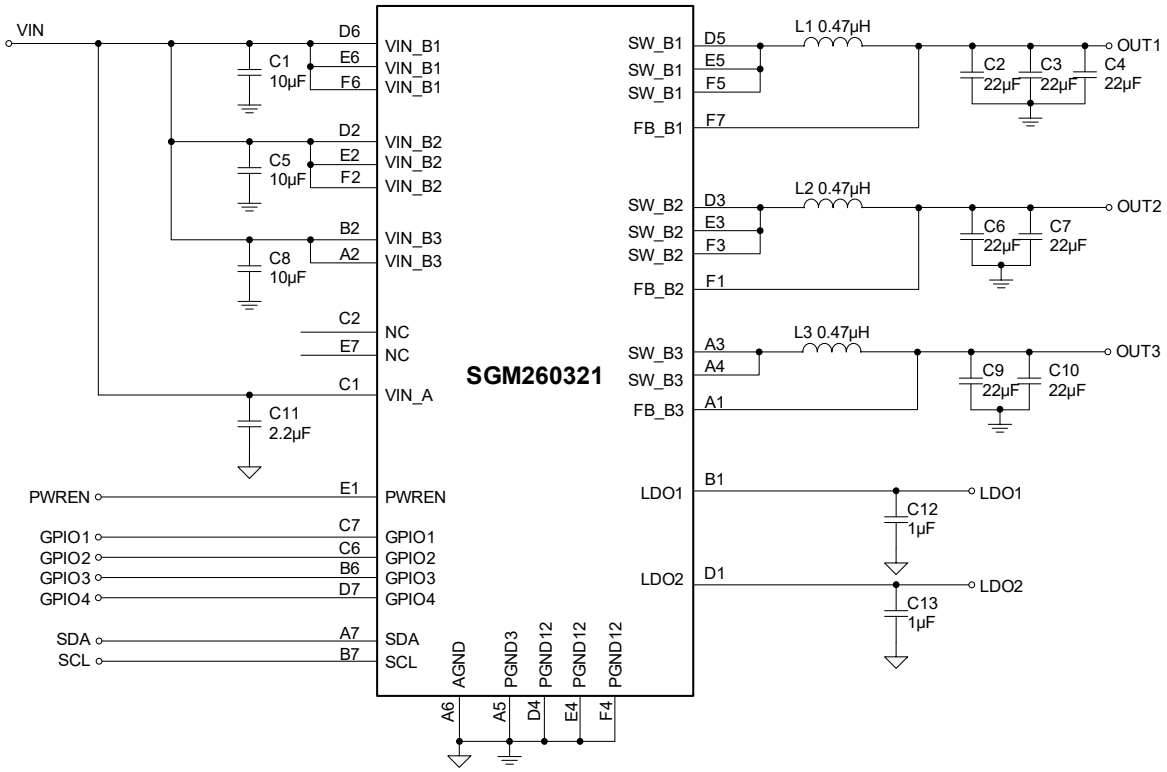


Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

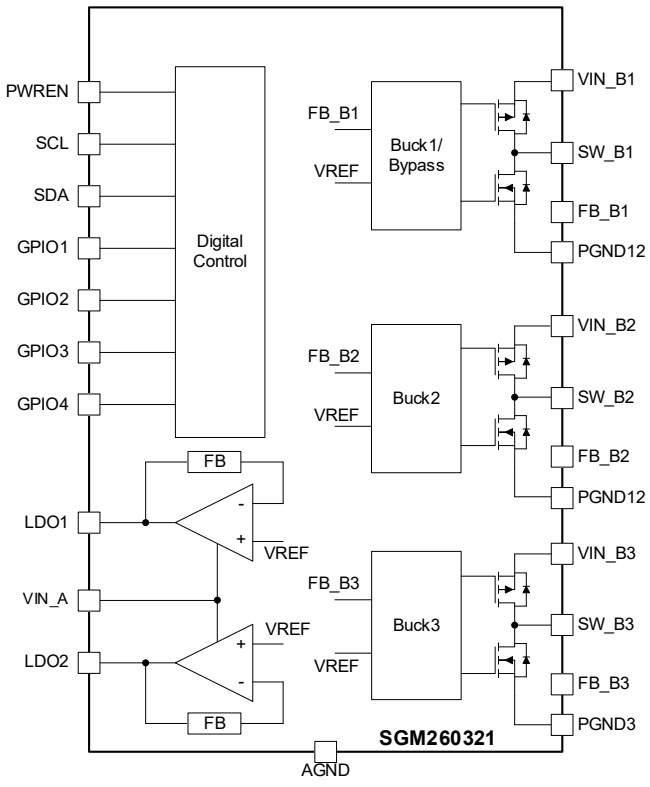


Figure 3. Block Diagram

DETAILED DESCRIPTION: SYSTEM CONTROL

General

The SGM260321 represents an integrated power management IC engineered for next-generation solid state drive controllers. This system-on-chip solution delivers three high efficient Buck converters and two LDOs, specifically optimized for mission-critical storage controllers and industrial automation processors. It integrates three Buck converters, two LDOs, achieving space-saving and cost-effective power delivery through advanced integration. SGM260321 contains a master controller governing critical operations: start-up sequence, turn-on delay, turn-off delay, voltage of each channel, soft-start time, sleep or DPSLP state, and fault conditions.

System parameters can be dynamically adjusted through I^2C interface, without physical hardware modifications. A built-in bypass switch for Buck1 enhances sequencing flexibility in 3.3V power architectures.

The master controller continuously tracks all output channels, transmitting status information through I^2C protocol communication and hardware-level status signals. User can configure fault thresholds and response mechanisms via I^2C interface, including selective fault masking capabilities.

Factory-defined parameters for SGM260321 are established through Code Matrix Index (CMI). The device supports extensive customization for different GPIO configuration and each channel's voltage and current limit, etc. It is specifically defined for each SGM260321 CMI part number.

I^2C Serial Interface

Standard I^2C interface is used to program SGM260321 parameters and get status reports. It operates as a slave device, and can be configured by factory to one of four 7-bit slave addresses. The base address incorporates an extension bit which defining the operation is read or write.

Refer to each specific CMI for the IC's slave address.

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25	010 0101	0x4A	0x4B
0x27	010 0111	0x4E	0x4F
0x67	110 0111	0xCE	0xCF
0x6B	110 1011	0xD6	0xD7

The I^2C controller does not have a timeout feature. However, whenever it detects a new start signal, it will immediately stop and reset the current data processing, even if a valid data packet is being transmitted.

I^2C is 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The SDA pin operates in open-drain configuration and requires an external pull-up resistor. Signal transitions on this pin must comply with the timing parameters specified in the Electrical Characteristics on page 8.

I^2C Registers

The SGM260321 integrates internal configuration registers that store critical operational parameters, including output voltage setting, start-up sequencing, fault detection thresholds, and fault mask configurations. These registers provide the core programmability of the device. Two register categories are implemented.

Basic Volatile

These registers are R/W (read/write) and R (read only). After power-up, user can modify R/W registers to adjust IC functions, such as masking faults. R registers display IC status, including faults. All changes are lost on power cycle. Default values are fixed and cannot be altered by the factory or user.

Basic Non-Volatile

These registers are R/W and R types. Once the IC is powered up, user can change the R/W registers to adjust functions like output voltage, start-up delay, and current limit thresholds. These modifications are lost when power is cycled. The default values can be set at the factory to optimize the IC for specific applications. Please contact sales for custom options and minimum order quantities. When updating only certain bits within a register, be careful not to alter the other bits, as doing so may cause unexpected device behavior.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

State Machine

Figure 4 shows the SGM260321 internal state machine.

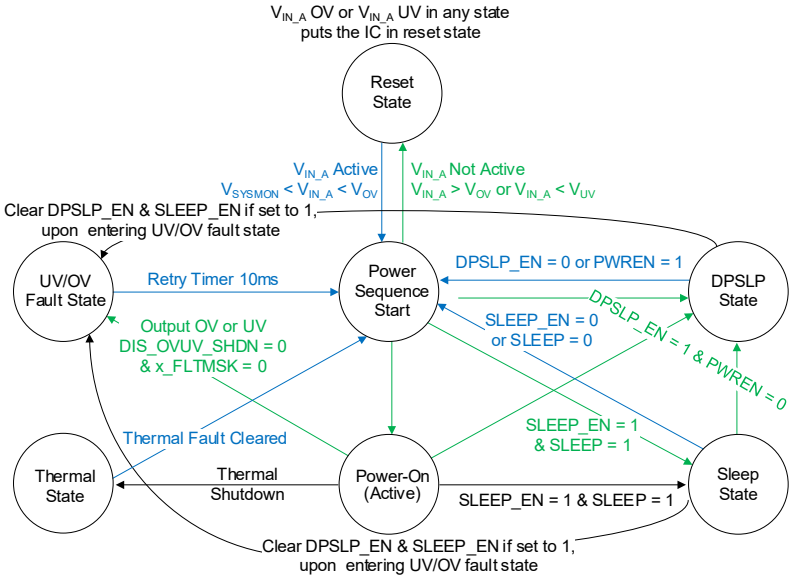


Figure 4. State Machine

Reset State

During the reset state, the SGM260321 monitors VIN_A until it stabilizes within the acceptable range specified by V_{SYSMON} and V_{OV}. In this state, all regulators remain off and the outputs are maintained at a low level. When the input voltage drops below the V_{UV} threshold or exceed the V_{OV} limit, the IC will revert to the reset state regardless of its current operating state.

Power Sequence Start State

During the power sequence start state, the system is in a transitional phase as the regulators begin their activation. During this period, outputs are activated and start their ramp-up. As soon as the regulators stabilize and enter regulation, the IC promptly shifts to the power-on, sleep or DPSLP state.

Power-On (Active) State

The active state represents normal operation, where the input voltage remains within the acceptable range, all outputs are enabled, and no faults are detected.

Sleep State

In sleep state, each output can be configured to remain on/off. When transitioning into/out of sleep mode, the outputs follow their programmed sequencing delay time for turning on/off.

The IC can enter the sleep state through the SLEEP and SLEEP_EN registers. Table 1 shows the conditions required for this transition. In sleep mode, the SGM260321's I^2C interface remains active. The IC exits sleep mode once the entry conditions are no longer met.

If an output over-voltage (OV) or under-voltage (UV), occurs in sleep mode, the IC resets SLEEP_EN and DPSLP_EN bits and returns to the power-on state.

Table 1. Sleep Mode Truth Table

SLEEP_EN Bit (0x04h)	SLEEP Bit (0x04h)	Enter Sleep Mode
0	0	No
0	1	No
1	0	No
1	1	Yes

DPSLP State

The DPSLP state is designed for even lower power consumption than the sleep mode. While similar to the sleep state, DPSLP state has different entry and exit configurations. Each output can be individually set to be on/off in DPSLP mode, with setting that may differ from those in the sleep state. When transitioning into/out of DPSLP mode, the outputs follow their programmed sequencing delay time for turning on/off.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

The device can enter the DPSLP mode through pulling the PWREN pin low and setting DPSLP = 1. Table 2 shows the conditions required for this transition. In DPSLP mode, the I^2C interface remains active. The device exits DPSLP mode once the entry conditions are no longer met.

If an output over-voltage (OV) or under-voltage (UV) occurs in DPSLP state, the IC resets SLEEP_EN and DPSLP_EN bits and returns to the power-on state.

Table 2. DPSLP Mode Truth Table

PWREN Pin	DPSLP_EN Bit (0x04h)	Enter DPSLP Mode
0	1	Yes
1	1	No
0	0	No
1	0	No

Thermal State

When the chip temperature exceeds the thermal shutdown temperature, all regulators automatically turn off to protect the IC and the nRESET signal is pulled low. The TMSK control bit stops the nIRQ from triggering when temperature exceeds the warning level ($T_J > T_{WARN}$), but the TWARN status bit still shows the overheating condition even when TMSK bit is set to 1.

UV/OV Fault State

When any regulator's output goes above the over-voltage (OV) threshold or below the under-voltage (UV) threshold after soft-start, the IC enters UV/OV state. All regulators turn off, and the nRESET is pulled low. The system tries to restart after a 10ms delay. If the OV/UV condition remains, the IC returns to UV/OV state, repeating this cycle until the fault is removed or input power is disconnected. While over-current conditions do not directly trigger UV/OV state, sustained over-current causing UV conditions will lead to PMIC enter UV/OV state.

Each regulator provides OV/UV fault control through mask bits (x_OV_FLTMSK/x_UV_FLTMSK). UV/OV fault state is enabled only when both conditions are met: the fault mask bits are cleared to 0 and the DIS_OVUV_SHDN = 0. When fault mask is active, the nIRQ signal remains high during faults and PMIC does not enter UV/OV state. But OV/UV still provides the over-/under-voltage fault status even if x_OV_FLTMSK/ x_UV_FLTMSK = 1.

Start-Up/Shutdown

The IC automatically moving from the reset state to the power sequence start state upon input power is applied. Then PMIC transitions to either power-on, sleep, or DPSLP states is determined by input conditions defined in Table 1 and Table 2. A standard start-up sequence progresses from reset to power-on state when input power is applied. For V_{IN}, POWER_OFF bit or SYS_EN shutdown, there is no shutdown sequence, all channels are shutdown at the same time.

Sequencing

The SGM260321 delivers advanced sequencing control for multi-rail power systems. Each of its five outputs has four programmable parameters: input trigger, turn-on delay, turn-off delay, and output voltage. Buck regulators additionally support soft-start time adjustment. All parameters are programmed through dedicated configuration registers, enabling application specific optimization without hardware changes. Detailed sequencing profiles for this device and related parameters are provided at the end of datasheet. Contact sales for custom sequencing configurations.

Input Trigger

The input trigger determines when a regulator turns on. Each output channel can use independent trigger sources, including internal channel's power ok (POK), internal V_{IN_A} power ok (V_{SYSMON}), and external signal through GPIO pin.

This flexibility enables system designers to implement a wide range of sequencing possibilities with external power supply or host controllers. For instance, configuring Buck1 as LDO1's input trigger, LDO1 will not turn on until Buck1 achieves stable regulation. Input triggers are predefined at the factory and can only be modified through a custom CMI configuration.

Additionally, GPIOx outputs can be linked to an internal power supply's POK signal to trigger external power supply sequencing. Also, GPIOx inputs can connect to an external power supply's power good output, serving as an input trigger for an SGM260321 supply.

Turn-On Delay

The turn-on delay is the time from when an input trigger activates to the output begins turning on. This timing parameter for each output is set using the x_ON_DLY[1:0] bits in the I^2C registers. Do not change this x_ON_DLY[1:0] bits when PMIC is powered on. Change this turn-on delay when CMI configuration is initially determined.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

Turn-Off Delay

The turn-off delay is the time from sleep/DPSLP mode activation to the output begins shutting down. Each output's delay time is set using the x_OFF_DLY[4:0] bits in the I^2C registers. The setting can be adjusted during operation but is temporary, it will reset to default value when power is recycled.

Soft-Start Time

The soft-start time for all Buck converters is managed through the BUCK_SS control bit. Setting this bit to 0 selects a 500μs start-up period, while setting it to 1 set the period to 250μs. Though adjustable after power-up, the setting is temporary and resets to factory defaults when power is recycled.

Output Voltage

The output voltage defines the target voltage for each regulator. For Buck converters, this value is set through I^2C using Bx_VSET0[7:0] bits (active mode) and Bx_VSET1[7:0] bits (DVS mode). LDOs utilize a single LDOx_VSET[7:0] register for voltage configuration. All output voltages can be adjusted during operation, though new setting is temporary and resets to factory defaults when power is recycled.

Output voltages can be adjusted while the IC is operating. For significant voltage changes, use multiple small steps instead of a single large adjustment. This avoids accidental triggering of over-voltage (OV) or under-voltage (UV) protection because the fault detection thresholds update immediately, but the output voltage changes more slowly.

Dynamic Voltage Scaling (DVS)

The three Buck converters support dynamic voltage scaling through either the I^2C interface or GPIO pins. This feature enables power optimization by dynamically adjusting processor voltage based on workload demands. DVS operates within the active state, modifying output voltages without changing the IC's operational mode.

Each Buck converter maintains its Bx_VSET0 setting during normal operation and switches to Bx_VSET1 when the DVS trigger activates. Voltage transitions occur seamlessly while the IC remains fully operational.

The IC can enter DVS mode through I^2C, a GPIO pin, or by transitioning into sleep mode. DVS can be applied to all Buck converters simultaneously via I^2C. When using I^2C, the user can choose between two different configurations for enabling DVS. However, note that DVS via I^2C is disabled if EN_DVS_I2C = 0.

Enable DVS via I2C_DVS_ON Bit

Set EN_DVS_I2C = 1 and SEL_DVS_IN = 0 through I^2C. Writing 1 to I2C_DVS_ON enables DVS mode, while writing 0 disables it.

Enable DVS when Enter Sleep State

With EN_DVS_I2C = 1 and SEL_DVS_IN = 1, entering sleep state automatically activates DVS mode (I2C_DVS_ON value becomes irrelevant).

Note that the IC cannot be configured to enter DVS in DPSLP state. Table 3 summarizes I^2C DVS functionality.

Table 3. I^2C DVS Control

EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON	DVS Mode
0	X	X	Off
1	0	0	Off
1	0	1	On
1	1	X	On in Sleep State

Input Voltage Monitoring (V_{SYSMON})

The SGM260321 continuously tracks input voltages on VIN_A pin to maintain system operational limits. Initial activation occurs when V_{IN_A} exceeds the under-voltage rising threshold, but outputs remain disabled until V_{IN_A} rises above the programmable V_{SYSMON} (2.7V to 4.2V).

The nIRQ pin pulls low if V_{IN_A} drops below V_{SYSMON}, while outputs continue normal operation. Full system shutdown triggers when V_{IN_A} falls below V_{UV}.

VSYSSTAT bit flags input status (1 = $V_{IN\_A} < V_{SYSMON}$, 0 = $V_{IN\_A} > V_{SYSMON}$), $V_{IN\_A} < V_{SYSMON}$ will pull nIRQ low, it is latched and required I^2C VSYSSTAT bit in register 0x00h reads to clear, and this fault is masked via VSYSMSK bit by default. SGM260321 also has a real-time VSYSDAT status bit.

DETAILED DESCRIPTION: SYSTEM CONTROL (continued)

Fault Protection

The SGM260321 has multiple levels of fault protections, including:

- Input Under-Voltage/Over-Voltage
- Output Over-Voltage
- Output Under-Voltage
- Output Current Limit and Short-Circuit
- Thermal Warning
- Thermal Shutdown

The IC implements two types of registers for each fault condition: fault bits and mask bits. Fault bits are always valid, even when masking is active. Mask bits determine whether a fault triggers the nIRQ signal. User can selectively mask faults through I^2C configuration. Unmasked faults immediately pull low the nIRQ pin, which remains low until both the fault clears and the status register is read via I^2C. Masked faults can still be read in the fault bit.

Input Voltage (UV)

The SGM260321 continuously checks the input voltage at the VIN_A pin to detect UV condition. If the voltage drops below the V_{UV} threshold, the IC enters the reset state, disabling all outputs and pulling the nRESET signal low. When the input voltage rises above V_{SYSMON} and V_{UV} rising threshold, the PMIC transitions to the active state, and begins normal start-up procedures.

Input Voltage (OV)

The SGM260321 monitors the input voltage at the VIN_A pin for an over-voltage (OV) condition. The VIN_OV_SEL threshold is factory programmable between 3.8V and 5.7V. If the input voltage exceeds this threshold, the IC enters the reset state, turning off all outputs and asserting nRESET low. Once the input voltage drops below the V_{OV} falling threshold, the IC transitions back to the power sequence start state and resumes normal start-up.

Output (UV/OV)

The SGM260321 continuously checks all outputs for under-voltage (UV) and over-voltage (OV) conditions. When detecting a UV/OV fault, the IC enters the UV/OV fault state, disabling all outputs and pulling nRESET low. After a 10ms delay, the system restarts using the programmed start-up sequence.

During current limit conditions, output voltages may drop below UV thresholds, triggering system shutdown. To prevent this, user can mask the UV fault bits. Each output continues to report OV fault conditions through its fault bit, regardless of masking setting. Masking OV/UV faults prevents both nIRQ signal pulling low and entering UV/OV fault state, while maintaining real-time fault monitoring capability.

Output Current Limit

The SGM260321 employs a two-level over-current protection strategy for the Buck converters and a single-level over-current protection for the LDOs.

For the Buck converters, Buck1 monitors peak switch current, while Buck2/Buck3 monitors valley switch current. The first protection level triggers when switch current exceeds 75% of the current limit for 16 consecutive cycles. It logs Bx_ILIM_WARN fault status and pulls the nIRQ pin low if unmasked. The second level of protection occurs when the current reaches the cycle-by-cycle limit. In response, the Buck converter limits the peak switch current for Buck1 and the valley switch current for Buck2 and Buck3 during each switching cycle. This reduces duty cycle and potentially causes output voltage drop. If this triggers an unmasked under-voltage condition, all outputs are disabled for 10ms before restarting.

For the LDOs, the over-current thresholds are determined by each LDO's output current limit setting. When the output current reaches this threshold, the LDO restricts the output current, causing the output voltage to drop. If this results in a UV condition, all supplies are turned off for 10ms before restarting.

The over-current fault limits for each output can be adjusted via I^2C.

All current limit thresholds are configurable through I^2C registers.

Thermal Warning and Thermal Shutdown

The SGM260321 continuously tracks its internal die temperature. When the die temperature exceeds the +125℃ warning threshold, the nIRQ is pulled low. If temperatures rises further to the +155℃ shutdown limit, all outputs are immediately disabled. The thermal warning is mask via I^2C by default, though the status bit still reflects temperature conditions even when masked. Masking only prevents the fault from being reported by nIRQ.

PWREN

The PWREN pin controls the IC's operational mode selection between power-on state and DPSLP state. PWREN has a bidirectional filter to prevent false triggering. When pulled low, user can program the Bucks and LDOs to either maintain operation or power down, enabling system-wide power saving states through a single control signal.

GPIO CONFIGURATION

Table 4. Configurable GPIO Features

GPIO Configuration	Input Functions	EXT_PG
		DVS Control
		SYS_EN
		LSW LDO Control
	Output Functions	EXT_EN
		nRESET
		nIRQ (Interrupt)
		SYSMON

Input Functions

EXT_PG

The IC provides an external input trigger (EXT_PG) to coordinate start-up timing with additional power supplies. EXT_PG can initiate one or multiple power rails, enabling seamless integration of external regulators into the system's start-up sequence. CMI setting designate the GPIO pin used for EXT_PG functionality.

DVS Control

GPIOx can be configured as input pins for different Buck channel DVS control. Whenever GPIOx is pulled low, the channel enters DVS state and the input voltage switches from x_VSET0[7:0] to x_VSET1[7:0].

SYS_EN

GPIOx can be configured as the system's enable pin. When GPIOx is pulled low, the system shuts down. If GPIOx is pulled high, the system starts using the programmed start-up sequence.

LSW LDO Control

GPIOx can be configured as input pins for different LDO channel mode control. When GPIOx is pulled high, LDOx is set for LDO mode. If GPIOx is pulled low, LDOx is set for LSW mode. Do not change LDO's working mode after PMIC is powered on.

Output Functions

EXT_EN

The SGM260321 includes an enable function (EXT_EN) for controlling external regulators or providing system control signals. This feature supports programmable input triggers and delay time to align with specific power sequencing requirements. The assigned GPIO pin for EXT_EN operation is defined through CMI configuration.

nRESET

The SGM260321 includes a reset function to initiate system-level CPU/controller resets. The nRESET signal pulls low during thermal shutdown events. This signal also pulls low instantly if input voltage exceeds OV threshold, drops below UV threshold, or when any outputs that are connected to nRESET functionality experience OV or UV situations. The CMI configuration determines which power rails are monitored for nRESET triggering.

Following system start-up, nRESET pulls high after a programmable delay period when input voltage and all connected channel's output voltage are above their respective thresholds. This delay interval (20ms ~ 100ms) is programmed through the TRST_DLY[1:0] bits. CMI setting additionally assigns the dedicated GPIO pin for nRESET signal output and program which regulator outputs are monitored for nRESET functionality.

nIRQ (Interrupt)

The nIRQ interrupt output serves as a system processor alert signal, generated by various monitored conditions within the SGM260321. Individual fault conditions can be masked through the I^2C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet. nIRQ can be triggered from:

- Input Voltage Lower than V_{SYSMON}.
- Die Temperature Above Warning Threshold.
- Buck Converter Exceeding Current Limit for 16 Consecutive Cycles after Soft-Start or the UV/OV Condition.
- LDO Regulator Exceeding Current Limit after Soft-Start or the UV/OV Condition.

If any of these faults occur, the nIRQ output is pulled low. After being pulled low, reading the interrupt status registers via I^2C clears both the interrupt signal and status bit only when the fault is removed. If the fault persists, nIRQ remains low and the status bit stays unchanged. The relevant status registers are located at 0x00, 0x30, 0x40, 0x50, 0x60, and 0x65. The CMI configuration defines which GPIO serves as the nIRQ pin.

SYSMON

GPIOx pins can be configured to output active-low SYSMON signals for host system monitoring. It gets low when $V_{IN\_A} < V_{SYSMON}$ falling threshold, and it gets high when $V_{IN\_A} > V_{SYSMON}$, It is a real-time signal.

DETAILED DESCRIPTION: BUCK CONVERTERS

General Description

The SGM260321 integrates three Buck converters: Buck1 provides a 4A output, while Buck2 and Buck3 each deliver 3A. Buck1 operates as a fixed-frequency, constant-off-time (COFT) controlled synchronous converter, whereas Buck2 and Buck3 use constant-on-time (COT) control. These Buck converters switch at either 1.125MHz or 2.25MHz and feature internal compensation, requiring only three small external components (C_{IN}, C_{OUT}, and L) for operation.

To minimize noise in sensitive applications, the regulators incorporate a switching phase delay and offset. Additionally, all regulators support a range of standard and custom output voltages and can be controlled via the I^2C interface, enabling advanced power management capabilities.

Each Buck converter has its own dedicated input pin and power ground pin. To ensure optimal performance, each converter requires a dedicated input capacitor placed strategically to minimize power routing loops. Although the Buck converters have separate input pins, all inputs must be tied to the same voltage potential.

Buck1 can be configured as a bypass switch for systems operating with a 3.3V bus voltage. This bypass mode enables full sequencing functionality, allowing the 3.3V bus to serve as the input for other power supplies while maintaining proper sequencing to the downstream load.

The SGM260321 Buck regulators offer extensive configurability and can be easily adjusted via I^2C, eliminating the need for PCB modifications when hardware requirements change. The following I^2C controlled functions are available:

- Real-Time Monitoring of Power Good, Over-Voltage (OV), Under-Voltage and Current Limit
- Selective Fault Masking
- Dynamic Output Voltage Adjustment
- On/Off Control
- Soft-Start Ramp Configuration
- Switching Delay and Phase Control
- Power Save Mode
- Over-Current Thresholds Adjustment

100% Duty Cycle Operation

Buck1 supports 100% duty cycle operation, where the high-side FET remains continuously on. This creates a direct connection from the input to the output through the inductor, minimizing dropout voltage, an essential feature for battery-powered applications.

Operating Mode

By default, all Buck converters operate in fixed-frequency PWM mode under medium to heavy loads. At light loads, it automatically transitions to a proprietary power-saving mode that reduces conduction losses by preventing negative inductor current.

Power save mode (PSM) minimizes quiescent current between switching cycles, allowing users to optimize power consumption, voltage ripple, and transient response based on their specific application. PSM is activated when the Bx_FORCE_CCM bit is set to 0.

Alternatively, the Buck converters can be forced to remain in PWM mode at light loads by setting Bx_FORCE_CCM = 1. While this reduces efficiency at light load condition, it enhances transient response.

Synchronous Rectification

Buck1, Buck2, and Buck3 each incorporate integrated synchronous rectifiers, enhancing efficiency while reducing overall solution size and cost by eliminating the need for external rectifiers.

Soft-Start

Buck1, Buck2, and Buck3 feature built-in soft-start ramps to control the output voltage rise, reducing input inrush current and ensuring a smooth, monotonic start-up regardless of load conditions. This mechanism is activated after the regulator is enabled and recovered from short-circuit or other fault. The soft-start duration can be adjusted via the BUCK_SS bit. If the BUCK_SS bit is set to 0, it is 500μs. If the BUCK_SS bit is set to 1, it is 250μs.

DETAILED DESCRIPTION: BUCK CONVERTERS (continued)

Output Voltage Setting

Buck1, Buck2, and Buck3 regulate their output voltage based on the value set in the I^2C register Bx_VSET0 during normal operation and Bx_VSET1 in DVS mode. The SGM260321 provides two programmable output voltage ranges.

Output Range 1 is available for Buck1 and Buck2, allowing voltages to be set between 0.6V and 2.991V in 9.375mV steps. The output voltage is determined by:

$$V_{BUCKx} = 0.6V + V_{Bx\_VSETx} \times 0.009375V$$

where V_{Bx_VSETx} represents the decimal equivalent of the value in the I^2C Bx_VSETx register for each regulator. The Bx_VSETx registers use an unsigned 8-bit binary format. For example, if Buck1's B1_VSET0 register contains the binary value 0100 0000 (decimal 64), the output voltage will be 1.2V.

Output range 2 is available for Buck1, Buck2, and Buck3, supporting voltages between 0.8V and 3.9875V in 12.5mV steps. The voltage calculation follows:

$$V_{BUCKx} = 0.8V + V_{Bx\_VSETx} \times 0.0125V$$

The following table summarizes the available reference voltage options for each Buck converter.

Table 5. Buck1/Buck2 Voltage Reference Selections

	B1_VREF/B2_VREF = 0	B1_VREF/B2_VREF = 1
V_{REF}	0.6V	0.8V
V_{OUT} Range	0.6V ~ 2.991V	0.8V ~ 3.9875V
V_{OUT} Step Size	9.375mV	12.5mV

Refer to each IC's CMI for the specific programming range of each Buck converter. It is important to note that the programming range for Buck1 and Buck2 is not user accessible. Modifying this register value may lead to unpredictable IC behavior.

DVS

Each Buck converter supports dynamic voltage scaling (DVS). Under normal conditions, for most CMI options, each output is regulated to the voltage set by its Bx_VSET0[7:0] I^2C register. When DVS is activated, the output can be configured to regulate to its Bx_VSET1[7:0] voltage, allowing for dynamic adjustments based on system requirements.

During the voltage transition between Bx_VSET0[7:0] and Bx_VSET1[7:0], as well as from Bx_VSET1[7:0] back to Bx_VSET0[7:0], the Buck converters is forced into PWM mode. This ensures a rapid transition to the new voltage level. The outputs adjust between the two set points at a controlled slew rate to minimize inrush currents and maintain system stability.

To ensure fault-free operation, the user must ensure that the combined output load current and the current needed to charge the output capacitance during a DVS rising voltage transition do not exceed the regulator's current limit setting. As with any power supply, excessively fast output voltage changes may demand a current beyond the set current limit. The user should carefully consider the voltage step size, slew rate, and load conditions to avoid instantaneous loading that could trigger a current limit event.

Enable/Disable Control

During normal operation, each Buck converter can be enabled or disabled via the I^2C interface by writing to the regulator's Bx_ON bit. It is important to note that disabling a regulator serving as an input trigger for another regulator may or may not disable the dependent regulators, depending on the specific CMI setting. Each Buck converter includes a load discharge function that rapidly pulls the output voltage to ground when the converter is disabled. This function utilizes an internal resistor (4.4Ω for Buck1 and 6.6Ω for Buck2/3) connected from the output to PGND upon disabling the converter.

Optimizing Noise

Each Buck converter includes several I^2C configurable features to enhance functionality. The turn-on timing of the top PMOS can be shifted by approximately 100ns from the master clock edge using the Bx_PHASE_DLY bit. Additionally, the Bx_PHASE bit allows the turn-on timing to be aligned with either the rising or falling edge of the clock.

DETAILED DESCRIPTION: BUCK CONVERTERS (continued)

Over-Current and Short-Circuit Protection

Each Buck converter includes over-current and short-circuit protection. Over-current protection is implemented using cycle-by-cycle current limit. The peak current threshold for Buck1 and the valley current threshold for Buck2/3 are set by the Bx_ILIM_SET[1:0] bit.

For Buck1, if the peak current reaches 75% of the programmed threshold for 16 consecutive cycles, the IC asserts nIRQ low and sets the B1_ILIM_WARN bit to 1, but it continues to operate normally. When peak current reaches the set threshold, the IC immediately turns off the high-side FET for the switching cycle. The FET turns on only after the low-side current falls below the valley current limit threshold. If B1_ILIM_WARN_FLTMSK = 1 and peak thresholds are exceeded for 16 consecutive cycles, the IC pulls the nIRQ pin low if the fault is not masked.

For Buck2 and Buck3, if the valley current exceeds 75% of the programmed threshold for 16 consecutive switching cycles, the IC asserts nIRQ low and sets the Bx_ILIM_WARN bit to 1, but it continues to operate normally. Buck2 and Buck3 regulate the maximum valley current of the low-side FET by preventing the high-side FET from turning on until the low-side FET current falls below the valley current limit. If Bx_ILIM_WARN_FLTMSK is set to 1 and the valley current reaches the threshold for 16 consecutive switching cycles, the IC asserts nIRQ low if the fault is not masked. This often triggers system shutdown through an unmasked under-voltage (UV) protection response.

If a short-circuit condition causes the output voltage to drop below 30% of its nominal value, the regulator shuts down. It then attempts to restart after a 10ms delay. If the fault condition is not masked, the IC enters the over-voltage/short-circuit protection (UV/OV) fault state, disabling all power supplies before initiating a system restart after 10ms.

The Buck converters have built-in current foldback protection. Once soft-start is complete, if a short-circuit or overload condition causes the switch current to exceed the cycle-by-cycle current limit for more than 16 consecutive switching cycles, and the output voltage drops below 30% of its nominal value, the IC reduces the current limit to protect the system.

This mechanism helps minimize system-level power dissipation during short-circuit or overload conditions. If the load current decreases sufficiently, allowing the output voltage to recover and reach regulation within the reduced current limit, the IC restores the default current limit and resumes normal operation.

If a Buck converter triggers over-current or short-circuit protection, the event is recorded in the ILIM I^2C registers. These registers latch their status until they are read via I^2C. The over-current condition can be masked using the Bx_ILIM_FLTMSK bit.

Compensation

The Buck converters use COFT (Buck1) and COT (Buck2/3) control with an internal compensation scheme that simplifies external component selection and enhances transient performance across the entire operating range. No compensation design is needed, just follow the simple guidelines below when selecting external components.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. 10μF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. The input voltage ripple is calculated using the following Equation:

$$V_{RIPPLE} = I_{OUT} \times \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{sw} \times C_{IN}}$$

Consider the capacitor's DC bias effects and maximum ripple current rating when using sizes smaller than 0805, as DC bias significantly impacts actual capacitance. The input capacitor is typically X5R, X7R, or a similar dielectric. Proper placement is critical. Each Buck's input capacitor must be positioned as close to the IC as possible. The traces from V_{IN_Bx} to the capacitor and from the capacitor to PGNDx should be as short and wide as possible.

DETAILED DESCRIPTION: BUCK CONVERTERS (continued)

Inductor Selection

The Buck converters use COFT (Buck1) and COT (Buck2 and Buck3) control with a proprietary internal compensation scheme that simplifies external component selection and optimizes transient performance across the full operating range. The SGM260321 is designed for 0.47μH inductors. Select an inductor with low DC resistance and a DC rating at least 30% higher than the maximum output current to prevent saturation. The inductor ripple current is calculated using the following equation:

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times V_{OUT}}{f_{sw} \times L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The SGM260321 is optimized for compact, low-ESR ceramic output capacitors. Buck1 generally requires three 22μF capacitors, while Buck2 and Buck3 each require two 22μF capacitors. Increasing the output capacitance can help minimize voltage ripple and enhance load transient response if necessary. Ensure the output ripple voltage remains below 1% of the output voltage. The equation below defines the relationship between output voltage ripple and output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 \times f_{sw} \times C_{OUT}}$$

Where ΔI_L is the inductor ripple current, f_{SW} is the switching frequency, and C_{OUT} is the effective output capacitance, considering DC bias effects. When using capacitors smaller than 0805, ensure they meet the required ripple current rating and account for capacitance reduction due to DC bias. The actual capacitance can vary significantly based on voltage conditions. Typically, X5R, X7R, or similar dielectric capacitors are recommended for the output stage.

Buck1 Bypass Mode

Buck1 can be configured as a bypass switch for systems with a 3.3V bus. In bypass mode, the Buck1 PMOS functions as a switch, while the NMOS remains disabled. The bypass switch activates the 3.3V rail with the programmed delay and soft-start time.

OV protection is disabled, and no over-voltage detection circuitry is present on the bypass switch output. After the PMIC is powered on, please do not modify the working mode of Buck1.

DETAILED DESCRIPTION: LDO CONVERTERS

General Description

The SGM260321 integrates two 300mA low dropout (LDO) regulators, optimized for minimal dropout voltage and high power supply rejection ratio (PSRR). They can also operate in load switch mode. Each LDO requires only two small external capacitors (C_{IN} and C_{OUT}) for proper function. The default output voltages are factory-set but can be adjusted via the I^2C interface for advanced power management needs.

Soft-Start

Each LDO includes a soft-start circuit that controls the output voltage ramp, reducing input inrush current and ensuring monotonic start-up. This function is active whenever the LDO is enabled and after recovery from a short-circuit or other fault conditions. The soft-start time for each LDO is fixed at 300μs.

Output Voltage Setting

The LDOs regulate the output voltage based on their I^2C registers, LDO1_VSET[7:0] and LDO2_VSET[7:0]. Unlike the Buck converters, they do not have a second VSET register. The LDOs support two output voltage range setting, controlled by the I^2C register bits LDOx_VREF, which is factory-set and cannot be changed by the user.

Table 6. Output Voltage Setting

	LDOx_VREF = 0	LDOx_VREF = 1
V_{REF}	0.6V	0.8V
V_{OUT} Range	0.6V ~ 2.991V	0.8V ~ 3.9875V
V_{OUT} Step Size	9.375mV	12.5mV

When LDOx_VREF = 1, the LDO output voltages are determined by the following equation.

$$V_{LDOx} = 0.8V + V_{LDOx\_VSET} \times 0.0125V$$

When LDOx_VREF = 0, the LDO output voltages are determined by the following equation.

$$V_{LDOx} = 0.6V + V_{LDOx\_VSET} \times 0.009375V$$

Enable/Disable Control

During normal operation, each LDO can be enabled or disabled through the I^2C interface by setting the regulator's LDOx_ON bit. Disabling an LDO that serves as an input trigger for another regulator may or may not affect the downstream regulators, depending on the specific CMI setting. Each LDO includes a load discharge function that rapidly pulls the output voltage to ground when the LDO is disabled. This is achieved by connecting an internal 50Ω resistor from the output to AGND when the LDO is turned off.

Over-Current and Short-Circuit Protection

Each LDO features over-current detection and short-circuit protection. Upon reaching the current limit, the IC can either turn off the output to enter hiccup mode or reduce the output current limit until the overload is resolved. This function is controlled by the LDOx_ILIM_SHDN bit.

The over-current threshold is controlled by the LDOx_ILIM_SET bit. During overload or short-circuit conditions, the LDO limits the output current, causing the output voltage to drop. This can lead to both a current limit fault and an under-voltage fault. If the LDO load hits the over-current threshold, the status is stored in the ILIM_LDOx I^2C registers, which remain latched until read. If current limiting causes the output voltage to drop to 30% of the nominal value, triggering an under-voltage condition, the IC will shut down all power supplies, pull nIRQ low, and enter the UV/OV fault state, unless the faults are masked. Once in the UV/OV fault state, the IC restarts after 10ms and follows the default sequencing. The over-current conditions resulting in under-voltage or short-circuit protection can be masked by the LDOx_UV_FLTMSK bit and LDOx_ILIM_FLTMSK bit. When masked, nIRQ won't assert, but the LDO will still shut down or limit current according to the LDOx_ILIM_SHDN bit. In this case, the IC will not enter the UV/OV fault state due to the masking. If the LDO shuts down due to the LDOx_ILIM_SHDN bit, it will automatically restart after 10ms.

DETAILED DESCRIPTION: LDO CONVERTERS (continued)

Input Capacitor Selection

The VIN_A pin provides input power to both LDOs and requires a high-quality, low-ESR ceramic capacitor. A 2.2μF capacitor is typically sufficient, but a larger value can be used without restriction. The input capacitor should have an X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high-quality, low-ESR ceramic output capacitor, A 1μF is a typical choice. The capacitor should have an X5R, X7R, or similar dielectric.

Load Switch Mode

LDOs can operate in load switch mode, where they pass the input voltage directly to the output. In this mode, the device continues to monitor load current and shuts off if it exceeds LDOx_ILIM_SET[1:0] value, entering hiccup mode until the fault is cleared. However, output over-voltage is not monitored. Load switch mode is enabled by setting the LDOx_LSW_EN bit to 1. After the PMIC is powered on, please do not modify the working mode of LDOx.

I²C COMPATIBLE INTERFACE

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM260321 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM260321 operates as a slave device that address (adjustable) is 0x25 (25H). It has fifty 8-bit registers, numbered from 0x00 to 0x69. A register read beyond REG69 (0x69) returns 0xFF.

Physical Layer

The standard I²C interface of SGM260321 supports standard mode and fast mode plus communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode plus is up to 1000kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I2C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown Figure 5. All transactions begin by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

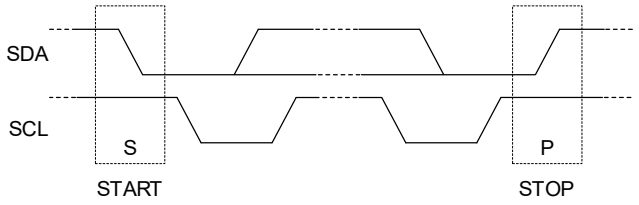


Figure 5. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 6.

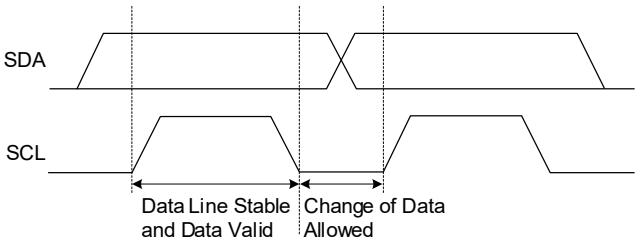


Figure 6. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 7 shows the byte transfer process with I²C interface.

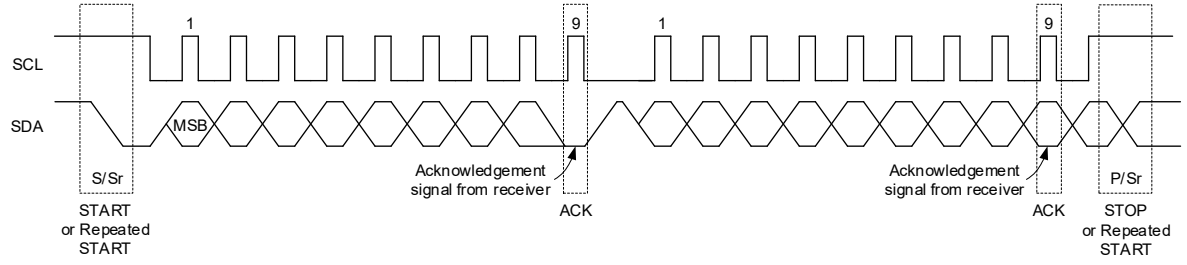


Figure 7. Byte Transfer Process

I²C COMPATIBLE INTERFACE (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 8.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 9 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 10), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

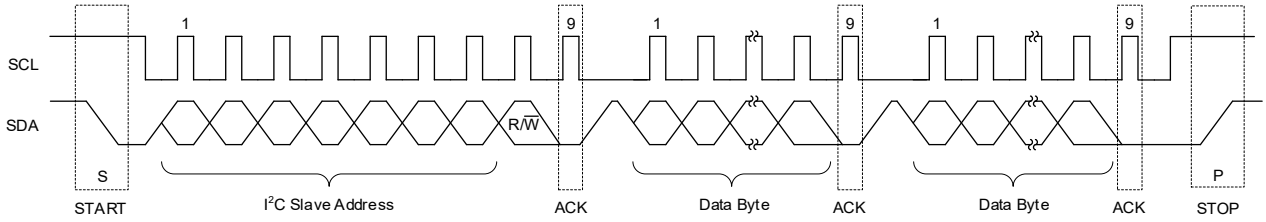


Figure 8. Data Transfer Transaction

I²C COMPATIBLE INTERFACE (continued)

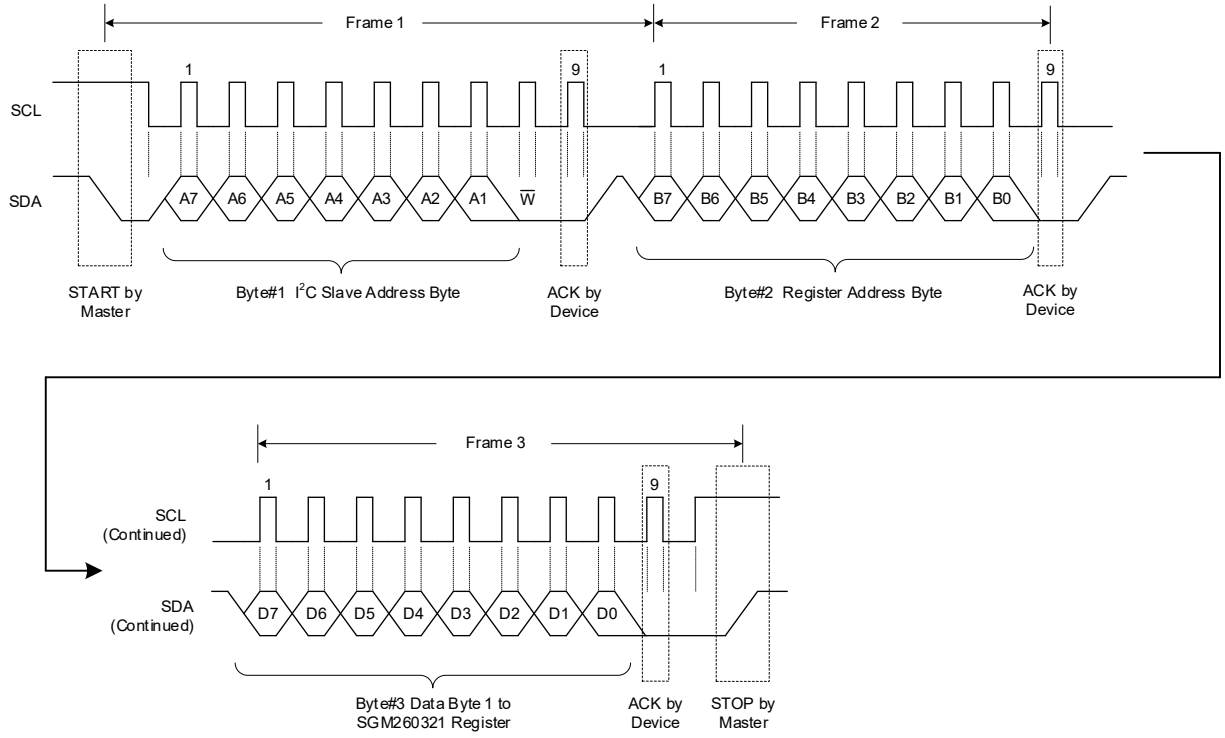


Figure 9. A Single Write Transaction

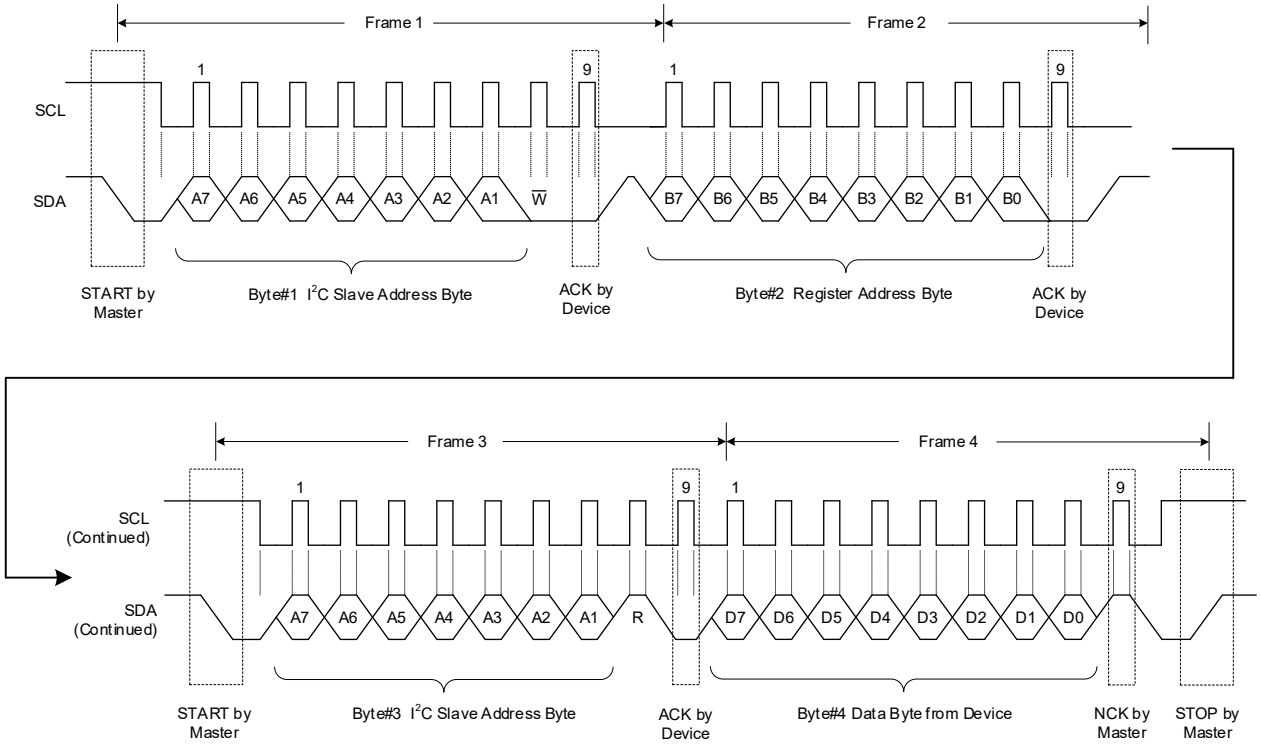


Figure 10. A Single Read Transaction

I²C COMPATIBLE INTERFACE (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM260321 for REG00 through REG69 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

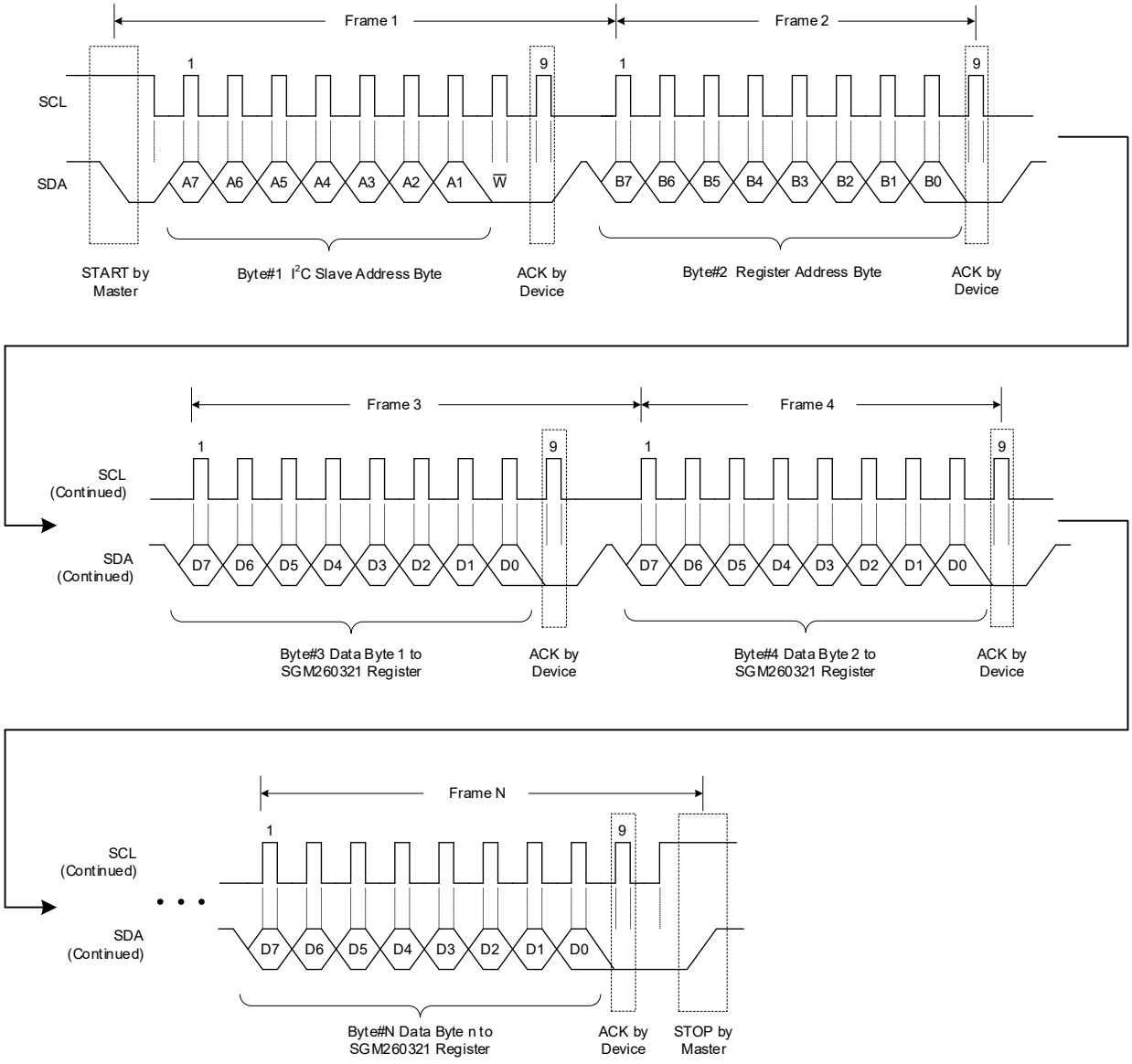


Figure 11. A Multi-Write Transaction

I²C COMPATIBLE INTERFACE (continued)

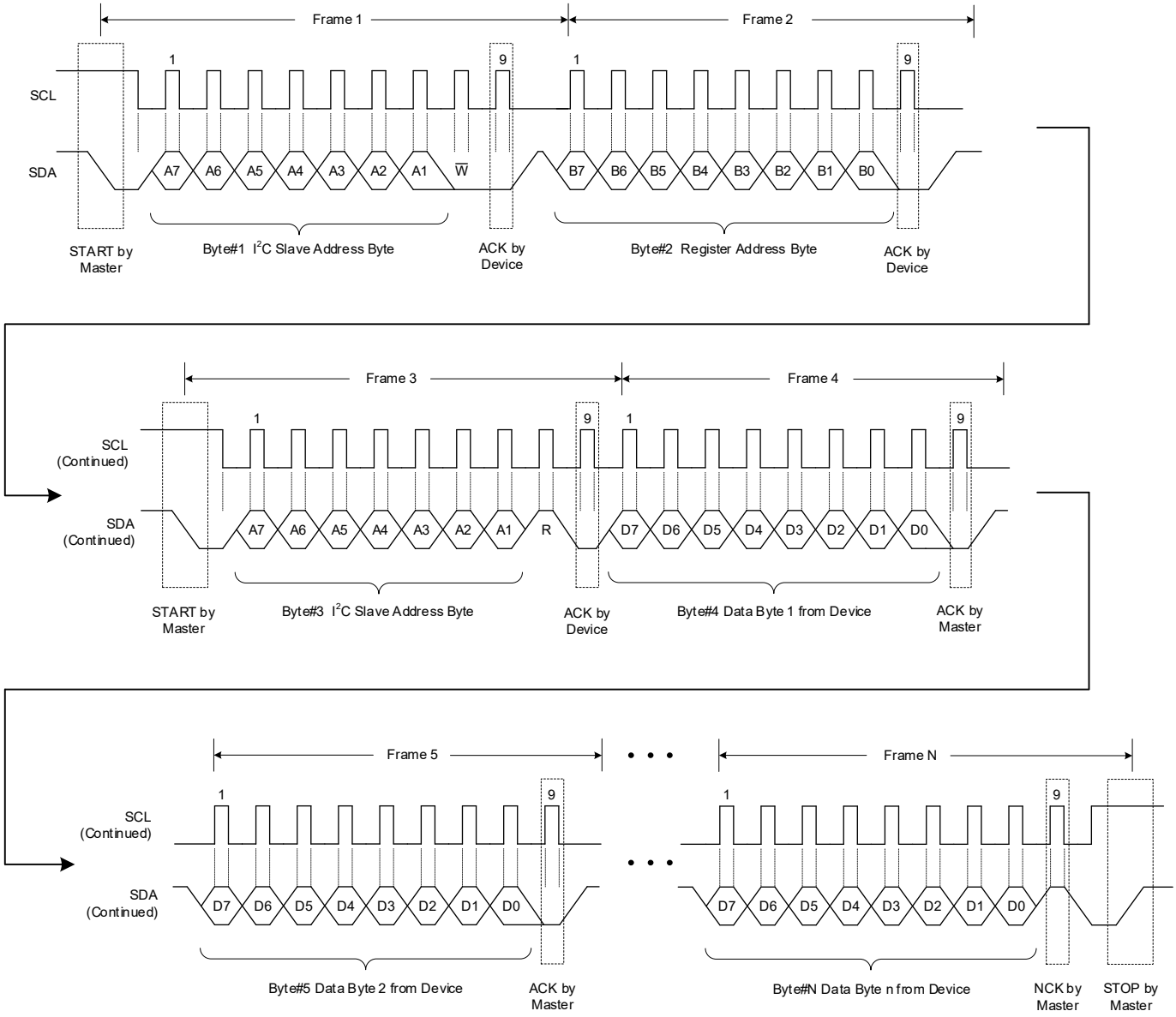


Figure 12. A Multi-Read Transaction

CMI OPTIONS

The SGM260321 is available in default configurations with a CMI code. It is programmed in the default configuration at the factory. Configurable options include system level sequencing, output voltage, start-up delay, soft-start time, sleep and DPSLP modes, and operating modes, etc. Please contact SGMICRO for a custom configuration with a new CMI code.

CMI 003: SGM260321-003

The following tables describe the SGM260321-003 IC setting.

Table 7. Voltage and Currents

Rail	Active Mode Voltage Bx_VSET0 (V)	DVS Voltage Bx_VSET1 (V)	DVS Input Trigger	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	f_{SW} (kHz)
Buck1	2.5	N/A	N/A	Off	Off	5.6	2250
Buck2	0.8	0.7	GPIO4	On	On	4.2	2250
Buck3	1.8	1.2	GPIO2	Off	Off	3.4	2250
LDO1	1.8	N/A	N/A	On	On	0.46	N/A
LDO2	1.8 (LDO Mode) 3.3 (LSW Mode)	N/A	GPIO3	On	On	0.365	N/A

Table 8. Start-Up and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	Start-Up Delay (ms)	Soft-Start (μs)	Shutdown Delay (ms) (Enter Sleep or DPSLP)
LDO2	1	SYSMON	0	300	0.5
LDO1	1	SYSMON	0	300	0.5
Buck2	2	LDO1	0	500	0.5
Buck1	3	Buck2	0	500	0
Buck3	4	Buck1	0.25	500	0

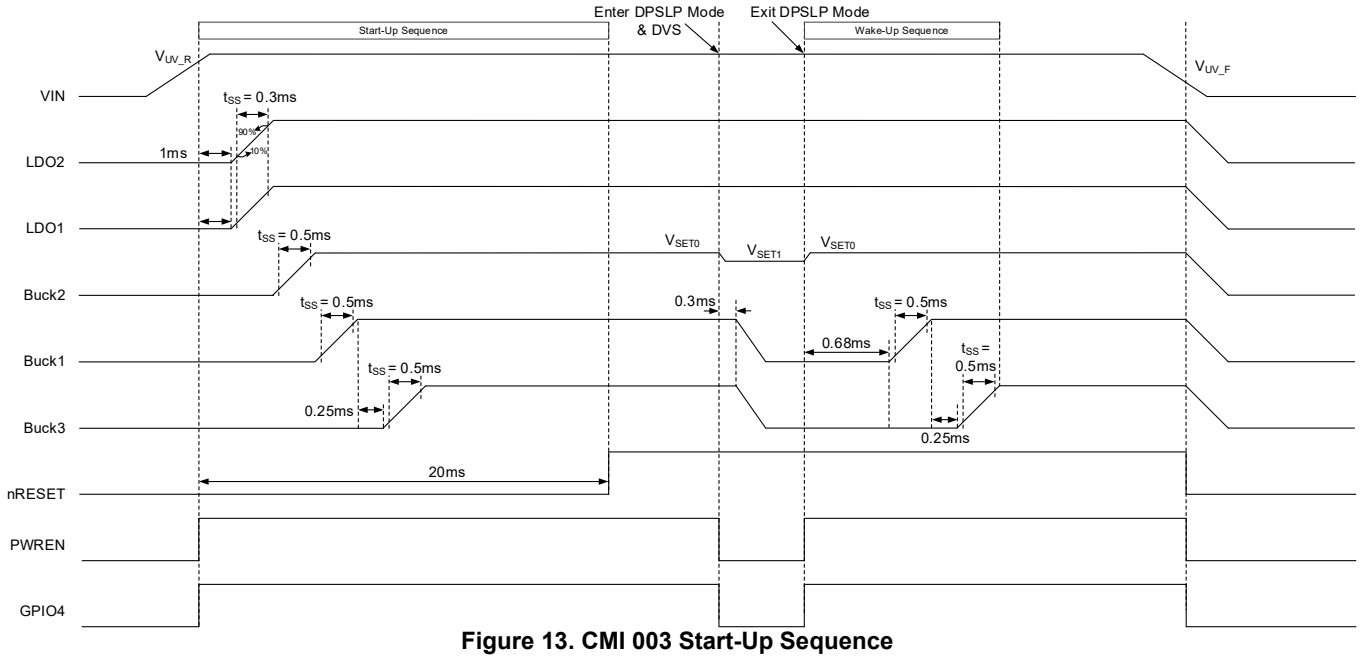


Figure 13. CMI 003 Start-Up Sequence

CMI OPTIONS (continued)

I^2C Address
The SGM260321-003 7-bit I^2C address is 0x25. Use address 0x4A when writing and 0x4B when reading.

GPIO1 (Pin C7) - nRESET
GPIO1 is configured as an open-drain nRESET. nRESET goes high 20ms after $V_{IN\_A} > V_{SYSMON}$.

GPIO2 (Pin C6) - Buck3 DVS Voltage Select
GPIO2 is configured as an input to select the Buck3 output voltage. When GPIO2 is high, B3_VSET0[7:0] sets Buck3 to 1.8V. When GPIO2 is low, B3_VSET1[7:0] sets Buck3 to 1.2V.

GPIO3 (Pin B6) - LDO2 Mode Select
GPIO3 is configured as an input to select the LDO mode. When GPIO3 is high, LDO2 works in LDO mode, and LDO2_VSET0[7:0] sets LDO2 to 1.8V. When GPIO3 is low, LDO2 works in the load switch mode.

GPIO4 (Pin D7) - Buck2 DVS Voltage Select
GPIO4 is configured as an input to select the Buck2 output voltage. When GPIO4 is high, B2_VSET0[7:0] sets Buck2 to 0.8V. When GPIO4 is low, B2_VSET1[7:0] sets Buck2 to 0.7V.

PWREN (Pin E1) - DPSLP Mode Select
When PWREN is high, the IC is in active mode. When PWREN is low, the IC is in DPSLP mode.

V_{SYSMON}
V_{SYSMON} = 2.9V

Buck1 Voltage Setting
Buck1 reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.9875V in 12.5mV steps.

Buck2 Voltage Setting
Buck2 reference voltage is 0.6V. This sets the allowable voltage range between 0.6V and 2.991V in 9.375mV steps.

LDO Voltage Setting
The LDO reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.9875V in 12.5mV steps.

REGISTER MAPS

The SGM260321 is a power management unit designed to supply power to a variety of processors, peripherals, microcontrollers, FPGAs, and solid-state drive applications. The SGM260321 features three DC/DC Buck converters with integrated power FETs and two low dropout regulators (LDOs). Output voltage of each regulator can be adjusted over a wide range using the I^2C interface.

Modern processors have complex start-up and sequencing requirements, including the need to manage transitions into/out of sleep or DPSLP mode. The SGM260321 is engineered to meet these stringent power system demands.

While the SGM260321 has a default configuration pre-programmed from the factory, the setting can be customized via the I^2C interface to optimize performance for specific processors and applications. System level sequencing, output voltage, switching frequency, start-up delay, soft-start time, sleep and DPSLP modes, operating modes, and other setting can all be configured. These configurations are identified using a Code Matrix Index (CMI). Note that the default register values provided below are specific to the SGM260321's CMI 003.

Register Types

The register types of SGM260321 are as follows.

- **Basic Volatile: R/W and R**

The register values can be modified to change the device function. However, if the power is recycled, the changes are lost. The default values of register are fixed and cannot be altered.

- **Basic Non-Volatile: R/W and R**

The register values can be modified to change the device function. Although changes are lost upon power is recycled, the default values can be pre-set at the factory to tailor the device for specific applications. For more demands, please consult with sales.

- **Factory Non-Volatile: Factory Bits**

The bits are used by the factory to set the function of the product. Customers can read but not write to these bits. The factory can modify the default values to optimize the device for particular applications.

The SGM260321 includes six primary register areas.

Master Register	0x00 to 0x15
Buck1 Register	0x30 to 0x35
Buck2 Register	0x40 to 0x45
Buck3 Register	0x50 to 0x55
LDO1 Register	0x60 to 0x64
LDO2 Register	0x65 to 0x69

The following table shows the SGM260321 register map. Please note that the register addresses are not all in order.

REGISTER MAPS (continued)

Address (HEX)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
	Master Registers							
0x00	TWARN	VSYSSTAT	VSYSDAT	TMSK	VSYSMSK	Factory Mode	Reserved	Reserved
0x01	Reserved							
0x02	TRST_DLY[1:0]		VSYSMON[3:0]				BUCK_SS	B1_BYP_EN
0x03	DIS_DPSLP_OFF_DLY	DIS_OVUV_SHDN	POWER_OFF	EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON	IO1_ADD_DLY	IO2_ADD_DLY
0x04	LDO1_LSW_EN	LDO2_LSW_EN	EXT_EN_OFF_AT_SLEEP	EXT_EN_OFF_AT_DPSLP	Reserved	SLEEP	SLEEP_EN	DPSLP_EN
0x05	ADDRESS[1:0]		VIN_OV_SEL	B1_VREF	B2_VREF	LDO1_VREF	LDO2_VREF	Reserved
0x06	Reserved						IO1_DLY[2:0]	
0x07	Reserved						IO2_DLY[2:0]	
0x08	Reserved						IO3_DLY[2:0]	
0x09	Reserved						IO4_DLY[2:0]	
0x0A	Reserved							
0x0B	Reserved							
0x0C	Reserved							
0x0D	Reserved							
0x0E	Reserved							
0x0F	Reserved							
0x10	Reserved							
0x11	Reserved							
0x12	CMI NUMBER[7:0]							
0x13	Manufacture ID[7:0]							
0x14	Device ID[7:0]							
0x15	Reserved							
	Buck1 Registers							
0x30	B1_POK	B1_OV	B1_ILIM	B1_ILIM_WARN	B1_UV_FLTMSK	B1_OV_FLTMSK	B1_ILIM_FLTMSK	B1_ILIM_WARN_FLTMSK
0x31	B1_VSET0[7:0]							
0x32	B1_VSET1[7:0]							
0x33	B1_ON	B1_SLEEP_EN	B1_DPSLP_EN	B1_ILIM_SET[1:0]		B1_RST	B1_FORCE_CCM	B1_FSW
0x34	B1_QLTCH	B1_ON_DLY[1:0]		B1_OFF_DLY[4:0]				
0x35	B1_PHASE_DLY	B1_PHASE	Reserved					
	Buck2 Registers							
0x40	B2_POK	B2_OV	B2_ILIM	B2_ILIM_WARN	B2_UV_FLTMSK	B2_OV_FLTMSK	B2_ILIM_FLTMSK	B2_ILIM_WARN_FLTMSK
0x41	B2_VSET0[7:0]							
0x42	B2_VSET1[7:0]							
0x43	B2_ON	B2_SLEEP_EN	B2_DPSLP_EN	B2_ILIM_SET[1:0]		B2_RST	B2_FORCE_CCM	B2_FSW
0x44	B2_QLTCH	B2_ON_DLY[1:0]		B2_OFF_DLY[4:0]				
0x45	B2_PHASE_DLY	B2_PHASE	Reserved					
	Buck3 Registers							
0x50	B3_POK	B3_OV	B3_ILIM	B3_ILIM_WARN	B3_UV_FLTMSK	B3_OV_FLTMSK	B3_ILIM_FLTMSK	B3_ILIM_WARN_FLTMSK
0x51	B3_VSET0[7:0]							
0x52	B3_VSET1[7:0]							
0x53	B3_ON	B3_SLEEP_EN	B3_DPSLP_EN	B3_ILIM_SET[1:0]		B3_RST	B3_FORCE_CCM	B3_FSW
0x54	B3_QLTCH	B3_ON_DLY[1:0]		B3_OFF_DLY[4:0]				
0x55	B3_PHASE_DLY	B3_PHASE	Reserved					

REGISTER MAPS (continued)

Address (HEX)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
	LDO1 Registers							
0x60	LDO1_POK	LDO1_OV	ILIM_LDO1	Reserved	LDO1_UV_FLTMSK	LDO1_OV_FLTMSK	LDO1_ILIM_FLTMSK	Reserved
0x61	LDO1_VSET[7:0]							
0x62	LDO1_ON	LDO1_SLEEP_EN	LDO1_DPSLP_EN	LDO1_ILIM_SET[1:0]		LDO1_RST	LDO1_ILIM_SHDN	Reserved
0x63	LDO1_QLTCH	LDO1_ON_DLY[1:0]		LDO1_OFF_DLY[4:0]				
0x64	Reserved							
	LDO2 Registers							
0x65	LDO2_POK	LDO2_OV	ILIM_LDO2	Reserved	LDO2_UV_FLTMSK	LDO2_OV_FLTMSK	LDO2_ILIM_FLTMSK	Reserved
0x66	LDO2_VSET[7:0]							
0x67	LDO2_ON	LDO2_SLEEP_EN	LDO2_DPSLP_EN	LDO2_ILIM_SET[1:0]		LDO2_RST	LDO2_ILIM_SHDN	Reserved
0x68	LDO2_QLTCH	LDO2_ON_DLY[1:0]		LDO2_OFF_DLY[4:0]				
0x69	Reserved							

NOTE: Avoid altering these reserved register values, as doing so may impact the device's functionality.

MASTER REGISTERS

I²C Slave Address of SGM260321-003: 0x25

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

Register Address: 0x00

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	TWARN	0	R	0 = T_J < T_{WARN} threshold (default) 1 = T_J > T_{WARN} threshold If die temperature > +125℃, this bit goes high. It stays high until die temperature < +105℃ and it is read.
D[6]	VSYSSTAT	0	R	0 = V_{IN_A} > V_{SYSMON} threshold (default) 1 = V_{IN_A} < V_{SYSMON} threshold When V_{IN_A} < V_{SYSMON}, this bit goes high and stays high until V_{IN_A} > V_{SYSMON} and it is read.
D[5]	VSYSDAT	0	R	0 = V_{IN_A} > V_{SYSMON} (default) 1 = V_{IN_A} < V_{SYSMON} Real-time status indicating whether the input voltage is higher or lower than the V_{SYSMON} threshold.
D[4]	TMSK	1	R/W	0 = Interrupt is not masked 1 = Interrupt is masked (default) Mask the thermal warning status interrupt bit.
D[3]	VSYSMSK	1	R/W	0 = Interrupt is not masked 1 = Interrupt is masked (default) Mask the V_{IN_A} < V_{SYSMON} status interrupt bit.
D[2]	FACTORY MODE	0	R	0 = In normal mode (default) 1 = In factory mode Status indicator, which is used to check whether the device is running normally. Factory mode is not accessible to user.
D[1:0]	Reserved	00	R	Reserved

Register Address: 0x01

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0000	R	Reserved

Register Address: 0x02

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	TRST_DLY[1:0]	00	R/W	nRESET Delay Time 00 = 20ms (default) 01 = 40ms 10 = 60ms 11 = 100ms
D[5:2]	VSYSMON[3:0]	0010	R/W	V_{SYSMON} Rising Threshold Voltage Range: 2.7V (0000) - 4.2V (1111) Step size = 0.1V
D[1]	BUCK_SS	0	R/W	Buck SS Time 0 = 500μs (default) 1 = 250μs
D[0]	B1_BYP_EN	0	R/W	0 = Buck mode (default) 1 = Bypass mode

MASTER REGISTERS (continued)

Register Address: 0x03

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	DIS_DPSLP_ OFF_DLY	0	R/W	0 = Activate power-off delay when transitioning to DPSLP state (default) 1 = Deactivate power-off delay when transitioning to DPSLP state
D[6]	DIS_OVUV_SHDN	0	R/W	0 = If UV/OV fault event occurs, the device shuts down all rails and enters the system hiccup mode (default) 1 = Disable the system hiccup mode
D[5]	POWER_OFF	0	R/W	0 = Start a power-on sequence (default) 1 = Shut down all regulators at the same time
D[4]	EN_DVS_I2C	0	R/W	I^2C DVS Function 0 = Disable 1 = Enable
D[3]	SEL_DVS_IN	0	R/W	0 = The I2C_DVS_ON bit controls the DVS function (default) 1 = The device enters DVS when it enters sleep mode This bit is applicable only when the EN_DVS_I2C is set to 1
D[2]	I2C_DVS_ON	0	R/W	0 = Normal device operation (default) 1 = Turn on DVS mode on the device. This bit is applicable only when the SEL_DVS_IN is set to 0
D[1]	IO1_ADD_DLY	0	R/W	0 = Disable additional 2.5ms delay for GPIO1 (default) 1 = Enable additional 2.5ms delay for GPIO1
D[0]	IO2_ADD_DLY	0	R/W	0 = Disable additional 2.5ms delay for GPIO2 (default) 1 = Enable additional 2.5ms delay for GPIO2

Register Address: 0x04

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO1_LSW_EN	0	R/W	LDO1 Function 0 = As a low dropout regulator (LDO) (default) 1 = As a load switch
D[6]	LDO2_LSW_EN	1	R/W	LDO2 Function 0 = As a low dropout regulator (LDO) 1 = As a load switch (default)
D[5]	EXT_EN_OFF_ AT_SLEEP	1	R/W	0 = Normal operation 1 = Set EXT_EN to low if the device enters sleep mode (default)
D[4]	EXT_EN_OFF_ AT_DPSLP	1	R/W	0 = Normal operation 1 = Set EXT_EN to low if the device enters DPSLP mode (default)
D[3]	Reserved	0	R/W	Reserved
D[2]	SLEEP	0	R/W	0 = PMIC is in power-on state (default) 1 = PMIC transitions to sleep state
D[1]	SLEEP_EN	0	R/W	0 = SLEEP mode is turned off (default) 1 = SLEEP mode is turned on
D[0]	DPSLP_EN	1	R/W	0 = DPSLP mode is turned off 1 = DPSLP mode is turned on (default)

MASTER REGISTERS (continued)

Register Address: 0x05

Factory Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	ADDRESS[1:0]	00	R	I^2C Address 00 = 010 0101b (0x25h) address (default) 01 = 010 0111b (0x27h) address 10 = 110 0111b (0x67h) address 11 = 110 1011b (0x6Bh) address
D[5]	VIN_OV_SEL	1	R	V_{IN} OV Threshold. 0 = V_{OV} = 5.7V 1 = V_{OV} = 3.8V (default)
D[4]	B1_VREF	1	R	Buck1 Reference Voltage 0 = 0.6V 1 = 0.8V (default)
D[3]	B2_VREF	0	R	Buck2 Reference Voltage 0 = 0.6V (default) 1 = 0.8V
D[2]	LDO1_VREF	1	R	LDO1 Reference Voltage 0 = 0.6V 1 = 0.8V (default)
D[1]	LDO2_VREF	1	R	LDO2 Reference Voltage 0 = 0.6V 1 = 0.8V (default)
D[0]	Reserved	0	R	Reserved

Register Address: 0x06

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00 0100	R/W	Reserved
D[1:0]	IO1_DLY[1:0]	00	R/W	Delay Setting for Both Input Mode/Output Mode of GPIO1 00 = 0ms (default) 01 = 0.25ms 10 = 0.5ms 11 = 1ms

Register Address: 0x07

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	10 0000	R/W	Reserved
D[1:0]	IO2_DLY[1:0]	00	R/W	Delay Setting for Both Input Mode/Output Mode of GPIO2 00 = 0ms (default) 01 = 0.25ms 10 = 0.5ms 11 = 1ms

Register Address: 0x08

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	10 0011	R/W	Reserved
D[1:0]	IO3_DLY[1:0]	00	R/W	Delay Setting for Both Input Mode/Output Mode of GPIO3 00 = 0ms (default) 01 = 0.25ms 10 = 0.5ms 11 = 1ms

MASTER REGISTERS (continued)

Register Address: 0x09

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	10 0000	R/W	Reserved
D[1:0]	IO4_DLY[1:0]	00	R/W	Delay Setting for Both Input Mode/Output Mode of GPIO4 00 = 0ms (default) 01 = 0.25ms 10 = 0.5ms 11 = 1ms

Register Address: 0x0A

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0011 0100	R/W	Reserved

Register Address: 0x0B

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0000	R/W	Reserved

Register Address: 0x0C

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0010 0110	R/W	Reserved

Register Address: 0x0D

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0111	R/W	Reserved

Register Address: 0x0E

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0001	R/W	Reserved

Register Address: 0x0F

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0010 0000	R/W	Reserved

MASTER REGISTERS (continued)

Register Address: 0x10

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0110 0000	R/W	Reserved

Register Address: 0x11

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	1000 0000	R/W	Reserved

Register Address: 0x12

Factory Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CMI NUMBER[7:0]	0000 0011	R	OTP configure version code

Register Address: 0x13

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Manufacture ID[7:0]	0100 0010	R	0x42 for SGM260321-003

Register Address: 0x14

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DEVICE_ID[7:0]	0100 0110	R	0x46 for SGM260321-003

Register Address: 0x15

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0010	R/W	Reserved

BUCK1 REGULATOR REGISTERS

Register Address: 0x30

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_POK	0	R	Real-Time Power Good Status for Buck1 Voltage 0 = V_{OUT_B1} < V_{PG_B1} (default) 1 = V_{OUT_B1} > V_{PG_B1}
D[6]	B1_OV	0	R	0 = V_{OUT_B1} < V_{OV_B1} (default) 1 = V_{OUT_B1} > V_{OV_B1} If V_{OUT_B1} > V_{OV_B1}, this bit goes high. It stays high until V_{OUT_B1} < V_{OV_B1} and the bit is read.
D[5]	B1_ILIM	0	R	0 = I_{PEAK_B1} < I_{LIM_B1} (default) 1 = I_{PEAK_B1} > I_{LIM_B1} If the I_{PEAK_B1} > I_{LIM_B1} threshold, this bit goes high. It stays high until I_{PEAK_B1} < I_{LIM_B1} and the bit is read.
D[4]	B1_ILIM_WARN	0	R	0 = I_{PEAK_B1} < $I_{LIM\_B1\_WARN}$ (default) 1 = I_{PEAK_B1} > $I_{LIM\_B1\_WARN}$ If the I_{PEAK_B1} reaches the 75% of I_{LIM_B1} threshold, this bit goes high. It stays high until I_{PEAK_B1} < 75% of I_{LIM_B1} and the bit is read.
D[3]	B1_UV_FLTMSK	0	R/W	0 = Buck1 UV fault unmasked (default) 1 = Buck1 UV fault masked If set to 1, the Buck1 UV fault is masked and does not trigger the nIRQ signal. And the device does not enter the UV/OV state. If set to 0, the Buck1 UV fault asserts the nIRQ signal. nIRQ is real time UV/OV status. And the device enters the UV/OV state when UV fault occurs.
D[2]	B1_OV_FLTMSK	0	R/W	0 = Buck1 OV fault unmasked (default) 1 = Buck1 OV fault masked If set to 1, the Buck1 OV fault is masked and does not trigger the nIRQ signal. B1_OV still provides OV status. And the device does not enter the UV/OV state. If set to 0, the Buck1 OV fault asserts the nIRQ signal. It stays low until output voltage < V_{OV_B1} falling threshold and the B1_OV bit is read. And the device enters the UV/OV state when OV fault occurs.
D[1]	B1_ILIM_FLTMSK	0	R/W	0 = Buck1 ILIM fault unmasked (default) 1 = Buck1 ILIM fault masked If set to 1, the Buck1 ILIM fault is masked and does not trigger the nIRQ signal. B1_ILIM still provides current limit status. If set to 0, the Buck1 ILIM fault asserts the nIRQ signal. It stays low until I_{PEAK_B1} < I_{LIM_B1} and the B1_ILIM bit is read.
D[0]	B1_ILIM_WARN_ FLTMSK	0	R/W	0 = Buck1 ILIM warning fault unmasked (default) 1 = Buck1 ILIM warning fault masked If set to 1, the Buck1 ILIM warning fault is masked and does not trigger the nIRQ signal. B1_ILIM_WARN still provides current limit warning status. If set to 0, the Buck1 ILIM warning fault asserts the nIRQ signal. It stays low until I_{PEAK_B1} < 75% of I_{LIM_B1} and the B1_ILIM_WARN bit is read.

Register Address: 0x31

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B1_VSET0[7:0]	1000 1000	R/W	In active mode, the Buck1 output voltage setting is determined as follows: When the reference voltage is 800mV, V_{BUCK1} = V_{B1_VSET0} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{BUCK1} = V_{B1_VSET0} × 0.009375V + 0.6V. This setting is not used in bypass mode. It's important to note that the Buck reference voltage setting is not adjustable by the user.

Register Address: 0x32

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B1_VSET1[7:0]	1010 1000	R/W	Set the output voltage of Buck1 for dynamic voltage scaling and sleep mode. When the reference voltage is 800mV, V_{BUCK1} = V_{B1_VSET1} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{BUCK1} = V_{B1_VSET1} × 0.009375V + 0.6V. This setting is not used in Bypass mode. It's important to note that the Buck reference voltage setting is not adjustable by the user.

BUCK1 REGULATOR REGISTERS (continued)

Register Address: 0x33

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_ON	1	R/W	0 = Buck1 disables 1 = Buck1 enables (default)
D[6]	B1_SLEEP_EN	1	R/W	When in Sleep Mode 0 = Buck1 stays on 1 = Buck1 turns off (default)
D[5]	B1_DPSLP_EN	1	R/W	When in DPSLP Mode 0 = Buck1 stays on 1 = Buck1 turns off (default)
D[4:3]	B1_ILIM_SET[1:0]	00	R/W	Buck1 Peak Current Limit 00 = 5.6A (default) 01 = 4.8A 10 = 3.8A 11 = 3.0A
D[2]	B1_RST	0	R/W	Influence of Buck1 on nRESET Output 0 = No affect (default) 1 = Turn off
D[1]	B1_FORCE_CCM	0	R/W	0 = Buck1 enters PSM at light load (default) 1 = Buck1 forced into PWM at light load
D[0]	B1_FSW	1	R/W	Buck1 Switching Frequency 0 = 1.125MHz 1 = 2.25MHz (default)

Register Address: 0x34

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_QLTCH	1	R/W	Behavior of Buck1 when its previous sequenced rail shuts down. 0 = Buck1 shuts down 1 = Buck1 stays on (default)
D[6:5]	B1_ON_DLY[1:0]	00	R/W	00 = No delay (default) 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms Program the delay time between the input trigger of Buck1 and the start of turning on.
D[4:0]	B1_OFF_DLY[4:0]	0 0000	R/W	Buck1 Turn-Off Delay Time t_{D_OFF} = B1_OFF_DLY × 0.25ms Program the delay time between the input trigger for sleep or DPSLP mode being asserted and the start of turning off.

Register Address: 0x35

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B1_PHASE_DLY	0	R/W	0 = Align converter switching with the main clock edge (default) 1 = Delay converter switching by 100ns from the main clock edge
D[6]	B1_PHASE	0	R/W	Options for Converter Switching Alignment with the Main Clock Edge 0 = Alignment with the main clock rising edge (default) 1 = Alignment with the main clock falling edge
D[5:0]	Reserved	00 1001	R/W	Reserved

BUCK2 REGULATOR REGISTERS

Register Address: 0x40

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B2_POK	0	R	Real-Time Power Good Status for Buck2 Voltage 0 = V_{OUT_B2} < V_{PG_B2} (default) 1 = V_{OUT_B2} > V_{PG_B2}
D[6]	B2_OV	0	R	0 = V_{OUT_B2} < V_{OV_B2} (default) 1 = V_{OUT_B2} > V_{OV_B2} If V_{OUT_B2} > V_{OV_B2}, this bit goes high. It stays high until V_{OUT_B2} < V_{OV_B2} and the bit is read.
D[5]	B2_ILIM	0	R	0 = I_{VALLEY_B2} < I_{LIM_B2} (default) 1 = I_{VALLEY_B2} > I_{LIM_B2} If the I_{VALLEY_B2} > I_{LIM_B2} threshold, this bit goes high. It stays high until I_{VALLEY_B2} < I_{LIM_B2} and the bit is read.
D[4]	B2_ILIM_WARN	0	R	0 = I_{VALLEY_B2} < $I_{LIM\_B2\_WARN}$ (default) 1 = I_{VALLEY_B2} > $I_{LIM\_B2\_WARN}$ If the I_{VALLEY_B2} reaches the 75% of I_{LIM_B2} threshold, this bit goes high. It stays high until I_{VALLEY_B2} < 75% of I_{LIM_B2} and the bit is read.
D[3]	B2_UV_FLTMSK	0	R/W	0 = Buck2 UV fault unmasked (default) 1 = Buck2 UV fault masked If set to 1, the Buck2 UV fault is masked and does not trigger the nIRQ signal. And the device does not enter the UV/OV state. If set to 0, the Buck2 UV fault asserts the nIRQ signal. nIRQ is real time UV/OV status. And the device enters the UV/OV state when UV fault occurs.
D[2]	B2_OV_FLTMSK	0	R/W	0 = Buck2 OV fault unmasked (default) 1 = Buck2 OV fault masked If set to 1, the Buck2 OV fault is masked and does not trigger the nIRQ signal. B2_OV still provides OV status. And the device does not enter the UV/OV state. If set to 0, the Buck2 OV fault asserts the nIRQ signal. It stays low until output voltage < V_{OV_B2} falling threshold and the B2_OV bit is read. And the device enters the UV/OV state when OV fault occurs.
D[1]	B2_ILIM_FLTMSK	0	R/W	0 = Buck2 ILIM fault unmasked (default) 1 = Buck2 ILIM fault masked If set to 1, the Buck2 ILIM fault is masked and does not trigger the nIRQ signal. B2_ILIM still provides current limit status. If set to 0, the Buck2 ILIM fault asserts the nIRQ signal. It stays low until I_{VALLEY_B2} < I_{LIM_B2} and the B2_ILIM bit is read.
D[0]	B2_ILIM_WARN_ FLTMSK	0	R/W	0 = Buck2 ILIM warning fault unmasked (default) 1 = Buck2 ILIM warning fault masked If set to 1, the Buck2 ILIM warning fault is masked and does not trigger the nIRQ signal. B2_ILIM_WARN still provides current limit warning status. If set to 0, the Buck2 ILIM warning fault asserts the nIRQ signal. It stays low until I_{VALLEY_B2} < 75% of I_{LIM_B2} and the B2_ILIM_WARN bit is read.

Register Address: 0x41

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B2_VSET0[7:0]	0001 0101	R/W	In active mode, the Buck2 output voltage setting is determined as follows: When the reference voltage is 800mV, V_{BUCK2} = V_{B2_VSET0} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{BUCK2} = V_{B2_VSET0} × 0.009375V + 0.6V. It's important to note that the Buck reference voltage setting is not adjustable by the user.

Register Address: 0x42

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B2_VSET1[7:0]	0000 1011	R/W	Set the output voltage of Buck2 for dynamic voltage scaling and sleep mode. When the reference voltage is 800mV, V_{BUCK2} = V_{B2_VSET1} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{BUCK2} = V_{B2_VSET1} × 0.009375V + 0.6V. It's important to note that the Buck reference voltage setting is not adjustable by the user.

BUCK2 REGULATOR REGISTERS (continued)

Register Address: 0x43

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B2_ON	1	R/W	0 = Buck2 disables 1 = Buck2 enables (default)
D[6]	B2_SLEEP_EN	0	R/W	When in Sleep Mode 0 = Buck2 stays on (default) 1 = Buck2 turns off
D[5]	B2_DPSLP_EN	0	R/W	When in DPSLP Mode 0 = Buck2 stays on (default) 1 = Buck2 turns off
D[4:3]	B2_ILIM_SET[1:0]	00	R/W	Buck2 Valley Current Limit 00 = 4.2A (default) 01 = 3.6A 10 = 3.0A 11 = 2.5A
D[2]	B2_RST	0	R/W	Influence of Buck2 on nRESET Output 0 = No affect (default) 1 = Turn off
D[1]	B2_FORCE_CCM	0	R/W	0 = Buck2 enters PSM at light load (default) 1 = Buck2 forced into PWM at light load
D[0]	B2_FSW	1	R/W	Buck2 Switching Frequency 0 = 1.125MHz 1 = 2.25MHz (default)

Register Address: 0x44

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B2_QLTCH	1	R/W	Behavior of Buck2 when its previous sequenced rail shuts down. 0 = Buck2 shuts down 1 = Buck2 stays on (default)
D[6:5]	B2_ON_DLY[1:0]	00	R/W	00 = No delay (default) 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms Program the delay time between the input trigger of Buck2 and the start of turning on.
D[4:0]	B2_OFF_DLY[4:0]	0 0010	R/W	Buck2 Turn-Off Delay Time t_{D_OFF} = B2_OFF_DLY × 0.25ms Program the delay time between the input trigger for sleep or DPSLP mode being asserted and the start of turning off.

Register Address: 0x45

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B2_PHASE_DLY	0	R/W	0 = Align converter switching with the main clock edge (default) 1 = Delay converter switching by 100ns from the main clock edge
D[6]	B2_PHASE	1	R/W	Options for Converter Switching Alignment with the Main Clock Edge 0 = Alignment with the main clock rising edge 1 = Alignment with the main clock falling edge (default)
D[5:0]	Reserved	01 0000	R/W	Reserved

BUCK3 REGULATOR REGISTERS

Register Address: 0x50

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_POK	0	R	Real-Time Power Good Status for Buck3 Voltage 0 = V_{OUT_B3} < V_{PG_B3} (default) 1 = V_{OUT_B3} > V_{PG_B3}
D[6]	B3_OV	0	R	0 = V_{OUT_B3} < V_{OV_B3} (default) 1 = V_{OUT_B3} > V_{OV_B3} If V_{OUT_B3} > V_{OV_B3}, this bit goes high. It stays high until V_{OUT_B3} < V_{OV_B3} and the bit is read.
D[5]	B3_ILIM	0	R	0 = I_{VALLEY_B3} < I_{LIM_B3} (default) 1 = I_{VALLEY_B3} > I_{LIM_B3} If the I_{VALLEY_B3} > I_{LIM_B3} threshold, this bit goes high. It stays high until I_{VALLEY_B3} < I_{LIM_B3} and the bit is read.
D[4]	B3_ILIM_WARN	0	R	0 = I_{VALLEY_B3} < $I_{LIM\_B3\_WARN}$ (default) 1 = I_{VALLEY_B3} > $I_{LIM\_B3\_WARN}$ If the I_{VALLEY_B3} reaches the 75% of I_{LIM_B3} threshold, this bit goes high. It stays high until I_{VALLEY_B3} < 75% of I_{LIM_B3} and the bit is read.
D[3]	B3_UV_FLTMSK	0	R/W	0 = Buck3 UV fault unmasked (default) 1 = Buck3 UV fault masked If set to 1, the Buck3 UV fault is masked and does not trigger the nIRQ signal. And the device does not enter the UV/OV state. If set to 0, the Buck3 UV fault asserts the nIRQ signal. nIRQ is real time UV/OV status. And the device enters the UV/OV state when UV fault occurs.
D[2]	B3_OV_FLTMSK	0	R/W	0 = Buck3 OV fault unmasked (default) 1 = Buck3 OV fault masked If set to 1, the Buck3 OV fault is masked and does not trigger the nIRQ signal. B3_OV still provides OV status. And the device does not enter the UV/OV state. If set to 0, the Buck3 OV fault asserts the nIRQ signal. It stays low until output voltage < V_{OV_B3} falling threshold and the B3_OV bit is read. And the device enters the UV/OV state when OV fault occurs.
D[1]	B3_ILIM_FLTMSK	0	R/W	0 = Buck3 ILIM fault unmasked (default) 1 = Buck3 ILIM fault masked If set to 1, the Buck3 ILIM fault is masked and does not trigger the nIRQ signal. B3_ILIM still provides current limit status. If set to 0, the Buck3 ILIM fault asserts the nIRQ signal. It stays low until I_{VALLEY_B3} < I_{LIM_B3} and the B3_ILIM bit is read.
D[0]	B3_ILIM_WARN_ FLTMSK	0	R/W	0 = Buck3 ILIM warning fault unmasked (default) 1 = Buck3 ILIM warning fault masked If set to 1, the Buck3 ILIM warning fault is masked and does not trigger the nIRQ signal. B3_ILIM_WARN still provides current limit warning status. If set to 0, the Buck3 ILIM warning fault asserts the nIRQ signal. It stays low until I_{VALLEY_B3} < 75% of I_{LIM_B3} and the B3_ILIM_WARN bit is read.

Register Address: 0x51

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B3_VSET0[7:0]	0101 0000	R/W	In active mode, the Buck3 output voltage setting is determined as follows: V_{BUCK3} = V_{B3_VSET0} × 0.0125V + 0.8V.

Register Address: 0x52

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	B3_VSET1[7:0]	0010 0000	R/W	Setting the output voltage of Buck3 for dynamic voltage scaling and sleep mode. V_{BUCK3} = V_{B3_VSET1} × 0.0125V + 0.8V.

BUCK3 REGULATOR REGISTERS (continued)

Register Address: 0x53

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_ON	1	R/W	0 = Buck3 disables 1 = Buck3 enables (default)
D[6]	B3_SLEEP_EN	1	R/W	When in Sleep Mode 0 = Buck3 stays on 1 = Buck3 turns off (default)
D[5]	B3_DPSLP_EN	1	R/W	When in DPSLP Mode 0 = Buck3 stays on 1 = Buck3 turns off (default)
D[4:3]	B3_ILIM_SET[1:0]	01	R/W	Buck3 Valley Current Limit 00 = 4.0A 01 = 3.4A (default) 10 = 2.8A 11 = 2.3A
D[2]	B3_RST	0	R/W	Influence of Buck3 on nRESET Output 0 = No affect (default) 1 = Turn off
D[1]	B3_FORCE_CCM	0	R/W	0 = Buck3 enters PSM at light load (default) 1 = Buck3 forced into PWM at light load
D[0]	B3_FSW	1	R/W	Buck3 Switching Frequency 0 = 1.125MHz 1 = 2.25MHz (default)

Register Address: 0x54

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_QLTCH	1	R/W	Behavior of Buck3 when its previous sequenced rail shuts down. 0 = Buck3 shuts down 1 = Buck3 stays on (default)
D[6:5]	B3_ON_DLY[1:0]	01	R/W	00 = No delay 01 = 0.25ms (default) 10 = 0.5ms 11 = 1.0ms Program the delay time between the input trigger of Buck3 and the start of turning on.
D[4:0]	B3_OFF_DLY[4:0]	0 0000	R/W	Buck3 Turn-Off Delay Time t_{D_OFF} = B3_OFF_DLY × 0.25ms Program the delay time between the input trigger for sleep or DPSLP mode being asserted and the start of turning off.

Register Address: 0x55

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	B3_PHASE_DLY	0	R/W	0 = Align converter switching with the main clock edge (default) 1 = Delay converter switching by 100ns from the main clock edge
D[6]	B3_PHASE	1	R/W	Options for Converter Switching Alignment with the Main Clock Edge 0 = Alignment with the main clock rising edge 1 = Alignment with the main clock falling edge (default)
D[5:0]	Reserved	00 0100	R/W	Reserved

LDO1 REGISTERS

Register Address: 0x60

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO1_POK	0	R	Real-Time Power Good Status for LDO1 Voltage 0 = V_{OUT_LDO1} < V_{PG_LDO1} (default) 1 = V_{OUT_LDO1} > V_{PG_LDO1}
D[6]	LDO1_OV	0	R	0 = V_{OUT_LDO1} < V_{OV_LDO1} (default) 1 = V_{OUT_LDO1} > V_{OV_LDO1} If the V_{OUT_LDO1} > V_{OV_LDO1}, this bit goes high. It stays high until V_{OUT_LDO1} < V_{OV_LDO1} and the bit is read.
D[5]	ILIM_LDO1	0	R	0 = I_{OUT_LDO1} < I_{LIM_LDO1} (default) 1 = I_{OUT_LDO1} > I_{LIM_LDO1} If I_{OUT_LDO1} > I_{LIM_LDO1}, this bit goes high. It stays high until I_{OUT_LDO1} < I_{LIM_LDO1} and the bit is read.
D[4]	Reserved	0	R	Reserved
D[3]	LDO1_UV_FLTMSK	0	R/W	0 = LDO1 UV fault unmasked (default) 1 = LDO1 UV fault masked If set to 1, the LDO1 UV fault is masked and does not trigger the nIRQ signal. And the device does not enter UV/OV state. If set to 0, the LDO1 UV fault asserts the nIRQ signal. nIRQ is real time UV/OV status. And the device enters UV/OV state when UV fault occurs.
D[2]	LDO1_OV_FLTMSK	0	R/W	0 = LDO1 OV fault unmasked (default) 1 = LDO1 OV fault masked If set to 1, the LDO1 OV fault is masked and does not trigger the nIRQ signal. LDO1_OV still provides OV status. And the device does not enter UV/OV state. If set to 0, the LDO1 OV fault asserts the nIRQ signal. It stays low until output voltage < $V_{OV\_LDO1\_}$ falling threshold and the LDO1_OV bit is read. And the device enters UV/OV state when OV fault occurs.
D[1]	LDO1_ILIM_FLTMSK	0	R/W	0 = LDO1 ILIM fault unmasked (default) 1 = LDO1 ILIM fault masked If set to 1, the LDO1 ILIM fault is masked and does not trigger the nIRQ signal. LDO1_ILIM still provides current limit status. If set to 0, the LDO1 ILIM fault asserts the nIRQ signal. It stays low until I_{OUT_LDO1} < I_{LIM_LDO1} and the LDO1_ILIM bit is read.
D[0]	Reserved	0	R/W	Reserved

Register Address: 0x61

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO1_VSET[7:0]	0101 0000	R/W	LDO1 output voltage setting. When the reference voltage is 800mV, V_{LDO1} = V_{LDO1_VSET} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{LDO1} = V_{LDO1_VSET} × 0.009375V + 0.6V. This setting is not used in bypass mode. It's important to note that the LDO reference voltage setting is not adjustable by the user.

LDO1 REGISTERS (continued)

Register Address: 0x62

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO1_ON	1	R/W	0 = LDO1 disables 1 = LDO1 enables (default)
D[6]	LDO1_SLEEP_EN	0	R/W	When in Sleep Mode 0 = LDO1 stays on (default) 1 = LDO1 turns off
D[5]	LDO1_DPSLP_EN	0	R/W	When in DPSLP Mode 0 = LDO1 stays on (default) 1 = LDO1 turns off
D[4:3]	LDO1_ILIM_SET[1:0]	11	R/W	00 = 0.155A 01 = 0.245A 10 = 0.365A 11 = 0.46A (default)
D[2]	LDO1_RST	0	R/W	Influence of LDO1 on nRESET Output 0 = No affect (default) 1 = Turn off
D[1]	LDO1_ILIM_SHDN	0	R/W	0 = LDO1 does not shut down after current limit is reached (default) 1 = LDO1 shuts down after current limit is reached LDO will shut down and restart after 10ms when this bit = 1.
D[0]	Reserved	0	R/W	Reserved

Register Address: 0x63

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO1_QLTCH	1	R/W	Behavior of LDO1 when its previous sequenced rail shuts down. 0 = LDO1 shuts down 1 = LDO1 stays on (default)
D[6:5]	LDO1_ON_DLY[1:0]	00	R/W	00 = No delay (default) 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms Program the delay time between the input trigger of LDO1 and the start of turning on.
D[4:0]	LDO1_OFF_DLY[4:0]	0 0010	R/W	LDO1 Turn-Off Delay Time t_{D_OFF} = LDO1_OFF_DLY × 0.25ms Program the delay time between the input trigger for sleep or DPSLP mode being asserted and the start of turning off.

Register Address: 0x64

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0000	R/W	Reserved

LDO2 REGISTERS

Register Address: 0x65

Basic Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO2_POK	0	R	Real-Time Power Good Status for LDO2 Voltage 0 = V_{OUT_LDO2} < V_{PG_LDO2} (default) 1 = V_{OUT_LDO2} > V_{PG_LDO2}
D[6]	LDO2_OV	0	R	0 = V_{OUT_LDO2} < V_{OV_LDO2} (default) 1 = V_{OUT_LDO2} > V_{OV_LDO2} If V_{OUT_LDO2} > V_{OV_LDO2}, this bit goes high. It stays high until V_{OUT_LDO2} < V_{OV_LDO2} and the bit is read.
D[5]	ILIM_LDO2	0	R	0 = I_{OUT_LDO2} < I_{LIM_LDO2} (default) 1 = I_{OUT_LDO2} > I_{LIM_LDO2} If I_{OUT_LDO2} > I_{LIM_LDO2}, this bit goes high. It stays high until I_{OUT_LDO2} < I_{LIM_LDO2} and this bit is read.
D[4]	Reserved	0	R	Reserved
D[3]	LDO2_UV_FLTMSK	0	R/W	0 = LDO2 UV fault unmasked (default) 1 = LDO2 UV fault masked If set to 1, the LDO2 UV fault is masked and does not trigger the nIRQ signal. And the device does not enter UV/OV state. If set to 0, the LDO2 UV fault asserts the nIRQ signal. nIRQ is real time UV/OV status. And the device enters UV/OV state when UV fault occurs.
D[2]	LDO2_OV_FLTMSK	0	R/W	0 = LDO2 OV fault unmasked (default) 1 = LDO2 OV fault masked If set to 1, the LDO2 OV fault is masked and does not trigger the nIRQ signal. LDO2_OV still provides OV status. And the device does not enter UV/OV state. If set to 0, the LDO2 OV fault asserts the nIRQ signal. It stays low until output voltage < V_{OV_LDO2} falling threshold and the LDO2_OV bit is read. And the device enters UV/OV state when OV fault occurs.
D[1]	LDO2_ILIM_FLTMSK	0	R/W	0 = LDO2 ILIM fault unmasked (default) 1 = LDO2 ILIM fault masked If set to 1, the LDO2 ILIM fault is masked and does not trigger the nIRQ signal. LDO2_ILIM still provides current limit status. If set to 0, the LDO2 ILIM fault asserts the nIRQ signal. It stays low until I_{OUT_LDO2} < I_{LIM_LDO2} and the LDO2_ILIM bit is read.
D[0]	Reserved	0	R/W	Reserved

Register Address: 0x66

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	LDO2_VSET[7:0]	0101 0000	R/W	LDO2 output voltage setting. When the reference voltage is 800mV, V_{LDO2} = V_{LDO2_VSET} × 0.0125V + 0.8V. When the reference voltage is 600mV, V_{LDO2} = V_{LDO2_VSET} × 0.009375V + 0.6V. This setting is not used in bypass mode. It's important to note that the LDO reference voltage setting is not adjustable by the user.

LDO2 REGISTERS (continued)

Register Address: 0x67

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO2_ON	1	R/W	0 = LDO2 disables 1 = LDO2 enables (default)
D[6]	LDO2_SLEEP_EN	0	R/W	When in Sleep Mode 0 = LDO2 stays on (default) 1 = LDO2 turns off
D[5]	LDO2_DPSLP_EN	0	R/W	When in DPSLP Mode 0 = LDO2 stays on (default) 1 = LDO2 turns off
D[4:3]	LDO2_ILIM_SET[1:0]	10	R/W	00 = 0.155A 01 = 0.245A 10 = 0.365A (default) 11 = 0.46A
D[2]	LDO2_RST	0	R/W	Influence of LDO2 on nRESET Output 0 = No affect (default) 1 = Turn off
D[1]	LDO2_ILIM_SHDN	0	R/W	0 = LDO2 does not shut down after current limit is reached (default) 1 = LDO2 shuts down after current limit is reached LDO will shut down and restart after 10ms when this bit = 1.
D[0]	Reserved	0	R/W	Reserved

Register Address: 0x68

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	LDO2_QLTCH	1	R/W	Behavior of LDO2 when its previous sequenced rail shuts down. 0 = LDO2 shuts down 1 = LDO2 stays on (default)
D[6:5]	LDO2_ON_DLY[1:0]	00	R/W	00 = No delay (default) 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms Program the delay time between the input trigger of LDO2 and the start of turning on.
D[4:0]	LDO2_OFF_DLY[4:0]	0 0010	R/W	LDO2 Turn-Off Delay Time t_{D_OFF} = LDO2_OFF_DLY × 0.25ms Program the delay time between the input trigger for sleep or DPSLP mode being asserted and the start of turning off.

Register Address: 0x69

Basic Non-Volatile

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	Reserved	0000 0000	R/W	Reserved

APPLICATION INFORMATION

Layout Guide

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. The following guidelines provided here are necessary to design a good layout:

1. Bypass VIN_Bx pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN_Bx pin on the top layer eliminates the need for vias. Refer to the pin descriptions for the specific VIN_Bx and PGNDx pins of each buck converter.

2. Keep the switch node trace between each SW_Bx pin and the inductor as short as possible. For optimal routing, run this trace between the pads of the input capacitor. Using 0805-sized input capacitors is recommended. Avoid placing sensitive analog signal traces near these high-frequency, high dV/dt nodes to minimize noise interference.

3. Position the LDO input capacitor near the VIN_A pin, ensuring a direct connection to VIN_A and AGND on the top layer for optimal performance.

4. Place the Buck output capacitors close to the inductor, ensuring direct connections with short, wide traces to both the inductor and ground plane. The output capacitor ground should be tightly linked to the input capacitor ground. Use multiple vias if necessary to maintain low impedance.

5. Each regulator's FB_Bx pin should be Kelvin connected to its output capacitor using the shortest possible trace while maintaining adequate distance from switching nodes to minimize noise injection. The IC regulates the output voltage based on this Kelvin connection.

6. The PGNDx and AGND pins must be electrically connected. Since the AGND plane serves as the ground for analog, digital, and LDO circuits, full isolation from other PCB grounds is not required. However, ensure that Buck converter switching currents do not flow through the analog ground connections to prevent interference. Connect the AGND and PGND pins to the ground planes using vias placed next to the bypass capacitors for optimal grounding.

7. Ensure that all open-drain outputs have appropriate pull-up resistors.

8. Figure 14 illustrates the recommended power and signal connections, as well as the routing beneath the IC. For a detailed routing example, refer to the SGM260321 evaluation kit.

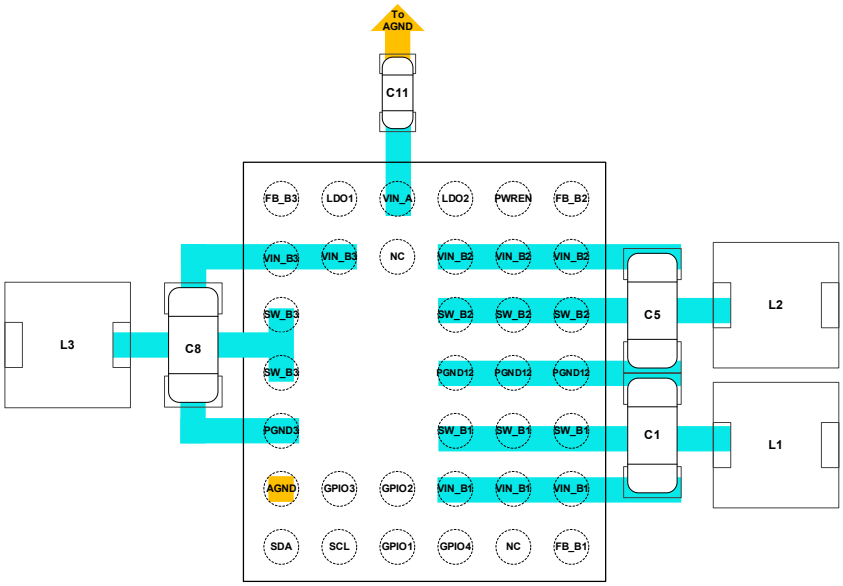


Figure 14. Recommended Layout

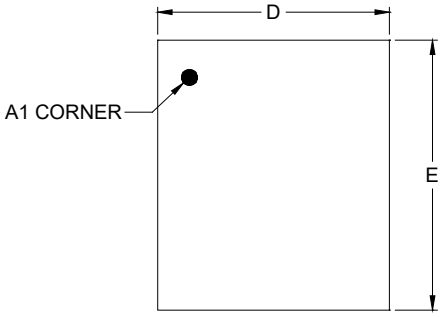
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

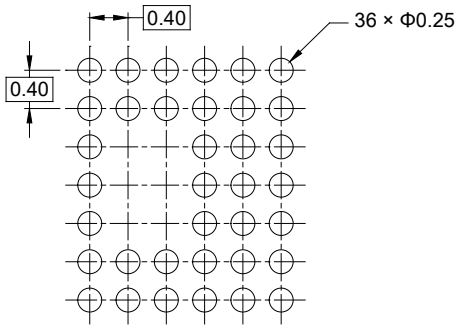
Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

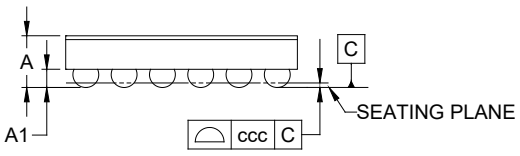
WLCSP-2.42×2.82-36B



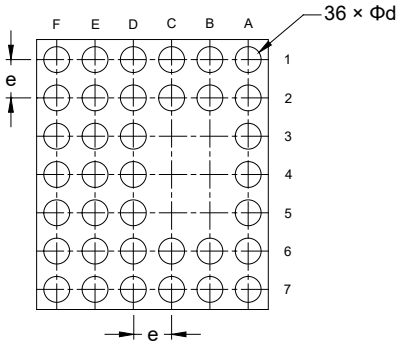
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



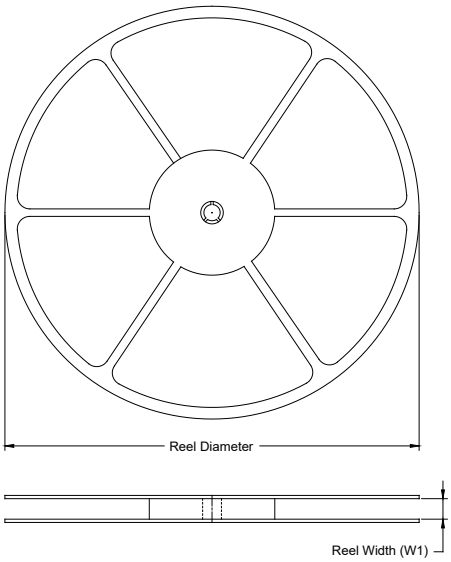
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.590
A1	0.170	-	0.210
D	2.390	-	2.450
E	2.790	-	2.850
d	0.240	-	0.300
e	0.400 BSC		
ccc	0.050		

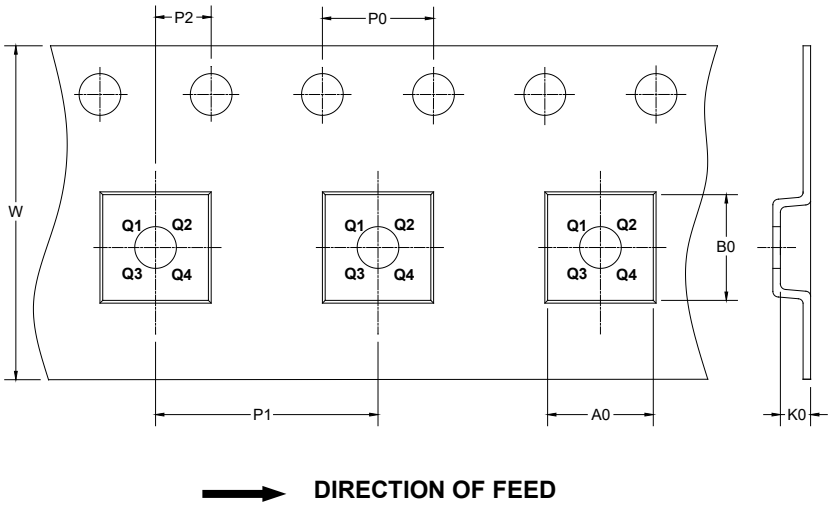
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



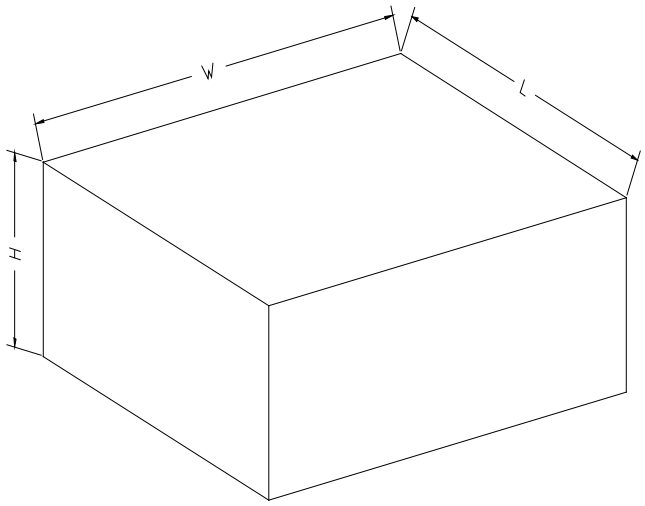
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.42×2.82-36B	13"	12.4	2.59	2.99	0.80	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002