

GENERAL DESCRIPTION

The GRM2030 is a highly integrated power delivery sub-system SoC device of voltage Buck DC/DC power conversion. It integrates power inductor, power switches and voltage regulation circuit in a proprietary 3D structure. The compact and low profile device is in a LGA package of 2.8mm × 3.0mm × 1.1mm, allowing the system to achieve high density.

The device has up to 2.0MHz synchronous switching step-down converter. This high frequency device is a perfect solution for compact designs. For the GRM2030, the device operates in continuous current mode (CCM) at light and heavy loads.

The GRM2030 device has a unique 3D structure that lowers the thermal impedance from the top to the bottom below general lead-framed LGA packages. The device structure has significantly enhanced thermal conductivity. Other key features include under-voltage lockout (UVLO), integrated soft-start to limit inrush current at startup, over current protection and thermal shutdown detection.

The GRM2030 is available in a Green LGA-2.8×3-8L package.

FEATURES

- 3D Integrated SoC Device with Power IC, Power Inductor
- Switching Frequency: 2.0MHz
- 2.5V to 5.5V Input Voltage Range
- Adjustable Output Voltage from 0.6V to V_{IN}
- Adaptive Off-Time Architecture
- Fast Load Transient Response
- Continuous Current Mode (CCM)
- Enable Input, Soft-Start and Input Under-Voltage Lockout
- 100% Duty Cycle Capability for Low Dropout
- Startup with Pre-biased Output
- Output Discharge Function
- Power Good Output
- Hiccup Mode Short-Circuit Protection and Thermal Shutdown
- Super Ease-of-Use in System Designs
- Available in a Green LGA-2.8×3-8L Package

APPLICATIONS

Optical Modules
 Battery-Powered Applications
 Point-of-Load
 Processor Power Supplies
 Hard Disk Drives (HDD)/Solid State Drives (SSD)

SIMPLIFIED SCHEMATIC

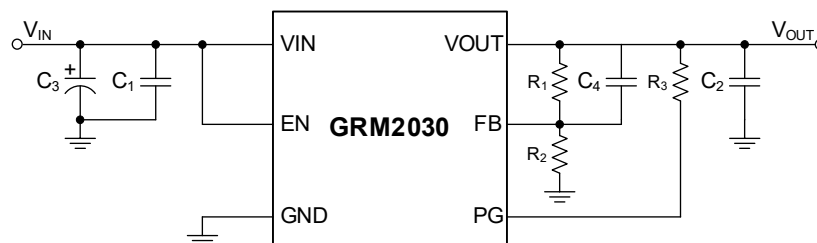


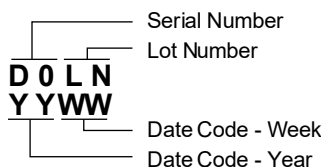
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
GRM2030	LGA-2.8×3-8L	-40°C to +125°C	GRM2030-LGA-R	D0LN YYWW	Tape and Reel, 3000

MARKING INFORMATION

NOTE: YYWW = Date Code



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, FB, EN, PG Voltages	-0.3V to 6.0V
VOU (DC) Voltage	-0.3V to VIN + 0.3V
Package Thermal Resistance	
LGA-2.8×3-8L, θ_{JA}	53.6°C/W
LGA-2.8×3-8L, θ_{JB}	11.6°C/W
LGA-2.8×3-8L, θ_{JC} (TOP)	33.6°C/W
LGA-2.8×3-8L, θ_{JC} (BOT)	14.1°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM	±4000V
CDM	±1000V

NOTES:

- For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
- For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	2.5V to 5.5V
Output Current	0A to 3.0A
Output Voltage Range, VOUT	0.6V to VIN
PG Pin Sink Current, ISINK_PG	1mA
Maximum Pull-Up Voltage for PG, VPG	5.5V
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

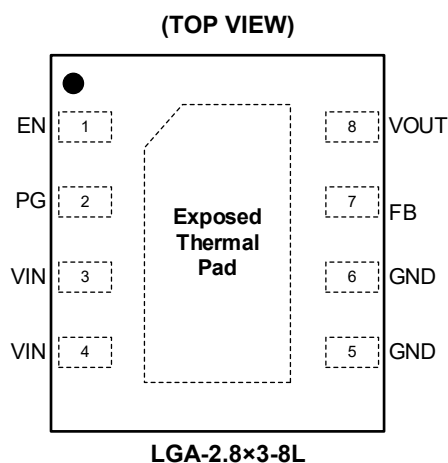
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

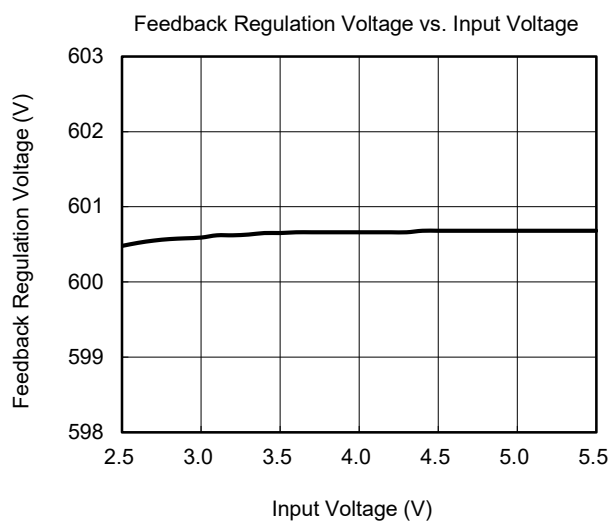
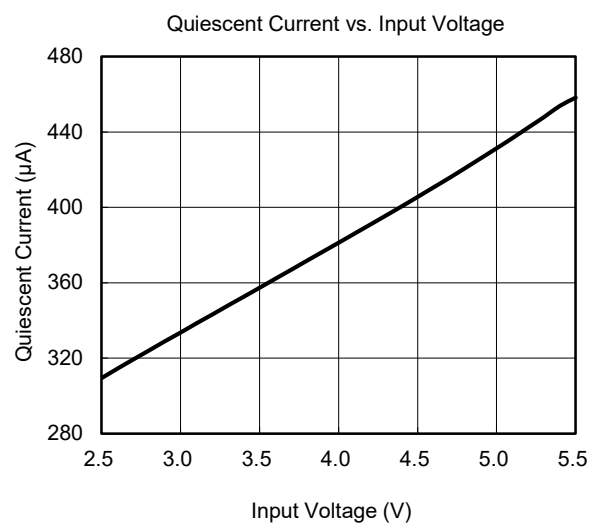
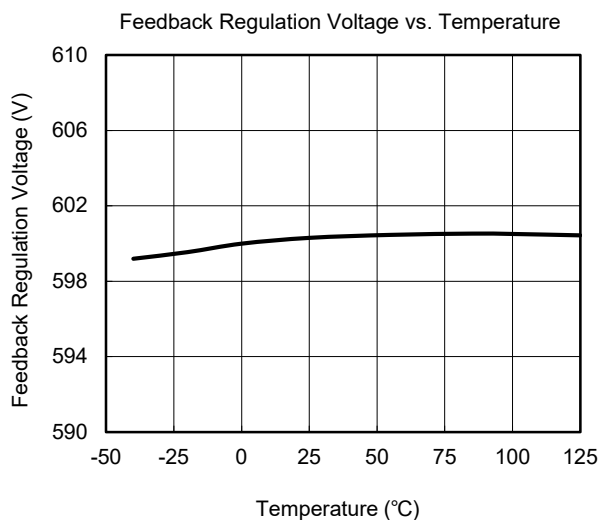
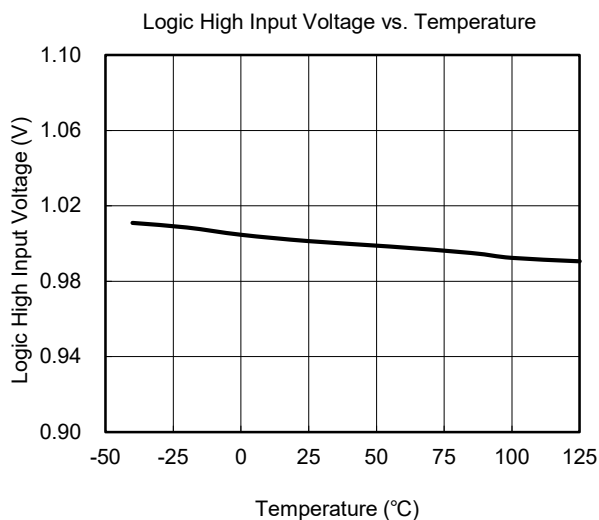
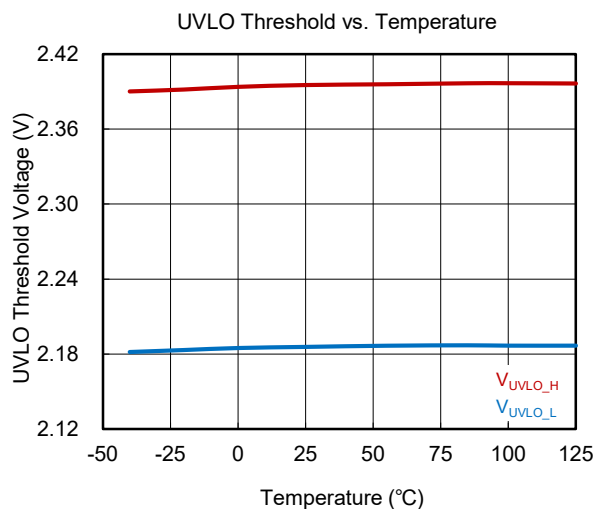
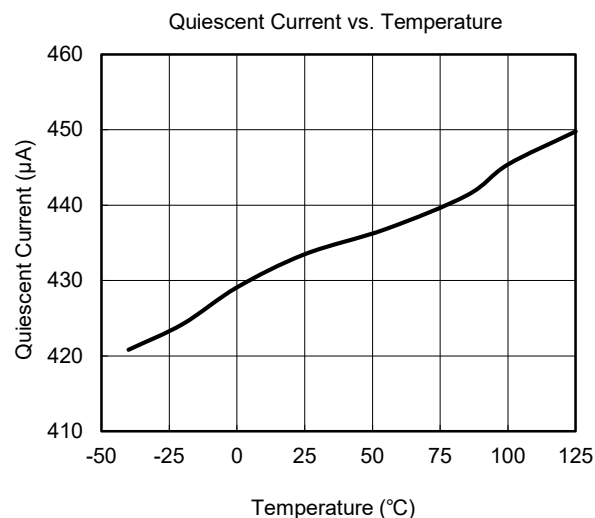
PIN	NAME	TYPE	FUNCTION
1	EN	I	Active-High Device Enable Input Pin. Pull this pin to logic high to enable the device and pull it low to disable it. An internal 540kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.
2	PG	O	Open-Drain Power Good Output Pin. This output is released to go high if the device is in power good status. Pull up this pin to a 5.5V or less voltage rail. It can be left open if not used.
3, 4	VIN	P	Input Voltage Pin.
5, 6	GND	G	Ground Pin.
7	FB	I	Feedback Pin. Connect a resistor divider between the output voltage sense point and ground and tap it to the FB pin to set the output voltage.
8	VOUT	O	Output Voltage Pin.
Exposed Pad	Exposed Thermal Pad	—	The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

NOTE: I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS(V_{IN} = 5.0V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.)

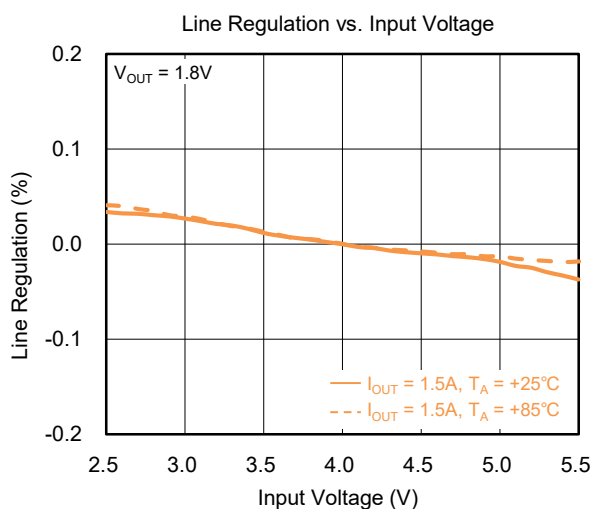
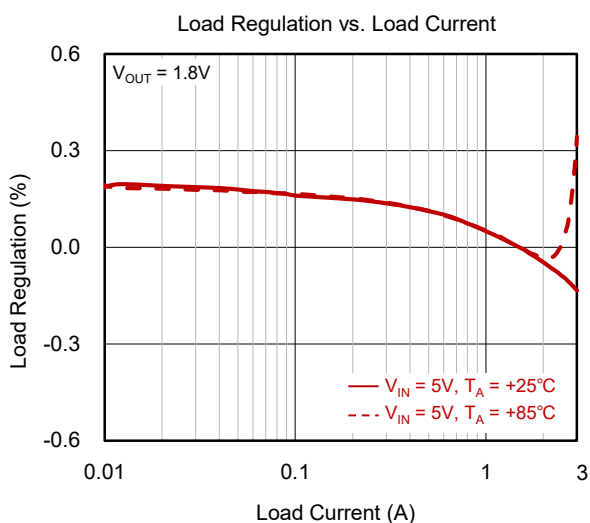
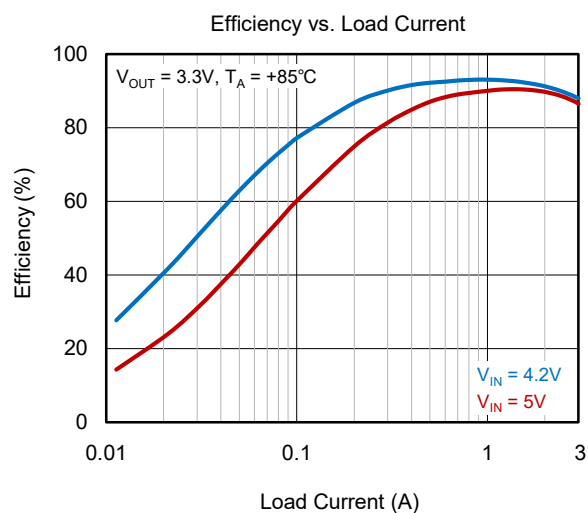
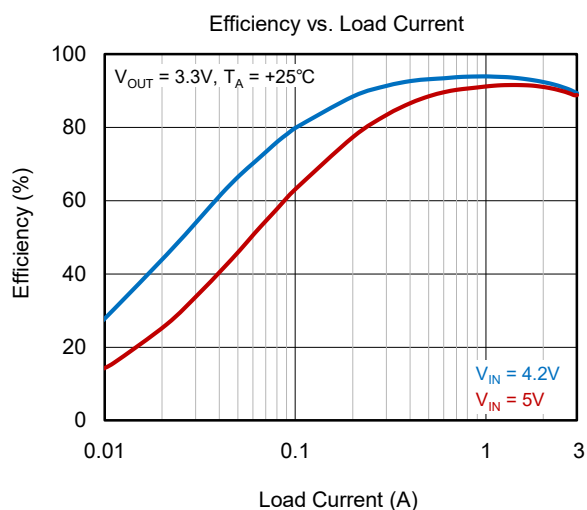
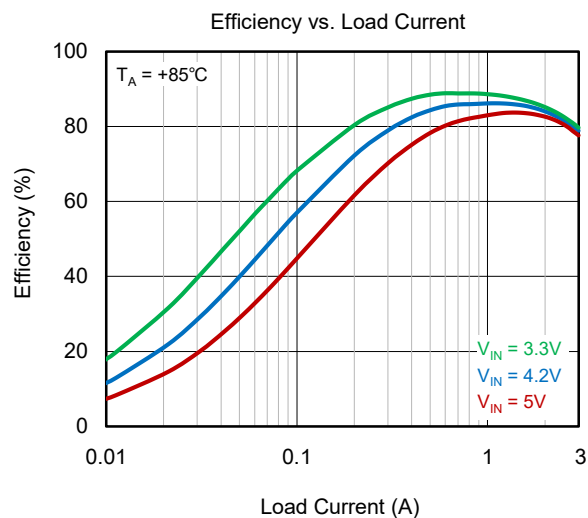
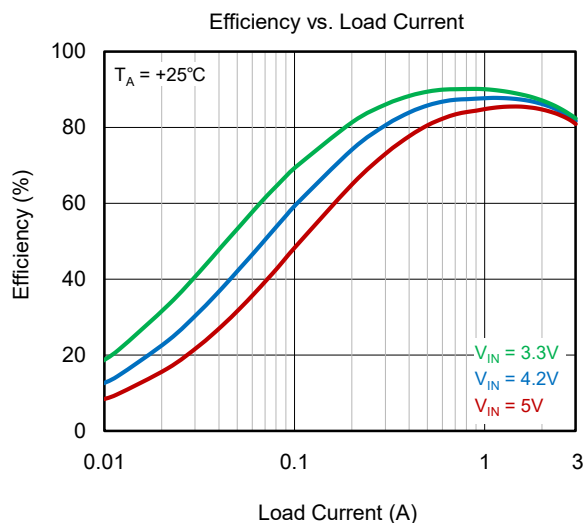
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Input Voltage	V _{IN}			2.5		5.5	V
Device Activated Voltage	V _{UVLO}	VIN falling		2.1	2.2	2.3	V
	V _{UVLO_HYS}	VIN rising			210		mV
Device Input Current	I _Q	V _{IN} = 5.0V, no load, no switching			0.43	0.60	mA
Shutdown Current	I _{SD}	V _{IN} = 5.0V, no load, EN = GND			0.12	1.5	μA
Integrated Power Switches, Inductor							
Inductance of the Integrated Inductor	L	At 500KHz			360		nH
Total PWM-On Resistance	R _{PWM_ON}	PWM on, resistance from VIN to VOUT, T _J = +25°C			80	95	mΩ
Total PWM-Off Resistance	R _{PWM_OFF}	PWM off, resistance from VOUT to GND, T _J = +25°C			64	80	
PMOS On-Switch Current Limit	I _{SW}			4.5	5.8	7.1	A
Switching Frequency	f _{SW}	V _{IN} = 5.0V			2.0		MHz
Output Characteristics and Feedback							
Feedback Regulation Voltage	V _{FB}	V _{IN} = 2.5V to 5.5V,	T _J = +25°C	596	600	604	mV
			T _J = -40°C to +125°C	592		608	
Feedback Input Leakage Current	I _{FB_LKG}	V _{FB} = 1V			10	100	nA
Load Current Limit	I _{LIM_LOAD}	V _{IN} = 5.0V, V _{OUT} = 1.8V, resistive load		3			A
Output Discharge Resistance	R _{DIS}	EN = low, V _{OUT} = 1.8V			43		Ω
Performance							
Efficiency	η	V _{IN} = 5.0V, V _{OUT} = 1.8V	I _{LOAD} = 1.0A		85.1		%
			I _{LOAD} = 2.0A		85.2		
			I _{LOAD} = 3.0A		81.3		
Logic Inputs: EN							
Logic High Voltage	V _{IH}			1.2			V
Logic Low Voltage	V _{IL}					0.4	V
Input Leakage Current	I _{EN}	V _{IN} = 5.5V, V _{EN} = 5.5V			0.01	1	μA
Pull-Down Resistance	R _{PD}	EN = low			540		kΩ
Thermal Shutdown Protection							
Thermal Shutdown	T _{SD}				160		°C
Thermal Shutdown Hysteresis	T _{HYS}				25		°C
Soft-Start, Power Good							
Soft-Start Time	t _{SS}	V _{IN} = 5.0V, V _{EN} = 3.6V, EN high to 95% V _{OUT} nominal			880		μs
Power Good Threshold	V _{PG}	V _{OUT} rising, as percentage of the nominal V _{OUT}			95%		V _{OUT} (set)
		V _{OUT} failing, as percentage of the nominal V _{OUT}			90%		
PG Low State Output Voltage	V _{PG_OL}	I _{SNK} = 1mA, T _J = -40°C to +125°C			0.14	0.3	V
PG Leakage Current (into PG Pin)	I _{PG_LKG}	V _{PG} = 5V, T _J = -40°C to +125°C			0.01	0.5	μA

TYPICAL PERFORMANCE CHARACTERISTICS



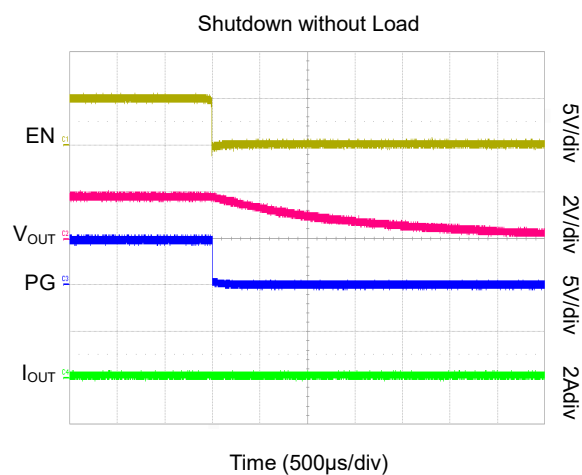
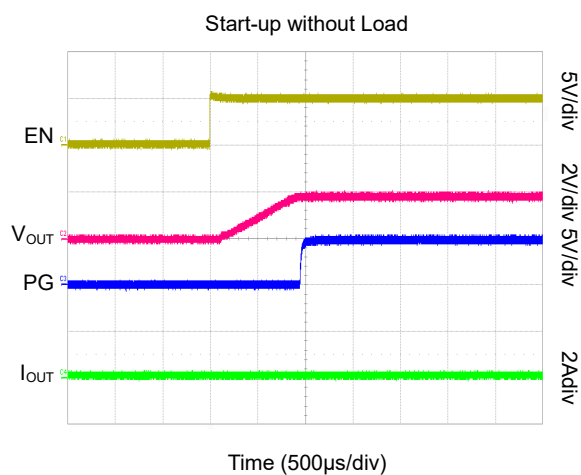
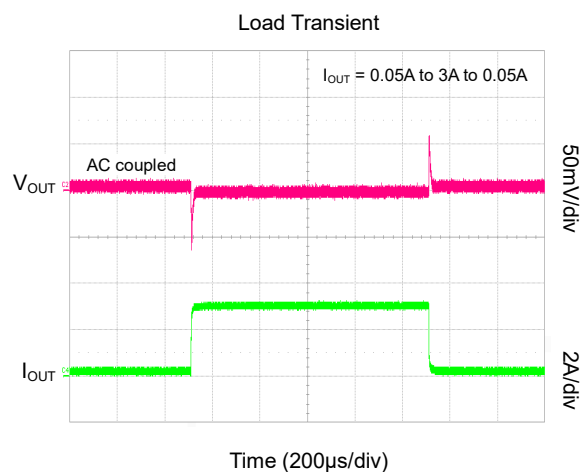
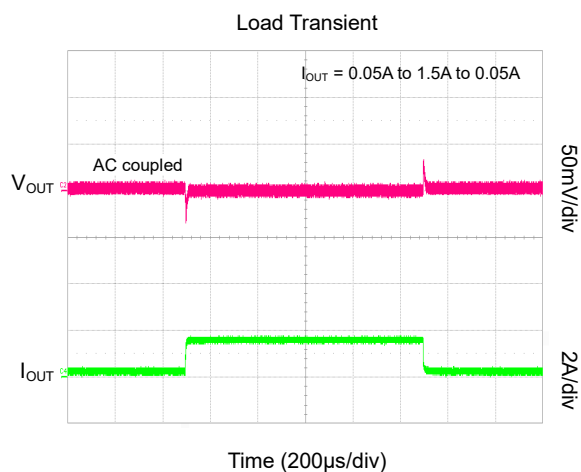
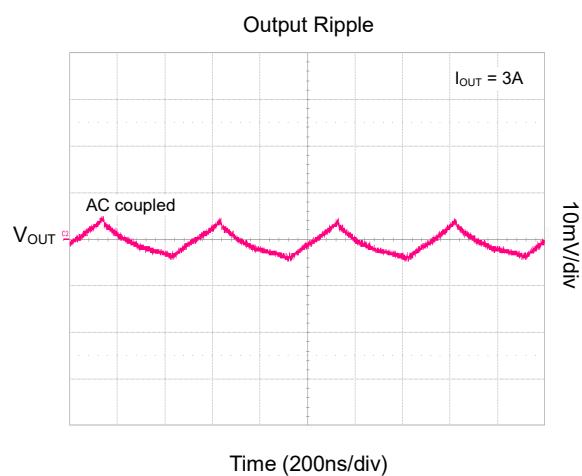
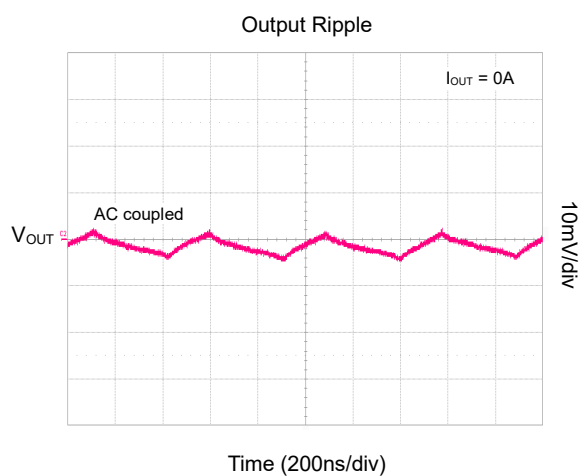
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$, $V_{OUT} = 1.8V$, and $C_{OUT} = 47\mu F$, unless otherwise noted.

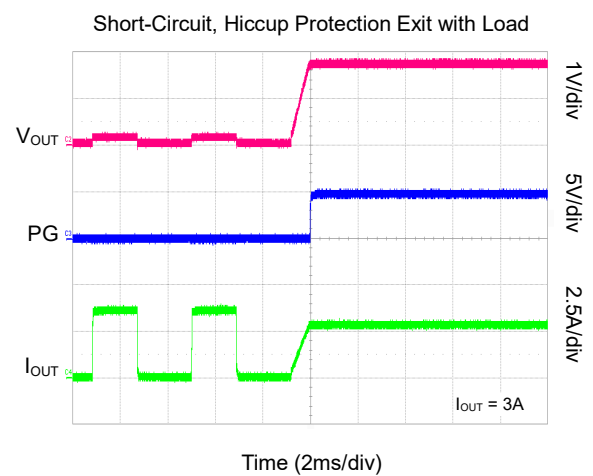
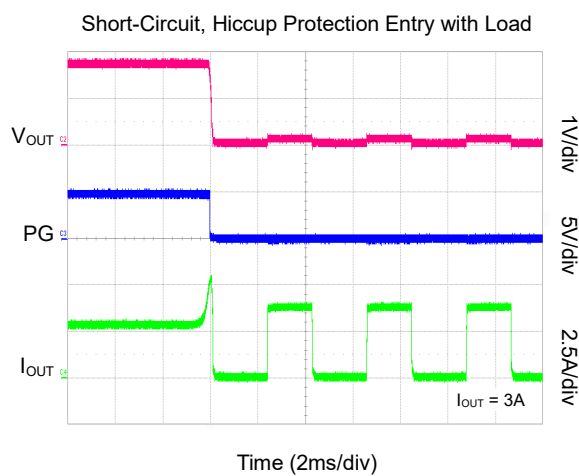
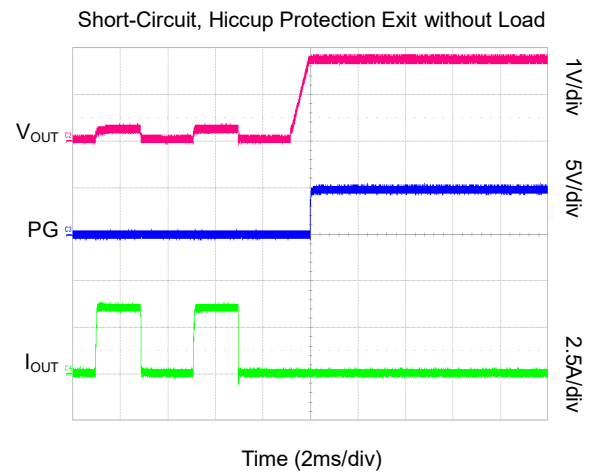
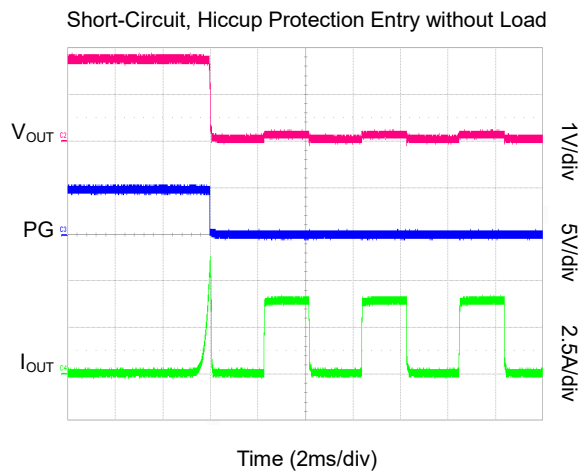
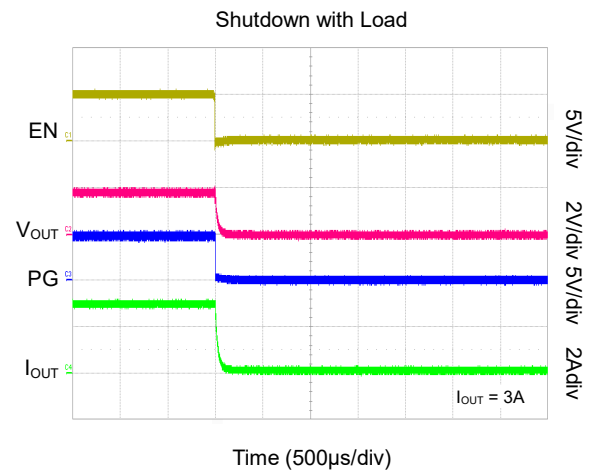
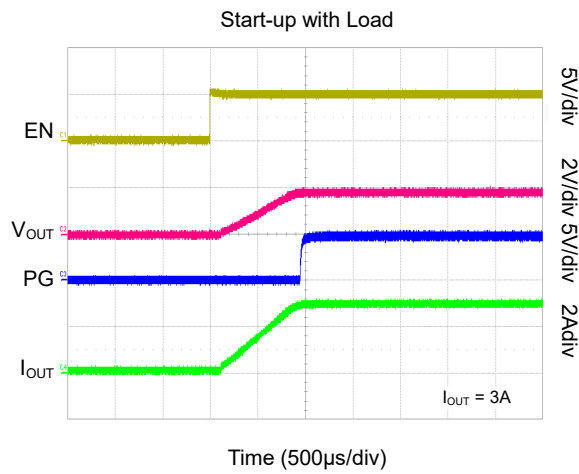


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$, $V_{OUT} = 1.8V$, $C_{OUT} = 47\mu F$, and $T_A = +25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



FUNCTIONAL BLOCK DIAGRAM

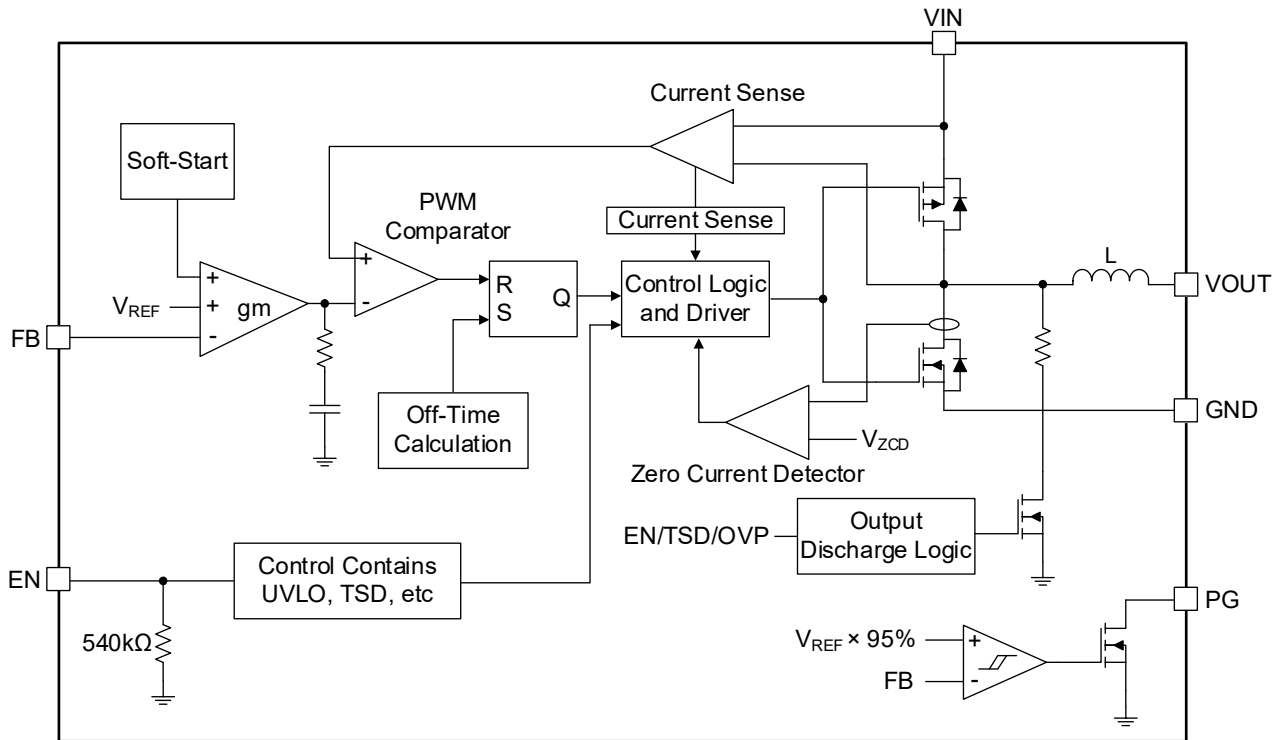


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The GRM2030 is synchronous DC/DC PowerSoC available with switching frequency up to 2.0MHz. Operating from an input voltage between 2.5V and 5.5V, the PowerSoC can deliver up to 3A of load current at an adjustable output voltage.

Under-Voltage Lockout (UVLO)

Operating with insufficient supply voltage can cause device malfunction or failure. The UVLO protection shuts down the device if the input voltage is below the V_{UVLO} threshold. The UVLO comparator has a 210mV hysteresis band.

Device Enable and Disable

When the input voltage is valid, pulling the EN input to logic high will enable the device, and pulling it to logic low will shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.12 μ A (TYP). A 540k Ω pull-down resistor is internally placed between EN and GND pins when the device is disabled.

During shutdown, an internal 43 Ω resistor is connected between VOUT and GND pins and softly discharges the output capacitors. This discharge function is also activated when the shutdown is caused by a thermal shutdown, UVLO, or short-circuit protection.

Power Good Output (PG)

The PG pin is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. PG remains low until V_{OUT} exceeds 95% of its nominal (set) value and goes low if V_{OUT} drops below 90% of its nominal value. Table 1 shows how the PG state is changed in different conditions. V_{PG} is the threshold of the PG hysteretic comparator. It has a 5% hysteresis band and goes high when V_{FB} rises above 95% of the V_{REF} .

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is

connected to the EN input of the subsequent power supply to implement such sequencing.

Table 1. PG Output State in Different Conditions

Reason	Condition(s)	PG State	
		High-Z	Low
Output Voltage	EN = High, $V_{FB} \geq V_{PG}$	✓	
	EN = High, $V_{FB} \leq V_{PG}$		✓
Shutdown by EN	EN = Low		✓
Thermal Shutdown	$T_J > T_{JSD}$		✓
UVLO	$0.6V < V_{IN} < V_{UVLO}$		✓
Power Supply Removal	$V_{IN} \leq 0.6V$	✓	

Soft-Start and Pre-biased Output

An 880 μ s internal soft-start circuit is designed to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage ($V_{REF} = 0.6V$) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The GRM2030 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to start up properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

Continuous Conduction Mode

In continuous conduction mode (CCM), the frequency is fixed and the output voltage ripple will be minimal. The maximum output current of 3A is supplied in CCM.

DETAILED DESCRIPTION (continued)**Low Dropout Operation (100% Duty Cycle)**

When the input voltage reduces, the on-time increases. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the GRM2030 goes into 100% duty cycle mode. The high-side switch is always turned on, and the output voltage is determined by the load current times the $R_{DS(on)}$ composed by the high-side switch and inductor.

**Current Limit and Hiccup Mode
Short-Circuit Protection**

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch will be turned on to reduce the inductor current and limit the peak.

If 2ms consecutive repetition of this event occurs, the controller will stop switching and turns the output discharge circuit on. Then a new startup will be automatically initiated (hiccup) after 2.5ms (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

Thermal Shutdown

Thermal protection is designed to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching stops and the device shuts down. Automatic recovery with a soft-start will begin when the junction temperature drops below the +135°C falling threshold.

APPLICATION INFORMATION

In this section, power supply design with the GRM2030 synchronous Buck converter and selection of the external component will be explained based on the typical application.

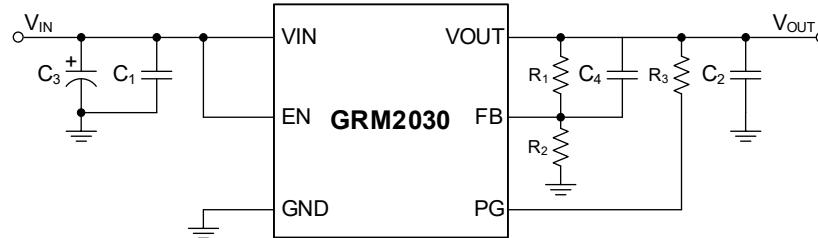


Figure 3. Application Circuit

Table 1. Recommended Components

V _{OUT} (V)	Part	Value	Package
1.8	C ₁	10μF, 10V, X5R	0805
	C ₂	47μF, 10V, X5R	0805
	C ₃	Optional	
	C ₄	6pF, 50V, C0G	0402
	R ₁	100kΩ, ±1%	0402
	R ₂	49.9kΩ, ±1%	0402
	R ₃	499kΩ, ±1%	0603

Input Capacitor Selection (C_{IN})

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Output Capacitor Selection (C_{OUT})

This device is capable to operate with low ESR ceramic capacitors to get low voltage ripple and fast response. 47μF capacitors with X7R or X5R dielectric type are recommended. If an output capacitor larger than 150μF is used, appropriate startup current reduction should be considered to avoid current limiting or false triggering of the short-circuit protection during startup.

Output Voltage Setting

Use Equation 1 to select the R₁/R₂ resistor divider to set the V_{OUT}. Select the R₂ value less than 100kΩ to compromise noise sensitivity and light load losses.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Layout Guidelines and Example

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the

GRM2030.

It is recommended to place all components as close as possible to the IC. Specially, the input capacitor placement must be closest to the VIN and GND pins of the device.

- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to Figure 4 for an example of component placement, routing and thermal design.
- For best manufacturing results, it is important to create the pads as solder mask defined (SMD). This keeps each pad the same size and avoids solder pulling the device during reflow.

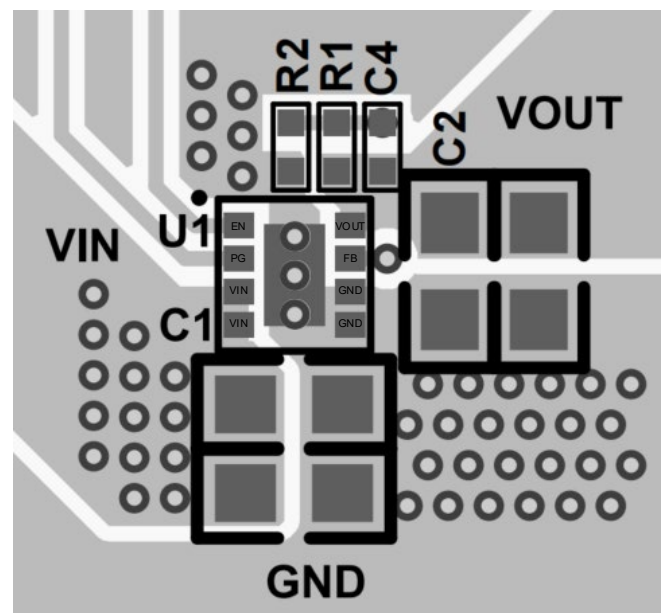


Figure 4. Layout Top Layer

REVISION HISTORY

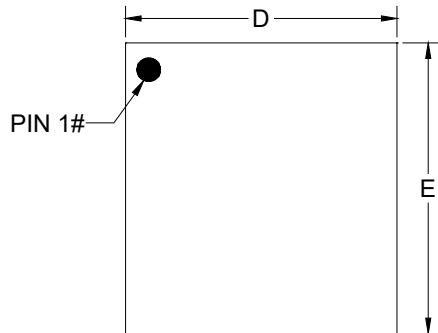
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data.....	All

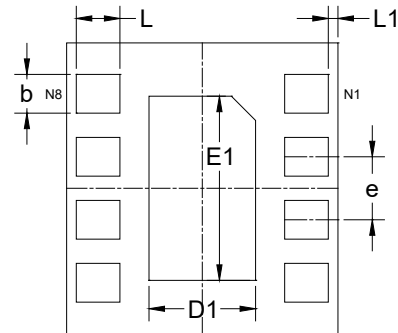
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

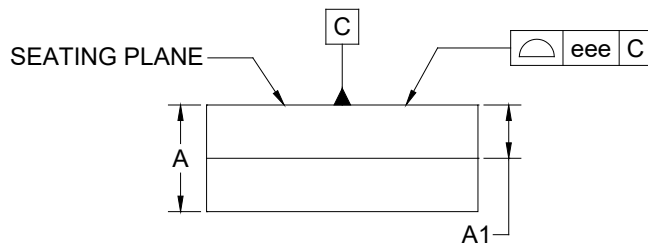
LGA-2.8×3-8L



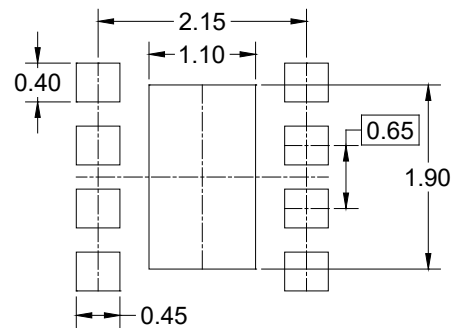
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

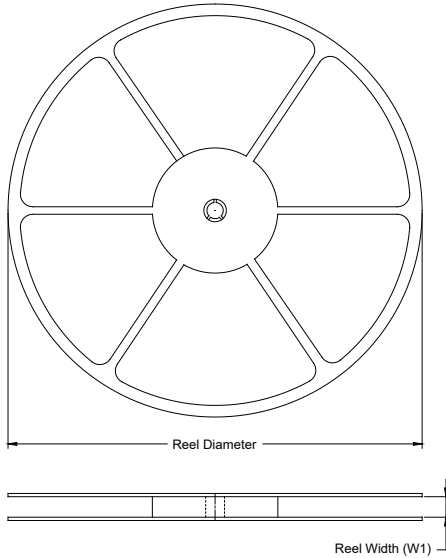
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	1.100	1.150
A1	0.550 REF		
b	0.350	-	0.450
D	2.650	-	2.950
D1	1.000	-	1.200
E	2.850	-	3.150
E1	1.800	-	2.000
e	0.650 BSC		
L	0.400	-	0.500
L1	0.100 REF		
eee	0.100		

NOTE: This drawing is subject to change without notice.

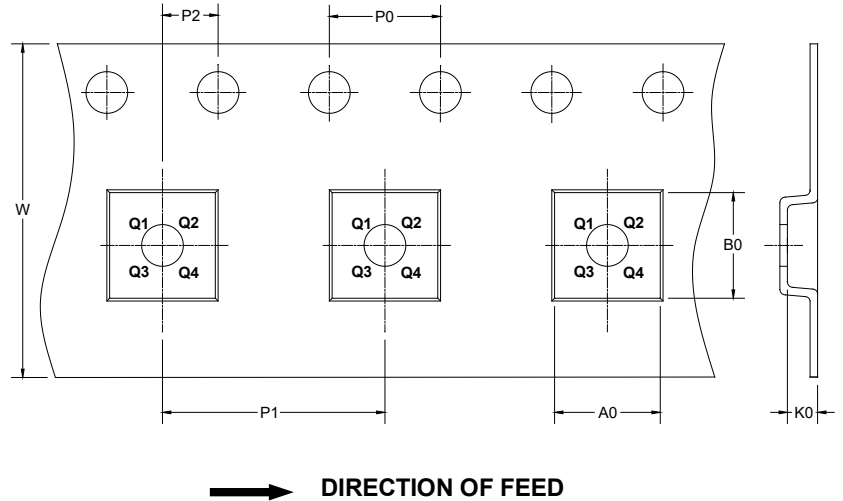
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



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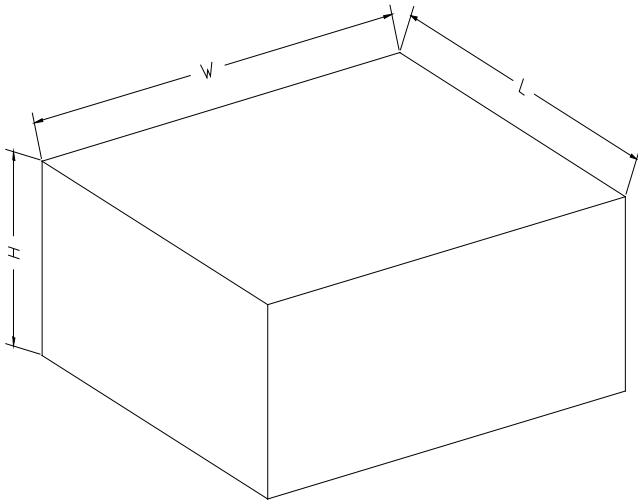
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
LGA-2.8×3-8L	13"	12.4	3.10	3.30	1.45	4.00	8.00	2.00	12.00	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DP0002