

GENERAL DESCRIPTION

The SGM66025 is a synchronous Boost converter with integrated load disconnect function. The device is capable to start up from 0.65V (TYP) input, and the input voltage can operate down to 0.6V after startup. Output voltage ranges from 1.8V to 4V. The device integrates a 1.8A power switch with a fixed 1MHz switching frequency. Bypass mode is also supported when V_{IN} is higher than V_{OUT} .

The P channel synchronous rectifier provides short-circuit protection and load disconnect feature to minimize leakage current drawn from the input source. The device also implements soft-start feature to minimize inrush current during startup.

The SGM66025 implements various protection features such as short-circuit protection and thermal shutdown to improve device robustness.

The SGM66025 is available in a Green TSOT-23-8 package and operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- 1V Startup Input Voltage
- 0.6V Operation Input Voltage after Startup
- 1.8V to 4V Output Voltage Range
- Up to 96% Efficiency
- 1MHz Switching Frequency
- 30 μ A (TYP) Quiescent Current
- 0.4 μ A (TYP) Shutdown Current
- Current-Mode Control with Internal Compensation
- True Output Disconnection from Input
- $V_{IN} > V_{OUT}$ Bypass Mode & Down Mode
- High Efficiency under Light-Load Conditions
- Internal Soft-Start
- Load Disconnect
- Short-Circuit Protection
- Over-Current Protection
- -40°C to +85°C Operating Temperature Range
- Available in a Green TSOT-23-8 Package

APPLICATIONS

Alkaline Battery
System 3.3V Bias
Medical Equipment
Wireless System Bias
VR

TYPICAL APPLICATION

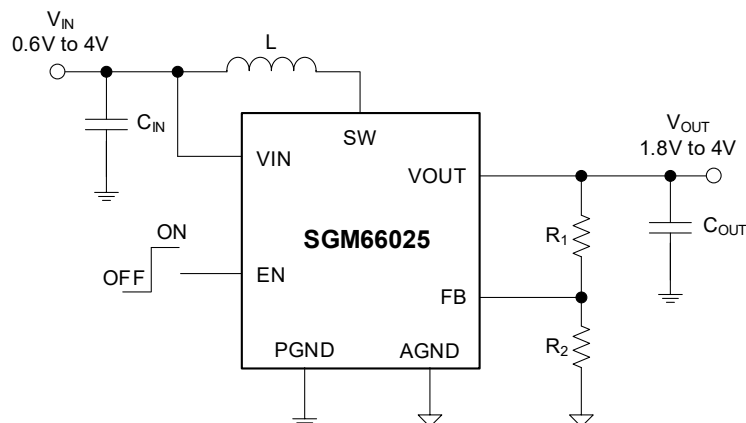


Figure 1. Typical Application Circuit

SGM66025 1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM66025	TSOT-23-8	-40°C to +85°C	SGM66025YTN8G/TR	0J3XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.

YYY X X

— Date Code - Week

— Date Code - Year

— Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

SW, VOUT.....-0.3V to 6V

VIN, EN, FB.....-0.3V to 6V

Package Thermal Resistance

TSOT-23-8, θ_{JA} 132°C/W

TSOT-23-8, θ_{JB} 44.1°C/W

TSOT-23-8, θ_{JC} 85.4°C/W

Junction Temperature.....+150°C

Storage Temperature Range.....-65°C to +150°C

Lead Temperature (Soldering, 10s).....+260°C

ESD Susceptibility ^{(1) (2)}

HBM.....±4000V

CDM±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN}.....0.6V to 4V

Input Voltage Range, V_{OUT}.....1.8V to 4V

Operating Junction Temperature Range.....-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

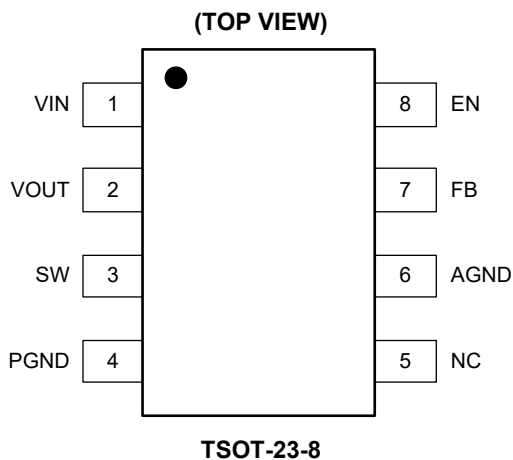
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VIN	Input Voltage Pin.
2	VOUT	Output Voltage Pin.
3	SW	Switch Node Pin.
4	PGND	Power Ground Pin.
5	NC	No Connect Pin.
6	AGND	Analog Ground Pin.
7	FB	Feedback Pin. Connect a voltage divider from VOUT to this node.
8	EN	Enable Pin. Logic high turns the converter on. Logic low turns the converter off.

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1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

ELECTRICAL CHARACTERISTICS

($V_{IN} = V_{EN} = 1.8V$, $V_{OUT} = 3.3V$, $T_J = -40^{\circ}C$ to $+85^{\circ}C$, typical values are at $T_J = +25^{\circ}C$, unless otherwise noted.)

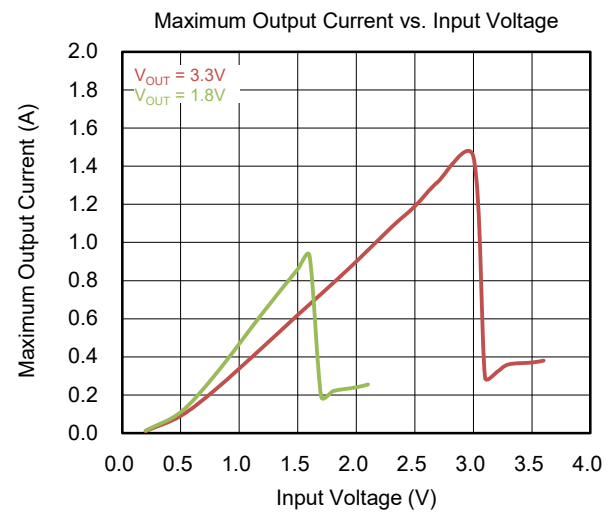
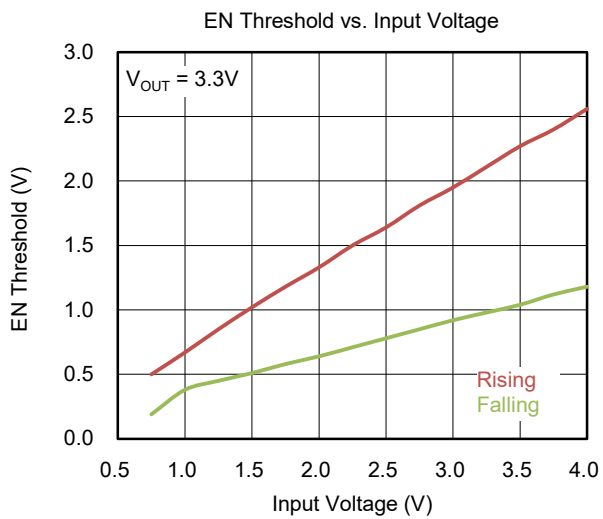
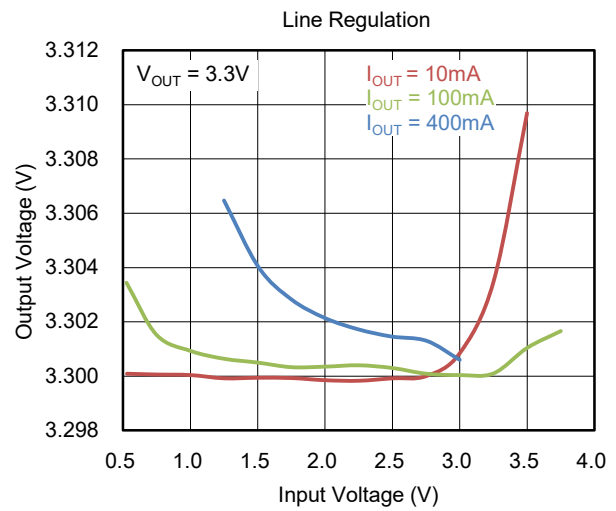
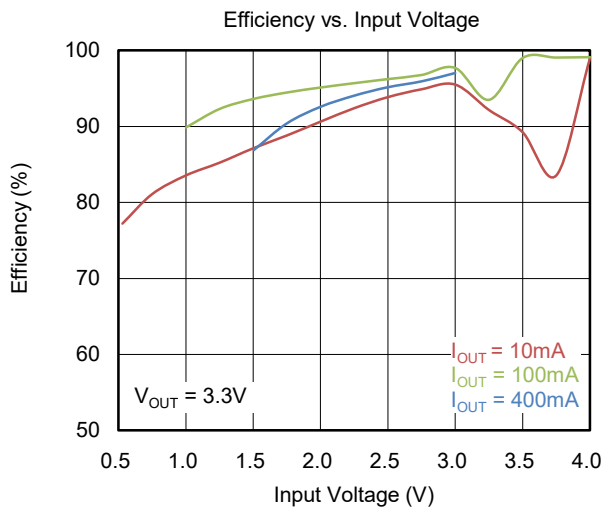
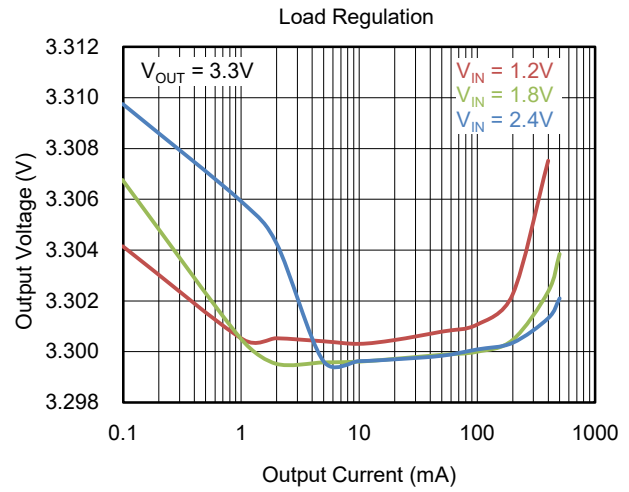
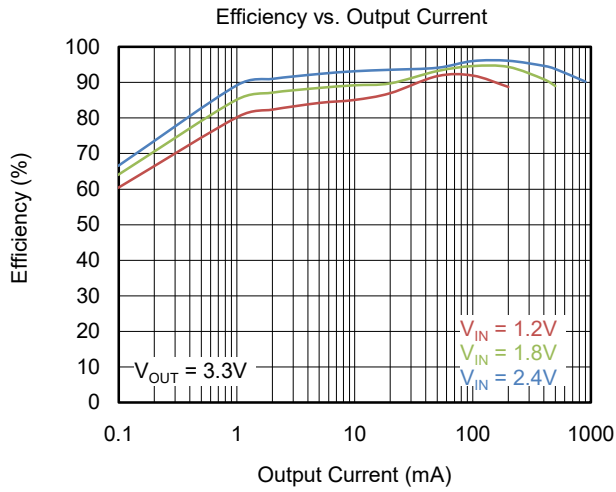
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	$T_J = +25^{\circ}C$	0.6		4	V
Input Voltage UVLO	V_{IN_UVLO}	V_{IN} Rising	0.4	0.65	1.0	V
Output Voltage Range	V_{OUT}	$T_J = +25^{\circ}C$	1.8		4	V
Quiescent Current	I_Q			30	70	μA
Shutdown Current	I_{SD}			0.4	2.0	μA
Switching Frequency	f_{SW}		0.7	1.0	1.3	MHz
Feedback Voltage	V_{FB}		1.156	1.20	1.236	V
Feedback Leakage Current	I_{FB_LKG}			4	100	nA
Low-side FET On-Resistance	$R_{DS(on)}$			95		m Ω
High-side FET On-Resistance				90		m Ω
Maximum Duty Cycle	D_{MAX}		85	97		%
Startup Current Limit	I_{ST_LIMIT}			0.72		A
Low-side FET Current Limit	I_{SW}		1.4	1.8		A
EN Input High Level	V_{EN_H}		$0.8 \times V_{IN}$			V
EN Input Low Level	V_{EN_L}				$0.2 \times V_{IN}$	V
PMOS Leakage Current	I_{PLK}	$V_{SW} = 4V$, $V_{OUT} = 0V$		1	500	nA
NMOS Leakage Current	I_{NLK}	$V_{SW} = 4V$		20	500	nA
Thermal Shutdown				140		$^{\circ}C$
Thermal Shutdown Hysteresis				15		$^{\circ}C$

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1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 3.3\text{V}$ and $L = 3.3\mu\text{H}$, unless otherwise noted.

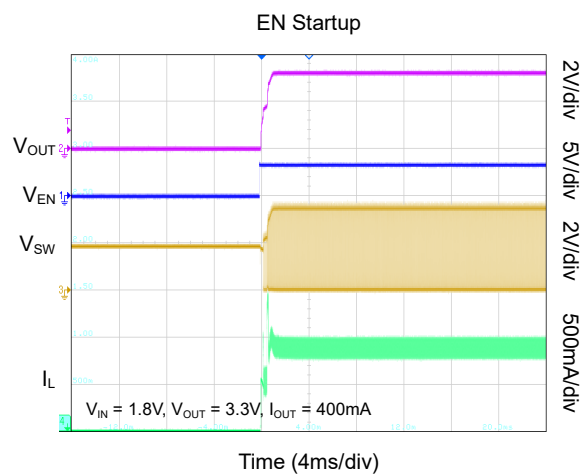
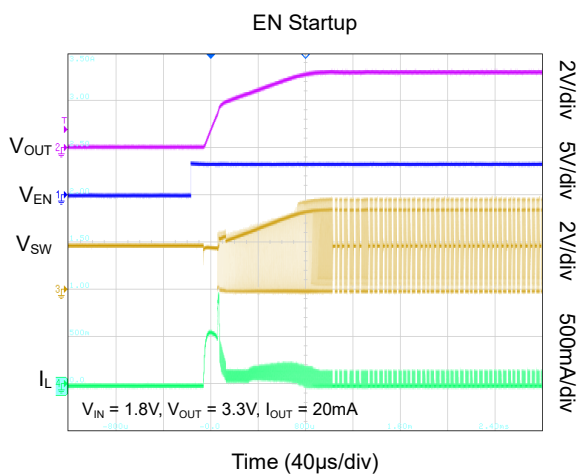
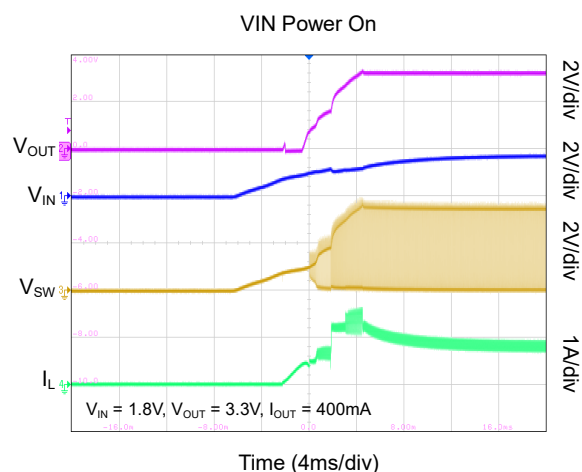
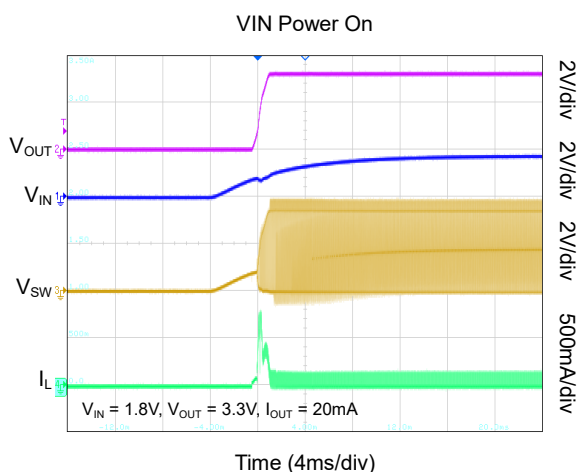
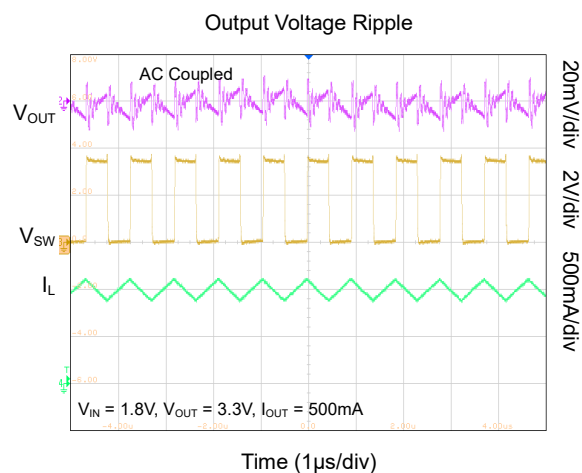
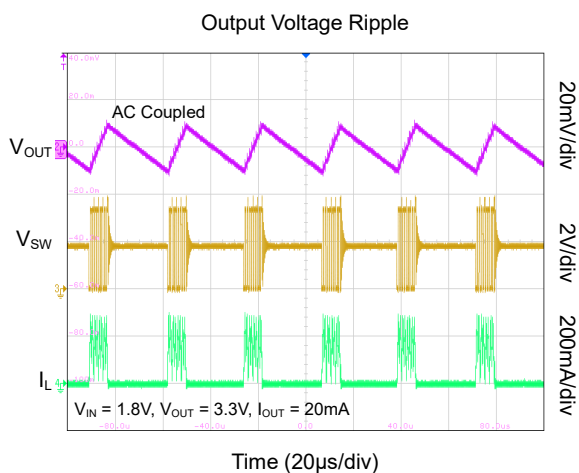


SGM66025

1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 3.3\text{V}$ and $L = 3.3\mu\text{H}$, unless otherwise noted.

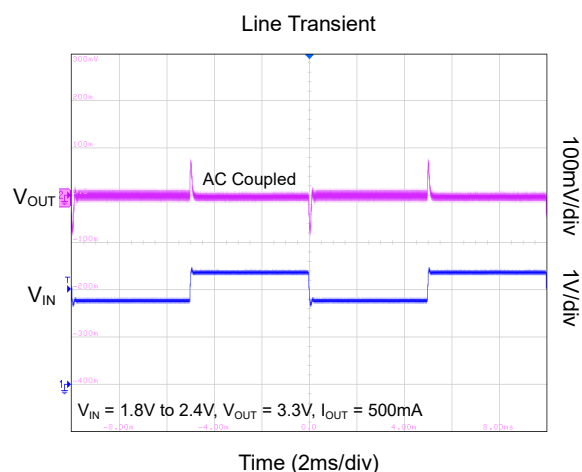
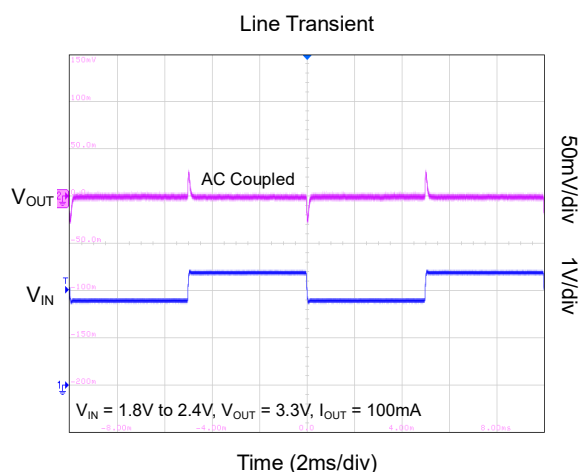
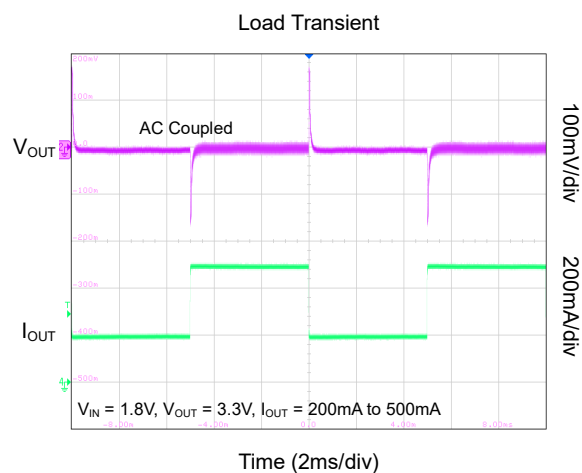
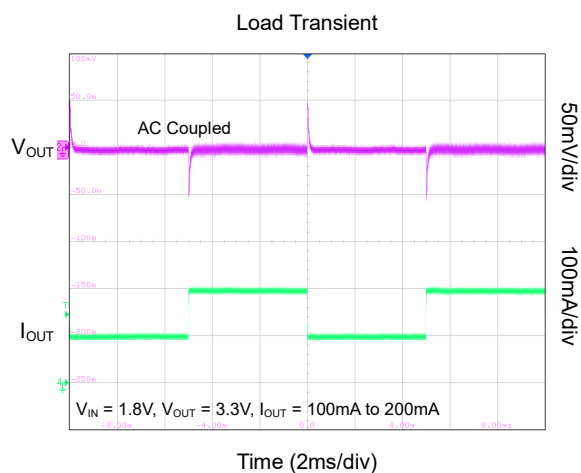


SGM66025

1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{IN} = 1.8\text{V}$, $V_{OUT} = 3.3\text{V}$ and $L = 3.3\mu\text{H}$, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

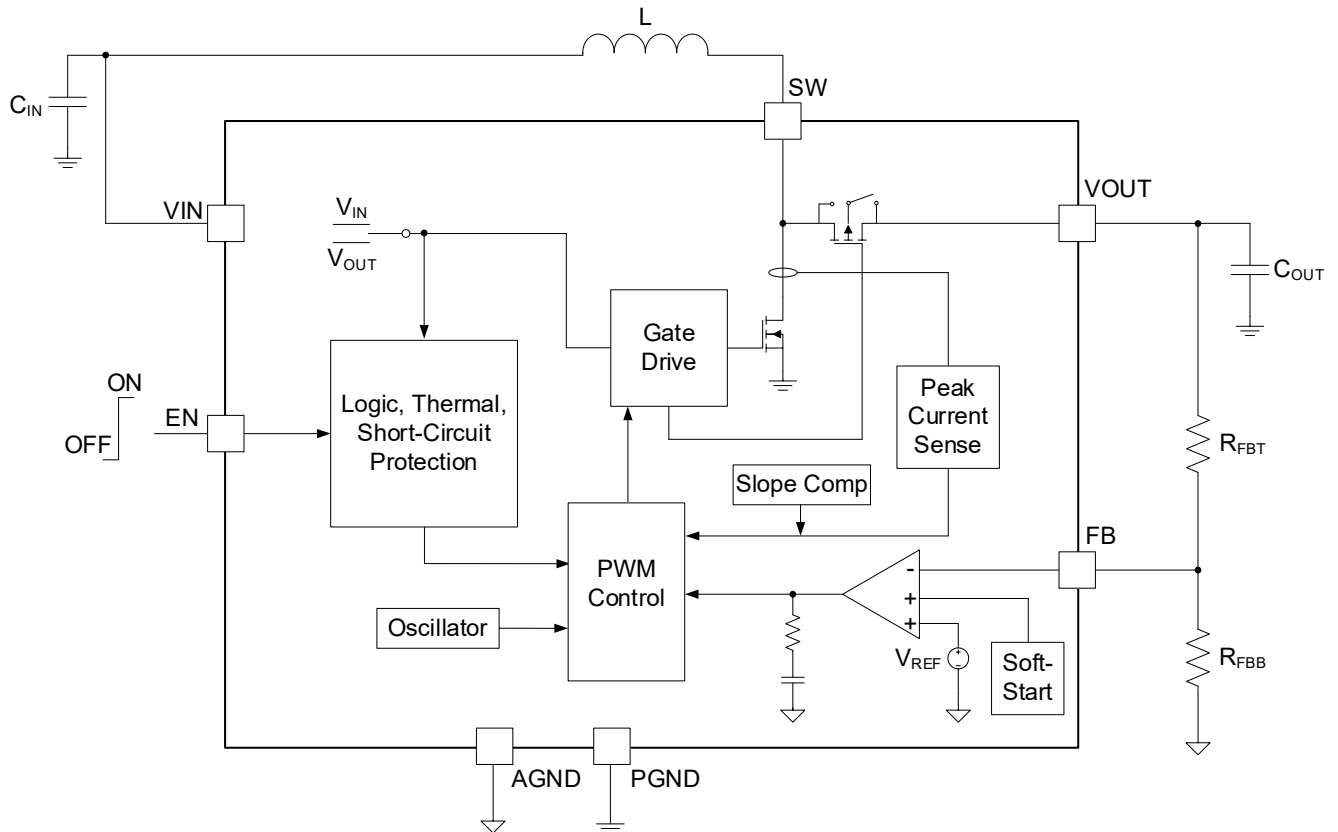


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM66025 is a Boost converter in a TSOT-23-8 package operates with a fixed 1MHz frequency. It integrates the function of true output disconnect and is able to start up with 0.65V (TYP) input. The fixed frequency peak current control mode is adopted as the control architecture. The built-in soft-start feature and loop compensation simplify the design and minimize the number of external components. The internal low R_{DS(on)} power MOSFETs ensure high efficiency under heavy current load and power-save mode operation enables high efficiency under light current load.

Synchronous Rectifier

The synchronous rectification function is realized by an internal N-channel MOSFET and a P-channel MOSFET. Compared with the traditional Schottky diode, the PMOS can improve the operating efficiency.

True disconnection function is realized by controlling the body diode of the rectifier PMOS. This feature ensures that there is no leakage current path between input and output even the device is disabled.

Startup

The SGM66025 starts up with a 720mA precharge current to charge the output voltage to $V_{IN} - 270\text{mV}$ by turning on the PMOS. The current limiting function ensures the safety of the device under short-circuit conditions.

The SGM66025 starts switching after precharge phase. The device operates in free-running mode when V_{OUT} is below 1.77V. The switching frequency is fixed at 500kHz in this mode and the duty cycle is fixed to around 70%. The switching current is limited to about 800mA.

The internal soft-start follows the FB voltage during the precharge and free running period. Once the output voltage exceeds 1.77V, the device will enter closed-loop control, the output voltage will be controlled by soft-start and the current limit threshold goes to 1.5A. When the soft-start is complete, the current limit threshold is set to 1.8A. It then works in Boost mode or

Down mode depending on the voltage value of V_{IN} and V_{OUT} . If V_{IN} is 270mV higher than the preset voltage of V_{OUT} at startup, the chip will continue to work in Bypass mode. Please refer to Table 1 for more details about operating modes.

Table 1. Operation Mode during Startup Sequence

$V_{OUT} < V_{IN} - 270\text{mV}$	Bypass Mode
$V_{OUT} \geq V_{IN} - 270\text{mV} \ \& \ V_{OUT} < 1.77\text{V}$	Free Running
$V_{IN} - 270\text{mV} < V_{OUT} < V_{IN} + 250\text{mV} \ \& \ V_{OUT} \geq 1.7\text{V}$	Down Mode
$V_{OUT} > V_{IN} + 250\text{mV} \ \& \ V_{OUT} \geq 1.77\text{V}$	Boost Mode

When V_{OUT} is greater than V_{IN} , the SGM66025 is powered by V_{OUT} instead of V_{IN} in normal mode. The device is able to operate down to 0.6V, thus only the energy of battery will limit the application.

Device Enable

The device is enabled when EN is pulled higher than $0.8 \times V_{IN}$. It will be shut down when EN is grounded. In shutdown mode, the device turns off all power MOSFETs and logic circuits, and the body diode of the rectifier PMOS is reversed to achieve complete isolation of input and output.

Power-Save Mode

When the load is lightened, the device enters power-save mode (PSM). When the V_{OUT} drops below the programmed threshold, several successive pulses are performed in PWM mode logic to restore the V_{OUT} . Once V_{OUT} returns to the programmed value, the power-save mode will resume. Power-save mode consumes less circuit resources, and power consumption is significantly reduced. The control mode of the device is the peak current control mode through sampling the voltage of FB.

Typically, output voltage ripple can be reduced to less than 1% of the peak-to-peak output value by adding output capacitor. Whether the device operates in PSM or PWM depends on load current, output capacitance, input voltage, output voltage, and inductor value.

DETAILED DESCRIPTION (continued)

Under-Voltage Lockout

Under-voltage lockout protection will be triggered when the voltage of VIN pin falls below 0.5V (TYP) and the device will stop switching.

Error Amplifier

The voltage of FB pin and the internal 1.20V reference will be used as input signals of the error amplifier. The error signal generated during this process is compared with the sampled inductor peak current to adjust the switching duty cycle to regulate the output voltage.

Current Sensing

The current flowing through the NMOS is sampled as a voltage signal that will be summed with a slope compensation signal used for PWM duty cycle generation. The leading edge blanking time of 60ns enhances the noise suppression during current sampling. The peak current is limited to around 1.8A.

Thermal Protection

To protect the device from damage due to overheating, a thermal shutdown feature is implemented to disable the device when the die temperature exceeds +140°C (TYP). The chip is automatically enabled when the temperature falls below +125°C (15°C hysteresis, TYP).

Output Disconnect and Inrush Limiting

The SGM66025 integrates the function of true output disconnection by switching the internal PMOS body diode direction. The true disconnect function ensures that the VOUT pin cannot maintain any voltage or sink any current. Inrush and surge currents from the input supply are limited by precharge circuit.

When the external Schottky diode between SW and VOUT is connected, the true disconnect function is disabled.

To reduce the spike voltage on the SW pin, please keep the output capacitor close to the VOUT pin and GND pin. Using low ESR/ESL ceramic capacitors will achieve better filtering.

Short-Circuit Protection

The SGM66025 implements output short-circuit protection by turning off the NMOS when the output voltage drops below 1V. Then the device enters in Bypass mode as power-on period. The thermal regulation loop will also control the current flows through PMOS when the die temperature exceeds the over-temperature threshold.

Down Mode ($V_{IN} - 270\text{mV} < V_{OUT} < V_{IN} + 250\text{mV}$) Operation

The SGM66025 will continue to regulate the output voltage when the input voltage operates in a range that is very close to the output voltage. The V_{GS} of the PMOS is dynamically adjusted to provide a down slope to the inductor current, thus higher efficiency can be achieved than in the conventional Down mode. When V_{IN} gradually approaches V_{OUT} , the system will dynamically adjust the frequency since $V_{IN} > V_{OUT} - 0.7\text{V}$, from 1MHz in normal operation to a minimum of 300kHz. In this mode, the peak current is limited to around 600mA.

Bypass ($V_{OUT} + 270\text{mV} < V_{IN}$) Operation

When the input voltage is larger than $V_{OUT} + 270\text{mV}$, the SGM66025 works in Bypass mode, which includes linear charging of output capacitance during startup and bypass operation in steady state. In this mode, the rectifier MOSFET is always on, and the load current flows only through the rectifier PMOS, the current limiting threshold is around 720mA in bypass mode.

SGM66025 1V Startup Input Voltage, 1.8A I_{SW} Synchronous Boost Converter with Load Disconnect

APPLICATION INFORMATION

Output Voltage Adjustment

By connecting the FB pin to the center tap of the external resistive divider, the device's output voltage can be adjusted from 1.8V to 4V. Please refer to Equation 1 to calculate the desired output voltage:

$$V_{OUT} = 1.20V \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Larger divider resistance can lower the quiescent current. Setting R₁ larger than 300kΩ is recommended for better stability.

Input Capacitor Selection

For better filtering, the low ESR ceramic capacitors are recommended to be used as input capacitor. Placing the input capacitors as close to the device as possible to reduce noise from power supply. Add a 10μF ceramic capacitor in parallel with a 100nF ceramic capacitor is recommended.

Output Capacitor Selection

To ensure the loop stability, please use a minimum capacitor of 22μF as the output capacitor and low ESR ceramic capacitors are recommended. The larger output capacitance will improve the transient response while reduce the output ripple. Please refer to the Equation 2 below to calculate the theoretical capacitance value.

$$C_O \geq \frac{I_O \times (V_{OUT_MAX} - V_{IN_MIN})}{f_S \times V_{OUT_MAX} \times \Delta V} \quad (2)$$

where

V_{OUT_MAX} = Maximum output voltage

V_{IN_MIN} = Minimum input voltage

I_O = Output current

f_S = Switching frequency

ΔV = Acceptable output ripple

Increasing the capacitance can reduce ripple in Down mode where V_{IN} ≈ V_{OUT} and ensure stability in PWM mode with heavy load conditions.

Inductor Selection

The SGM66025 operates at a fixed switching frequency of 1MHz in most situations, a 3.3μH inductor is recommended for majority of applications. Large inductors can slightly reduce the PSM operating threshold and increase the load current capability by reducing the ripple current. Please refer to the Equation 3 below to calculate the minimum theoretical inductance.

$$L \geq \frac{V_{IN_MIN} \times (V_{OUT_MAX} - V_{IN_MIN})}{V_{OUT_MAX} \times \Delta I_L \times f_S} \quad (3)$$

where

ΔI_L = Peak-to-peak inductor current

It is recommended to select the inductor ripple current to 30%~40% of the maximum input current. In general, high frequency ferrite-core inductors help reduce frequency-dependent power losses. Try to use low DCR inductance, when the DCR is much lower than R_{DS(on)}, the efficiency will be significantly improved. Also, make sure that the saturation current of the inductor is higher than the current limit.

PCB Layout Considerations

In order to avoid poor performance, EMI problems, and resistance losses, please refer to the following recommendations to optimize the PCB layout.

1. Add an about 100nF decoupling capacitor as close as possible to the VOUT and GND pins. Adding vias on VOUT net near the output capacitance will increase the parasitic inductance, which is not beneficial to reduce the spike voltage of the SW pin.
2. Using short and wide path to connect the power devices (Such as input capacitor, output capacitor, and inductor).
3. Feedback divider resistors should be close to AGND.
4. Use a larger copper area to increase heat dissipation.

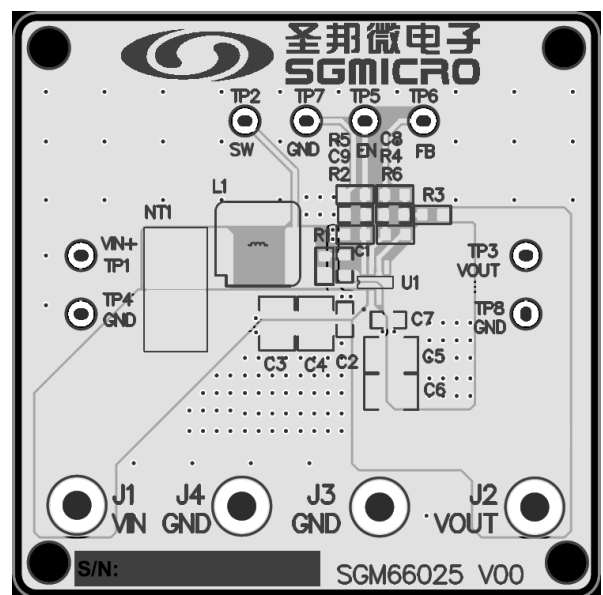


Figure 3. Layout Example

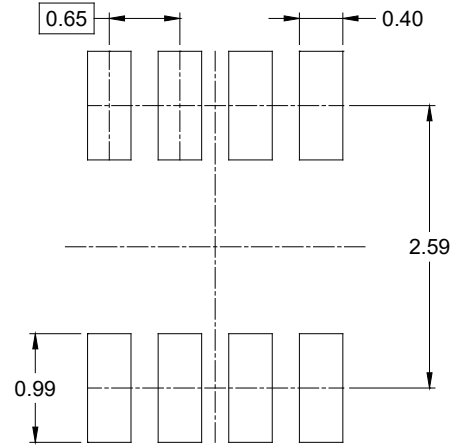
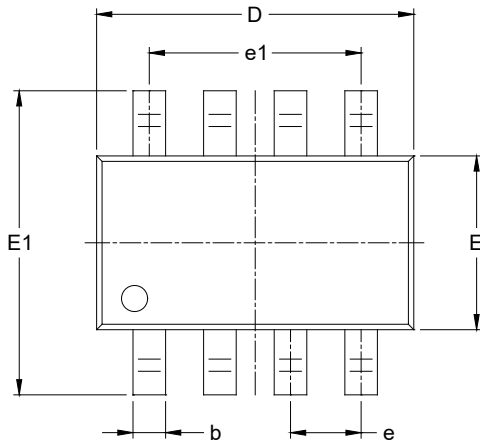
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

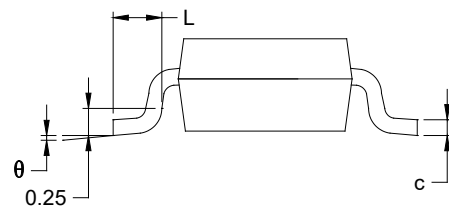
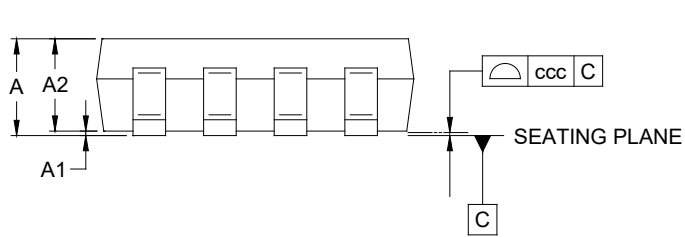
JULY 2025 – REV.A.2 to REV.A.3	Page
Changed the 0.8V on the page header to 1V	All
Updated the GENERAL DESCRIPTION and Overview sections (Changed 0.8V to 0.65V)	1, 9
Added notes for ESD	2
Updated the TYPICAL PERFORMANCE CHARACTERISTICS (Maximum Output Current vs. Input Voltage and Load Transient curves)	5, 7
Updated the Equation 3	11
MAY 2024 – REV.A.1 to REV.A.2	Page
Updated the Functional Block Diagram	8
Added θ_{JB} and θ_{JC}	2
APRIL 2024 – REV.A to REV.A.1	Page
Updated the Electrical Characteristics and Typical Performance Characteristics sections	4, 6
Changes from Original to REV.A (DECEMBER 2023)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TSOT-23-8



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700	-	1.000
b	0.220	-	0.380
c	0.080	-	0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.550	-	3.050
e	0.650 BSC		
e1	1.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

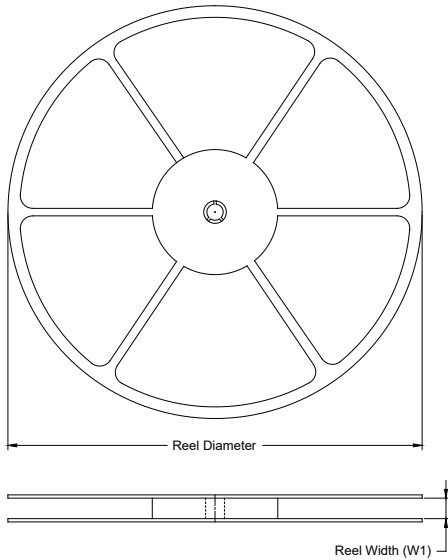
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

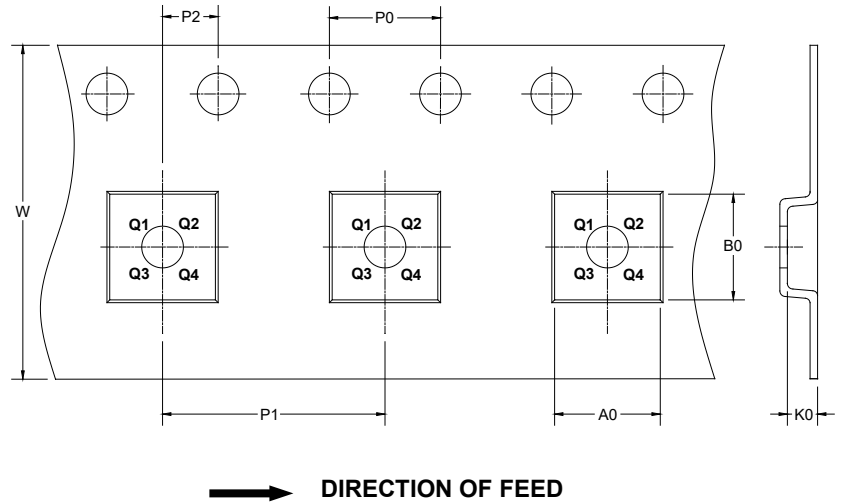
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

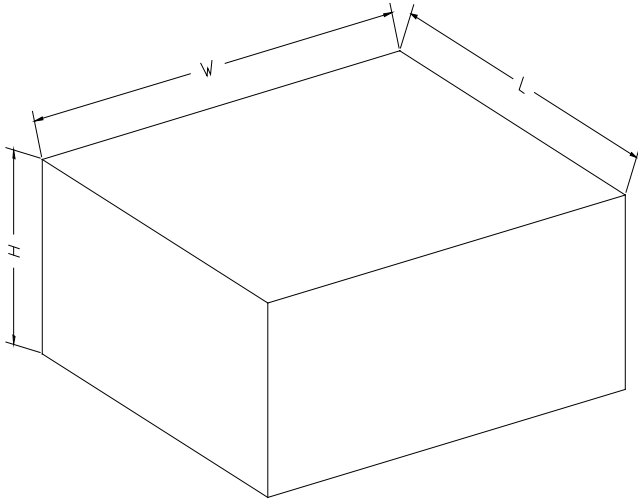
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-8	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002