

SGM4553YVS Level Translator

2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

GENERAL DESCRIPTION

The SGM4553YVS is a 2-bit, non-inverting, bidirectional voltage-level translator which features two independent configurable power-supply lines. The A and B ports track the $V_{\rm CCA}$ supply and $V_{\rm CCB}$ supply respectively. The supply voltage range is 1.65V to 5.5V for A ports and 2.3V to 5.5V for B ports. The device provides a bidirectional translation function among the different voltage nodes (including 1.8V, 2.5V, 3.3V and 5V).

The SGM4553YVS has an output-enabled (OE) function, which controls the inputs and outputs states. When OE goes low, all I/Os enter into the high-impedance state. It is beneficial for reducing quiescent current consumption. When V_{CCA} is powered, OE has an internal pull-down current source.

The SGM4553YVS is available in a Green VSSOP-8 package. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- Power Supply Voltage Ranges (V_{CCA} ≤ V_{CCB})
 - + A Ports: 1.65V to 5.5V
 - B Ports: 2.3V to 5.5V
- Direction-Control Signal is Not Required
- Data Rates
 - Push-Pull: 24MbpsOpen-Drain: 2Mbps
- Support V_{CCA} or V_{CCB} Isolation
 - When V_{CCA} or V_{CCB} is Low, Device Enters Power-Down Mode
- No Specific Power Sequences Required for V_{CCA} and V_{CCB}
- Support Power-Down Mode
- -40°C to +85°C Operating Temperature Range
- Available in a Green VSSOP-8 Package

APPLICATIONS

Universal Asynchronous Receiver/Transmitter I²C/SMBus Interfaces
General Purpose I/O (GPIO)

TYPICAL APPLICATION

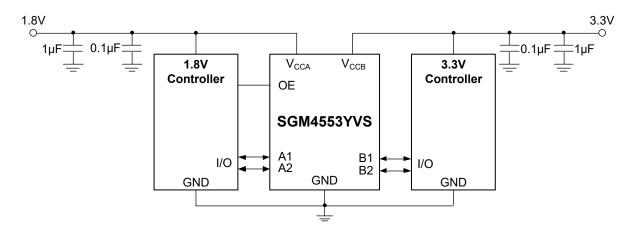


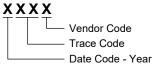
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4553YVS	VSSOP-8	-40°C to +85°C	SGM4553YVS8G/TR	4553 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RA	IINGS
Supply Voltage Range	
V _{CCA}	0.3V to 6V
V _{CCB}	0.3V to 6V
Input Voltage Range, V _I ⁽¹⁾	
A Ports, B Ports, OE	0.3V to 6V
Output Voltage Range for the High-In	npedance or Power-Off
State, V _O ⁽¹⁾	
A Ports	0.3V to 6V
B Ports	
Output Voltage Range for the High or I	Low State, V _O ^{(1) (2)}
A Ports	
B Ports	0.3V to V _{CCB} + 0.3V
Input Clamp Current, I_{IK} ($V_I < 0$)	50mA
Output Clamp Current, I_{OK} ($V_O < 0$)	50mA
Package Thermal Resistance	
VSSOP-8, θ_{JA}	221.5°C/W
VSSOP-8, θ_{JB}	151.1°C/W
VSSOP-8, θ _{JC}	126.9°C/W
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility (3) (4)	
HBM	±4000V
CDM	±1000V

NOTES:

- 1. When the input and output current ratings are observed, the input and I/O negative voltage ratings may be exceeded.
- 2. V_{CCA} and V_{CCB} values are shown in the recommended operating conditions in Electrical Characteristics section.
- 3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
- 4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range-40°C to +85°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

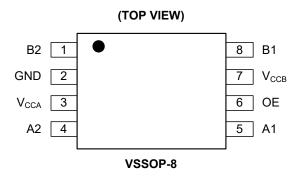
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	B2	I/O	Channel 2 Input/Output B. It tracks the V _{CCB} supply.
2	GND	G	Ground.
3	V _{CCA}	Р	Supply Voltage on A Ports. It can be operated from 1.65V to 5.5V, and V_{CCA} is always $\leq V_{CCB}$.
4	A2	I/O	Channel 2 Input/Output A. It tracks the V _{CCA} supply.
5	A1	I/O	Channel 1 Input/Output A. It tracks the V _{CCA} supply.
6	OE	I	Output-Enabled Control Pin. Active high. When OE goes low, all outputs enter into the high-impedance state. It tracks the V_{CCA} supply.
7	V _{CCB}	Р	Supply Voltage on B Ports. It can be operated from 2.3V to 5.5V.
8	B1	I/O	Channel 1 Input/Output B. It tracks the V _{CCB} supply.

NOTE: I = input, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V, T_A = -40°C to +85°C, typical values are measured at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS	
Recommended Operati	ng Conditio	ns ^{(1) (2)}					•		
Supply Voltage (3)	V _{CCA}	A ports			1.65		5.5		
Supply voltage **	V _{CCB}	B ports					5.5	V	
		A	V _{CCA} = 1.65V to 1.95V, V _{CCB} = 2.3V to 5.5V		V _{CCI} - 0.2		V _{CCI}		
High-Level Input		A ports	$V_{CCA} = 2.3V \text{ to } 5.5V,$	V _{CCI} - 0.4		V _{CCI}	.,		
Voltage	V _{IH}	B ports			V _{CCI} - 0.4		V _{CCI}	V	
		OE			V _{CCA} × 0.8		5.5		
		A ports			0		0.15		
Low-Level Input Voltage	V _{IL}	B ports			0		0.15	V	
		OE			0		V _{CCA} × 0.25		
Electrical Characteristic	cs								
High-Level Output	V _{OHA}	A ports	$I_{OH} = -20\mu A, V_{IB} \ge V_{C}$	_{CCB} - 0.4V	V _{CCA} × 0.7			V	
Voltage	V _{OHB}	B ports	$I_{OH} = -20\mu A, V_{IA} \ge V_{C}$	_{CCA} - 0.4V	V _{CCB} × 0.7			V	
Low-Level Output	V_{OLA}	A ports	$I_{OL} = 1 \text{mA}, V_{IB} \le 0.15$	5V			0.4		
Voltage	V _{OLB}	B ports	$I_{OL} = 1 \text{mA}, V_{IA} \le 0.15$	5V			0.4	V	
Input Leakage Current	l _l	OF	T _A = +25°C				±1		
input Leakage Current	lı lı	OE	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$				±1.5	μA	
	I _{OFF}	A ports	V _{CCA} = 0V,	T _A = +25°C			±0.5		
Power-Off Leakage		Aports	$V_{CCB} = 0V \text{ to } 5.5V$	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			±1	μΑ	
Current		B ports	$V_{CCA} = 0V \text{ to } 5.5V,$	T _A = +25°C			±0.5		
		D ports	V _{CCB} = 0V	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			±1		
2 Ctata Outrout Lastrana		A or B	T _A = +25°C				±0.6		
3-State Output Leakage	l _{OZ}	ports	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$				±1	μA	
			$V_1 = V_0 = OPEN,$	V_{CCA} = 1.65V to V_{CCB} , V_{CCB} = 2.3V to 5.5V			5.5		
	I _{CCA}	A ports	$I_0 = 0A$	$V_{CCA} = 5.5V$, $V_{CCB} = 0V$			5.5	μA	
				$V_{CCA} = 0V$, $V_{CCB} = 5.5V$			-1		
			$V_1 = V_0 = OPEN,$	V_{CCA} = 1.65V to V_{CCB} , V_{CCB} = 2.3V to 5.5V			15		
Quiescent Supply Current	I _{CCB}	B ports	$I_0 = 0A$	$V_{CCA} = 5.5V$, $V_{CCB} = 0V$			-1	μA	
Current				$V_{CCA} = 0V$, $V_{CCB} = 5.5V$			6		
	I _{CCA} + I _{CCB}	A and B ports	$V_1 = V_0 = OPEN,$ $I_0 = 0A$	$V_{CCA} = 1.65V \text{ to } V_{CCB},$ $V_{CCB} = 2.3V \text{ to } 5.5V$			20	μΑ	
	I _{CCZA}	A ports	$V_I = V_{CCI}$ or 0V, $I_O = 0A$, OE = GND	V_{CCA} = 1.65V to V_{CCB} , V_{CCB} = 2.3V to 5.5V			5.5	μΑ	
	I _{CCZB}	B ports	$V_I = V_{CCI}$ or 0V, $I_O = 0A$, OE = GND	V_{CCA} = 1.65V to V_{CCB} , V_{CCB} = 2.3V to 5.5V			5.5	μA	
OE Input Capacitance	Cı	OE	$V_{CCA} = 3.3V$, $V_{CCB} = 3.3V$	3.3V		4		pF	
Input/Output	C _{IO}	A ports	$V_{CCA} = 3.3V, V_{CCB} = 3.3V$	3 3V		5		pF	
Capacitance	010	B ports	VCCA O.OV, VCCB - V	U.U.		5		"	

NOTES:

- 1. V_{CCI} is the supply voltage associated with the data input ports.
- 2. V_{CCO} is the supply voltage associated with the data output ports.
- 3. Ensure that $V_{CCA} \le V_{CCB}$ and V_{CCA} must not exceed 5.5V.



SGM4553YVS

TIMING REQUIREMENTS

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$

DADAMETER	O)/MPOI	CONDITIONS	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	UNITS	
PARAMETER	SYMBOL	CONDITIONS	TYP	TYP	TYP	UNITS	
(V _{CCA} = 1.8V)							
Data Rate		Push-pull driving	21	22	24	Mhna	
Data Nate		Open-drain driving	2	2	2	Mbps	
Pulse Duration		Push-pull driving	47	45	41	200	
(Data Inputs)	t _W	Open-drain driving	500	500	500	ns	
(V _{CCA} = 2.5V)							
Data Data		Push-pull driving	20	22	24		
Data Rate		Open-drain driving	2	2	2	Mbps	
Pulse Duration		Push-pull driving	50	45	41	no	
(Data Inputs)	t _W	Open-drain driving	500	500	500	ns	
(V _{CCA} = 3.3V)	•		<u>.</u>				
Data Data		Push-pull driving		23	24	Mana	
Data Rate		Open-drain driving		2	2	Mbps	
Pulse Duration		Push-pull driving		43	41		
(Data Inputs)	t _W	Open-drain driving		500	500	ns	
(V _{CCA} = 5V)	•	•	•			•	
Data Rate		Push-pull driving			24	Mana	
		Open-drain driving			2	Mbps	
Pulse Duration		Push-pull driving			41		
(Data Inputs)	t _W	Open-drain driving			500	ns	

SWITCHING CHARACTERISTICS

(V_{CCA} = 1.8V, T_A = +25°C, unless otherwise noted.)

DADAMETED	OVMPOL	00	NOTIONS	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	LINUTO	
PARAMETER	SYMBOL	CO	NDITIONS	TYP	TYP	TYP	UNITS	
	+		Push-pull driving	2.4	3	4.3		
	t _{PHL}	From An to Bn	Open-drain driving	26	26.3	26.7	ne	
		FIOIII AII 10 BII	Push-pull driving	4	4	4	ns	
Branagation Dalay	t _{PLH}		Open-drain driving	175	145	110		
Propagation Delay			Push-pull driving	2	2.2	2.3		
	t _{PHL}	Franco Do to An	Open-drain driving	26	26.1	26.2		
	4	From Bn to An	Push-pull driving	1.7	1.5	1.4	ns	
	t _{PLH}		Open-drain driving	133	69	51		
Enable Time	t _{EN} (t _{PZH} & t _{PZL})	From OE to An	From OE to An or Bn		20	18	ns	
Disable Time	t _{DIS} (t _{PHZ} & t _{PLZ})	From OE to An	or Bn	1200	1200	1200	ns	
		A porto	Push-pull driving	7	5.8	5.4	ne	
Dies Time	t _{RA}	A ports	Open-drain driving	89	31	10	ns	
Rise Time		D is suite	Push-pull driving	6.5	5.3	4.5		
	t _{RB}	B ports	Open-drain driving	128	98	58	ns	
	4	A norto	Push-pull driving	2.9	2.7	2.6		
Fall Time	t _{FA}	A ports	Open-drain driving	1.9	1.7	1.6	ns	
Fall Time		D is suite	Push-pull driving	4.6	5.9	8		
	t _{FB}	B ports	Open-drain driving	2.2	2.3	2.9	ns	
Channel-to-Channel Skew	t _{sko}			0.5	0.5	0.5	ns	
Data Rate		Push-pull drivir	ng	21	22	24	Mhno	
Data Nate		Open-drain driving		2	2	2	Mbps	

SWITCHING CHARACTERISTICS (continued)

(V_{CCA} = 2.5V, T_A = +25°C, unless otherwise noted.)

242445752	O)/IIIDOI		UDITIONS	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	
PARAMETER	SYMBOL	COI	NDITIONS	TYP	TYP	TYP	UNITS
			Push-pull driving	2.7	3.3	4.8	
	t _{PHL}	From An to Bn	Open-drain driving	26.2	26.4	26.7]
		From An to Bn	Push-pull driving	2.6	2.6	2.6	ns
Duan anation Dalay	t _{PLH}		Open-drain driving	169	144	110	
Propagation Delay			Push-pull driving	2.3	2.3	2.6	
	t _{PHL}	Гиана Du 4a Au	Open-drain driving	26.3	26.4	26.5]
	_	From Bn to An	Push-pull driving	2	1.9	1.8	ns
	t _{PLH}		Open-drain driving	165	118	55	
Enable Time	t _{EN} (t _{PZH} & t _{PZL})	From OE to An	From OE to An or Bn		19	16	ns
Disable Time	t _{DIS} (t _{PHZ} & t _{PLZ})	From OE to An	or Bn	1200	1200	1200	ns
		A ports	Push-pull driving	3.4	3	2.8	ns
Rise Time	t _{RA}		Open-drain driving	120	70	10	
Rise Time		D = auta	Push-pull driving	5.3	3.8	3.1	
	t _{RB}	B ports	Open-drain driving	122	96	62	ns
		A norto	Push-pull driving	4.9	5	5.5	no
Fall Time	t_{FA}	A ports	Open-drain driving	2	1.9	1.7	ns
raii iiiile	4	Dinarta	Push-pull driving	4.8	6.1	8.3	20
	t _{FB}	B ports	Open-drain driving	1.9	2.1	2.7	ns
Channel-to-Channel Skew	t _{sko}			0.5	0.5	0.5	ns
Data Rate		Push-pull driving	ng	20	22	24	Malara
Data Rate		Open-drain driving		2	2	2	Mbps

SWITCHING CHARACTERISTICS (continued)

(V_{CCA} = 3.3V, T_A = +25°C, unless otherwise noted.)

DADAMETED	OVALDOL	00	NDITIONS	V _{CCB} = 3.3V	V _{CCB} = 5V	LINUTO	
PARAMETER	SYMBOL	CO	NDITIONS	TYP	TYP	UNITS	
			Push-pull driving	3.5	4.9		
	t _{PHL}	From An to Dr	Open-drain driving	26.3	26.7	T	
		From An to Bn	Push-pull driving	2.2	2.1	ns	
Duan anation Dalass	t _{PLH}		Open-drain driving	133	104		
Propagation Delay	_		Push-pull driving	3	3.2		
	t _{PHL}	F D 4. A	Open-drain driving	26.6	26.8		
	_	From Bn to An	Push-pull driving	1.8	1.7	ns	
	t _{PLH}		Open-drain driving	132	83		
Enable Time	t _{EN} (t _{PZH} & t _{PZL})	From OE to An or	Bn	18	15	ns	
Disable Time	t _{DIS} (t _{PHZ} & t _{PLZ})	From OE to An or	Bn	1200	1200	ns	
	4	A == ======	Push-pull driving	2.5	2.4	ne	
Dia a Tima	t _{RA}	A ports	Open-drain driving	87	36	ns	
Rise Time	4	Duranta	Push-pull driving	3	2.6		
	t _{RB}	B ports	Open-drain driving	87	56	ns	
	_	A ata	Push-pull driving	6.2	5.8		
Fall Time	t _{FA}	A ports	Open-drain driving	2.3	2	ns	
Fall Time		Duranta	Push-pull driving	6.5	8.2		
	t _{FB}	B ports	Open-drain driving	2 2.5		ns	
Channel-to-Channel Skew	t _{sko}			0.5	0.5	ns	
Data Rate		Push-pull driving		23	24	Mhna	
Data Rate		Open-drain driving	9	2	2	Mbps	

SWITCHING CHARACTERISTICS (continued)

(V_{CCA} = 5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CO	NDITIONS	V _{CCB} = 5V	UNITS	
PARAMETER	STWIBOL		HEITIONS	TYP	ONITS	
			Push-pull driving	6		
	t _{PHL}	From Archo Dr	Open-drain driving	26.7		
		From An to Bn	Push-pull driving	1.9	ns	
Draw a wation Dalay	t _{PLH}		Open-drain driving	120		
Propagation Delay			Push-pull driving	5.6		
	t _{PHL}	Francis Don to Am	Open-drain driving	27.3		
	,	From Bn to An	Push-pull driving	1.7	ns	
	t _{PLH}		Open-drain driving	126		
Enable Time	t _{EN} (t _{PZH} & t _{PZL})	From OE to An or	Bn	16	ns	
Disable Time	t _{DIS} (t _{PHZ} & t _{PLZ})	From OE to An or	Bn	1200	ns	
		A	Push-pull driving	2		
Dia a Time	t _{RA}	A ports	Open-drain driving	79	ns	
Rise Time		Duranta	Push-pull driving	2.3		
	t _{RB}	B ports	Open-drain driving	73	ns	
		A t -	Push-pull driving	8.7		
E 11 T	t _{FA}	A ports	Open-drain driving	2.7	ns	
Fall Time		.	Push-pull driving	8.6		
	t _{FB}	B ports	Open-drain driving	2.4	ns	
Channel-to-Channel Skew	t _{sko}			0.5	ns	
Data Rate		Push-pull driving		24	Mhno	
Dala Nale		Open-drain driving		2	Mbps	

WAVEFORMS

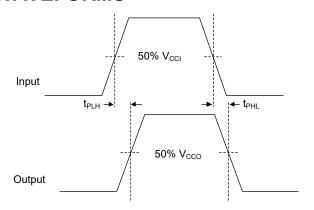


Figure 2. Propagation Delay

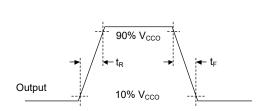


Figure 4. Rise Time and Fall Time of Data Output

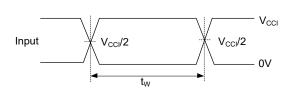
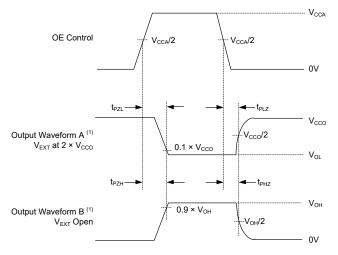


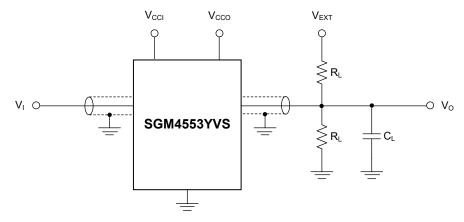
Figure 3. Pulse Duration



NOTE: 1. Waveform A indicates an output that is high except for OE is high. Waveform B indicates an output that is low except for OE is high.

Figure 5. Enable and Disable Times

TEST CIRCUIT



Definitions for test circuit:

R_L = Load resistance.

 C_L = Load capacitance includes jig and probe capacitance.

 V_{EXT} = External voltage for measuring switching times.

V_{CCI} = Supply voltage associated with the input.

 V_{CCO} = Supply voltage associated with the output.

Figure 6. Test Circuit for Measuring Switching Times

APPLICATION INFORMATION

Applications

The SGM4553YVS is a bridge between two digital systems with different power supplies as it can transmit the signal transparently. For the application of the SGM4553YVS, the output driver is open-drain or push-pull to drive the I²C or one-wire bus. In addition, if a device with push-pull driver is connected to the I/O pin of the SGM4553YVS, it will operate as normal.

Architecture

The SGM4553YVS can switch the direction of the transmission for A port and B port automatically without any external control.

It is not necessary to add an external direction control for the application of the SGM4553YVS. Also, each I/O pin can be an input or output of the voltage translator.

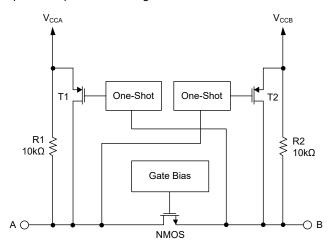


Figure 7. Architecture of an SGM4553YVS Cell

The explanation of two main parts of the internal circuit for the SGM4553YVS is shown as below:

- There is an NMOS between A port and B port to switch on or off the transmission.
- The one-shot accelerator can be used to accelerate the rising edges of the signal for A port and B port automatically.

Input Driver Requirements

The falling time of A port and B port and t_{PHL} depend on the output impedance of the connected device. The values of parameters which are t_{FA} , t_{FB} , t_{PHL} and data rates are specified when the resistance of external driver is less than 50Ω .

Power-Up

For the application of the SGM4553YVS, the V_{CCA} should be less than V_{CCB} . However, it does not matter if the power supply voltage is ramping, and the sequence of power-up for both V_{CCA} and V_{CCB} is not defined.

Output Load Considerations

To decrease the extend of capacitive loading and ensure the proper triggering of one-shot, the trace in PCB should be as short as possible. Also, to ensure that the round-trip reflection delay is smaller than the time period of one-shot, the users should also decrease the length of trace, which means that the signal integrity is guaranteed because of the low impedance for the reflection. The period of on-state for the one-shot part is 30ns. In addition, for the one-shot circuit, it can support lumped capacitive load. In addition, the one-shot circuit has the time-out function, which aims to handle the extremely heavy capacitive load. For the function of one-shot part of the SGM4553YVS, it can optimize the trade-off between the capability of load driving, maximum bit-rate and dynamic supply current. The length of PCB trace and output connectors will be considered as the capacitive load of the device, which may result in the retriggering of one-shot, contention of bus and the oscillations of the output.

Enable and Disable

The function of OE is used to disable SGM4553YVS by setting the transmitting I/O pins to high-impedance mode. The pull-down current source is integrated inside OE once it is powered by V_{CCA} . The definition of disable time (t_{DIS}) is the time period between OE goes low and when all of the I/O pins are in high-impedance mode. The enable time (t_{EN}) is defined as the time period between OE going to high position and one-shot part starting to operate.

Pull-Up or Pull-Down Resistors on I/O Lines

For the I/O pin of A and B side, there is a $10k\Omega$ pull-up resistor to provide a high position for each I/O pin. However, if a smaller pull-up resistor is required, the users can add an external resistor which is parallel with the $10k\Omega$ resistor. Also, the value of V_{OL} can be affected by the added external resistor. In addition, if the user wants to disable the device, the OE pin can be simply set to low position.

SGM4553YVS

2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

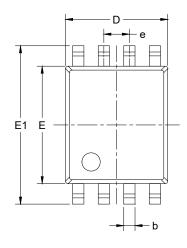
REVISION HISTORY

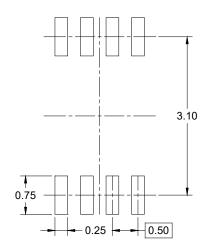
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (NOVEMBER 2025)

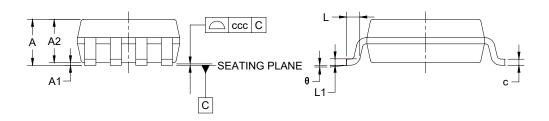
Page

PACKAGE OUTLINE DIMENSIONS VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)



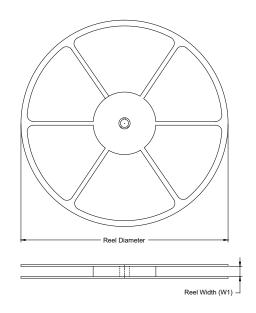
Cumbal	Dir	nensions In Millimet	ers			
Symbol	MIN	NOM	MAX			
А	-	-	1.000			
A1	0.000	-	0.150			
A2	0.600		0.850			
b	0.170	-	0.270			
С	0.080		0.230			
D	1.900	-	2.100			
Е	2.200	-	2.400			
E1	3.000	-	3.200			
е		0.500 BSC				
L	0.150	-	0.400			
L1	0.120 BSC					
θ	0°	-	8°			
ccc		0.100				

NOTES

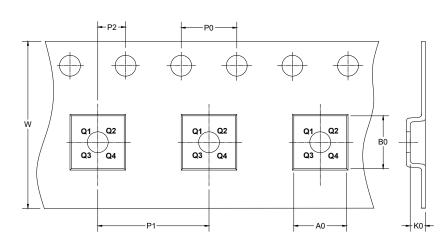
- 1. This drawing is subject to change without notice.
- 2. The dimensions do not include mold flashes, protrusions or gate burrs.
- 3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



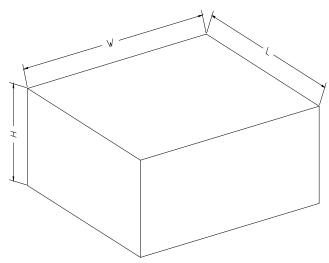
DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7"	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18