SGM12024A
0.4GHz to 5.0GHz, DP4T Switch with MIPI RFFE Interface

GENERAL DESCRIPTION

The SGM12024A is a dual-pole/four-throw (DP4T) addressable switch, which supports a wide operating frequency from 0.4GHz to 5.0GHz. The device provides low insertion loss and high isolation performance. These specifications make the device appropriate for 2G/3G/4G/5G applications, which need high power processing and high linearity.

The device has the ability to integrate serial control system compatible with RFFE standard. Internal driver and decoder for switch control signals are offered by the controller, which makes it flexible in RF path routing and bands selection.

No external DC blocking capacitors required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM12024A is available in a Green UTQFN-2×2-16AL package.

APPLICATIONS

Antenna Swapping
5G SRS Applications

FEATURES

- **Operating Frequency Range: 0.4GHz to 5.0GHz**
- **Low Insertion Loss**
- **Input 0.1dB Compression Point: 38dBm**
- **High Isolation**
- **MIPI RFFE V2.1 Interface Compatible**
- **No External DC Blocking Capacitors Required**
- **Available in a Green UTQFN-2×2-16AL Package**

BLOCK DIAGRAM

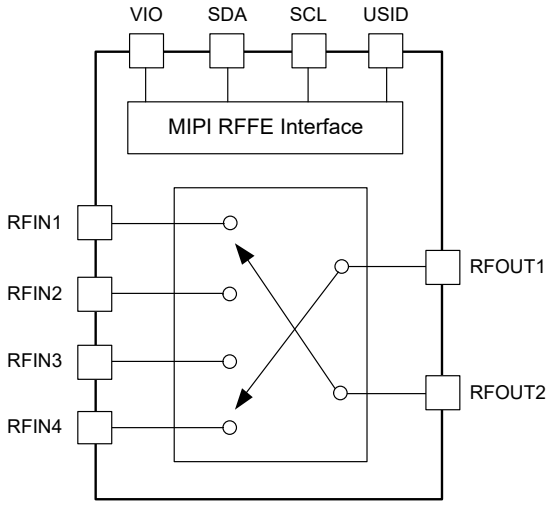


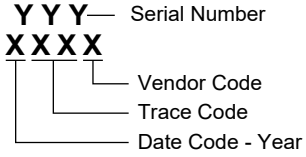
Figure 1. SGM12024A Block Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM12024A	UTQFN-2×2-16AL	-40℃ to +85℃	SGM12024AYURT16G/TR	017 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IO} 2.5V
SDA, SCL and USID Control Voltage 2.5V
RF Input Power, P_{IN} ..... 38dBm (f_0 = 0.4GHz to 5.0GHz)
Junction Temperature ..... +150℃
Storage Temperature Range ..... -55℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±1500V
CDM ..... ±2000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃
Operating Frequency Range ..... 0.4GHz to 5.0GHz
Supply Voltage, V_{IO} ..... 1.65V to 1.95V
SDA, SCL RFFE Bus High Voltage ..... (0.8 × V_{IO}) to V_{IO}
SDA, SCL RFFE Bus Low Voltage ..... 0V to (0.2 × V_{IO})
RFFE USID Voltage, V_{USID} ..... 0V to V_{IO}

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

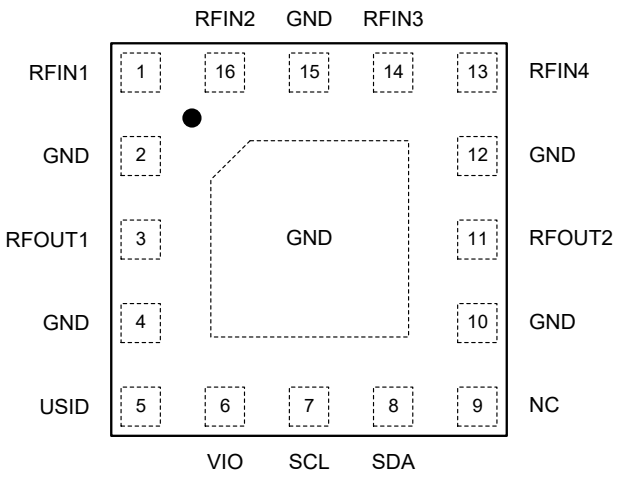
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTQFN-2×2-16AL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	RFIN1	RFIN Port 1.
2, 4, 10, 12, 15	GND	Ground.
3	RFOUT1	RFOUT Port 1.
5	USID	RFFE USID Select Pin.
6	VIO	Supply Voltage.
7	SCL	RFFE Clock Signal.
8	SDA	RFFE Data Signal.
9	NC	No Connection.
11	RFOUT2	RFOUT Port 2.
13	RFIN4	RFIN Port 4.
14	RFIN3	RFIN Port 3.
16	RFIN2	RFIN Port 2.
Exposed Pad	GND	Ground.

FUNCTION CHARACTERISTICS

Table 1. Register Mapping for RF Operating Modes

Register0	Output Switching Control Register							
Patch	D7	D6	D5	D4	D3	D2	D1	D0
DPDT Direct DP4T Direct (Default)	x	x	x	x	x	x	x	0
DP4T Cross	x	x	x	x	x	x	x	1

REGISTER TRUTH TABLE

Table 2. Register Truth Table (Register0[0] = 0)

State	Mode		Register1 (DP4T Switching Control Register)							
			D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation mode	Isolation mode	x	x	0	0	0	0	0	0
2	RFIN1 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	0	0	0	0	0	1
3	RFIN1 to RFOUT1; RFIN2 to RFOUT2	Dual through mode	x	x	0	1	0	0	1	1
4	RFIN1 to RFOUT1; RFIN3 to RFOUT2	Dual through mode	x	x	0	1	0	1	0	1
5	RFIN1 to RFOUT1; RFIN4 to RFOUT2	Dual through mode	x	x	0	1	1	0	0	1
6	RFIN2 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	0	0	0	0	1	0
7	RFIN2 to RFOUT1; RFIN1 to RFOUT2	Dual through mode	x	x	1	0	0	0	1	1
8	RFIN2 to RFOUT1; RFIN3 to RFOUT2	Dual through mode	x	x	0	1	0	1	1	0
9	RFIN2 to RFOUT1; RFIN4 to RFOUT2	Dual through mode	x	x	0	1	1	0	1	0
10	RFIN3 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	0	0	0	1	0	0
11	RFIN3 to RFOUT1; RFIN1 to RFOUT2	Dual through mode	x	x	1	0	0	1	0	1
12	RFIN3 to RFOUT1; RFIN2 to RFOUT2	Dual through mode	x	x	1	0	0	1	1	0
13	RFIN3 to RFOUT1; RFIN4 to RFOUT2	Dual through mode	x	x	0	1	1	1	0	0
14	RFIN4 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	0	0	1	0	0	0
15	RFIN4 to RFOUT1; RFIN1 to RFOUT2	Dual through mode	x	x	1	0	1	0	0	1
16	RFIN4 to RFOUT1; RFIN2 to RFOUT2	Dual through mode	x	x	1	0	1	0	1	0
17	RFIN4 to RFOUT1; RFIN3 to RFOUT2	Dual through mode	x	x	1	0	1	1	0	0
18	RFIN1 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	1	1	0	0	0	1
19	RFIN2 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	1	1	0	0	1	0
20	RFIN3 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	1	1	0	1	0	0
21	RFIN4 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	1	1	1	0	0	0

REGISTER TRUTH TABLE (continued)

Table 3. Register Truth Table (Register0[0] = 1)

State	Mode		Register1 (DP4T Switching Control Register)							
			D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation mode	Isolation mode	x	x	0	0	0	0	0	0
2	RFIN1 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	0	0	0	0	0	1
3	RFIN1 to RFOUT2; RFIN2 to RFOUT1	Dual through mode	x	x	0	1	0	0	1	1
4	RFIN1 to RFOUT2; RFIN3 to RFOUT1	Dual through mode	x	x	0	1	0	1	0	1
5	RFIN1 to RFOUT2; RFIN4 to RFOUT1	Dual through mode	x	x	0	1	1	0	0	1
6	RFIN2 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	0	0	0	0	1	0
7	RFIN2 to RFOUT2; RFIN1 to RFOUT1	Dual through mode	x	x	1	0	0	0	1	1
8	RFIN2 to RFOUT2; RFIN3 to RFOUT1	Dual through mode	x	x	0	1	0	1	1	0
9	RFIN2 to RFOUT2; RFIN4 to RFOUT1	Dual through mode	x	x	0	1	1	0	1	0
10	RFIN3 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	0	0	0	1	0	0
11	RFIN3 to RFOUT2; RFIN1 to RFOUT1	Dual through mode	x	x	1	0	0	1	0	1
12	RFIN3 to RFOUT2; RFIN2 to RFOUT1	Dual through mode	x	x	1	0	0	1	1	0
13	RFIN3 to RFOUT2; RFIN4 to RFOUT1	Dual through mode	x	x	0	1	1	1	0	0
14	RFIN4 to RFOUT2; RFOUT1 Isolation	Single through mode	x	x	0	0	1	0	0	0
15	RFIN4 to RFOUT2; RFIN1 to RFOUT1	Dual through mode	x	x	1	0	1	0	0	1
16	RFIN4 to RFOUT2; RFIN2 to RFOUT1	Dual through mode	x	x	1	0	1	0	1	0
17	RFIN4 to RFOUT2; RFIN3 to RFOUT1	Dual through mode	x	x	1	0	1	1	0	0
18	RFIN1 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	1	1	0	0	0	1
19	RFIN2 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	1	1	0	0	1	0
20	RFIN3 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	1	1	0	1	0	0
21	RFIN4 to RFOUT1; RFOUT2 Isolation	Single through mode	x	x	1	1	1	0	0	0

NOTE: x = Either 0 or 1.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{IO} = 1.65V to 1.95V, typical values are at V_{IO} = 1.8V, V_{IH} = 1.8V, V_{IL} = 0V, P_{IN} = 0dBm, VSWR = 1:1, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Supply Voltage	V_{IO}		1.65	1.8	1.95	V
Supply Current	I_{VIO}			150	203	μA
Turn-On Time	t_{ON}	50% V_{DD} to 90% RF			10	μs
RF Path Switching Time (One on Path to Another)	t_{SW}	Switching CMD 50% SCL to 90%/10% RF		2	3	μs
Wake Up Time	t_{WK}	Switching CMD 50% SCL to 90%/10% RF			10	μs
VIO Reset Time	t_{RST}	V_{IO} off to it starts to re-power up	10			μs
RF Characteristics						
Insertion Loss (RFINx to RFOUTx)	IL	f_0 = 0.4GHz to 0.9GHz		0.50	0.6	dB
				0.50	0.85 (1)	
		f_0 = 0.9GHz to 1.9GHz		0.56	0.65	
				0.56	0.95 (1)	
		f_0 = 1.9GHz to 2.7GHz		0.64	0.8	
				0.64	1.20 (1)	
		f_0 = 3.0GHz to 3.8GHz		0.84	1.1	
				0.84	1.45 (1)	
		f_0 = 4.0GHz to 5.0GHz		0.94	1.3	
				0.94	1.65 (1)	
Isolation (Dual through Mode, No-Adjacent Ports)	ISO	f_0 = 0.4GHz to 0.9GHz	35	49		dB
			31 (1)	49		
		f_0 = 0.9GHz to 1.9GHz	30	44		
			25 (1)	44		
		f_0 = 1.9GHz to 2.7GHz	26	41		
			22 (1)	41		
		f_0 = 3.0GHz to 3.8GHz	24	37		
			20 (1)	37		
		f_0 = 4.0GHz to 5.0GHz	20	31		
			16 (1)	31		
Isolation (Dual through Mode, Adjacent Ports)	ISO	f_0 = 0.4GHz to 0.9GHz	33	37		dB
			31 (1)	37		
		f_0 = 0.9GHz to 1.9GHz	28	33		
			25 (1)	33		
		f_0 = 1.9GHz to 2.7GHz	24	31		
			22 (1)	31		
		f_0 = 3.0GHz to 3.8GHz	23	26		
			20 (1)	26		
		f_0 = 4.0GHz to 5.0GHz	19	24		
			16 (1)	24		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = +25℃, V_{IO} = 1.65V to 1.95V, typical values are at V_{IO} = 1.8V, V_{IH} = 1.8V, V_{IL} = 0V, P_{IN} = 0dBm, VSWR = 1:1, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Return Loss (RFINx to RFOUTx)	RL	f_0 = 0.4GHz to 0.9GHz		26		dB
		f_0 = 0.9GHz to 1.9GHz		22		
		f_0 = 1.9GHz to 2.7GHz		21		
		f_0 = 3.0GHz to 3.8GHz		18		
		f_0 = 4.0GHz to 5.0GHz		10		
Input 0.1dB Compression Point (RFINx to RFOUTx)	$P_{0.1dB}$	f_0 = 0.4GHz to 2.7GHz, CW		38		dBm
		f_0 = 3.0GHz to 5.0GHz, CW		36		
2nd Harmonic	$2f_0$	f_0 = 900MHz at 35dBm		-51		dBm
3rd Harmonic	$3f_0$			-41		dBm
2nd Harmonic	$2f_0$	f_0 = 900MHz at 33dBm		-63		dBm
3rd Harmonic	$3f_0$			-59		dBm
2nd Harmonic	$2f_0$	f_0 = 1800MHz at 25dBm		-72		dBm
3rd Harmonic	$3f_0$			-65		dBm
2nd Harmonic	$2f_0$	f_0 = 1800MHz at 33dBm		-54		dBm
3rd Harmonic	$3f_0$			-63		dBm
IIP2	IIP2	f_0 = 1950MHz at 20dBm, f_1 = 4090MHz at -15dBm		110		dBm
IIP3	IIP3	f_0 = 1950MHz at 20dBm, f_1 = 1760MHz at -15dBm		70		dBm

NOTE:

1. The data contain the worst-case values after reliability verification.

MIPI RFFE READ AND WRITE TIMING

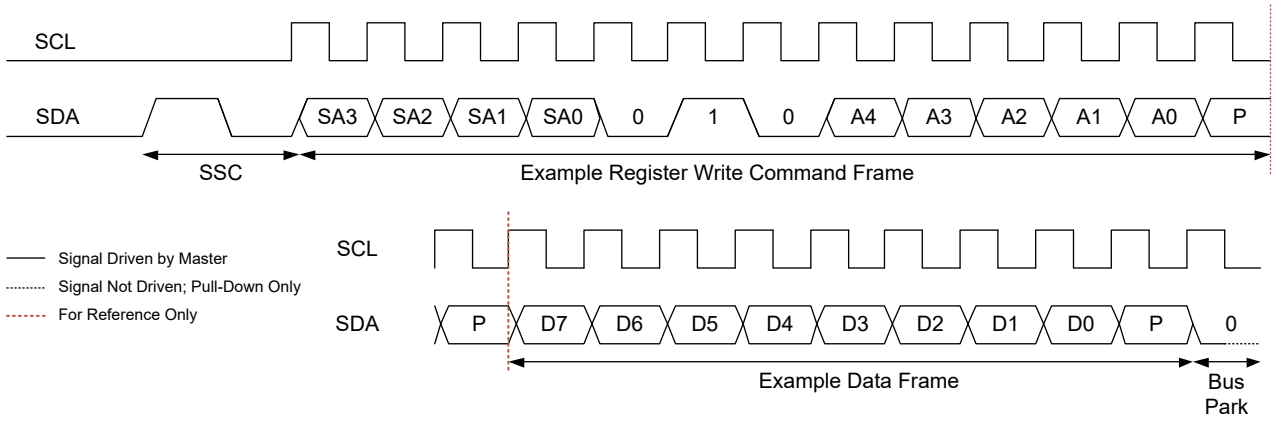


Figure 2. Register Write Command Timing Diagram

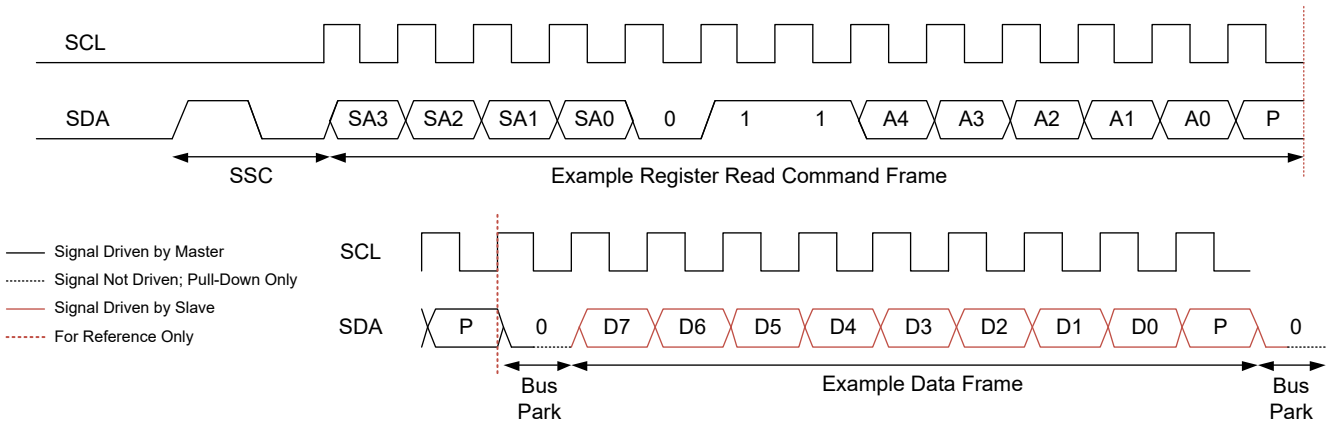


Figure 3. Register Read Command Timing Diagram

COMMAND SEQUENCE BIT DEFINITIONS

Type	SSC	Command Frame Bits					Parity Bits	Bus Park Cycle	Extended Operation					
		C[11:8]	C[7]	C[6:5]	C[4]	C[3:0]			Data Frame Bits	Parity Bits	Bus Park Cycle	Data Frame Bits	Parity Bits	Bus Park Cycle
Reg Write	Y	SA[3:0]	0	10	A[4]	A[3:0]	Y	-	D[7:0]	Y	Y	-	-	-
Reg Read	Y	SA[3:0]	0	11	A[4]	A[3:0]	Y	Y	D[7:0]	Y	Y	-	-	-
Reg0 Write	Y	SA[3:0]	1	D[6:5]	D[4]	D[3:0]	Y	Y	-	-	-	-	-	-

Legends:

SSC = Sequence Start Command

SA = Slave Address

A = Register Address

D = Data Bit

REGISTER MAPS

Register_0

Register Address: 0x00; R/W

Table 4. Register_0 Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MODE_CTRL0	See Table 2 and Table 3 section.	00000000	R/W	No	0, 1, 2

Register_1

Register Address: 0x01; R/W

Table 5. Register_1 Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MODE_CTRL1	See Table 2 and Table 3 section.	00000000	R/W	No	0, 1, 2

RFFE_STATUS

Register Address: 0x1A; R/W

Table 6. RFFE_STATUS Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7]	SOFTWARE_RESET	0: Normal 1: Software reset During software reset, this register and all configurable registers are set to their default values except for reserved registers.	0	R/W	No	No
D[6]	COMMAND_FRAME_ PARITY_ERR	Command frame parity error.	0	R/W	No	No
D[5]	COMMAND_LENGTH_ERR	Command length error.	0	R/W	No	No
D[4]	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error.	0	R/W	No	No
D[3]	DATA_FRAME_ PARITY_ERR	Data frame parity error.	0	R/W	No	No
D[2]	RD_IVD_ADD	Read command to an invalid address.	0	R/W	No	No
D[1]	WR_IVD_ADD	Write command to an invalid address.	0	R/W	No	No
D[0]	BID_GID_ERR	Read command with a BROADCAST_ID or GSID. When this register is read, it will reset.	0	R/W	No	No

GROUP_SID

Register Address: 0x1B; R and R/W

Table 7. GROUP_SID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:4]	Reserved	Reserved.	0000	R	No	No
D[3:0]	GSID	Group slave ID.	0000	R/W	No	No

REGISTER MAPS (continued)

PM_TRIG

Register Address: 0x1C; R/W and W

Table 8. PM_TRIG Register Details

Bits	Bit Name	Description		Default	Type	B/G	Trig
D[7]	PWR_MODE_1	0: Normal 1: Low power		0	R/W	Yes	No
D[6]	PWR_MODE_0	0: Active - Normal 1: Startup - All registers are reset to the default		0	R/W	Yes	No
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled	If any one of the three TRIGGER_MASK_x is set to logic '1', the corresponding trigger is disabled, in that case data written to a register associated with the trigger goes directly to the destination register. Otherwise, if the TRIGGER_MASK_x is set to logic '0', incoming data is written to the shadow register, and the destination register is unchanged until its corresponding trigger is asserted.	0	R/W	No	No
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled		0	R/W	No	No
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled 1: TRIGGER_0 disabled		0	R/W	No	No
D[2]	TRIGGER_2	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'		0	W	Yes	No
D[1]	TRIGGER_1	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'		0	W	Yes	No
D[0]	TRIGGER_0	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'		0	W	Yes	No

PRODUCT_ID

Register Address: 0x1D; R

Table 9. PRODUCT_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	PRODUCT_ID	Product number.	00000101	R	No	No

MANUFACTURER_ID

Register Address: 0x1E; R

Table 10. MANUFACTURER_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MANUFACTURER_ID[7:0]	Lower eight bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	01001010	R	No	No

MAN_USID

Register Address: 0x1F; R and R/W

Table 11. MAN_USID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:4]	MANUFACTURER_ID[11:8]	Upper four bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	0000	R	No	No
D[3:0]	USID	USID pin connected to GND.	1010	R/W	No	No
		USID pin connected to VIO.	1011			

POWER ON AND OFF SEQUENCE

Once the VIO voltage drops to 0V, the VIO waits at least 10μs before repowering (see Figure 4).

In order to ensure the correct data transmission, SDA/SCL must be sent after VIO has been applied at least 120ns. There must be at least 15μs to apply RF power after VIO has been applied. Wait a minimum of typically 10μs after RFFE bus is idle to apply an RF signal (see Figure 5).

Do not apply RF power during switching. To ensure this, the RF power needs to be removed before the register write operation that changes the switching mode is completed (see Figure 6).

When the low power mode is used, a delay time of 10μs is required to exit the low power mode (see Figure 7).

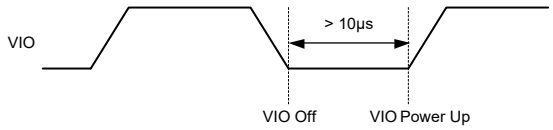


Figure 4. Digital Supply Detail

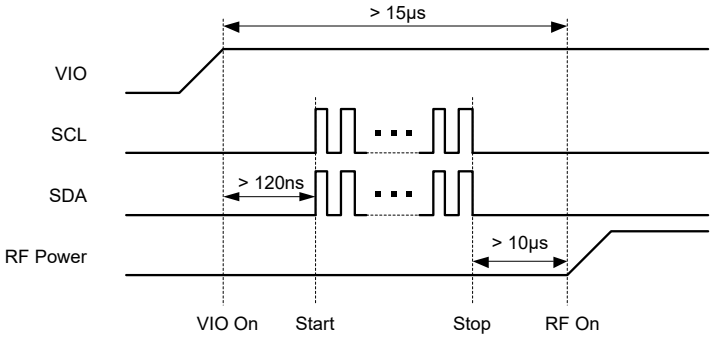


Figure 5. Digital Signal/RF Power-On Detail

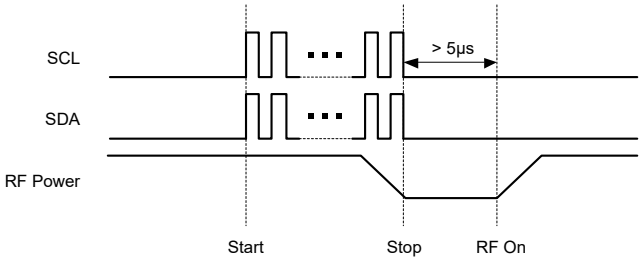


Figure 6. Switch Event Timing

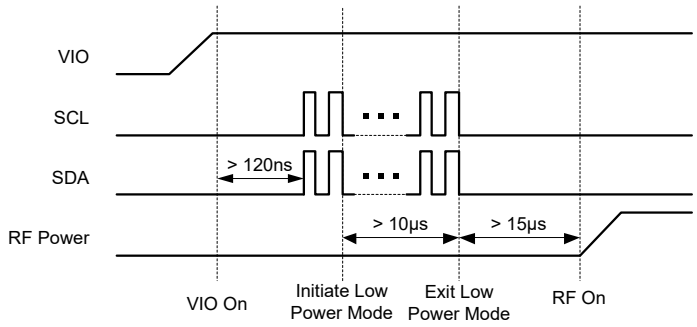
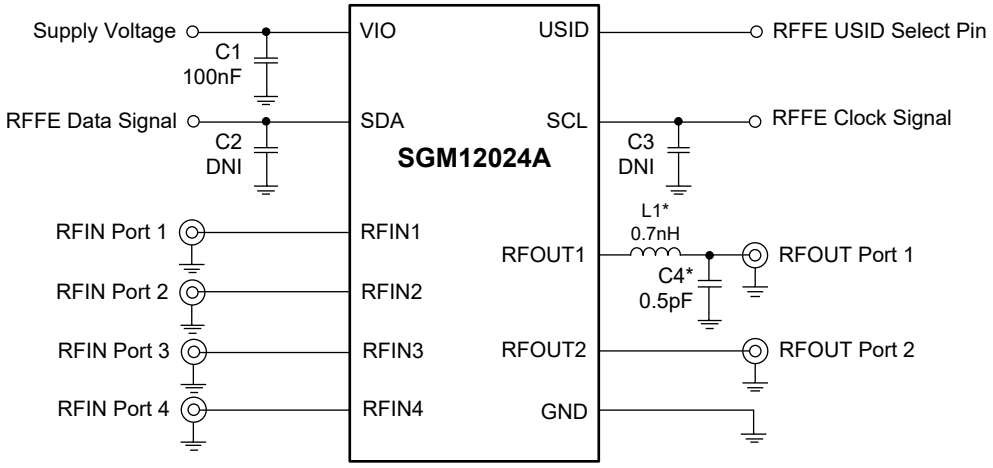


Figure 7. Low Power Mode Exit Timing

TYPICAL APPLICATION CIRCUIT



NOTE: * Matching for optimized RF performance, it may be changed according to different applications.

Figure 8. SGM12024A Typical Application Circuit

EVALUATION BOARD LAYOUT

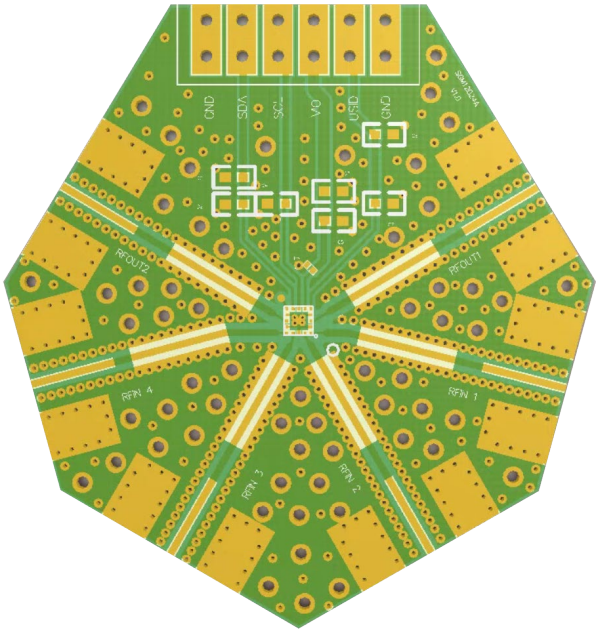


Figure 9. SGM12024A Evaluation Board Layout

REVISION HISTORY

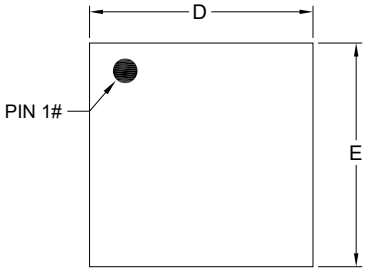
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2025 – REV.A to REV.A.1	Page
Updated Electrical Characteristics	4, 5

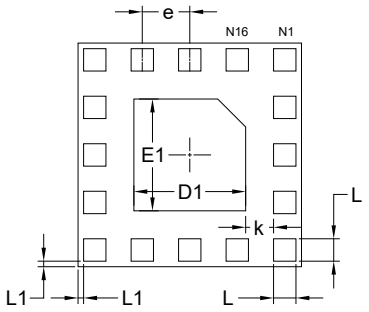
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

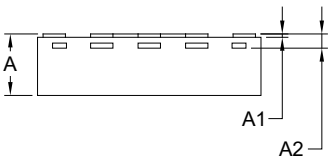
UTQFN-2×2-16AL



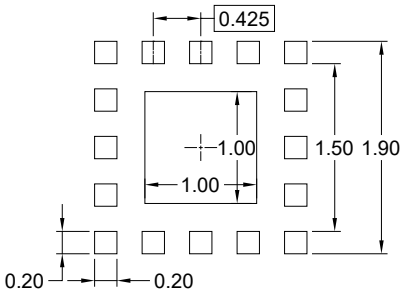
TOP VIEW



BOTTOM VIEW



SIDE VIEW



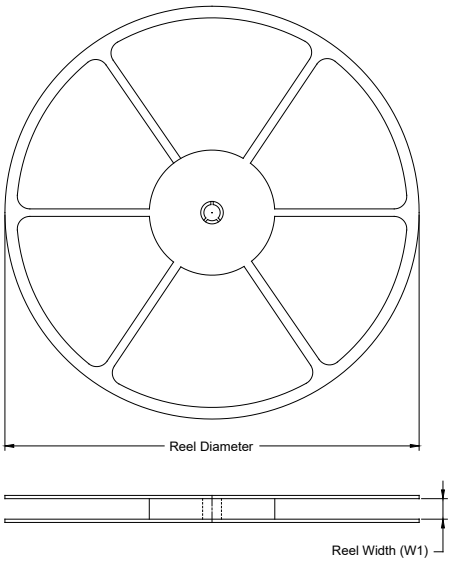
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	-	0.050
A2	0.127 REF		
D	1.900	2.000	2.100
D1	0.900	1.000	1.100
E	1.900	2.000	2.100
E1	0.900	1.000	1.100
e	0.425 BSC		
k	0.150	-	-
L	0.150	0.200	0.250
L1	0.000	0.050	0.100

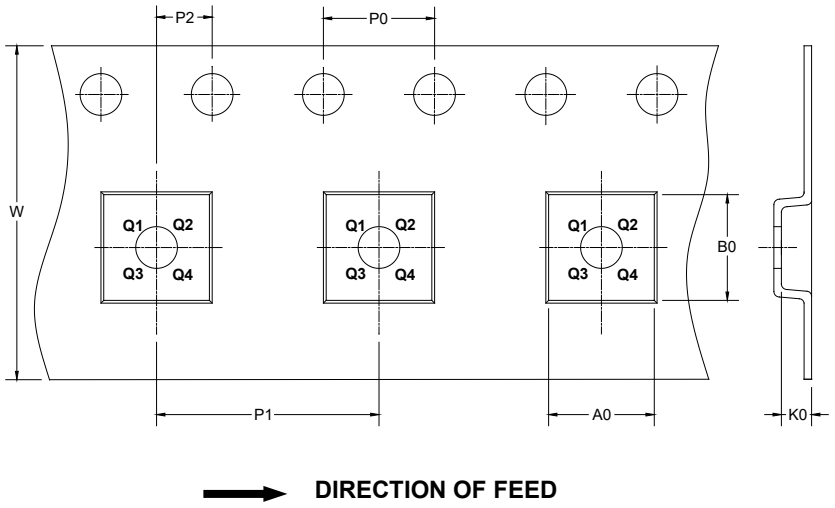
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



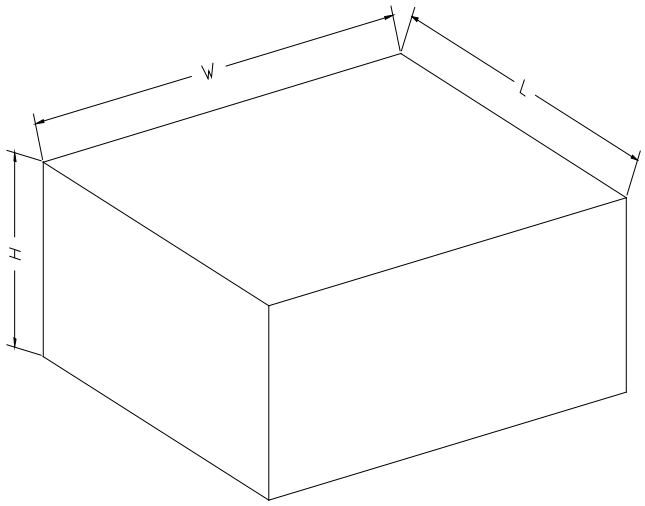
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-2×2-16AL	7″	9.5	2.25	2.25	0.75	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002