



SGM2562Q

5.5V, 2A, 53mΩ On-Resistance Load Switch for Automotive Applications

GENERAL DESCRIPTION

The SGM2562Q is a small single channel load switch. The switch operates from a wide range of 1.2V to 5.5V input supply voltage. It can provide a 2A maximum continuous switch current.

The rise time of V_{OUT} can be adjusted by setting an additional capacitor to the SS pin and used to avoid inrush current.

The SGM2562Q has a quick output discharge (QOD) function that controls the device's fall time, allowing for flexibility power down sequencing.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM2562Q is available in a Green SOT-23-6 package.

FEATURES

- AEC-Q100 Qualified for Automotive Applications Device Temperature Grade 1
 $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
- Single Channel Load Switch
- Input Voltage Range: 1.2V to 5.5V
- On-Resistance: 53mΩ (TYP) at $V_{IN} = 3.3\text{V}$
- Low Quiescent Current: 3μA (TYP) at $V_{IN} = 3.3\text{V}$
- Low-Control Input Threshold Enables Use of 1V or Higher GPIO
- Adjustable Quick Output Discharge (QOD)
- Adjustable Rise Time with SS Pin
- Maximum Continuous Current: 2A
- Available in a Green SOT-23-6 Package

APPLICATIONS

Industrial Systems
Set-Top Boxes
Blood Glucose Meters
Electronic Point of Sale
Automotive Applications

TYPICAL APPLICATION

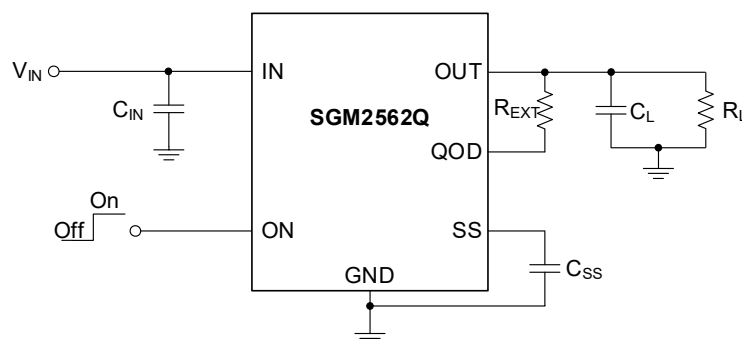


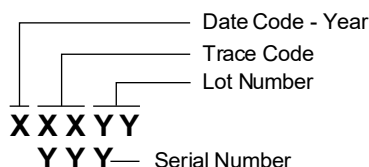
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2562Q	SOT-23-6	-40°C to +125°C	SGM2562QN6G/TR	XXXYY 21D	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXYY = Date Code, Trace Code and Lot Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN}	-0.3V to 6V
ON Pin Voltage, V_{ON}	-0.3V to 6V
Output Voltage, V_{OUT}	-0.3V to 6V
Maximum Continuous Switch Current, $T_J = +47^\circ\text{C}$, I_{MAX}	2A
Package Thermal Resistance	
SOT-23-6, θ_{JA}	147.1°C/W
SOT-23-6, θ_{JB}	37.7°C/W
SOT-23-6, θ_{JC}	81.3°C/W
Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (Soldering, 10s).....	+260°C
ESD Susceptibility ^{(1) (2)}	
HBM.....	±4000V
CDM.....	±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.
2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Voltage, V_{IN}	1.2V to 5.5V
ON Pin Voltage, V_{ON}	0V to 5.5V
Output Voltage, V_{OUT}	V_{IN} (MAX)
ON Pin High Voltage Range, V_{IH}	0.8V to 5.5V
ON Pin Low Voltage Range, V_{IL}	0V to 0.3V
Input Capacitor, C_{IN}	≥ 1μF
Operating Junction Temperature Range.....	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

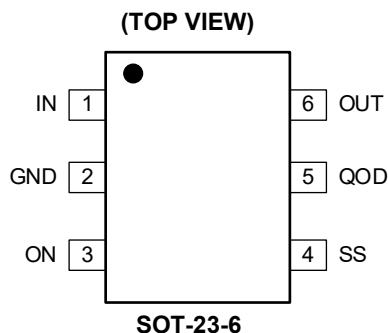
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	IN	I	Switch Input Pin. Use a bypass capacitor (C_{IN}) as close as possible between IN and GND pins.
2	GND	-	Ground.
3	ON	I	Switch Enable Input. Logic high sets the device active, logic low disables it and turns it into shutdown mode. Do not leave this pin floating.
4	SS	O	Slew Rate Control Pin. Connecting different capacitors allows configuration of different starting speed.
5	QOD	O	Three ways to configure the quick output discharge (QOD) pin: - External resistor mode: connect an external resistor between OUT and QOD pins. - Internal resistor mode: directly tie QOD to OUT pin, using the internal pull-down resistor (R_{PD}). - Disable QOD: leave the QOD pin unconnected.
6	OUT	O	Switch Output Pin.

NOTE: I = input, O = output.

ELECTRICAL CHARACTERISTICS(T_J = -40°C to +125°C, typical values are measured at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I _Q	V _{ON} = 5V, I _{OUT} = 0A	V _{IN} = 5.5V	4.2	12	μA
			V _{IN} = 3.3V	3.0	9	
			V _{IN} = 1.2V	1.1	6	
Shutdown Current	I _{SD}	V _{ON} = 0V, V _{OUT} = 0V	V _{IN} = 5.5V	0.3	1	μA
			V _{IN} = 3.3V	0.2	0.8	
			V _{IN} = 1.2V	0.1	0.6	
ON Pin Input Leakage Current	I _{ON}	V _{IN} = 5.5V, I _{OUT} = 0A, V _{ON} = 0V			0.1	μA
On-Resistance	R _{DS(ON)}	V _{IN} = 5.5V, I _{OUT} = -200mA		53	89	mΩ
		V _{IN} = 3.3V, I _{OUT} = -200mA		53	90	mΩ
		V _{IN} = 1.2V, I _{OUT} = -200mA		81	125	mΩ
ON Terminal Input Threshold	V _{IH}	Rising	0.8			V
	V _{IL}	Falling			0.3	
ON Pin Hysteresis	V _{HYS}	V _{IN} = 1.2V to 5.5V		27		mV
Output Pull-Down Resistance ⁽¹⁾	R _{PD}	V _{IN} = 5V, V _{ON} = 0V, I _{QOD} = 20mA		11	20	Ω
		V _{IN} = 3.3V, V _{ON} = 0V, I _{QOD} = 20mA		12	22	
		V _{IN} = 1.8V, V _{ON} = 0V, I _{QOD} = 20mA		19	32	

NOTE: 1. Output pull-down resistance varies with input voltage.

SWITCHING CHARACTERISTICS

 $V_{ON} = 5V$, $T_J = +25^\circ C$, QOD = open, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V _{IN} = 5V						
Turn-On Time	t _{ON}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		2185		μs
Turn-Off Time	t _{OFF}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		2.1		
V _{OUT} Rise Time	t _R	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		2400		
V _{OUT} Fall Time	t _F	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1.8		
Delay Time	t _D	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		940		
V _{IN} = 3.3V						
Turn-On Time	t _{ON}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1700		μs
Turn-Off Time	t _{OFF}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		2.4		
V _{OUT} Rise Time	t _R	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1560		
V _{OUT} Fall Time	t _F	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1.8		
Delay Time	t _D	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		860		
V _{IN} = 1.8V						
Turn-On Time	t _{ON}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1270		μs
Turn-Off Time	t _{OFF}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		3.1		
V _{OUT} Rise Time	t _R	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		970		
V _{OUT} Fall Time	t _F	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1.8		
Delay Time	t _D	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		760		
V _{IN} = 1.2V						
Turn-On Time	t _{ON}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1150		μs
Turn-Off Time	t _{OFF}	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		5		
V _{OUT} Rise Time	t _R	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		710		
V _{OUT} Fall Time	t _F	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		1.9		
Delay Time	t _D	C _{IN} = 1μF, C _L = 0.1μF, R _L = 10Ω, C _{SS} = 1nF		790		

PARAMETER MEASUREMENT INFORMATION

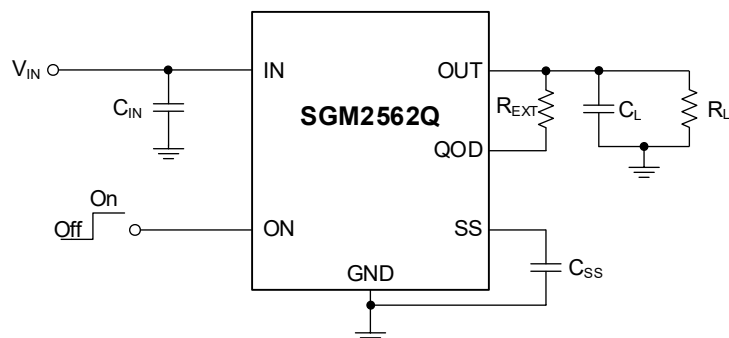


Figure 2. Test Circuit

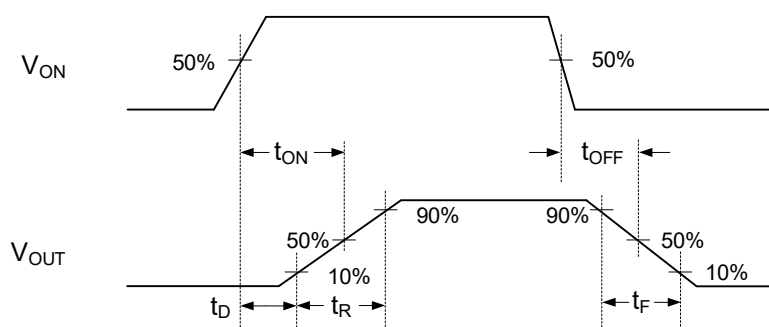


Figure 3. Turn-On and Turn-Off Waveforms

FUNCTIONAL BLOCK DIAGRAM

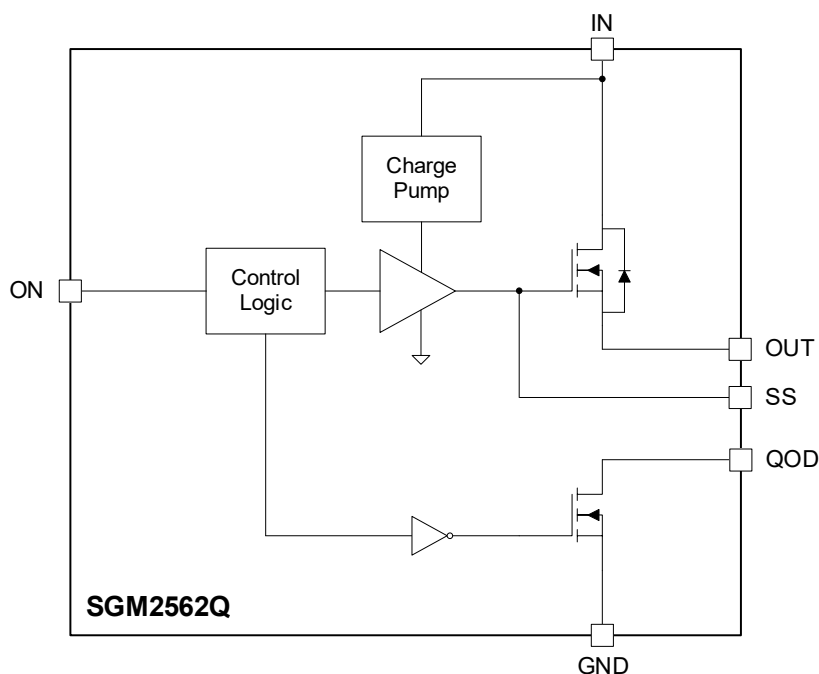
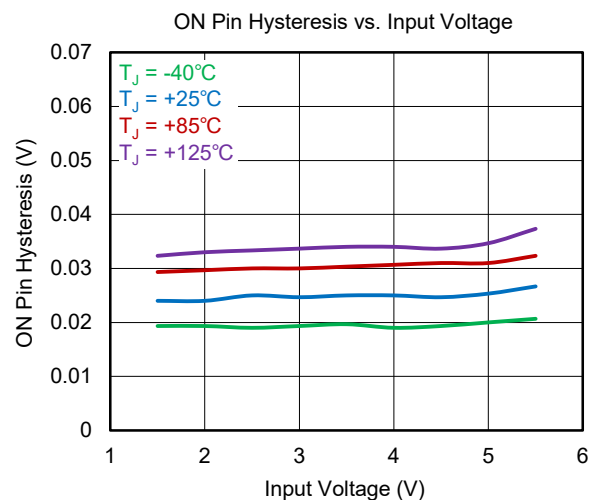
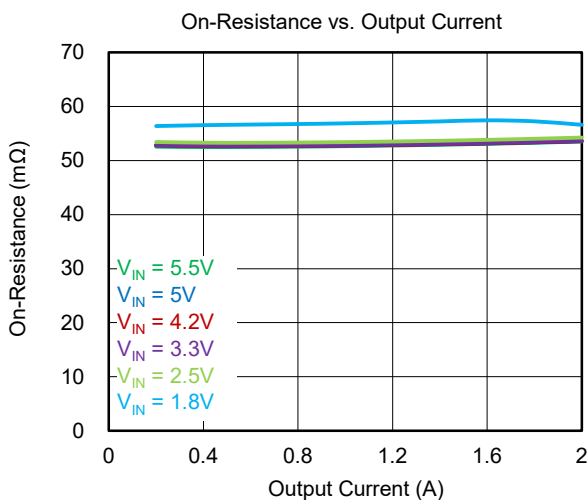
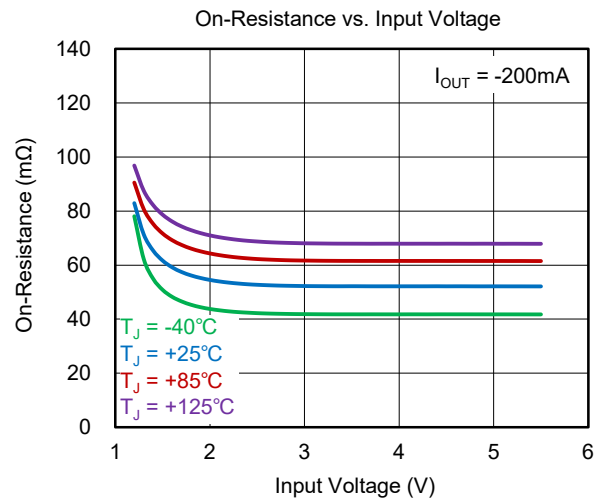
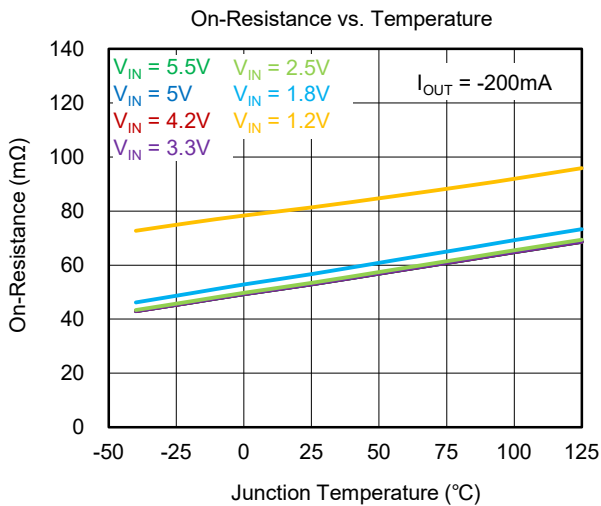
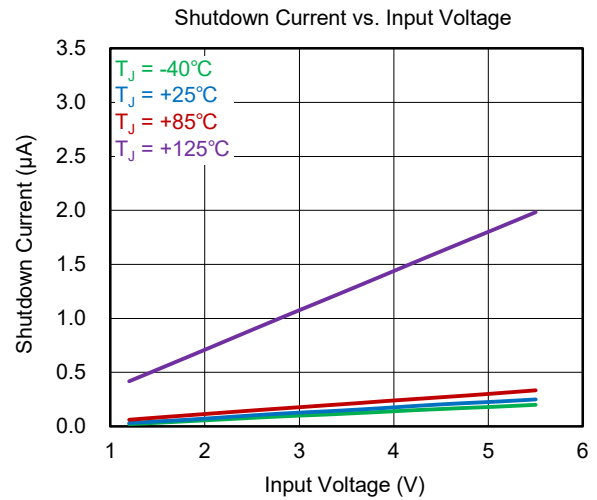
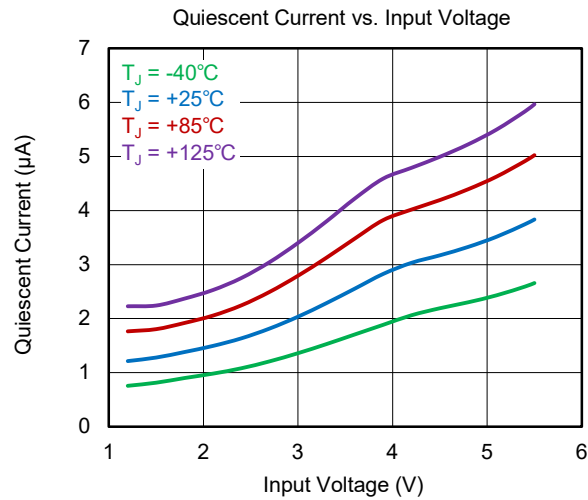


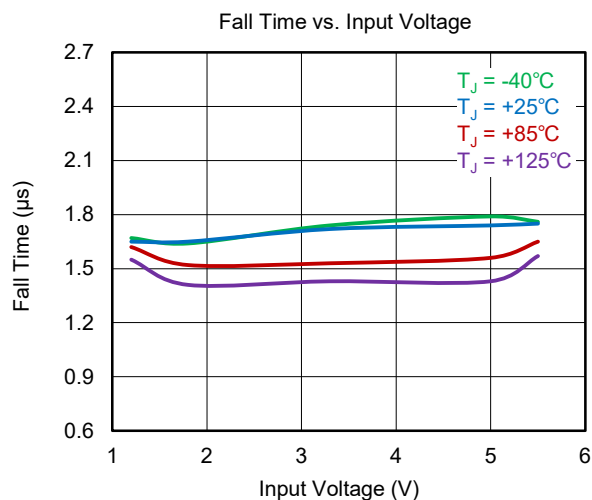
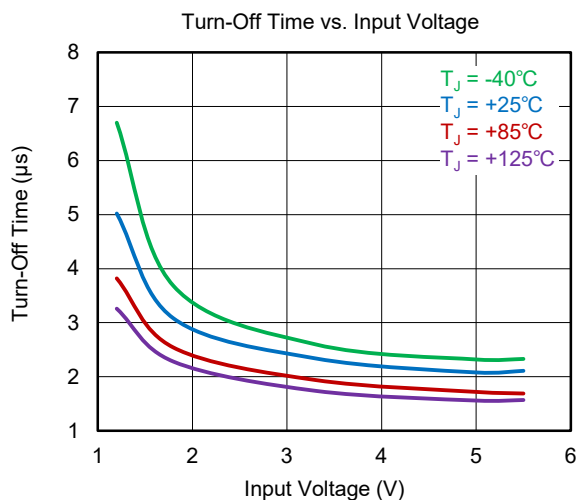
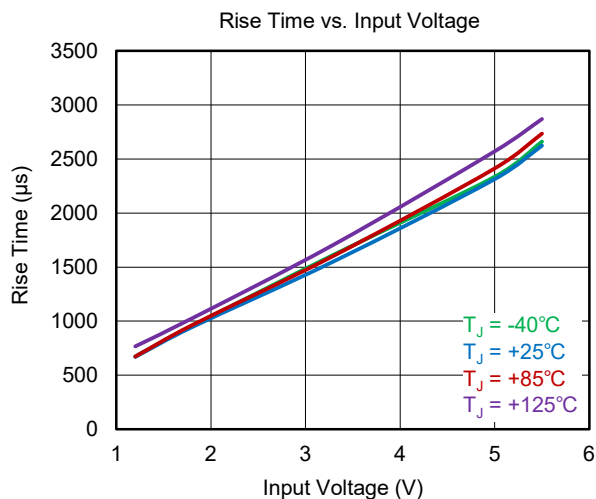
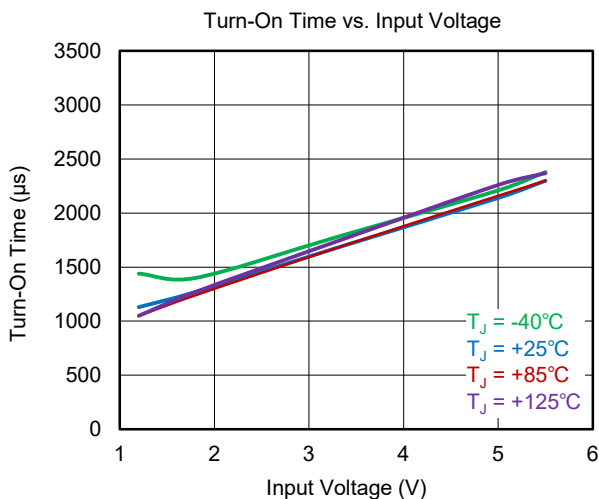
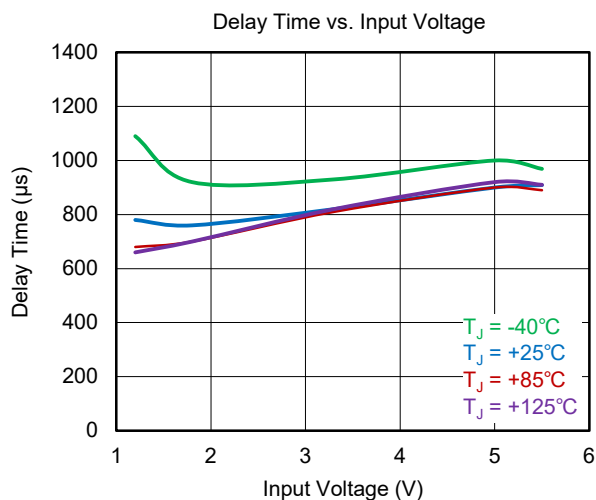
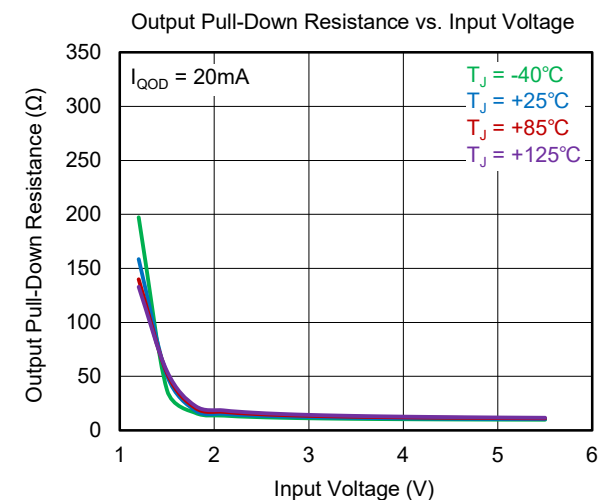
Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

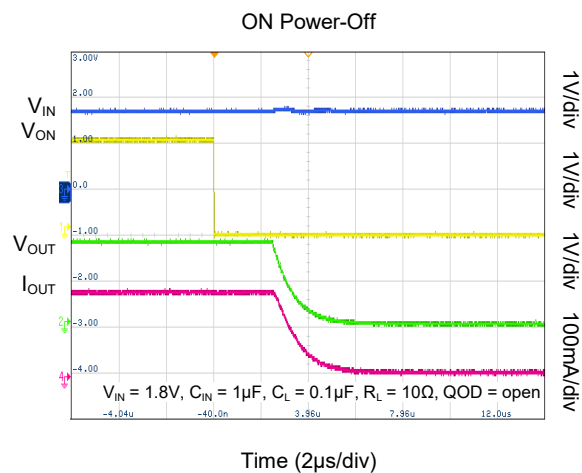
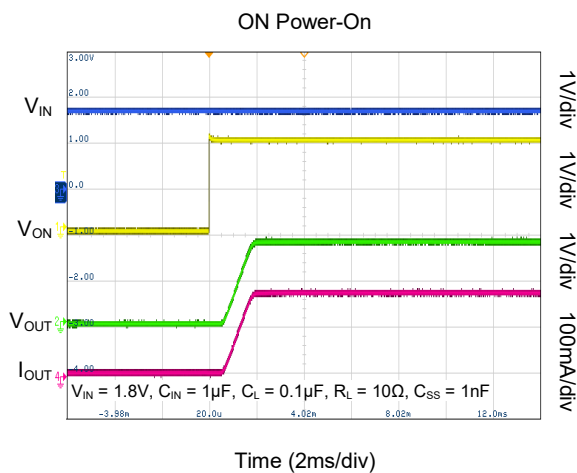
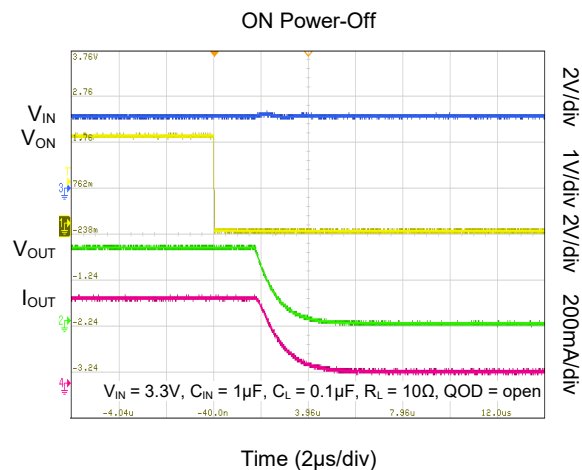
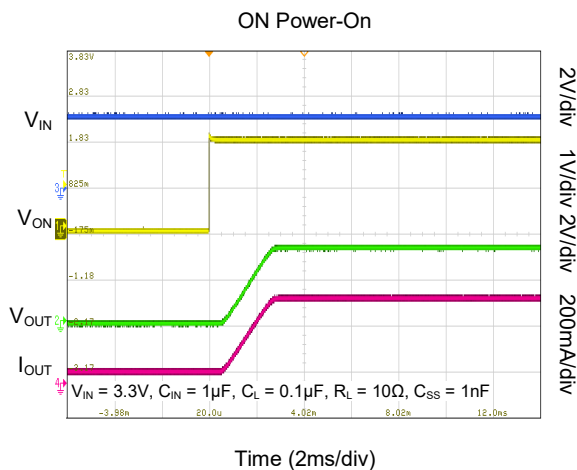
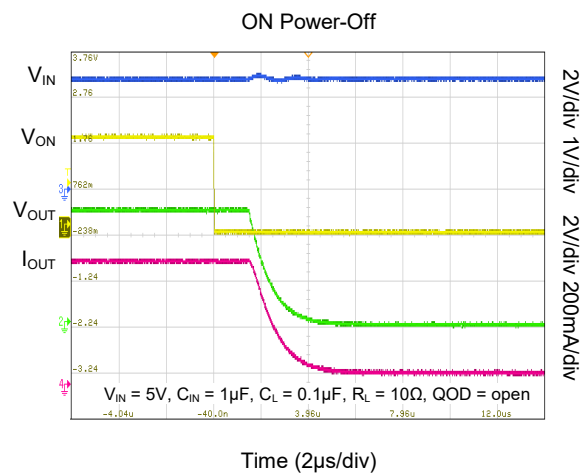
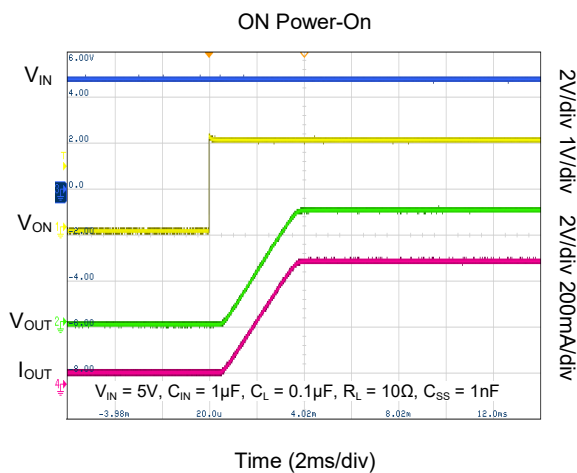
 $T_J = +25^\circ\text{C}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

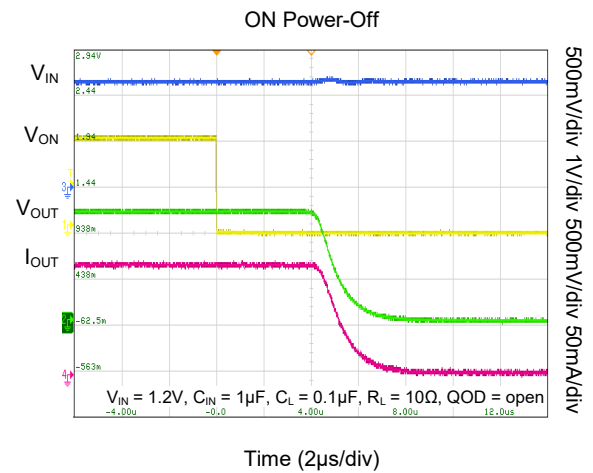
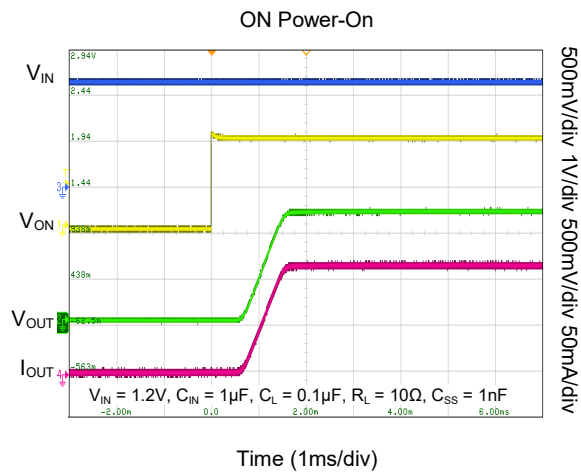
$T_J = +25^\circ\text{C}$, $C_{IN} = 1\mu\text{F}$, $C_L = 0.1\mu\text{F}$, $R_L = 10\Omega$, $C_{SS} = 1\text{nF}$, QOD = open, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 $T_J = +25^\circ\text{C}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

 $T_J = +25^\circ\text{C}$, unless otherwise noted.

DETAILED DESCRIPTION

Overview

The SGM2562Q is a 5.5V, integrated N-MOSFET, single-channel load switch. It can support a 2A maximum continuous load current and be enabled by the ON pin. The device also has adjustable quick output discharge (QOD) function to remove the remaining energy from the output when the switch is disabled.

The SGM2562Q is highly integrated. Using the device can reduce the PCB area and the BOM count greatly, even the cost.

Control Pin

There is a control pin ON to turn on or turn off the corresponding N-MOSFET. When the ON pin is driven high, the switch will be turned on, and when the ON pin is driven low, the switch will be turned off. The ON pin is compatible with standard GPIO logic level threshold, such as 1V or higher GPIO voltage.

The ON pin cannot be floating and must be connected to either high or low level as requirement.

Quick Output Discharge (QOD)

The QOD (quick output discharge) configuration options for the SGM2562Q as below:

1. Internal resistor mode: short QOD directly to OUT, using the internal pull-down resistor (R_{PD}) to discharge the output energy when switch is disabled. Discharge rate is controlled by the internal pull-down resistor (R_{PD}).

2. External resistor mode: connect QOD to OUT via an external resistor (R_{EXT}). Adjust R_{EXT} to fine-tune the discharge rate when switch is disabled. Total discharge resistance (R_{QOD}) is calculated as:

$$R_{QOD} = R_{PD} + R_{EXT} \quad (1)$$

where:

R_{QOD} is total output discharge resistance.

R_{PD} is internal pull-down resistance.

R_{EXT} is external resistance placed between the OUT and QOD pins.

3. Disable QOD: leave QOD floating, the output remains floating when switch is disabled.

When configuring the QOD pin is directly connecting to the OUT pin, special attention is required. The internal pull-down resistor (R_{PD}) is intended to provide a rapid discharge path for the load once the switch is turned off. It is important to prevent excessive current flow through R_{PD} during this discharge to avoid exceeding the maximum junction temperature rating of +125°C. If only the internal R_{PD} is used for discharging, the total connected capacitive load should not be greater than 200μF. If the load exceeds this value, an external resistor (R_{EXT}) must be introduced to limit the current passing through R_{PD} and keep the junction temperature within safe limits. Furthermore, to protect the device, the residual charge stored on the load capacitor (C_L) should dissipate naturally through the internal QOD resistor and must not be actively driven by an external source.

Table 1. QOD Fall Times

V_{IN} (V)	Fall Time ⁽¹⁾ (μs) 90% - 10%, $C_{IN} = 1\mu F$, $I_{OUT} = 0A$, $V_{ON} = 0V$		
	$T_J = +25^\circ C$		
	$C_L = 1\mu F$	$C_L = 10\mu F$	$C_L = 100\mu F$
5	31	171	2922
3.3	32	244	3161
2.5	36	283	5477
1.8	54	443	7658
1.2	170	1406	17510

NOTE: 1. Typical values with QOD shorted to OUT pin.

DETAILED DESCRIPTION (continued)**Table 2. Rise Time vs. C_{SS} Capacitor**

C _{SS} (pF)	Rise Time (μs) 10% - 90% ⁽¹⁾					
	V _{IN} = 5V	V _{IN} = 3.3V	V _{IN} = 2.5V	V _{IN} = 1.8V	V _{IN} = 1.5V	V _{IN} = 1.2V
0	150	135	115	105	100	90
220	675	580	335	255	220	180
470	1145	755	570	455	385	320
1000	2890	1780	1415	1070	890	760
2200	5470	3565	2895	2170	1820	1540
4700	11295	7710	5810	4670	3955	3280
10000	27310	16750	13225	10385	8565	7165

NOTE: 1. Typical values at T_J = +25°C, C_L = 0.1μF, C_{IN} = 1μF, R_L = 10Ω, with a 25V X7R 10% ceramic capacitor on SS.

Adjustable Rise Time (SS)

A capacitor between SS and GND pins determines the slew rate of V_{OUT}. The slew rate can be calculated using the below equation.

$$SR = 0.68 \times C_{SS} \quad (2)$$

where:

The units for the constant 0.68 are μs/(V × pF).

SR is the slew rate (in μs/V).

C_{SS} is the capacitance value on the SS pin (in pF).

This equation is based on the voltage transition from 10% to 90% on V_{OUT} and is not valid when C_{SS} = 0pF. For cases where C_{SS} = 0pF, please refer to Table 2 for the corresponding rise time values.

Rise time can also be estimated by dividing the input voltage by the slew rate. The rise times listed in Table 2 are derived from measurements taken on a typical device. The equation is for reference only, and the actual rise time of the device is subject to measurement.

Device Functional Modes

The connection of the OUT pin is shown in Table 3.

Table 3. OUT Connection

ON	QOD Configuration	OUT
L	QOD pin connected to OUT with R _{EXT}	GND (via R _{EXT} +R _{PD})
L	QOD pin tied to OUT directly	GND (via R _{PD})
L	QOD pin left open	Open
H	Any valid QOD configuration	IN

APPLICATION INFORMATION

Typical Application

This typical application demonstrates how the SGM2562Q can be used to power downstream modules.

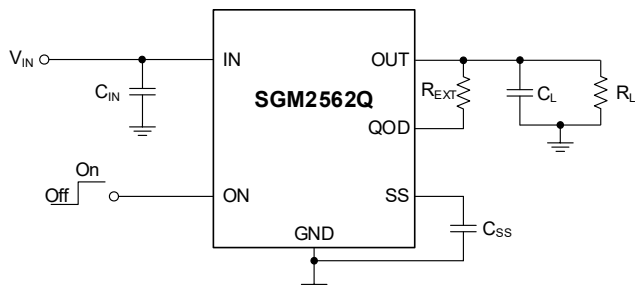


Figure 5. Typical Application Schematic

Design Requirements

Table 4 shows the SGM2562Q design parameters.

Table 4. Design Parameters

Design Parameter	Value
Input Voltage (V_{IN})	5V
Load Current	2A
Load Capacitance (C_L)	22μF
Desired Fall Time	4ms
Maximum Acceptable Inrush Current (I_{INRUSH})	400mA

Input Capacitor (C_{IN})

Turning on the N-MOSFET to charge load capacitor will generate inrush current, which may cause the V_{IN} drop. In order to prevent the drop, a capacitor must be placed between the IN and GND pins. Usually, a 1μF input capacitor (C_{IN}) placed close to the pins is sufficient. However, higher capacitance values could further reduce the voltage drop. So, larger C_{IN} can be used to reduce the voltage drop in high current applications.

Output Capacitor (C_L) (Optional)

A 0.1μF output capacitor (C_L) should be placed between OUT and GND close to the device pins. This capacitor will prevent parasitic board inductances from forcing OUT below GND when the switch is turned off. To improve the V_{IN} dropping when the device is turned on, it is recommended that C_{IN} is placed greater than C_L due to the C_{IN} is charge for C_L .

 V_{IN} to V_{OUT} Voltage Drop

The voltage drop from IN to OUT is determined by the on-resistance of the device and the load current. $R_{DS(on)}$ can be found in electrical specification. When the value

of $R_{DS(on)}$ is found, the following equation can be used to calculate the voltage drop across the device:

$$\Delta V = I_{LOAD} \times R_{DS(on)} \quad (3)$$

where ΔV is the voltage drop from input to output. I_{LOAD} is the load current. $R_{DS(on)}$ is the on-resistance of device determined by V_{IN} .

Inrush Current

This process causes the inrush current, and it can be calculated by Equation 4.

$$I_{INRUSH} = C_L \times dV/dt \quad (4)$$

where:

C_L is the output capacitance.

dV/dt is desired output slew rate.

The V_{OUT} rise time can be programmed. This function is used to control the inrush current during turn-on. The design requirements and inrush current equation can be used to calculate the appropriate rise time. See Equation 5 and Equation 6.

$$400mA = 22\mu F \times (80\% \times 5V)/dt \quad (5)$$

$$dt = 455\mu s \quad (6)$$

In order to ensure that the inrush current is less than 400mA, an appropriate C_{SS} capacitor should be selected to produce a rise time more than 455μs.

Layout Guidelines

Careful layout is always important to ensure good performance and stable operation to any kind of load switch.

- All traces should be as short as possible.
- Locate the input and output capacitors as close as possible to the device.
- Choose wide traces for IN, OUT and GND.

Thermal Considerations

Assuming a given ambient temperature and package thermal resistance, the maximum allowable power dissipation is calculated by:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (7)$$

where:

$P_{D(MAX)}$ is the maximum power dissipation.

$T_{J(MAX)}$ is the maximum operating junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package thermal resistance.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

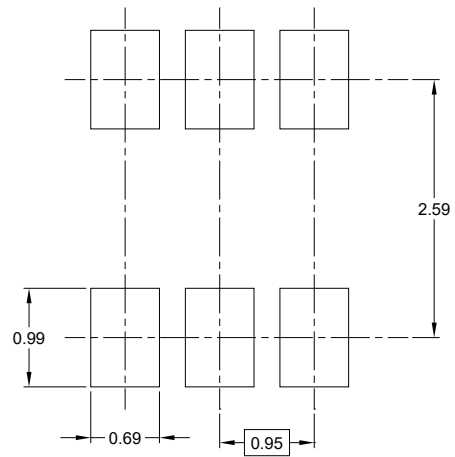
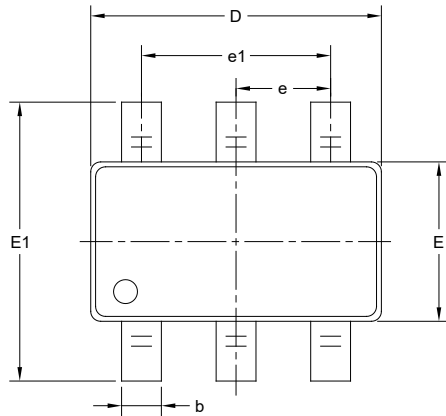
Changes from Original to REV.A (DECEMBER 2025)

Page

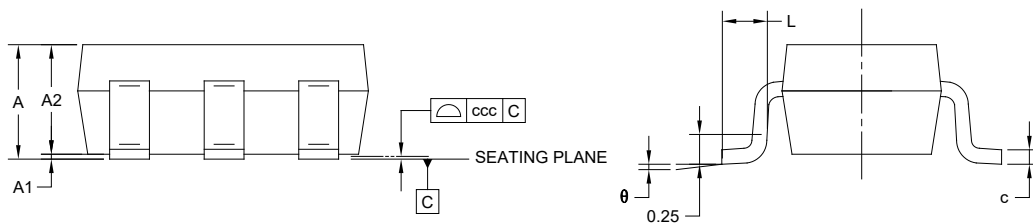
Changed from product preview to production data.....	All
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PACKAGE OUTLINE DIMENSIONS

SOT-23-6



RECOMMENDED LAND PATTERN (Unit: mm)



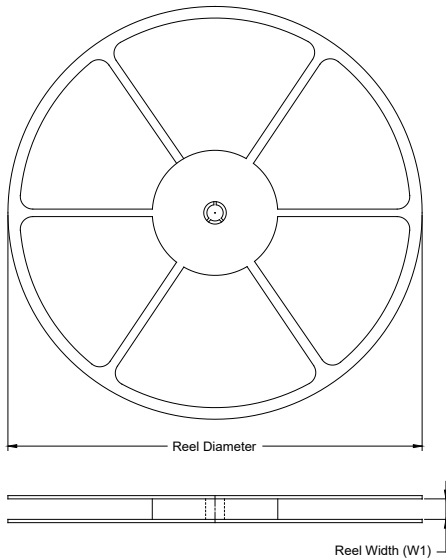
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:

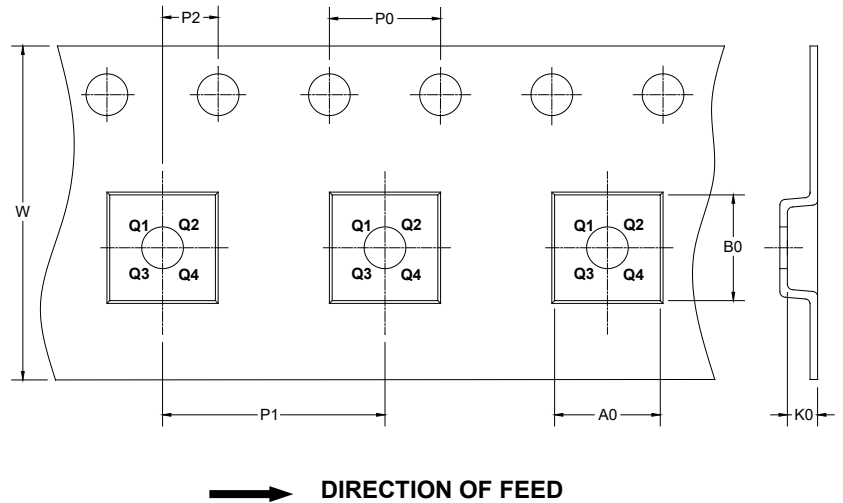
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

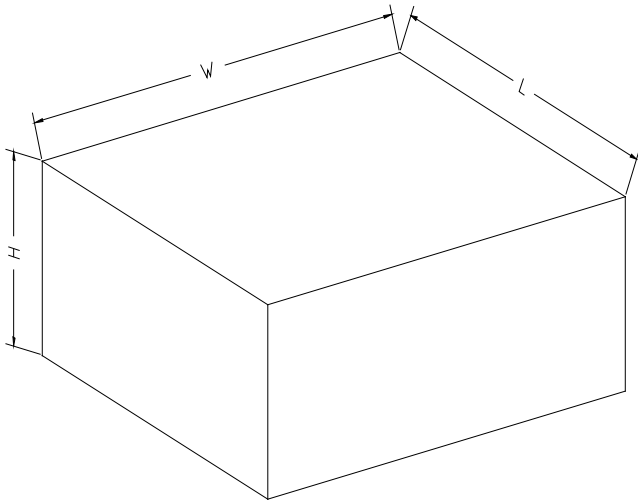
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002