SGM61410Q
1.2MHz, 600mA, 42V Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61410Q is a high frequency, synchronous Buck converter with integrated switches. It can deliver up to 600mA to the output over a wide input voltage range of 5V to 42V. The low 14μA quiescent current and ultra-low shutdown current of only 0.6μA make it a suitable choice for battery-powered applications.

SGM61410Q features high efficiency over a wide load range achieved by scaling down the switching frequency at light loads to reduce switching and gate driving losses. Other features include internal compensation, internal monotonic soft-start even with pre-biased output and fast loop response due to the peak-current mode controller.

Protection features include current limiting and short-circuit protection, thermal shutdown with auto recovery and output over-voltage protection. Frequency fold-back helps prevent inductor current runaway during startup.

This SGM61410Q is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

SGM61410Q is available in a Green SOT-23-6 package.

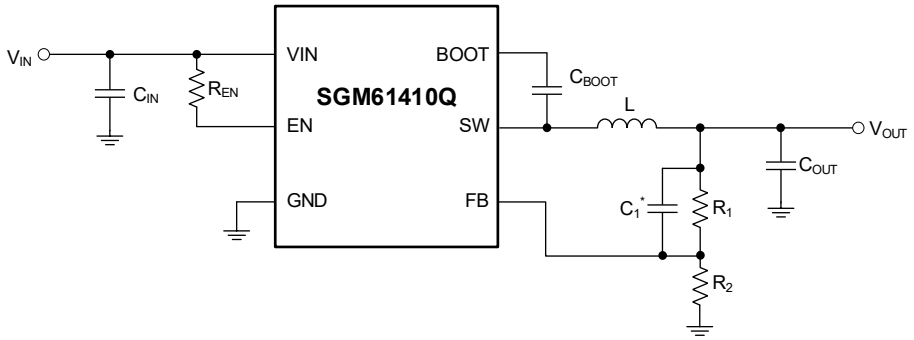
FEATURES

- **AEC-Q100 (Grade 1) Qualified for Automotive Applications**
  T_A = -40℃ to +125℃
- **Wide 5V to 42V Operating Input Voltage Range**
- **0.765V Internal Reference**
- **Low Quiescent Current: 14μA (TYP)**
- **Shutdown Current: 0.6μA (TYP)**
- **Current Output up to 600mA**
- **1.2MHz Switching Frequency**
- **Internal Compensation and Soft-Start**
- **Current Limit and Short-Circuit Protection**
- **Output Over-Voltage Protection and Thermal Shutdown**
- **Power-Save Mode at Light Load**
- **90% Maximum Duty Cycle**
- **Available in a Green SOT-23-6 Package**

APPLICATIONS

Automotive Systems
Battery-Powered Systems
General Purpose Wide VIN Power Supplies

TYPICAL APPLICATION



* NOTE: An optional feed-forward capacitor can be used across R_1 (as shown) to improve transient performance and reduce the over/undershoot peaks during load steps.

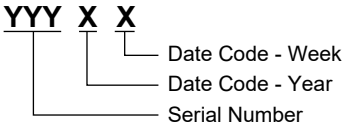
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61410Q	SOT-23-6	-40℃ to +125℃	SGM61410QN6G/TR	05PXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN to GND ..... -0.3V to 45V
EN to GND ..... -0.3V to V_{IN} + 0.3V
FB to GND ..... -0.3V to 5.5V
SW to GND ..... -0.3V to V_{IN} + 0.3V
BOOT to SW ..... -0.3V to 5.5V
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 129.9℃/W
SOT-23-6, θ_{JB} ..... 28.6℃/W
SOT-23-6, θ_{JC} ..... 57.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage Range ..... 5V to 42V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

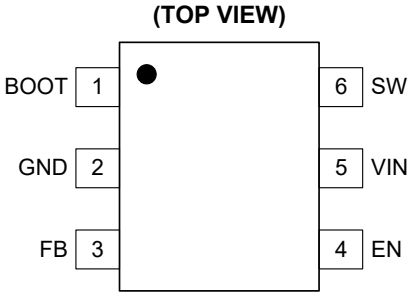
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	BOOT	Bootstrap Pin. It is used to provide a drive voltage, which is higher than the input voltage, to the topside power switch. Place a 0.47μF Boost capacitor (C_{BOOT}) as close as possible to the IC between this pin and SW pin.
2	GND	Ground Pin. It is the reference for input and the regulated output voltages. Special layout considerations are required.
3	FB	Feedback Pin for Programming the Output Voltage. The SGM61410Q regulates the FB pin to 0.765V (TYP). Connect the feedback resistor divider tap to this pin. If the FB voltage exceeds 117% of 0.765V, over-voltage protection (OVP) will stop all PWM switching.
4	EN	Enable Pin. It should not be left open and should not be driven above V_{IN} + 0.3V. Device will operate when the EN pin is high and shut down when the EN pin is low. EN must be tied to VIN pin via a resistor if the shutdown feature is not required or to a logic input for controlling shutdown.
5	VIN	VIN Pin. It is connected to the input supply voltage and powers the internal control circuitry. This voltage is monitored by a UVLO lockout comparator. VIN is also connected to the drain of the converter top switch. Due to power switching, this pin has high di/dt transition edges and must be decoupled to the GND by input capacitors as close as possible to the GND pin to minimize the parasitic inductances.
6	SW	Switching Node Pin. It is the output of the internal power converter and should be connect to the output inductor. Bootstrap capacitor also connects to this pin. This node should be kept small on the PCB to minimize capacitive coupling, noise coupling and radiation.

ELECTRICAL CHARACTERISTICS

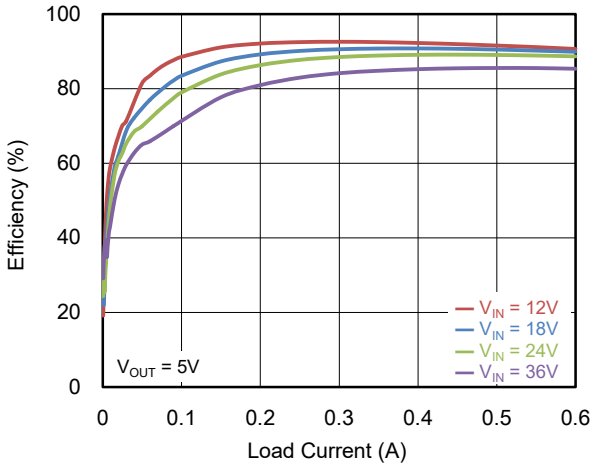
(V_{IN} = 12V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Input Voltage	V_{IN}		5		42	V
Under-Voltage Lockout Threshold	V_{UVLO}		4.40	4.7	5.00	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HYS}			370		mV
Shutdown Input Current	I_{SD}	V_{EN} = 0V		0.6	1.5	μA
Quiescent Input Current	I_Q	V_{EN} = 2V, not switching, V_{IN} ≤ 36V		14	22	μA
Feedback Reference Voltage	V_{FB}		0.747	0.765	0.786	V
Feedback Pin Input Current	I_{FB}	V_{FB} = 1V		0.1	1	μA
Minimum High-side Switch On-Time	t_{ON_MIN}	I_L = 600mA		95		ns
Minimum High-side Switch Off-Time	t_{OFF_MIN}			85		ns
Switching Frequency	f_{SW}		0.8	1.2	1.6	MHz
Switch Leakage Current	I_{SW_H}	V_{SW} = 42V		0.1	2	μA
	I_{SW_L}	V_{SW} = 0V		0.1	1	μA
Top Power NMOS Current Limit	I_{LIM}	T_J = +25℃	0.9	1.2	1.5	A
Top Power NMOS On-Resistance	R_{DSON}	I_L = 0.1A		700		mΩ
Bottom Power NMOS On-Resistance		I_L = 0.1A		300		mΩ
EN Input High Voltage	V_{IH}		1.2			V
EN Input Low Voltage	V_{IL}				0.5	V
EN Threshold, Hysteresis	V_{EN_HYS}			120		mV
Enable Leakage Current	I_{EN}	V_{EN} = 5V		0.1	1	μA
Output Over-Voltage Threshold	V_{OUT_OV}	OVP rising		117%	125%	V_{FB}
		OVP falling	102%	110%		
Thermal Shutdown	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

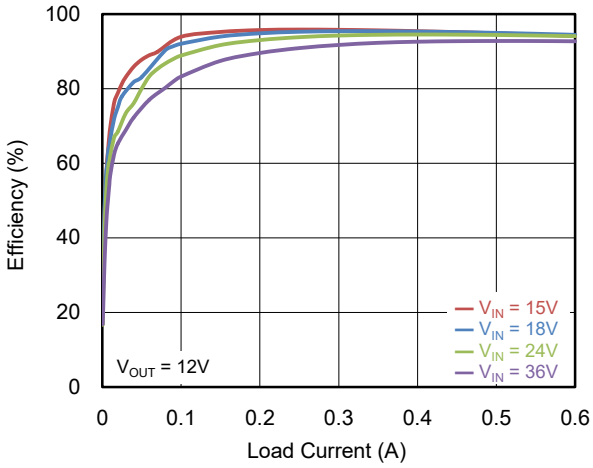
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, L = 22μH and C_{OUT} = 22μF, unless otherwise noted.

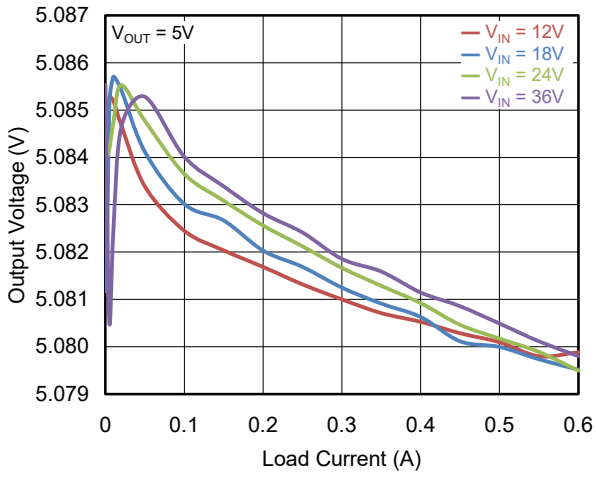
Efficiency vs. Load Current



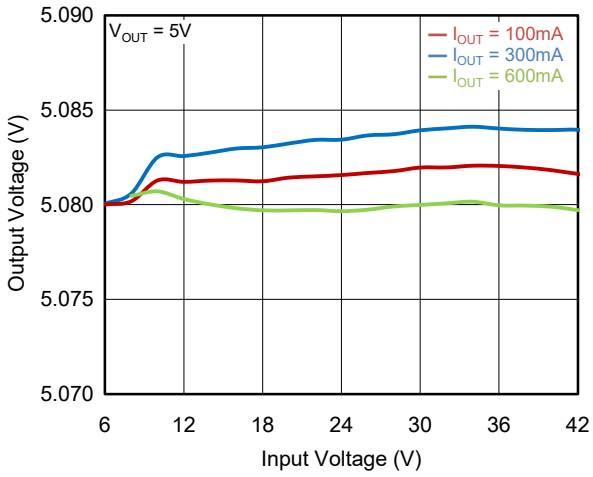
Efficiency vs. Load Current



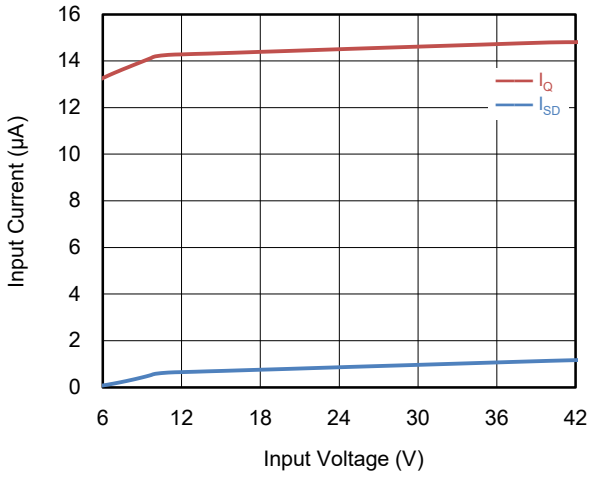
Load Regulation



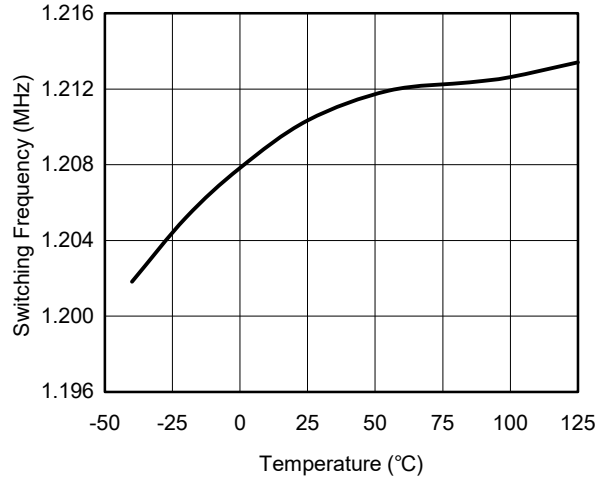
Line Regulation



Input Current vs. Input Voltage



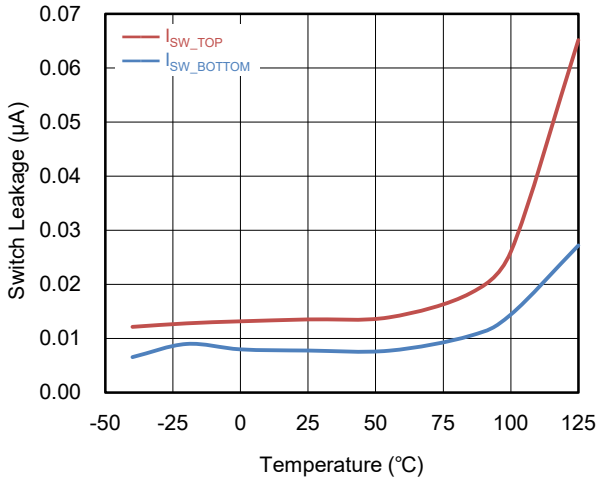
Switching Frequency vs. Temperature



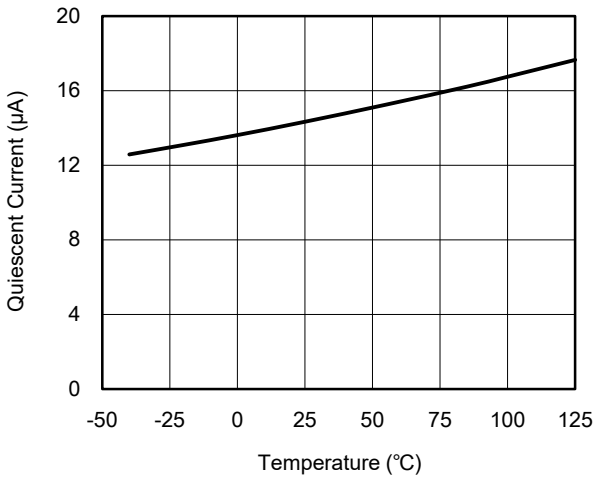
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, L = 22μH and C_{OUT} = 22μF, unless otherwise noted.

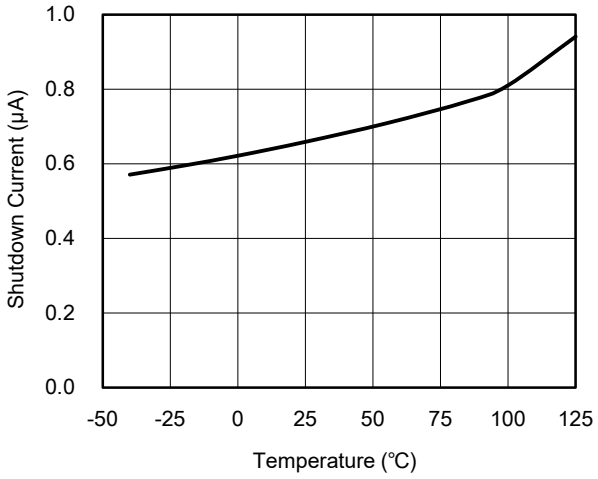
Switch Leakage vs. Temperature



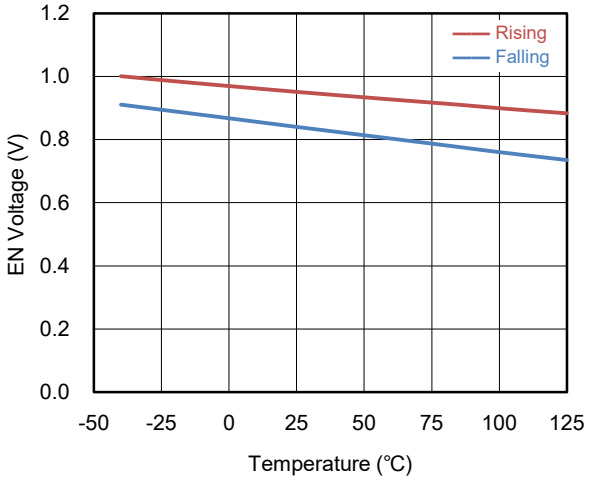
Quiescent Current vs. Temperature



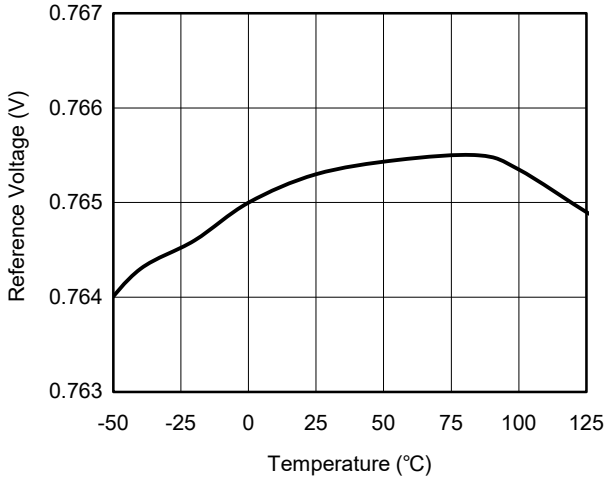
Shutdown Current vs. Temperature



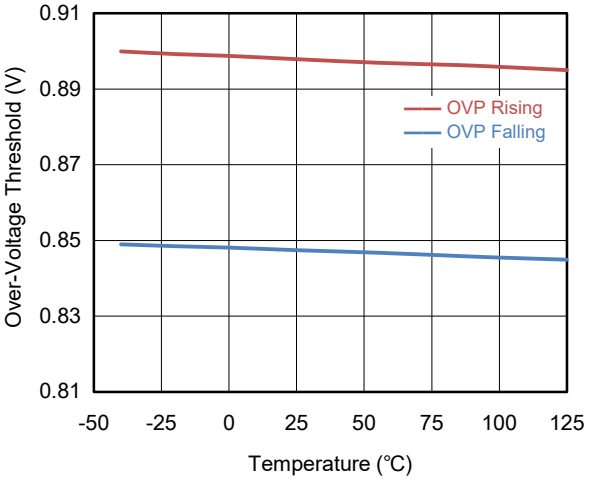
EN Voltage vs. Temperature



Reference Voltage vs. Temperature



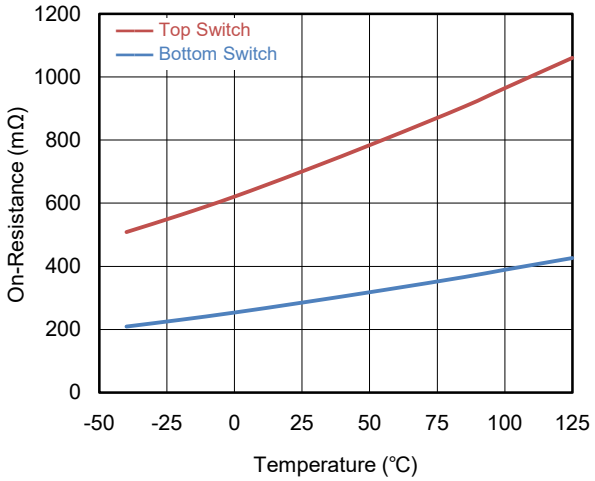
Over-Voltage Threshold vs. Temperature



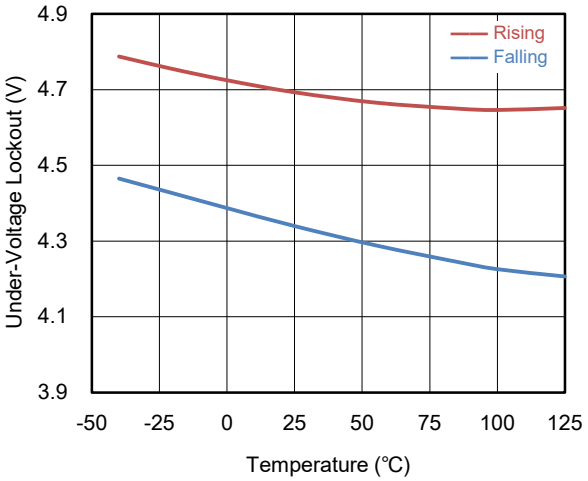
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, L = 22μH and C_{OUT} = 22μF, unless otherwise noted.

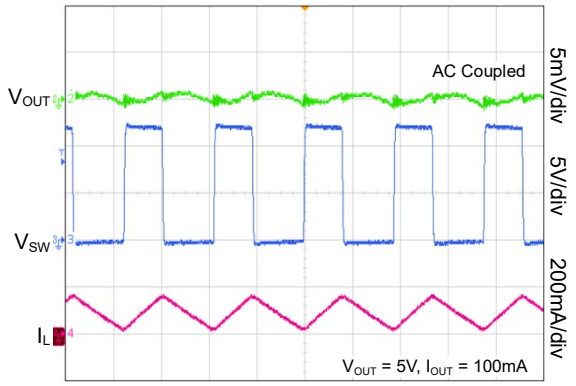
On-Resistance vs. Temperature



Under-Voltage Lockout vs. Temperature

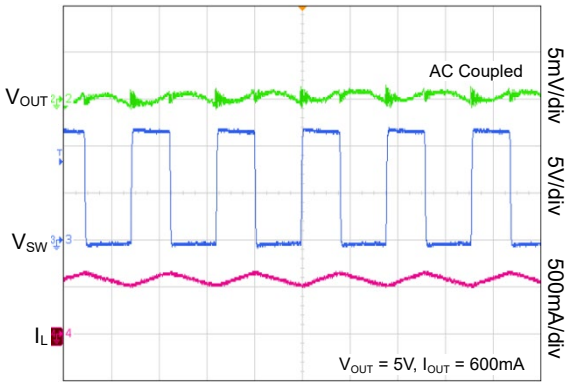


Steady State



Time (500ns/div)

Steady State



Time (500ns/div)

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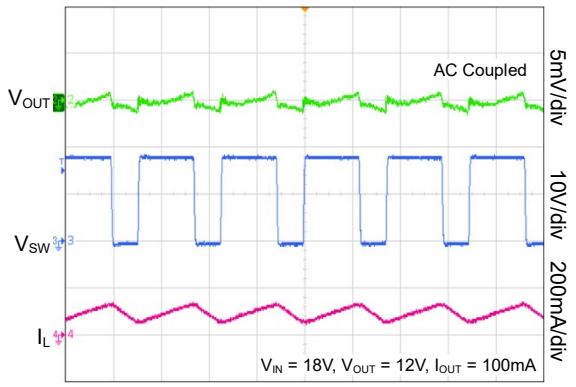
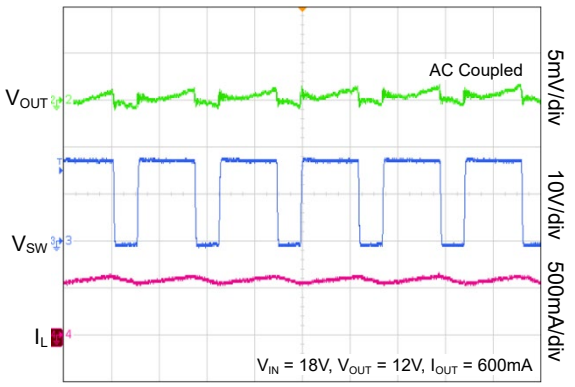


Time (500ns/div)

Steady State

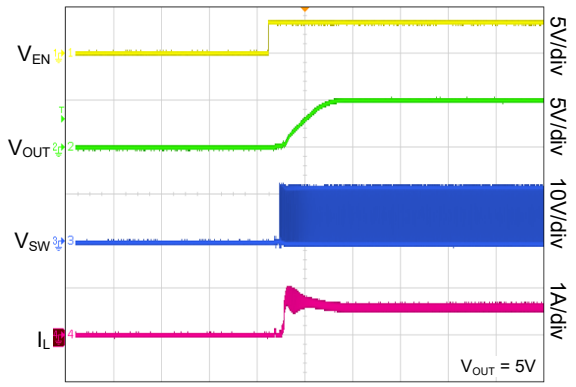


Time (500ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

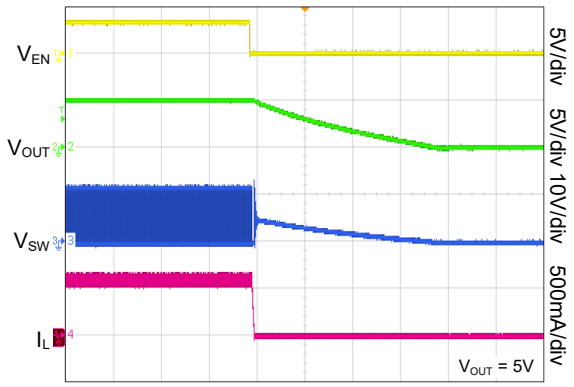
T_A = +25℃, V_{IN} = 12V, I_{OUT} = 600mA, L = 22μH and C_{OUT} = 22μF, unless otherwise noted.

EN Power-Up



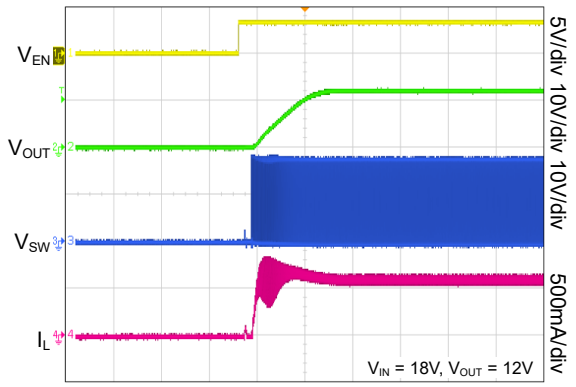
Time (1ms/div)

EN Power-Down



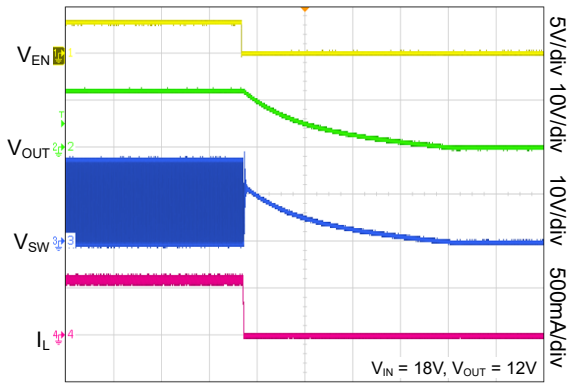
Time (50μs/div)

EN Power-Up



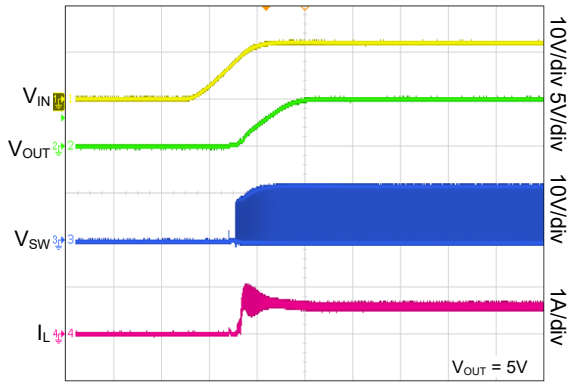
Time (1ms/div)

EN Power-Down



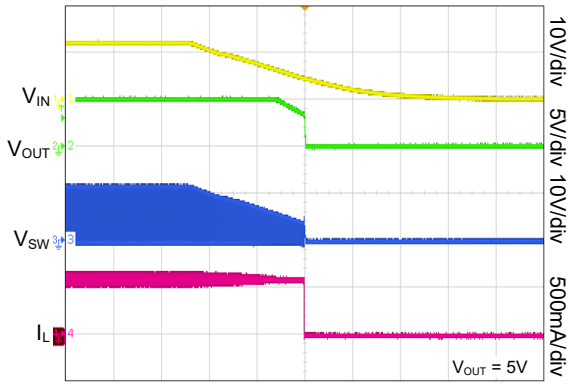
Time (100μs/div)

VIN Power-Up



Time (1ms/div)

VIN Power-Down

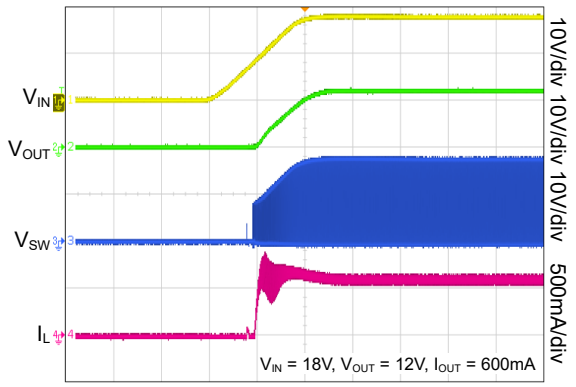


Time (5ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

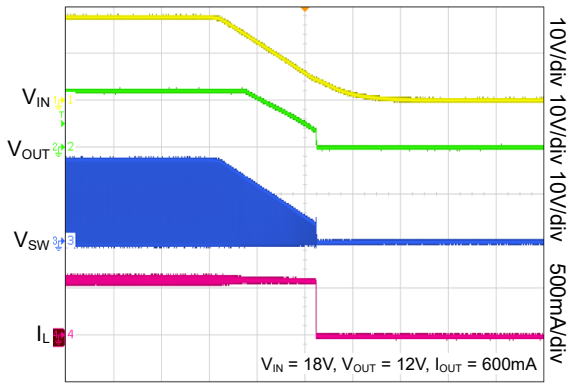
T_A = +25℃, V_{IN} = 12V, L = 22μH and C_{OUT} = 22μF, unless otherwise noted.

VIN Power-Up



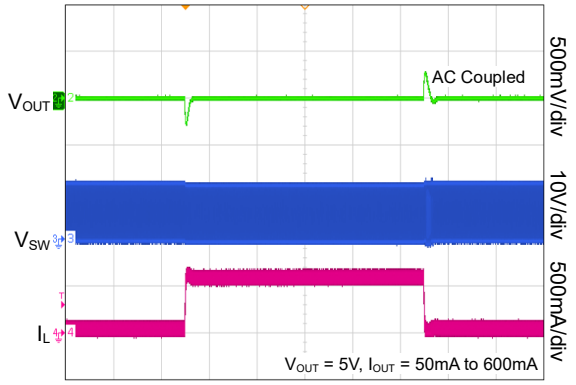
Time (1ms/div)

VIN Power-Down



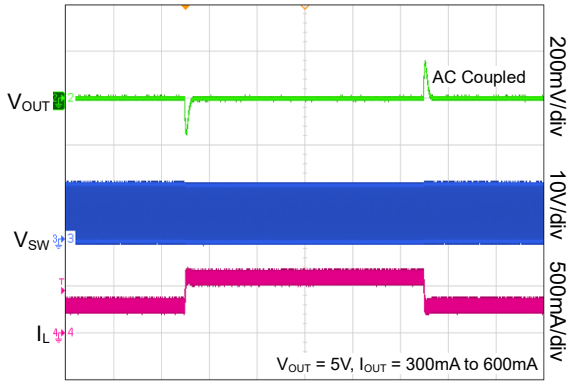
Time (10ms/div)

Load Transient Response



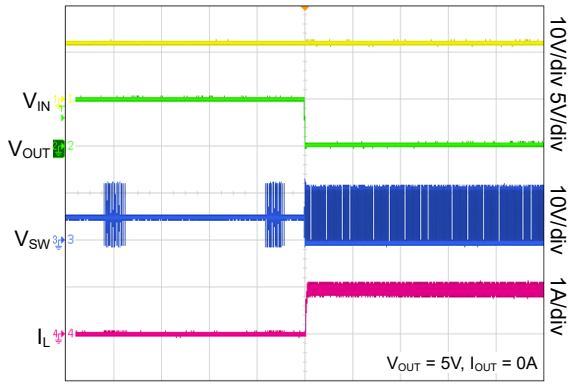
Time (1ms/div)

Load Transient Response



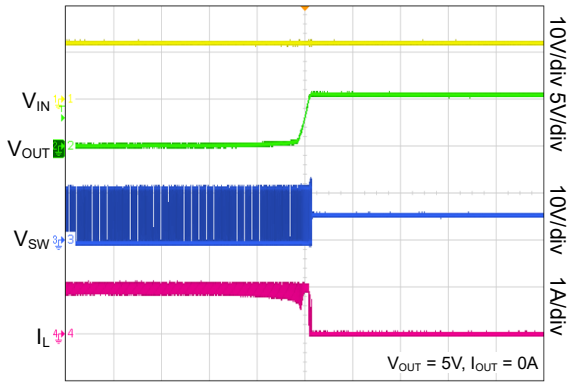
Time (1ms/div)

Short-Circuit Entry



Time (500μs/div)

Short-Circuit Recovery



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

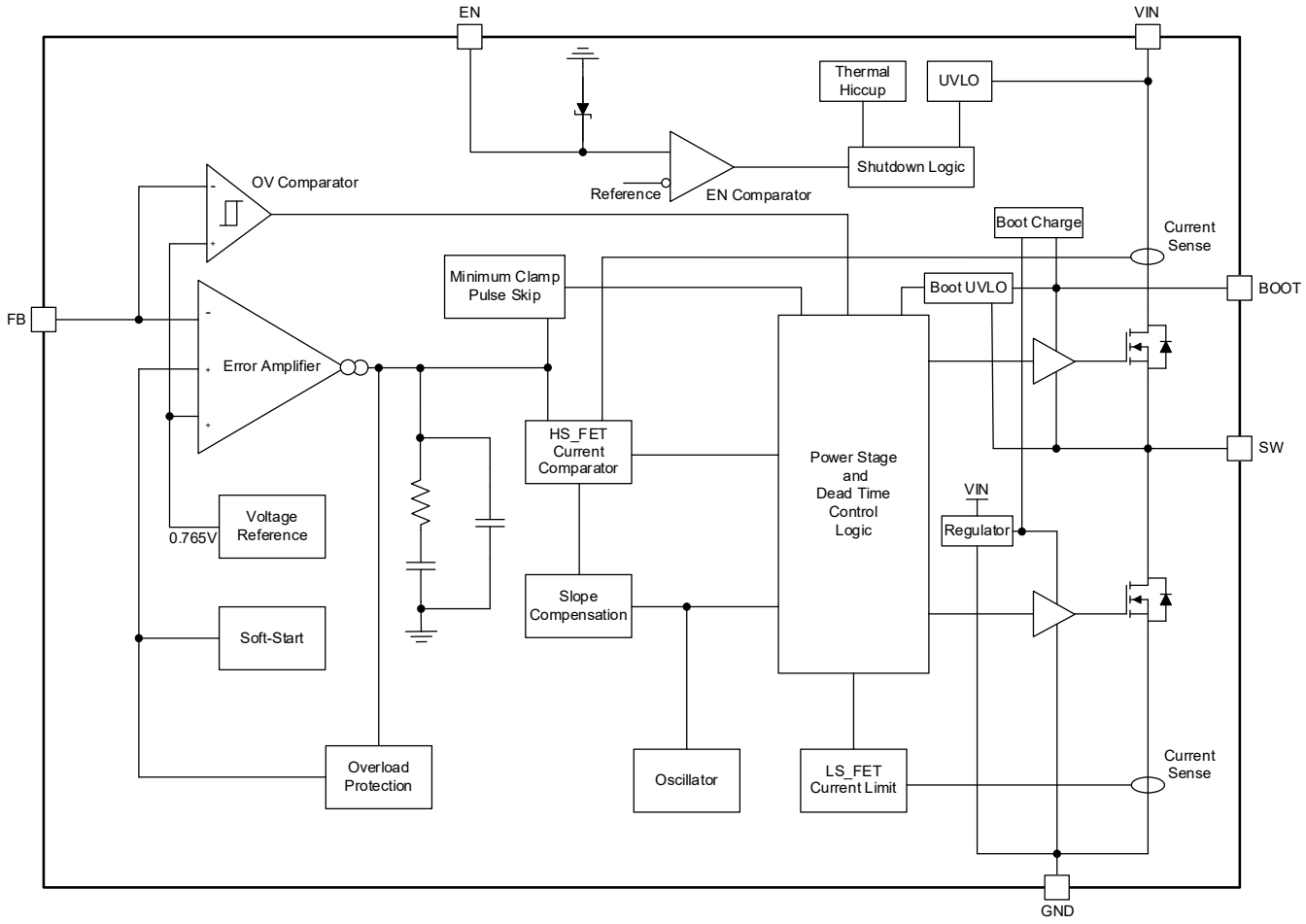


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61410Q is an internally compensated wide input range current mode controlled synchronous Buck converter. It is designed for high reliability and is particularly suitable for power conditioning from unregulated sources or battery-powered applications that need low sleep/shutdown currents. It also features a power-save mode in which operating frequency is adaptively reduced under light load conditions to reduce switching and gate losses and keep high efficiency. At no load and with switching stopped, the total operating current is approximately 14μA. If the device is disabled, the total consumption is typically 0.6μA.

Figure 2 shows the simplified block diagram of the SGM61410Q. The two integrated MOSFET switches of the power stage are both over-current protected and can provide up to 600mA of continuous current for the load. Current limiting of the switches also prevents inductor current runaway. The converter switches are optimized for high efficiency at low duty cycle.

At the beginning of each switching cycle, the high-side switch is turned on. This is the time that feedback voltage (V_{FB}) is below the reference voltage (V_{REF}) and power must be delivered to the output. After the on-period, the high-side switch is turned off and the low-side switch is turned on until the end of switching cycle. For reliable operation and preventing shoot-through, a short dead time is always inserted between gate pulses of the converter complimentary switches. During dead time, both switch gates are kept off.

If the junction temperature exceeds a maximum threshold (T_{SD}, typically +150℃), thermal shutdown protection will occur and switching will stop. The device will automatically recover with soft-start when the junction temperature drops back well below the trip point. This hysteresis is typically 20℃.

The SGM61410Q has current limit on both the high-side and low-side MOSFET switches. When current limit is activated, frequency fold-back is also activated. This occurs in the case of output overload or short-circuit. Note that SGM61410Q will continue to provide its maximum output current and will not shut down or hiccup. In such a case, the junction temperature may rise rapidly and trigger thermal shutdown.

During initial power-up of the device (soft-start), current limit and frequency fold-back are activated to prevent inductor current runaway while the output capacitor is charging to the desired V_{OUT}.

Peak-Current Mode (PWM Control)

Figure 2 shows the functional block diagram and Figure 3 shows the switching node operating waveforms of the SGM61410Q. Switching node voltage is generated by controlling the duty cycles of the complementary high-side and low-side switches. The high-side duty cycle is used as control parameter of the Buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side switch on-time and t_{SW} is the switching period. When high-side switch is turned on, the SW pin voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} - V_{OUT})/L slope. When high-side switch is turned off, the low-side switch is turned on after a very short dead time to avoid shoot-through, and I_L ramps down with -V_{OUT}/L slope. In ideal case, the output voltage is proportional to the input voltage and duty cycle ($D = V_{OUT}/V_{IN}$) if component parasitic parameters are ignored.

The SGM61410Q employs fixed-frequency peak-current mode control in continuous conduction mode (when inductor minimum current is above zero). In light load conditions (when the inductor current reaches zero), the SGM61410Q will enter discontinuous conduction mode and the control mode will change to shift frequency, peak-current mode to reduce the switching frequency and the associated switching and gate driving losses (power-save mode).

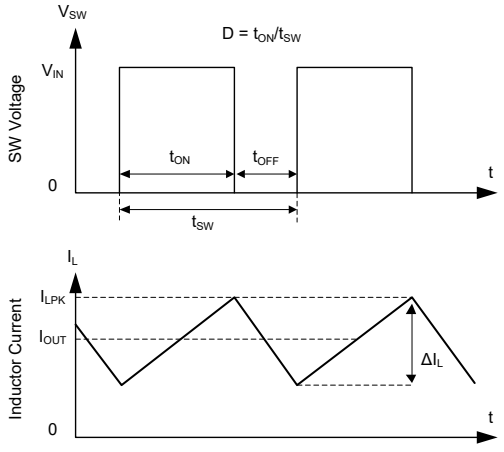


Figure 3. Converter Switching Waveforms in CCM

DETAILED DESCRIPTION (continued)

In continuous conduction mode, SGM61410Q operates at fixed-frequency using peak-current mode control scheme. The controller has an outer voltage feedback loop to get accurate DC voltage regulation. The output of the outer loop is fed to an inner peak-current control loop as reference command that adjusts the peak-current of the inductor. The inductor peak-current is sensed from the high-side switch and is compared to the peak-current reference to control the duty cycle. In other words, as soon as the inductor current reaches the reference peak-current determined by voltage loop, the high-side switch is turned off and the low-side switch is turned on after dead time.

The internally compensated voltage feedback loop allows for simpler design and fewer external components.

Power-Save Mode

When the load is reduced, the inductor minimum (valley) current eventually reaches zero level (boundary condition). Synchronous rectifier (low-side switch) current is always sensed and when it reaches zero, the controller turns off the low-side switch and does not let the low-side switch sink current. This prevents inductor current from going below zero (negative). This results in discontinuous conduction mode (DCM) operation in which inductor current remains zero until next switching cycle. Both switches are off during this period and do not act as complementary switches. This off-time will extend (that means lower frequency) until output voltage falls below reference voltage again and triggers a new switching cycle. With a new cycle, the high-side switch is turned on again for almost the same t_{ON} time as CCM. Therefore, the output capacitors take almost the same charge in each cycle and it will take longer off-times with lighter loads until output capacitor voltage falls below the reference voltage. The extended off-times mean lower switching frequency that is called frequency fold-back and significantly reduces the switching losses, but usually increases the output ripple a little bit.

Note that the on-time of synchronous rectifier switch should always be long enough to fully charge the bootstrap capacitor and prevent bootstrap under-voltage lockout due to insufficient voltage for the high-side switch gate driver.

Floating Driver and Bootstrap Charging UVLO Protection

The high-side MOSFET driver is powered by a floating supply provided by an external bootstrap capacitor. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between BOOT and SW nodes is below regulation, a PMOS pass transistor turns on and connects VIN and BOOT pins internally, otherwise it will turn off. The power supply for the floating driver has its own UVLO protection. The rising UVLO threshold is about 4.7V and with 370mV hysteresis, and the falling threshold is about 4.3V. In case of UVLO, the reference voltage of the controller is reset to zero and after recovery a new soft-start process will start.

Output Over-Voltage Protection (OVP)

The SGM61410Q contains an over-voltage comparator that monitors the FB pin voltage. The over-voltage threshold is approximately 117% of nominal FB voltage. When the voltage at the FB pin exceeds the over-voltage threshold (V_{OUT_OV}), PWM switching will be stopped and both high-side and low-side switches will be turned off. If the over-voltage fault is removed, the regulator will automatically recover.

The error amplifier is normally able to maintain regulation since the synchronous output stage has excellent sink and source capability. However, it is not able to regulate output when the FB pin is disconnected or when the output is shorted to a higher supply like input supply. Also when V_{OUT} is set to its minimum (0.765V) usually there is no voltage divider and V_{OUT} is directly connected to FB through a resistor (R_1 in the divider) and there is no resistor to ground (no R_2). In such case and with no load, an internal current source of 5μA ~ 6μA from BOOT into the SW pin, which can slowly charge the output capacitor and pull V_{OUT} up to V_{IN}. Therefore, a minimum load of at least 10μA must be always present on V_{OUT} (a 76.8kΩ resistor is preferred).

If the FB pin is disconnected, a tiny internal current source will force the voltage at the FB pin to rise above V_{OUT_OV} that triggers over-voltage protection and disables the regulator to protect the loads from a significant over-voltage. Also, if by accident a higher external voltage is shorted to the output, V_{FB} will rise above the over-voltage threshold and trigger an OVP event to protect the low-side switch.

DETAILED DESCRIPTION (continued)

Minimum High-side On/Off-Time and Frequency Fold-Back

The shortest duration for the high-side switch on-time (t_{ON_MIN}) is 95ns (TYP). For the off-time (t_{OFF_MIN}), the minimum value is 85ns (TYP). The duty cycle (or equivalently the V_{OUT}/V_{IN} ratio) range in CCM operation is limited by t_{ON_MIN} and t_{OFF_MIN} depending on the switching frequency. Note that at 1.2MHz the total cycle time is t_{SW} = 833ns.

The minimum and maximum duty cycles without frequency fold-back are given by Equations 1 and 2:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (1)$$

and

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (2)$$

For any given output voltage, the highest input voltage without frequency fold-back can be calculated from:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (3)$$

The minimum V_{IN} is estimated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (4)$$

Input Voltage

The SGM61410Q can operate efficiently for inputs as high as 42V. For CCM operation (continuous conduction mode) keep duty cycle between 11% and 90%.

Output Voltage

The output voltage can be stepped down to as low as the 0.765V reference voltage (V_{REF}). As explained before, when the output voltage is set to 0.765V and there is no voltage divider, a minimum small load will be needed. A 76.8kΩ resistor to ground will prevent the output voltage from floating.

Soft-Start

Soft-start is necessary to limit the input inrush current right after the device is powered up or enabled. Soft-start is implemented by slowly ramping up the reference voltage that in turn slowly ramps up the output voltage to its target regulation value.

Enable

EN pin turns the SGM61410Q operation on or off. If an applied voltage is less than 0.5V, the device will shut down. If the voltage is more than 1.2V, the device will start the regulator. The EN pin is an input and must not be left open. The simplest way to enable the device is to connect the EN pin to VIN pin via a resistor. This enables the SGM61410Q to start up automatically when V_{IN} is within the operating range. An external logic signal can be used to drive the EN input for power savings, power supply sequencing and/or protection. If the EN pin is driven by an external logic signal, a 10kΩ resistor in series with the input is recommended.

Note: Voltage on the EN pin should never exceed V_{IN} + 0.3V. Do not drive the EN pin with a logic level if V_{IN} is not present. This can damage the EN pin and the device.

Thermal Shutdown

Thermal protection is designed to protect the die against overheating damage. If the junction temperature exceeds +150℃, the switching stops and the device shuts down. Automatic recovery with an internal soft-start will begin when the junction temperature drops below the +130℃ falling threshold.

APPLICATION INFORMATION

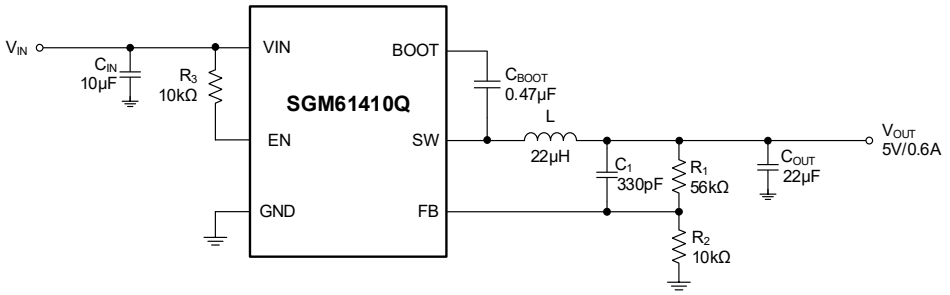


Figure 4. 5V Output Typical Application Circuit

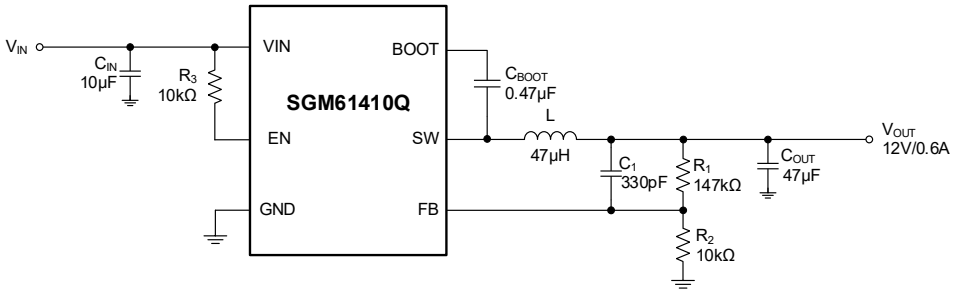


Figure 5. 12V Output Typical Application Circuit

External Components

The design method and component selection for the SGM61410Q Buck converter is explained in this section. Schematics of basic design are shown in Figure 4 and Figure 5. Only a few external components are needed to provide a constant output voltage from a wide input voltage range.

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_{FF} and divider resistor values are provided in Table 1 to simplify component selection.

Table 1. Recommended Component Values

f_{SW} (MHz)	C_1 (pF)	V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	L (μH)	C_{BOOT} (μF)	C_{IN} (μF)	C_{OUT} (μF)
1.2	330	3.3	33	10	10	0.47	10	10
		5	56	10	22	0.47	10	22
		12	147	10	47	0.47	10	47

Design Requirements

A typical application circuit for the SGM61410Q as a Buck converter is shown in Figure 4. It is used for converting a 6V to 42V supply voltage to a lower voltage level supply voltage (5V) suitable for the system. The design parameters given in Table 2 are used for this design example.

Table 2. Design Example Parameters

Parameter	Value
Input Voltage, V_{IN}	12V (TYP), range from 6V to 42V
Output Voltage, V_{OUT}	5V ± 3%
Maximum Output Current, I_{OUT_MAX}	600mA
Output Over/Undershoot (50mA to 600mA)	5% of V_{OUT}
Output Voltage Ripple (CCM)	0.5% of V_{OUT}
Operating Frequency	1.2MHz

Output Voltage Programming

Output voltage can be set with a resistor divider feedback network between output and FB pin as shown in Figure 4. Usually, a design is started by selecting lower resistor R_2 and calculating R_1 with the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

where V_{REF} = 0.765V.

To keep operating quiescent current small and prevent voltage errors due to leakage currents, it is recommended to choose R_2 in the range of 10kΩ to 100kΩ.

If the output has no load other than the FB divider, make sure the divider draws at least 10μA from V_{OUT} or an internal current source (5μA to 6μA) from BOOT to SW will slowly charge the output capacitor beyond the desired voltage.

APPLICATION INFORMATION (continued)

Inductor Selection

Higher operating frequency allows the designer to choose smaller inductor and capacitor values. However, the switching and gate losses are increased. On the other hand, at lower frequencies the current ripple (ΔI_L) is higher, which results in higher light load losses. Use Equation 6 to calculate the required inductance (L_{MIN}). K is the ratio of the inductor peak-to-peak ripple (ΔI_L) to the maximum operating DC current (I_{OUT}). The recommended selection range for K is between 0.2 and 0.4. Choosing a higher K value reduces the selected inductance, but a too high K factor may result in insufficient slope compensation. The inductance is selected based on the desired peak-to-peak ripple current (ΔI_L) for CCM. Equation 7 shows that ΔI_L is inversely proportional to $f_{SW} \times L$ and is increased at the maximum input voltage (V_{IN_MAX}). Therefore, by accepting larger ΔI_L values, smaller inductances can be chosen but the cost is higher output voltage ripple and increased core losses.

Inductor peak-current should never exceed the saturation even in transients to avoid over-current protection. Also inductor RMS rating should always be larger than operating RMS current even at maximum ambient temperature.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \quad (6)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

Note that it is generally desired to choose a smaller inductance value to have faster transient response, smaller size, and lower DCR. On the other hand, if the inductance is too small, current ripple will increase which can trigger over-current protection. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. For peak-current mode control, it is recommended to choose large current ripple, because controller comparator performs better with higher signal to noise ratio. So, for this design example, K = 0.4 is chosen, and the minimum inductor value is calculated to be 15.3μH. The nearest standard value would be a 22μH ferrite inductor with a 1A RMS current rating and 1.5A saturation current that are well above the designed converter output current RMS and DC respectively.

Bootstrap Capacitor Selection

The SGM61410Q requires a small external bootstrap capacitor, C_{BOOT}, between the BOOT and SW pins to provide the gate drive supply voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is conducted. An X7R or X5R 0.47μF ceramic capacitor with a voltage rating of 16V or higher is recommended for stable operating performance over-temperature and voltage variations.

Input Capacitor Selection

The input capacitor also provides the high frequency switching transient currents. So, choosing a low-ESR and small size capacitor with high self-resonance frequency and sufficient RMS rating is necessary. The recommended high frequency decoupling capacitor value is 10μF X5R or X7R or higher. It is recommended to choose the voltage rating of the capacitor(s) at least twice the maximum input voltage to avoid derating of the ceramic capacitors with DC voltage. Some bulk capacitances may be needed, especially if the SGM61410Q is not located within 5cm distance from the input voltage source for input stability. Bulk capacitors have high Equivalent Series Resistance (ESR) and can provide the damping needed to prevent input voltage spiking due to the wiring inductance of the input. The value for the input capacitor is not critical but must be rated to handle the maximum input voltage including ripple. For this design, one 10μF, X7R, 50V is selected for the input decoupling capacitor. To improve high frequency filtering, a small parallel 0.1μF capacitor may be placed as close as possible to the device pins.

Output Capacitor Selection

This device is designed to be used with external LC filters. The minimum required capacitance to keep cost and size down and bandwidth high. The main parts for designing the output capacitance are output voltage ripple, loop stability and the voltage over/undershoot during load current transients. So, C_{OUT} should be chosen carefully. The output voltage ripple is determined of two factors. One factor is caused by the inductor current ripple going through the ESR of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (8)$$

APPLICATION INFORMATION (continued)

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K_{IND} \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \quad (9)$$

These AC components are not in phase and the total peak-to-peak ripple is less than $\Delta V_{OUT\_ESR} + \Delta V_{OUT\_C}$.

Transient performance specification usually limits output capacitance if the system requires tight voltage regulation in presence of large current steps and/or fast slew rate. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. The control loop of regulator usually requires 8 or more clock cycles to adjust the inductance current to the new load level. The output capacitance must be as large as possible to provide a current difference of 8 clock cycles to keep the output voltage within the specified range. Equation 10 shows the minimum output capacitance required to specify output over/undershoot.

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \quad (10)$$

where:

I_{OL} = Low level of the output current step during load transient.

I_{OH} = High level of the output current during load transient.

V_{OUT_SHOOT} = Target output voltage over/undershoot.

For this design example, the target output ripple is 25mV. Assuming $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 25mV, and choosing K_{IND} = 0.4, Equation 8 requires ESR to be less than 104mΩ and Equation 9 requires C_{OUT} > 1μF. The target over/undershoot range of this design is ΔV_{OUT_SHOOT} = 5% × V_{OUT} = 250mV. From Equation 10, C_{OUT} > 8μF. So, in summary, the most stringent criteria for the output capacitor is transient constrain of C_{OUT} > 8μF. For the derating margin, one 22μF, 10V, X7R ceramic capacitor with 10mΩ ESR is used.

Layout Guideline

Careful layout is always important to ensure good performance and stable operation to any kind of switching regulator. Place the capacitors close to the device, use the GND pin of the device as the center of star-connection to other grounds, and minimize the trace area of the SW node. With smaller transient current loops, lower parasitic ringing will be achieved.

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R better dielectric) placed as close as possible to VIN pin.
- Use short, wide and direct traces for high-current connections (VIN, SW and GND).
- Keep the BOOT-SW voltage path as short as possible.
- Place the feedback resistors as close as possible to the FB pin that is sensitive to noise.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections and SW pin.

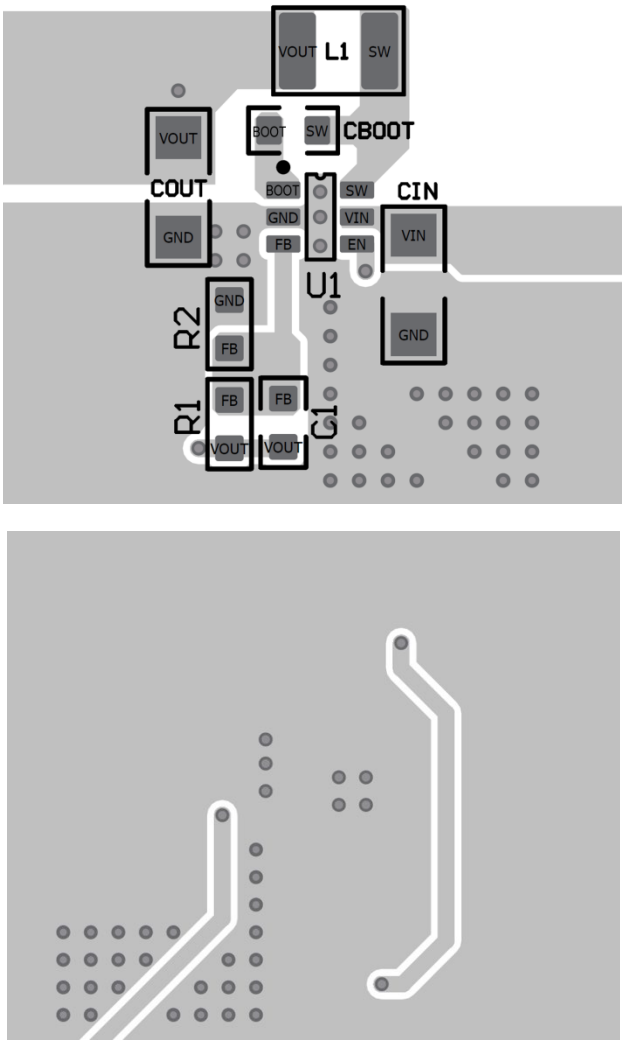


Figure 6. Suggested PCB

REVISION HISTORY

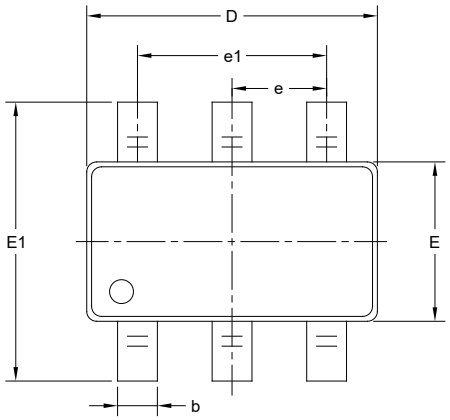
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

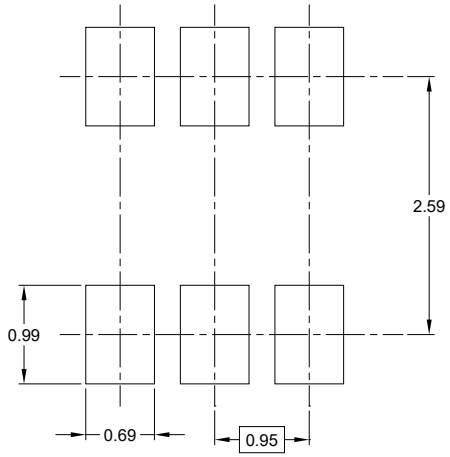
AUGUST 2024 – REV.A to REV.A.1	Page
Updated Package Thermal Resistance	All

Changes from Original (DECEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

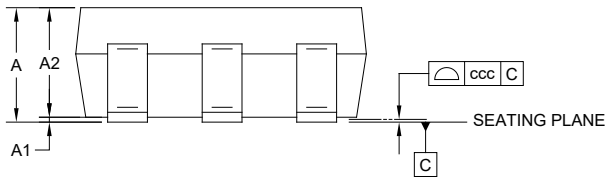
PACKAGE OUTLINE DIMENSIONS

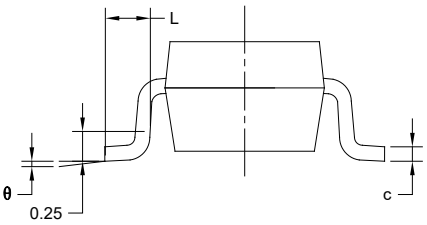
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



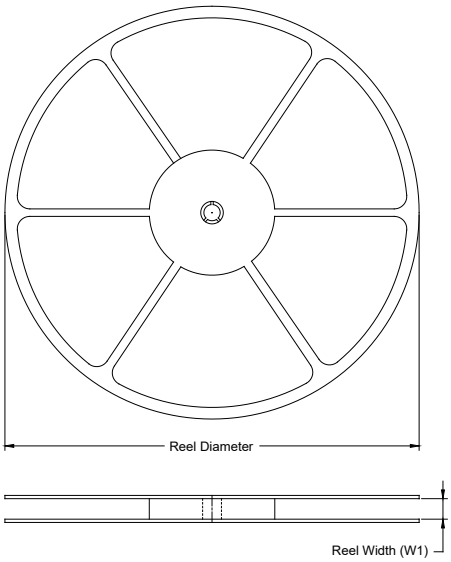


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

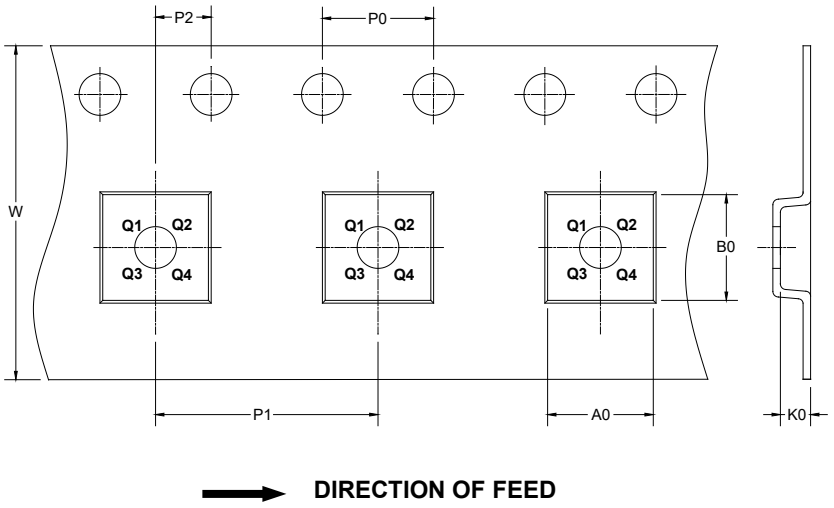
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



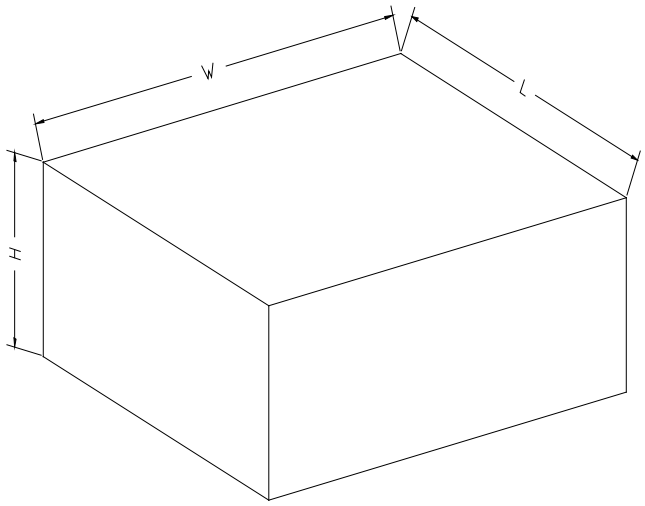
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002