SGM38121
4-Channel LDO PMIC for Camera Applications

GENERAL DESCRIPTION

The SGM38121 is a 4-channel LDO PMIC, which has two high efficiency and low output DVDD channels and two high PSRR and low noise AVDD channels.

For DVDD1 and DVDD2, the SGM38121 uses NMOS architecture without a charge pump. IN1 is used as an input source and IN2 is used as bias voltage. The IN1 input voltage range is from 0.7V to 2V and IN2 input voltage range is from 3V to 5.5V respectively. The DVDD1 and DVDD2 output ranges are both from 0.528V to 1.504V. Both of them are capable of supplying 1200mA output current with ultra-low dropout voltage.

For AVDD1 and AVDD2, the SGM38121 uses PMOS architecture with IN2 as an input source. Both of them can supply 1.504V to 3.424V output voltage with high PSRR performance. The output current limit is 330mA.

The SGM38121 has an external EN pin, internal enable bits and sequence control register. Other features include UVLO, high resolution output voltage configuration, and hiccup function during OCP and UVP. The SGM38121 has automatic discharge function to quickly discharge output voltage in the disabled status. Besides, the SGM38121 supports 400kHz I^2C interface with register address automatic increment for continuous writing.

The SGM38121 is qualified for phone camera sensors, camera sensors on wearable device.

The SGM38121 is available in a Green TDFN-2×2-10L package. It operates over an operating temperature range of -40℃ to +85℃.

FEATURES

- **IN1 Input Voltage Range: 0.7V to 2V**
- **IN2 Input Voltage Range: 3V to 5.5V**
- **Supply Quiescent Current: 340μA (TYP)**
- **Shutdown Current: 0.13μA (TYP)**
- **UVLO: 2.43V (TYP)**
- **DVDD1/2 Output Voltage Range: 0.528V to 1.504V**
- **AVDD1/2 Output Voltage Range: 1.504V to 3.424V**
- **DVDD1/2 Output Current: 1200mA**
- **AVDD1/2 Output Current: 330mA**
- **DVDD1/2 Dropout Voltage: 105mV (TYP) at 1200mA**
- **AVDD1/2 Dropout Voltage: 120mV (TYP) at 300mA**
- **AVDD1/2 Power Supply Rejection Ratio:**
  - **90dB (TYP) at 1kHz**
  - **85dB (TYP) at 10kHz**
  - **70dB (TYP) at 100kHz**
  - **55dB (TYP) at 1MHz**
- **AVDD1/2 Output Noise: 9μV_{RMS} (TYP)**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green TDFN-2×2-10L Package**

APPLICATIONS

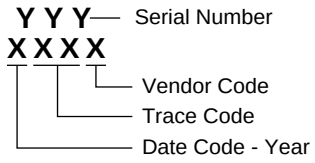
Camera Sensor
Smart Phone

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38121	TDFN-2×2-10L	-40℃ to +85℃	SGM38121YTHN10G/TR	0MC XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{IN} Range (V_{IN1}, V_{IN2}) ..... -0.3V to 6.5V
V_{EN} Range ..... -0.3V to (V_{IN} + 0.3V)
V_{OUT} Range ($V_{DVDD1/2}$, $V_{AVDD1/2}$) ..... -0.3V to (V_{IN} + 0.3V)
Package Thermal Resistance
TDFN-2×2-10L, θ_{JA} ..... 71.1℃/W
TDFN-2×2-10L, θ_{JB} ..... 33.1℃/W
TDFN-2×2-10L, $\theta_{JC(TOP)}$ ..... 71.9℃/W
TDFN-2×2-10L, $\theta_{JC(BOT)}$ ..... 4.9℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

IN1 Operating Supply Voltage Range ..... 0.7V to 2V
IN2 Operating Supply Voltage Range ..... 3V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

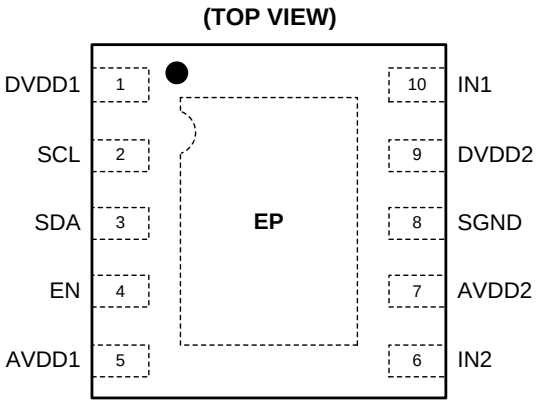
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	DVDD1	LDO1 Output Pin.
2	SCL	Serial Clock Input Pin.
3	SDA	Serial Data Pin.
4	EN	Enable Pin. Drive EN pin high to turn on the regulator. Drive EN pin low to turn off the regulator. Keep this pin low if I^2C control is used.
5	AVDD1	LDO3 Output Pin.
6	IN2	LDO3, LDO4 Supply Input, LDO1, LDO2 Bias.
7	AVDD2	LDO4 Output Pin.
8	SGND	Ground.
9	DVDD2	LDO2 Output Pin.
10	IN1	LDO1, LDO2 Supply Input Pin.
Exposed Pad	EP	Exposed Pad. Connect it to a large ground plane to maximize thermal performance. This pad is not an electrical connection point.

FUNCTIONAL BLOCK DIAGRAM

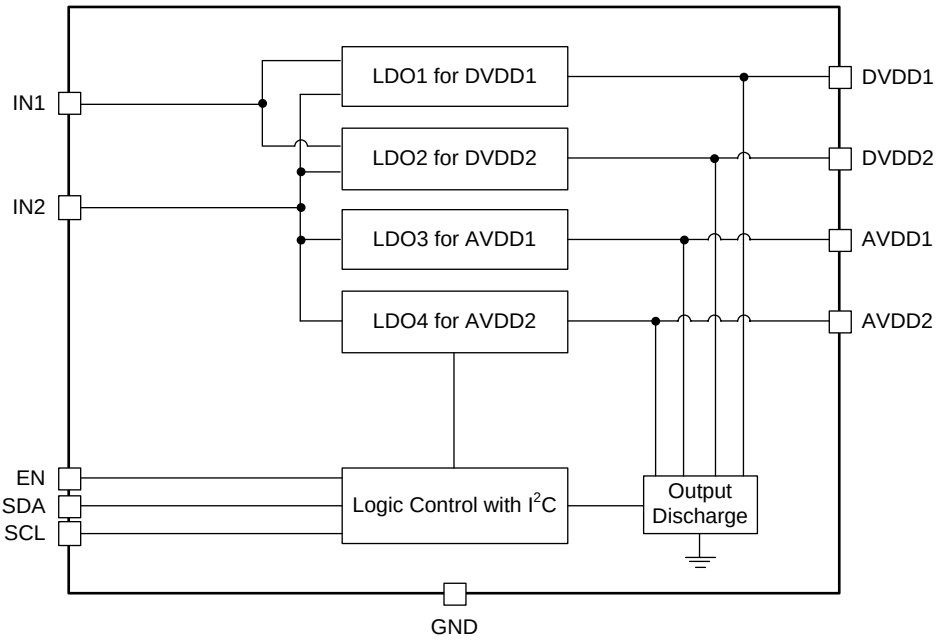


Figure 1. Block Diagram

TYPICAL APPLICATION

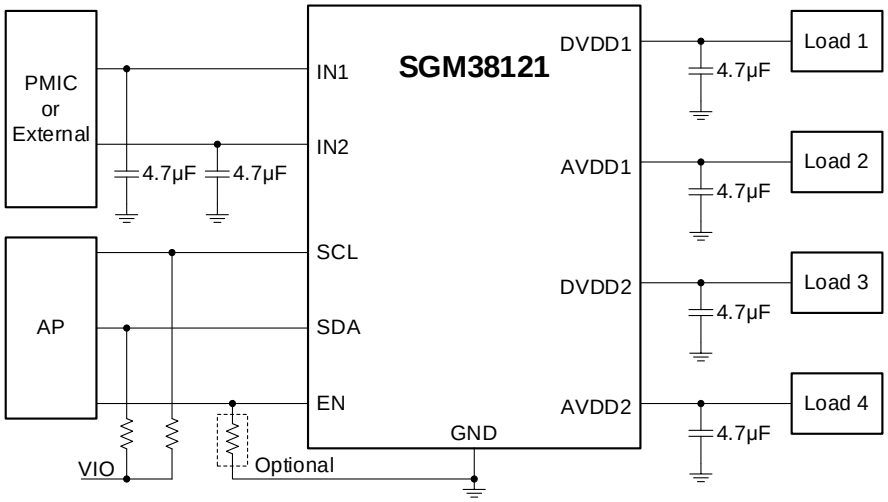


Figure 2. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Whole Device						
Quiescent Current at All LDO Active	I_Q	V_{EN} = V_{IN2}		340	460	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.13	1.5	μA
EN Logic High Voltage	V_{ENH}		0.9			V
EN Logic Low Voltage	V_{ENL}				0.4	V
EN Pin Internal Pull-Down Resistor	R_{EN}	V_{EN} = 0V to 5.5V		2.3		MΩ
Thermal Shutdown Threshold	T_{SHDN}			156		℃
Thermal Shutdown Hysteresis	ΔT_{SHDN}			18		℃
Output Discharge Resistor On-Resistance	$R_{DCHG\_DV1/2}$	V_{EN} = 0V		270		Ω
	$R_{DCHG\_AV1/2}$	V_{EN} = 0V		255		
Under-Voltage Lockout Threshold	V_{UVLO_RS}	Rising V_{IN2}	2.46	2.53	2.60	V
	V_{UVLO_FL}	Falling V_{IN2}	2.36	2.43	2.50	
LDO1, LDO2 (DVDD1/2)						
Input Voltage Range	V_{IN1}		0.7	1.35	2	V
Output Voltage Range	$V_{DVDD1/2}$	V_{EN} = 0V, programed by I^2C	0.528		1.504	V
Default Output Voltage	$V_{DVDD1/2}$	V_{EN} = V_{IN2}		1.2		V
Output Voltage Step Size				8		mV
Output Voltage Accuracy	$V_{OUT\_ACC\_DV1/2}$	$I_{DVDD1/2}$ = 10mA, $V_{DVDD1/2}$ = 0.8V to 1.2V, T_J = +25℃	-1		1	%
		$I_{DVDD1/2}$ = 10mA, $V_{DVDD1/2}$ = 0.8V to 1.504V, T_J = -40℃ to +85℃	-1.5		1.5	
		$I_{DVDD1/2}$ = 10mA, $V_{DVDD1/2}$ = 0.528V to 0.8V, T_J = -40℃ to +85℃	-1.8		1.6	
Dropout Voltage	$V_{DROP\_DV1/2}$	V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 1200mA		105	145	mV
		V_{IN2} = 4.4V, $V_{DVDD1/2}$ = 1.05V, $I_{DVDD1/2}$ = 500mA		40	60	
		V_{IN2} = 4.4V, $V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 500mA		40	60	
Turn-On Delay Time	$t_{DLY\_DV1/2}$	From assertion of enable signal to $V_{DVDD1/2}$ start ramp up, $I_{DVDD1/2}$ = 10mA		130		μs
Soft-Start Ramp Time	$t_{SS\_DV1/2}$	$V_{DVDD1/2}$ from 0% to 95%, $I_{DVDD1/2}$ = 10mA		180		μs
Output Current Limit	$I_{LIMIT\_DV1/2}$		1200	1500		mA
Startup Fault Disable Timer	$t_{SUFD\_DV1/2}$	Disable fault detection timer		300		μs
Hiccup Timer	t_{Hiccup}	Protection shutdown to recovery startup timer		22		ms
Load Regulation	$\Delta V_{LOAD\_DV1/2}$	$I_{DVDD1/2}$ = 1mA to 300mA		1		mV
Line Regulation	$\Delta V_{LINE\_DV1/2}$	$V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 10mA, V_{IN1} = 1.35V to 2V, V_{IN2} = 3.8V		0.1		mV
		$V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 10mA, V_{IN1} = 1.35V, V_{IN2} = 3V to 5.5V		0.1		mV
Output Voltage Noise	$e_{n\_DV1/2}$	$V_{DVDD1/2}$ = 1.2V, f = 10Hz to 100kHz, $I_{DVDD1/2}$ = 10mA		32		μV_{RMS}
Power Supply Rejection Ratio	$PSRR_{\_VIN1\_DV1/2}$	V_{IN1} = 1.5V + 0.2V_{P-P}, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 150mA, C_{IN1} = 100nF, f = 1kHz		80		dB
		f = 10kHz		70		
		f = 100kHz		50		
		f = 1MHz		38		
	$PSRR_{\_VIN2\_DV1/2}$	V_{IN2} = 3.8V + 0.2V_{P-P}, V_{IN1} = 1.5V, $V_{DVDD1/2}$ = 1.2V, $I_{DVDD1/2}$ = 150mA, no C_{IN2}, f = 1kHz		70		
		f = 10kHz		68		
		f = 100kHz		55		
		f = 1MHz		40		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LDO3, LDO4 (AVDD1/2)							
Input Voltage Range	V_{IN2}			3		5.5	V
Output Voltage Range	$V_{AVDD1/2}$	V_{EN} = 0V, programed by I^2C		1.504		3.424	V
Default Output Voltage	$V_{AVDD1/2}$	V_{EN} = V_{IN2}			2.8		V
Output Voltage Step Size					8		mV
Output Voltage Accuracy	$V_{OUT\_ACC\_AV1/2}$	$I_{AVDD1/2}$ = 10mA, $V_{AVDD1/2}$ = 1.504V to 3.424V	T_J = +25℃	-1		1	%
			T_J = -40℃ to +85℃	-1.5		1.5	
Dropout Voltage	$V_{DROP\_AV1/2}$	$V_{AVDD1/2}$ = 2.8V, $I_{AVDD1/2}$ = 300mA			120	175	mV
Turn-On Delay Time	$t_{DLY\_AV1/2}$	From assertion of enable signal to $V_{AVDD1/2}$ start ramp up, $I_{AVDD1/2}$ = 10mA			200		μs
Soft-Start Ramp Time	$t_{SS\_AV1/2}$	$V_{AVDD1/2}$ from 0% to 95%, $I_{AVDD1/2}$ = 10mA			520		μs
Output Current Limit	$I_{LIMIT\_AV1/2}$			330	430		mA
Startup Fault Disable Timer	$t_{SUFD\_AV1/2}$	Disable fault detection timer			3		ms
Hiccup Timer	t_{Hiccup}	Protection shutdown to recovery startup timer			22		ms
Load Regulation	$\Delta V_{LOAD\_AV1/2}$	$I_{AVDD1/2}$ = 1mA to 200mA			2		mV
Line Regulation	$\Delta V_{LINE\_AV1/2}$	V_{IN1} = 1.35V, V_{IN2} = 3V to 5.5V, $V_{AVDD1/2}$ = 2.8V, $I_{AVDD1/2}$ = 10mA			0.1		mV
Output Voltage Noise	$e_{n\_AV1/2}$	$V_{AVDD1/2}$ = 2.8V, f = 10Hz to 100kHz, $I_{AVDD1/2}$ = 0mA			9		μV_{RMS}
Power Supply Rejection Ratio	$PSRR_{\_VIN2\_AV1/2}$	V_{IN1} = 1.5V, V_{IN2} = 3.8V + 0.2V_{P-P}, $V_{AVDD1/2}$ = 2.8V, $I_{AVDD1/2}$ = 100mA, C_{IN2} = 100nF	f = 1kHz		90		dB
			f = 10kHz		85		
			f = 100kHz		70		
			f = 1MHz		55		
I^2C Timing and Performance							
SDA and SCL Logic Low Threshold	V_{IL}	V_{DD} = 1.2V				0.4	V
SDA and SCL Logic High Threshold	V_{IH}	V_{DD} = 1.2V		0.9			V

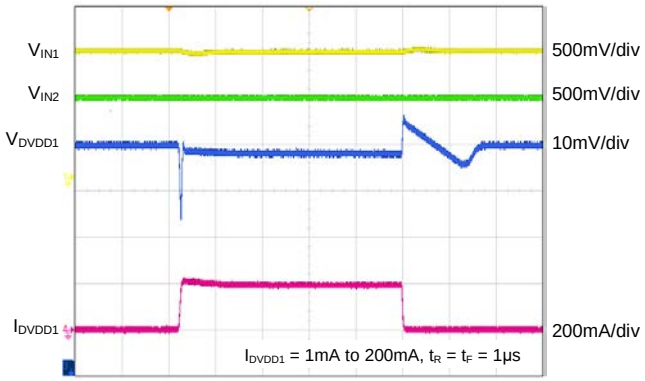
TIMING REQUIRMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}				400	kHz
Bus-Free Time between STOP and START Conditions	t_{BUF}		1.3			μs
START or Repeated Start Hold Time	t_{HDSTA}		0.6			μs
Repeated Start Setup Time	t_{SUSTA}		0.6			μs
STOP Condition Setup Time	t_{SUSTO}		0.6			μs
Date Hold Time	t_{HDDAT}		0			μs
Data Setup Time	t_{SUDAT}		100			ns
SCL Low Period	t_{LOW}		1.3			μs
SCL High Period	t_{HIGH}		0.6			μs
SCL and SDA Rise Time	t_R	V_{DD} = 1.2V	20		300	ns
SCL and SDA Fall Time	t_F	V_{DD} = 1.2V	4.4		300	ns
Data Valid Time	t_{VDDAT}				0.9	μs
Data Valid Acknowledge Time	t_{VDACK}				0.9	μs

TYPICAL PERFORMANCE CHARACTERISTICS

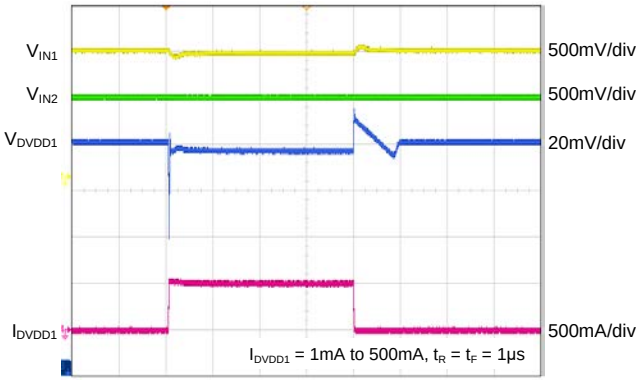
T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

DVDD1 Load Transient Response



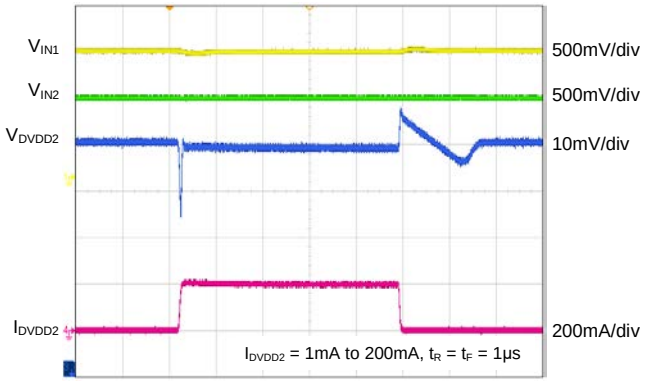
Time (20μs/div)

DVDD1 Load Transient Response



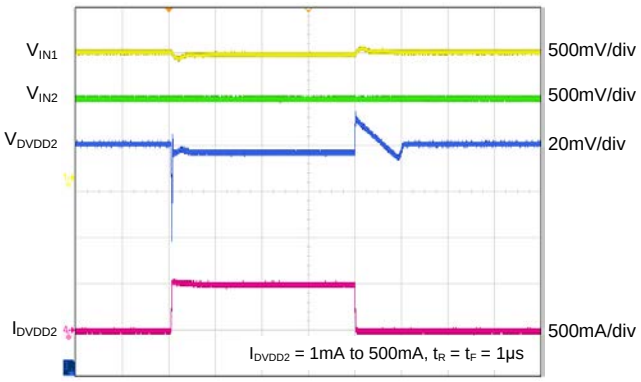
Time (50μs/div)

DVDD2 Load Transient Response



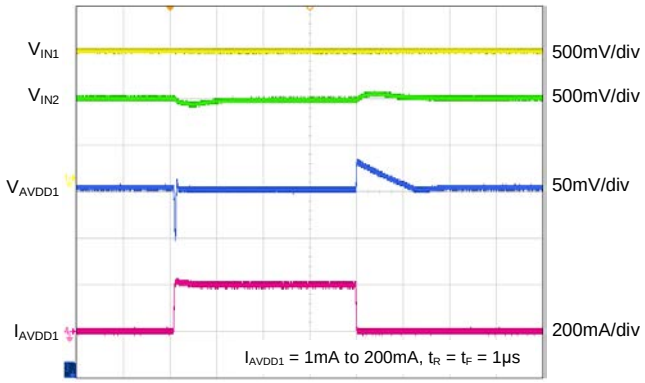
Time (20μs/div)

DVDD2 Load Transient Response



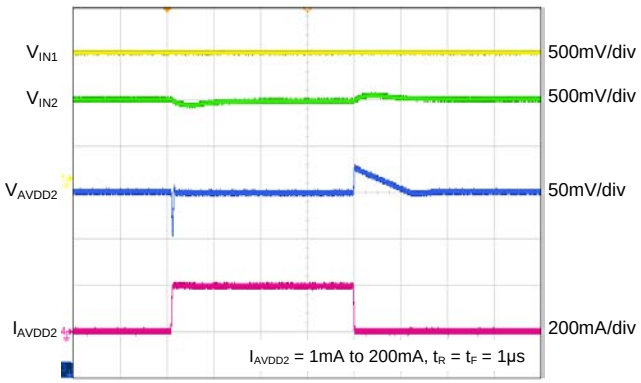
Time (50μs/div)

AVDD1 Load Transient Response



Time (50μs/div)

AVDD2 Load Transient Response

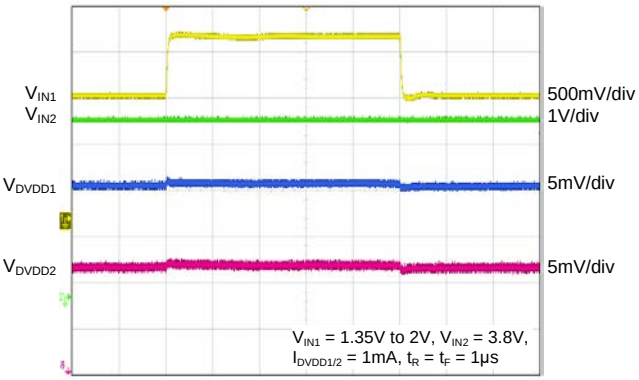


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

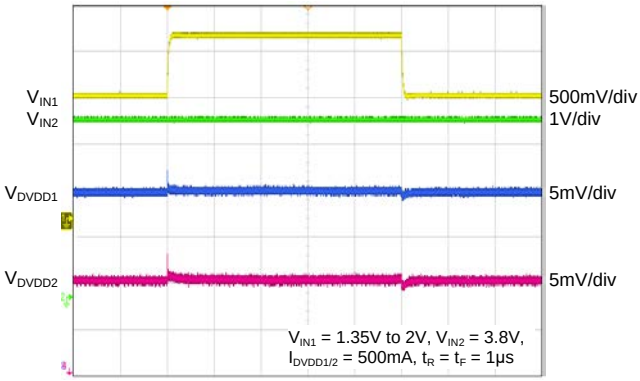
T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

DVDD1/2 Line Transient Response



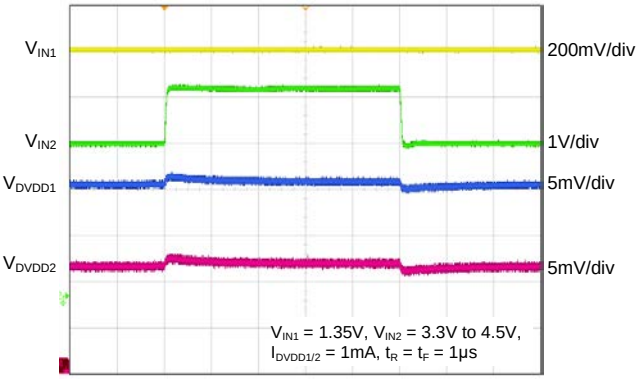
Time (200μs/div)

DVDD1/2 Line Transient Response



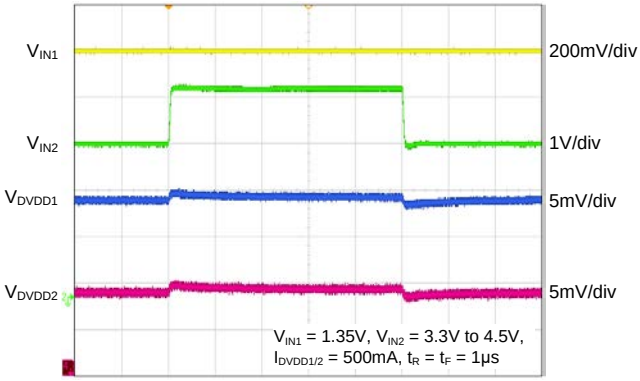
Time (200μs/div)

DVDD1/2 Line Transient Response



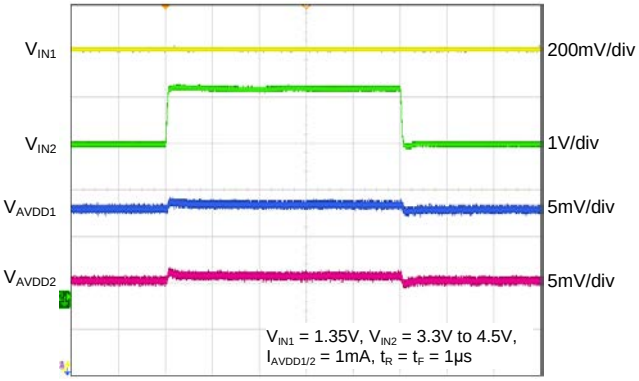
Time (200μs/div)

DVDD1/2 Line Transient Response



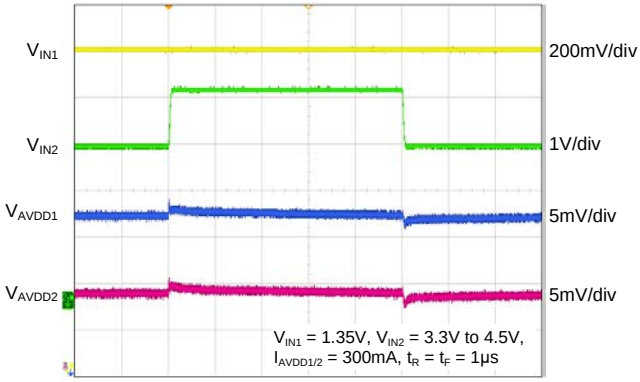
Time (200μs/div)

AVDD1/2 Line Transient Response



Time (200μs/div)

AVDD1/2 Line Transient Response

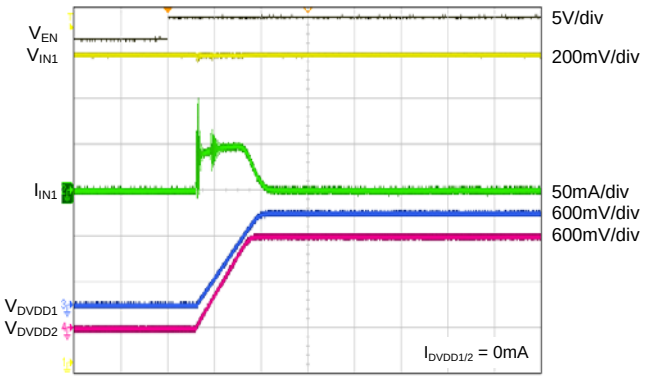


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

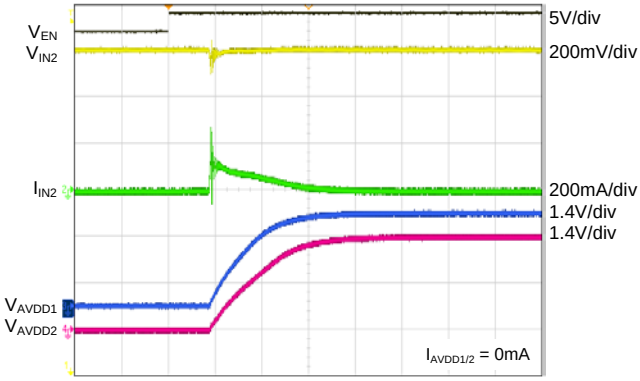
T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

EN Pin Startup (DVDD1/2)



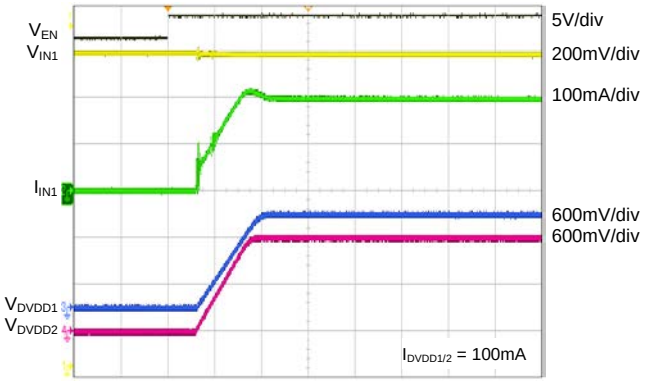
Time (200μs/div)

EN Pin Startup (AVDD1/2)



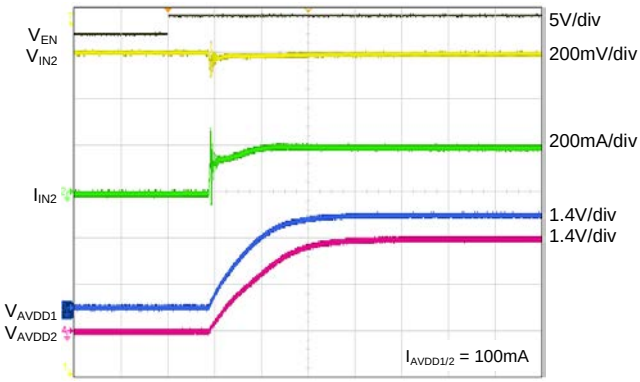
Time (200μs/div)

EN Pin Startup (DVDD1/2)



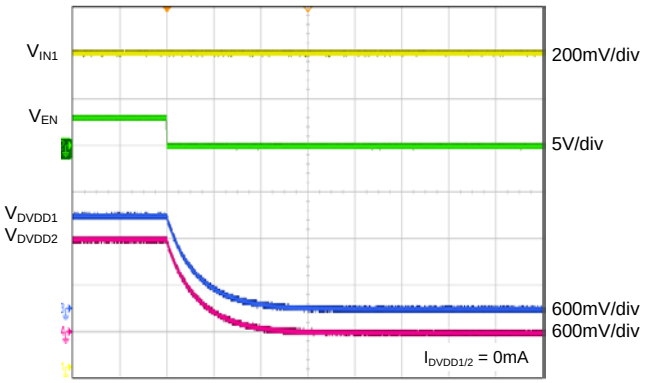
Time (200μs/div)

EN Pin Startup (AVDD1/2)



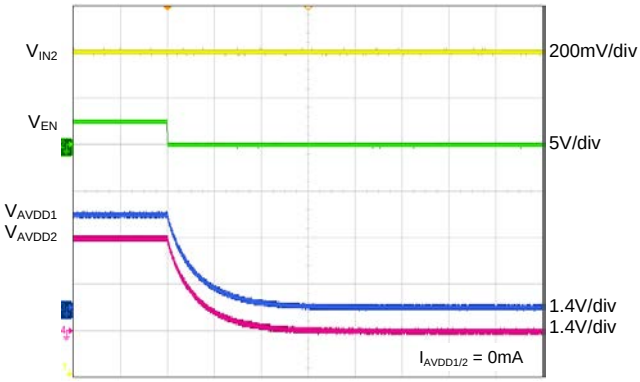
Time (200μs/div)

EN Pin Shutdown (DVDD1/2)



Time (2ms/div)

EN Pin Shutdown (AVDD1/2)

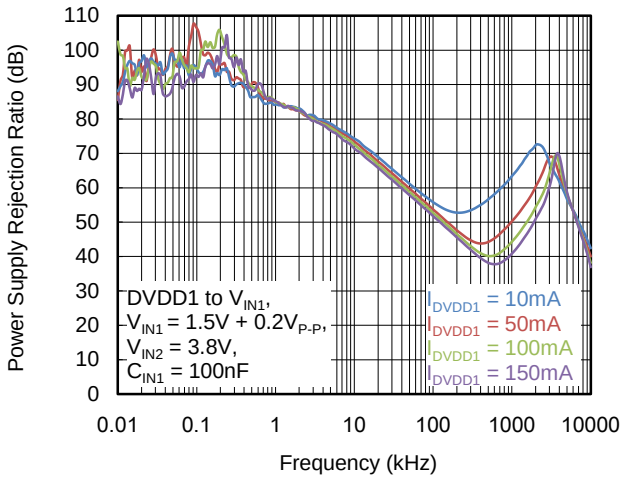


Time (2ms/div)

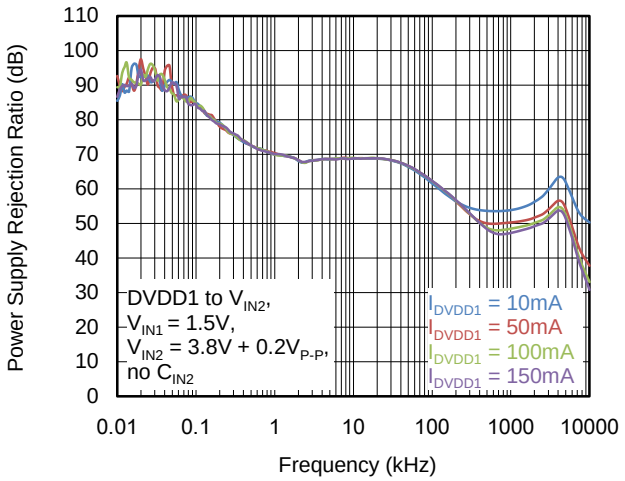
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

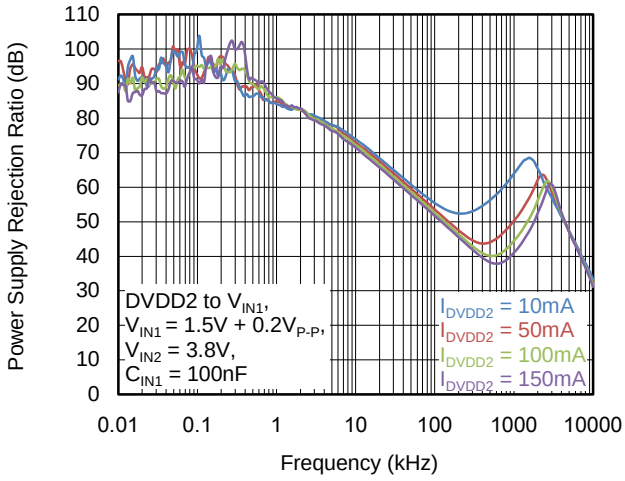
Power Supply Rejection Ratio vs. Frequency



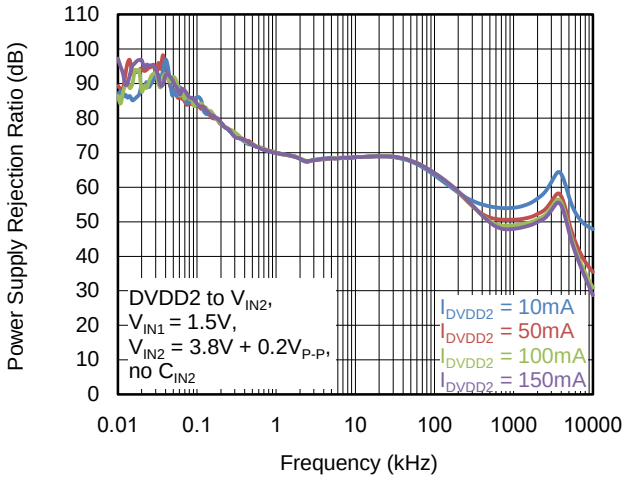
Power Supply Rejection Ratio vs. Frequency



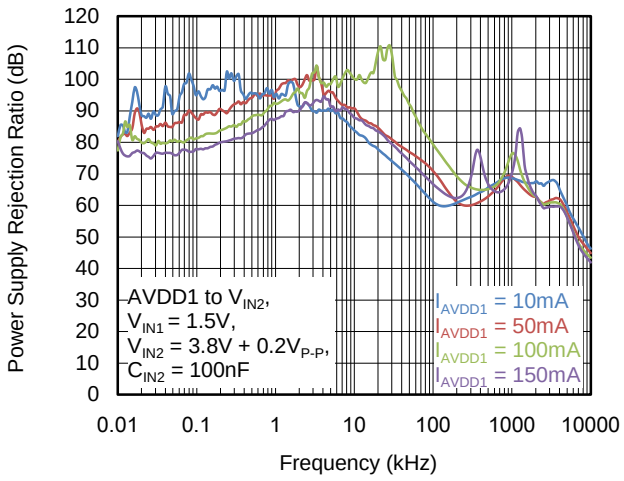
Power Supply Rejection Ratio vs. Frequency



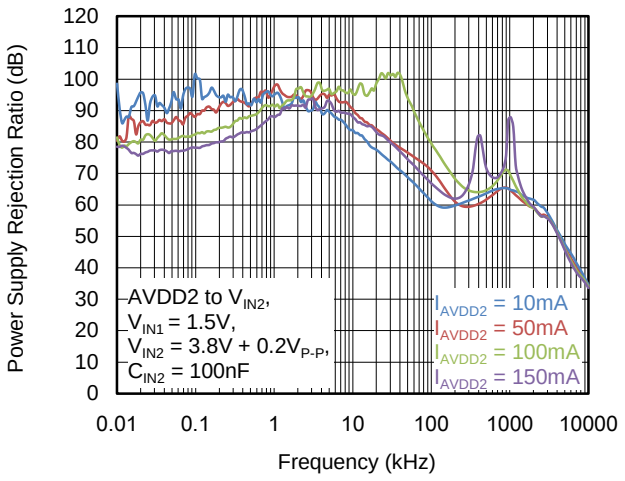
Power Supply Rejection Ratio vs. Frequency



Power Supply Rejection Ratio vs. Frequency



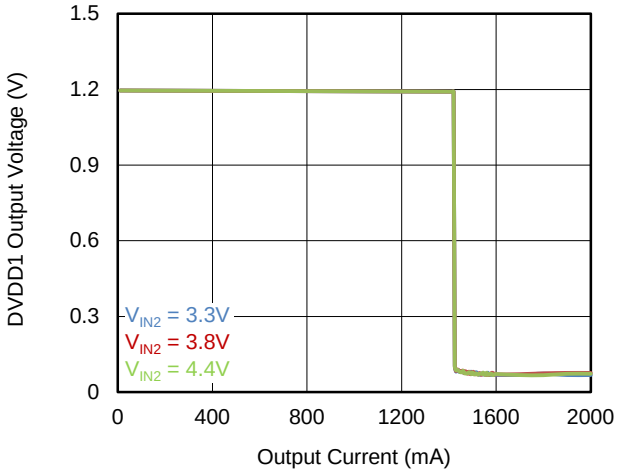
Power Supply Rejection Ratio vs. Frequency



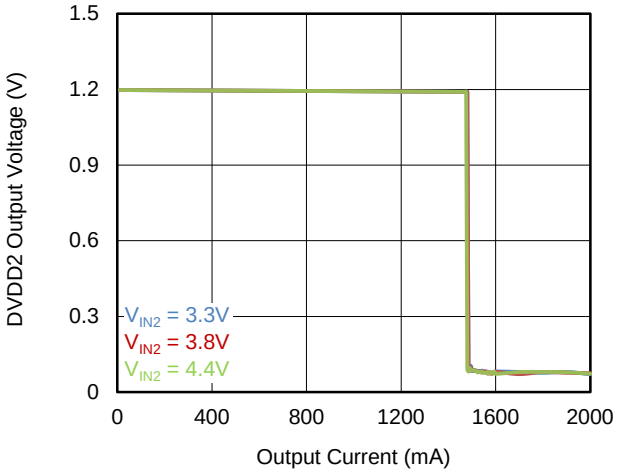
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

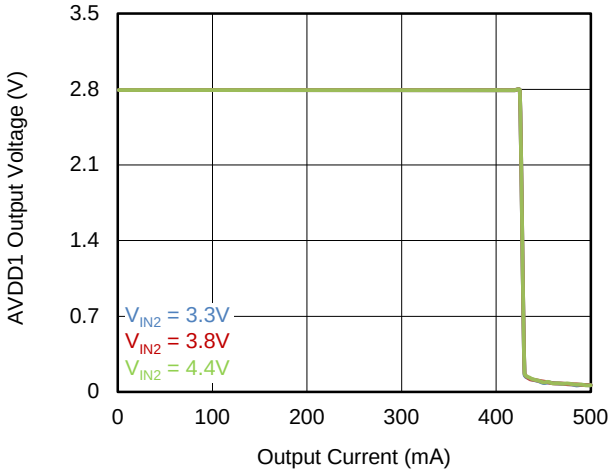
DVDD1 Output Voltage vs. Output Current



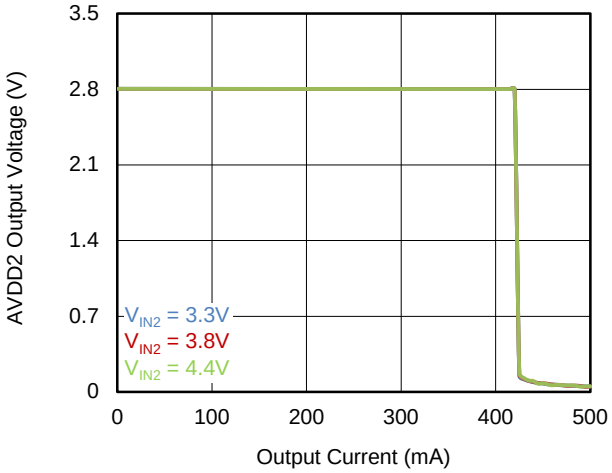
DVDD2 Output Voltage vs. Output Current



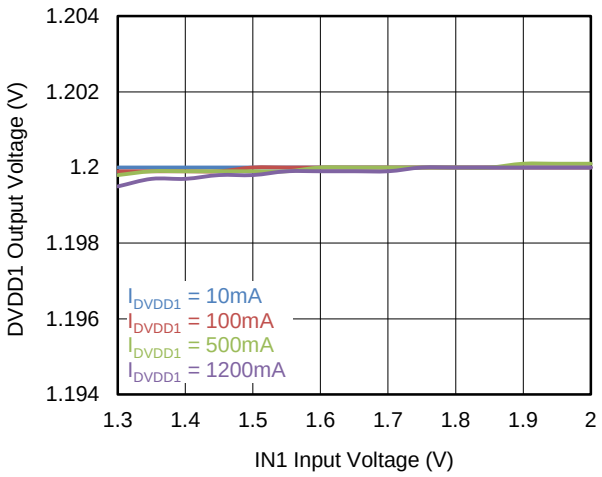
AVDD1 Output Voltage vs. Output Current



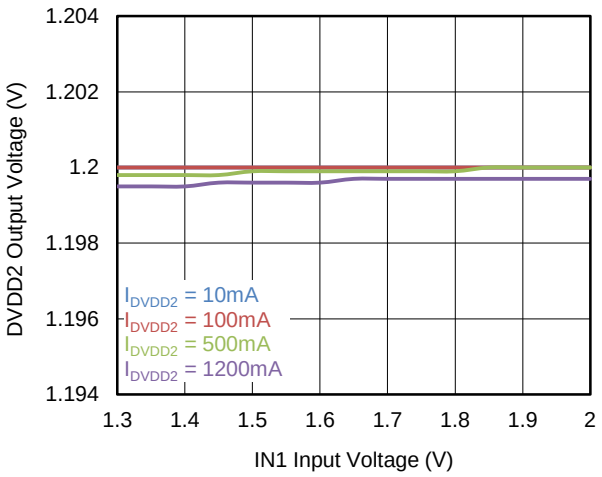
AVDD2 Output Voltage vs. Output Current



DVDD1 Output Voltage vs. IN1 Input Voltage



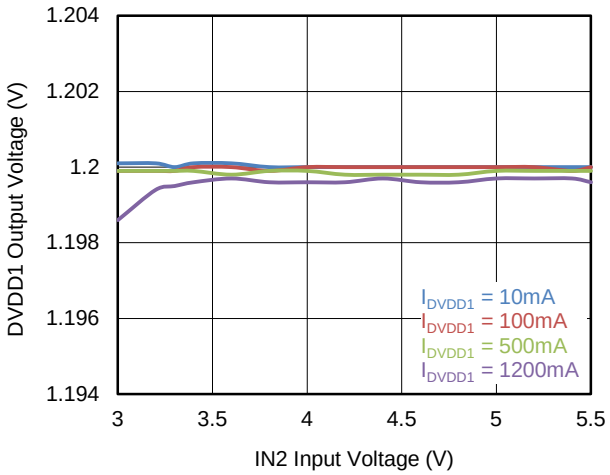
DVDD2 Output Voltage vs. IN1 Input Voltage



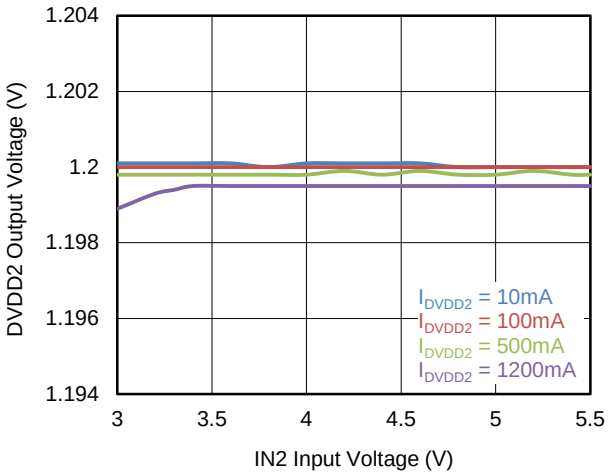
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

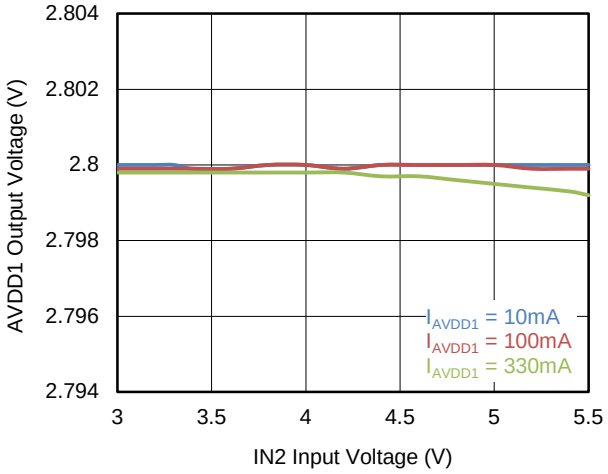
DVDD1 Output Voltage vs. IN2 Input Voltage



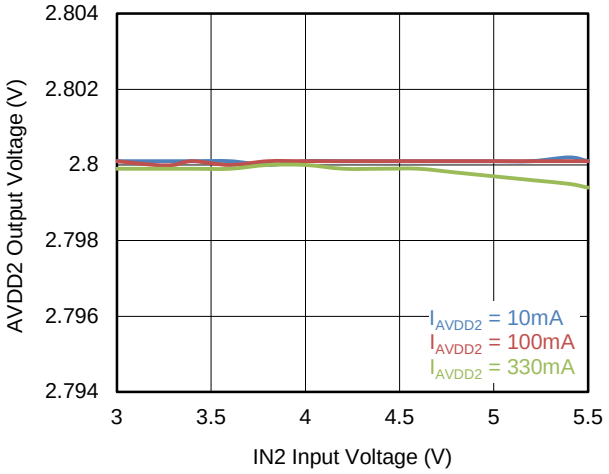
DVDD2 Output Voltage vs. IN2 Input Voltage



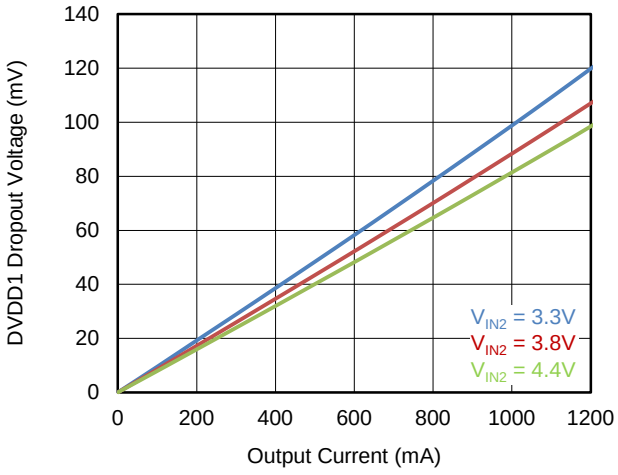
AVDD1 Output Voltage vs. IN2 Input Voltage



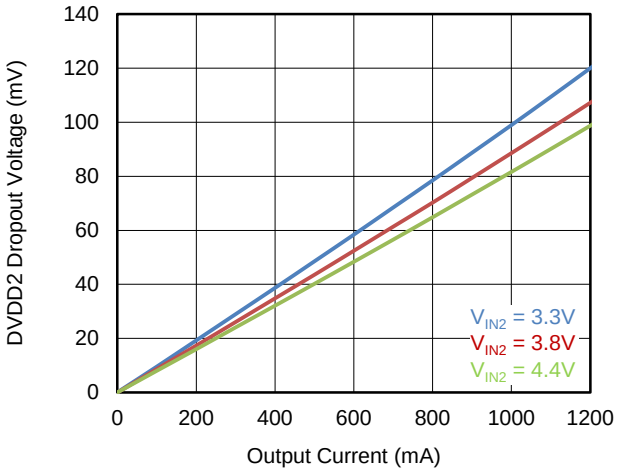
AVDD2 Output Voltage vs. IN2 Input Voltage



DVDD1 Dropout Voltage vs. Output Current



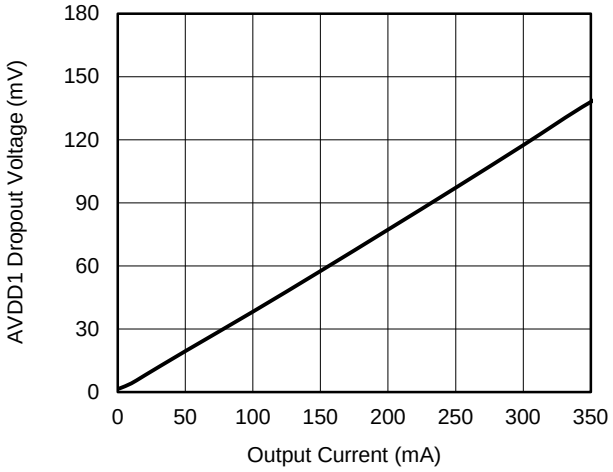
DVDD2 Dropout Voltage vs. Output Current



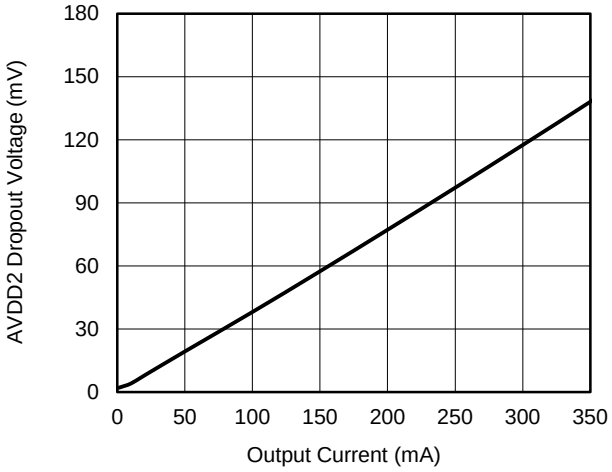
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, V_{IN1} = 1.35V, V_{IN2} = 3.8V, $V_{DVDD1/2}$ = 1.2V, $V_{AVDD1/2}$ = 2.8V, $C_{IN1/2}$ = 4.7μF, $C_{DVDD1/2}$ = 4.7μF, $C_{AVDD1/2}$ = 4.7μF, unless otherwise noted.

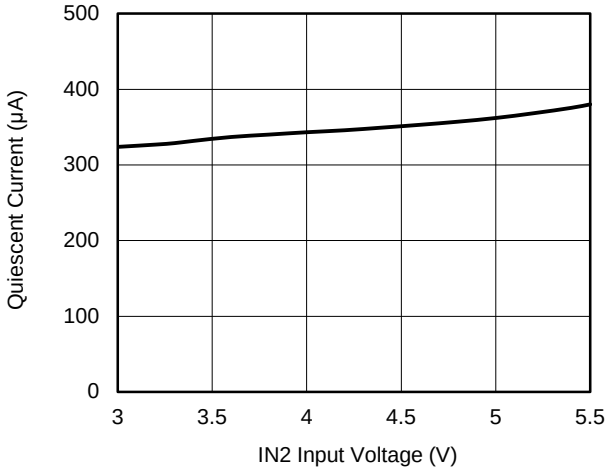
AVDD1 Dropout Voltage vs. Output Current



AVDD2 Dropout Voltage vs. Output Current



Quiescent Current vs. IN2 Input Voltage



DETAILED DESCRIPTION

The SGM38121 has 4 LDO regulators. Power up/down of each regulator can be controlled by the following three ways.

- Hardware Default On/off Setting
- Enable Register On/Off Setting via I^2C
- Programmable Time Slot Enable setting via I^2C

Hardware Default On/off Control

External EN pin toggles from low to high. It will force 4 LDO regulators powered up, of which output voltages are default voltages. Turn-on delay time is defined as the interval between the assertion of LDO output to the start of its ramp, and soft-start time means the time during soft-start ramp.

When external EN pin is high, the SGM38121 can ACK data from I^2C and update registers, but cannot power down LDOs and modify output voltages. Meanwhile, host can set enable control register to startup state, which will avoid LDO regulators powering down when external EN pin toggling from high to low.

Enable Register On/Off Control

The startup and shutdown of DVDD1/2 and AVDD1/2 channels can be controlled by enable control register, DVDD1/2_EN and AVDD1/2_EN bits, only if DVDD1/2_SEQ[3:0] and AVDD1/2_SEQ[3:0] bits set to ‘x000’. Before outputting, user can modify voltage level of each channel through output voltage level definition registers.

Programmable Time Slot Enable Control

The SGM38121 has 7 time slots to which each regulator can be assigned. Whichever regulator is assigned to the slot by setting its sequence number not equal to ‘x000’, the system can be powered up by setting SEQ_CTRL[1:0] to ‘01’. Then, SEQ_ON flips to high and SEQ_CTRL[1:0] is cleared to ‘00’ immediately.

Once SEQ_ON bit is high, SEQ_COUNT[2:0] starts incrementing from 0 (‘000’) to 7 (‘111’). If LDO’s sequence number is smaller than or equal to current SEQ_COUNT[2:0], this LDO will power up immediately. If SEQ_ON flips to low by setting SEQ_CTRL[1:0] to ‘10’, SEQ_COUNT[2:0] decrements from 7 (‘111’) to 0 (‘000’). The LDO will power off if its sequence number is larger than current SEQ_COUNT[2:0].

Besides, slot can be configured by SEQ_SPEED[1:0], which will take effect on the present slot if current slot time is less than the set value. Otherwise, SEQ_COUNT[2:0] will count up or down according to SEQ_ON bit or stop at the end.

It is recommended to use the same power up method to shut down specified LDOs.

Over-Temperature Protection

The SGM38121 includes over-temperature protection. If greater than +156℃, the PMIC is completely shut down.

Temperature hysteresis is incorporated, such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at the shutdown stage, they are ignored until the normal stage is reached. When the device cools enough to reach the normal stage and a start signal is present, the PMIC will power up immediately.

Output Over-Current Protection (OCP)

The LDOs are protected from excessive load and short-circuit. When an overload event occurs, the output current is automatically limited to the current limit. And once the current is limited, the LDO remains in current limit for fixed OCP deglitch timer. Then, the LDO will shut down, waiting for a hiccup timer to restart again. The restart will continue until faults disappear or new high priority faults (UVLO and OTP) appear, or user powers down this LDO output or the chip.

Output Under-Voltage Protection (UVP)

Under-voltage protection helps to quickly remove the potential excessive load and short-circuit fault. When an overload event occurs, the current is automatically limited to the current limit, at the same time the output voltage drops. Once the output voltage is below 90% and 80% for DVDD1/2 and AVDD1/2 respectively of the target output voltage, the LDO remains for a UVP deglitch timer before shutting down. Then, waiting for a hiccup timer, the shutdown LDO will ramp again without fault detection. If LDO is higher than 95% and 90% for DVDD1/2 and AVDD1/2 of the target voltage, LDO will not shut down again. The restart will continue until faults disappear or new priority faults (UVLO and OTP) appear, or user shuts down this LDO or the chip.

DETAILED DESCRIPTION (continued)

Output Discharge Setting

In default, the output discharge resistor set in auto mode. If users want to disconnect the output resistor, set MANUAL_DISCH bit to '1' into manual discharge mode. Then, set related bits to select output discharge function for discharge resistor. In case of normal shutdown (enable bit to low or SEQ_CTRL[1:0] to '10') and fault shutdown (UVLO, OCP, UVP, overheated), the output discharge setting is used. For load transient response, discharge function will not be considered.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM38121 parameters and get status reports. I²C is well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. The master generates the SCL signal. Slave devices have unique addresses to identify. The master is typically a micro controller or a digital signal processor.

The SGM38121 operates as a slave device that address is 0x28. It has sixteen 8-bit registers, numbered from REG00 to REG0F. A register read beyond REG0F (0x0F) returns 0xFF.

Physical Layer

The standard I²C interface of SGM38121 supports standard mode and fast mode communication speeds. The frequency of stand mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

REGISTER MAPS

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
CHIP_REV	0x00[7:0]				
MANUAL_DISCH	0x02[7]				
DVDD1					0x0E[0]
DVDD1_DISCH					0x02[0]
DVDD1_VOUT	0x03[7:0]				
DVDD1_SEQ	0x0A[3:0]				
DVDD2					0x0E[1]
DVDD2_DISCH					0x02[1]
DVDD2_VOUT	0x04[7:0]				
DVDD2_SEQ	0x0A[7:4]				
AVDD1					0x0E[2]
AVDD1_DISCH					0x02[2]
AVDD1_VOUT	0x05[7:0]				
AVDD1_SEQ	0x0B[3:0]				
AVDD2					0x0E[3]
AVDD2_DISCH					0x02[3]
AVDD2_VOUT	0x06[7:0]				
AVDD2_SEQ	0x0B[7:4]				
WAKEUP					0x07[2]
SEQ_CONTROL	0x0F[3]				0x0F[5:4]
SEQ_SPEED	0x0F[7:6]				
SEQ_COUNT	0x0F[2:0]				

REGISTER MAPS (continued)

I²C Slave Address of SGM38121: 0x28

Bit Types:
R: Read only
R/W: Read/Write

REG0x00: Chip Revision Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	CHIP_REV[7:0]	10000000	R	Indicates the device ID with revision.

REG0x02: Discharge Resistor Selection Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	MANUAL_DISCH	0	R/W	Discharge Mode Control 0 = Auto discharge mode, enable all LDOs discharge functions regardless of 0x02[3:0]. (default) 1 = Manual discharge mode, depending on 0x02[3:0] to enable discharge functions.
D[6:4]	Reserved	000	R/W	Reserved
D[3]	AVDD2_DISCH_EN	0	R/W	AVDD2 Discharge Resistor Enable/Disable Control 0 = Disable (default) 1 = Enable
D[2]	AVDD1_DISCH_EN	0	R/W	AVDD1 Discharge Resistor Enable/Disable Control 0 = Disable (default) 1 = Enable
D[1]	DVDD2_DISCH_EN	0	R/W	DVDD2 Discharge Resistor Enable/Disable Control 0 = Disable (default) 1 = Enable
D[0]	DVDD1_DISCH_EN	0	R/W	DVDD1 Discharge Resistor Enable/Disable Control 0 = Disable (default) 1 = Enable

REGISTER MAPS (continued)

REG0x03: DVDD1 Output Voltage Level Definition Register [Reset = 0x57]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
D[7:0]	DVDD1_VOUT[7:0]	01010111	R/W	Sets DVDD1 regulation target voltage. Equation: V_{DVDD1} = (504 + 8 × d) × 1mV, where d is the decimal value of the register.							
				Hex	**V_{DVDD1}**	**Hex**	**V_{DVDD1}**	**Hex**	**V_{DVDD1}**	**Hex**	**V_{DVDD1}**
				00	Reserved	40	1.016V	80	Reserved	C0	Reserved
				01	Reserved	41	1.024V	81	Reserved	C1	Reserved
				02	Reserved	42	1.032V	82	Reserved	C2	Reserved
				03	0.528V	43	1.040V	83	Reserved	C3	Reserved
				04	0.536V	44	1.048V	84	Reserved	C4	Reserved
				05	0.544V	45	1.056V	85	Reserved	C5	Reserved
				06	0.552V	46	1.064V	86	Reserved	C6	Reserved
				07	0.560V	47	1.072V	87	Reserved	C7	Reserved
				08	0.568V	48	1.080V	88	Reserved	C8	Reserved
				09	0.576V	49	1.088V	89	Reserved	C9	Reserved
				0A	0.584V	4A	1.096V	8A	Reserved	CA	Reserved
				0B	0.592V	4B	1.104V	8B	Reserved	CB	Reserved
				0C	0.600V	4C	1.112V	8C	Reserved	CC	Reserved
				0D	0.608V	4D	1.120V	8D	Reserved	CD	Reserved
				0E	0.616V	4E	1.128V	8E	Reserved	CE	Reserved
				0F	0.624V	4F	1.136V	8F	Reserved	CF	Reserved
				10	0.632V	50	1.144V	90	Reserved	D0	Reserved
				11	0.640V	51	1.152V	91	Reserved	D1	Reserved
				12	0.648V	52	1.160V	92	Reserved	D2	Reserved
				13	0.656V	53	1.168V	93	Reserved	D3	Reserved
				14	0.664V	54	1.176V	94	Reserved	D4	Reserved
				15	0.672V	55	1.184V	95	Reserved	D5	Reserved
				16	0.680V	56	1.192V	96	Reserved	D6	Reserved
				17	0.688V	**57**	**1.200V**	97	Reserved	D7	Reserved
				18	0.696V	58	1.208V	98	Reserved	D8	Reserved
				19	0.704V	59	1.216V	99	Reserved	D9	Reserved
				1A	0.712V	5A	1.224V	9A	Reserved	DA	Reserved
				1B	0.720V	5B	1.232V	9B	Reserved	DB	Reserved
				1C	0.728V	5C	1.240V	9C	Reserved	DC	Reserved
				1D	0.736V	5D	1.248V	9D	Reserved	DD	Reserved
				1E	0.744V	5E	1.256V	9E	Reserved	DE	Reserved
				1F	0.752V	5F	1.264V	9F	Reserved	DF	Reserved
				20	0.760V	60	1.272V	A0	Reserved	E0	Reserved
				21	0.768V	61	1.280V	A1	Reserved	E1	Reserved
				22	0.776V	62	1.288V	A2	Reserved	E2	Reserved
				23	0.784V	63	1.296V	A3	Reserved	E3	Reserved
				24	0.792V	64	1.304V	A4	Reserved	E4	Reserved
				25	0.800V	65	1.312V	A5	Reserved	E5	Reserved
				26	0.808V	66	1.320V	A6	Reserved	E6	Reserved

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{DVDD1}	Hex	V_{DVDD1}	Hex	V_{DVDD1}	Hex	V_{DVDD1}
D[7:0]	DVDD1_VOUT[7:0]	01010111	R/W	27	0.816V	67	1.328V	A7	Reserved	E7	Reserved
				28	0.824V	68	1.336V	A8	Reserved	E8	Reserved
				29	0.832V	69	1.344V	A9	Reserved	E9	Reserved
				2A	0.840V	6A	1.352V	AA	Reserved	EA	Reserved
				2B	0.848V	6B	1.360V	AB	Reserved	EB	Reserved
				2C	0.856V	6C	1.368V	AC	Reserved	EC	Reserved
				2D	0.864V	6D	1.376V	AD	Reserved	ED	Reserved
				2E	0.872V	6E	1.384V	AE	Reserved	EE	Reserved
				2F	0.880V	6F	1.392V	AF	Reserved	EF	Reserved
				30	0.888V	70	1.400V	B0	Reserved	F0	Reserved
				31	0.896V	71	1.408V	B1	Reserved	F1	Reserved
				32	0.904V	72	1.416V	B2	Reserved	F2	Reserved
				33	0.912V	73	1.424V	B3	Reserved	F3	Reserved
				34	0.920V	74	1.432V	B4	Reserved	F4	Reserved
				35	0.928V	75	1.440V	B5	Reserved	F5	Reserved
				36	0.936V	76	1.448V	B6	Reserved	F6	Reserved
				37	0.944V	77	1.456V	B7	Reserved	F7	Reserved
				38	0.952V	78	1.464V	B8	Reserved	F8	Reserved
				39	0.960V	79	1.472V	B9	Reserved	F9	Reserved
				3A	0.968V	7A	1.480V	BA	Reserved	FA	Reserved
				3B	0.976V	7B	1.488V	BB	Reserved	FB	Reserved
				3C	0.984V	7C	1.496V	BC	Reserved	FC	Reserved
				3D	0.992V	7D	1.504V	BD	Reserved	FD	Reserved
				3E	1.000V	7E	Reserved	BE	Reserved	FE	Reserved
				3F	1.008V	7F	Reserved	BF	Reserved	FF	Reserved

REGISTER MAPS (continued)

REG0x04: DVDD2 Output Voltage Level Definition Register [Reset = 0x57]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	DVDD2_VOUT[7:0]	01010111	R/W	Sets DVDD2 regulation target voltage. Equation: V_{DVDD2} = (504 + 8 × d) × 1mV, where d is the decimal value of the register.

Hex	V_{DVDD2}	Hex	V_{DVDD2}	Hex	V_{DVDD2}	Hex	V_{DVDD2}
00	Reserved	40	1.016V	80	Reserved	C0	Reserved
01	Reserved	41	1.024V	81	Reserved	C1	Reserved
02	Reserved	42	1.032V	82	Reserved	C2	Reserved
03	0.528V	43	1.040V	83	Reserved	C3	Reserved
04	0.536V	44	1.048V	84	Reserved	C4	Reserved
05	0.544V	45	1.056V	85	Reserved	C5	Reserved
06	0.552V	46	1.064V	86	Reserved	C6	Reserved
07	0.560V	47	1.072V	87	Reserved	C7	Reserved
08	0.568V	48	1.080V	88	Reserved	C8	Reserved
09	0.576V	49	1.088V	89	Reserved	C9	Reserved
0A	0.584V	4A	1.096V	8A	Reserved	CA	Reserved
0B	0.592V	4B	1.104V	8B	Reserved	CB	Reserved
0C	0.600V	4C	1.112V	8C	Reserved	CC	Reserved
0D	0.608V	4D	1.120V	8D	Reserved	CD	Reserved
0E	0.616V	4E	1.128V	8E	Reserved	CE	Reserved
0F	0.624V	4F	1.136V	8F	Reserved	CF	Reserved
10	0.632V	50	1.144V	90	Reserved	D0	Reserved
11	0.640V	51	1.152V	91	Reserved	D1	Reserved
12	0.648V	52	1.160V	92	Reserved	D2	Reserved
13	0.656V	53	1.168V	93	Reserved	D3	Reserved
14	0.664V	54	1.176V	94	Reserved	D4	Reserved
15	0.672V	55	1.184V	95	Reserved	D5	Reserved
16	0.680V	56	1.192V	96	Reserved	D6	Reserved
17	0.688V	**57**	**1.200V**	97	Reserved	D7	Reserved
18	0.696V	58	1.208V	98	Reserved	D8	Reserved
19	0.704V	59	1.216V	99	Reserved	D9	Reserved
1A	0.712V	5A	1.224V	9A	Reserved	DA	Reserved
1B	0.720V	5B	1.232V	9B	Reserved	DB	Reserved
1C	0.728V	5C	1.240V	9C	Reserved	DC	Reserved
1D	0.736V	5D	1.248V	9D	Reserved	DD	Reserved
1E	0.744V	5E	1.256V	9E	Reserved	DE	Reserved
1F	0.752V	5F	1.264V	9F	Reserved	DF	Reserved
20	0.760V	60	1.272V	A0	Reserved	E0	Reserved
21	0.768V	61	1.280V	A1	Reserved	E1	Reserved
22	0.776V	62	1.288V	A2	Reserved	E2	Reserved
23	0.784V	63	1.296V	A3	Reserved	E3	Reserved
24	0.792V	64	1.304V	A4	Reserved	E4	Reserved
25	0.800V	65	1.312V	A5	Reserved	E5	Reserved
26	0.808V	66	1.320V	A6	Reserved	E6	Reserved

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{DVDD2}	Hex	V_{DVDD2}	Hex	V_{DVDD2}	Hex	V_{DVDD2}
D[7:0]	DVDD2_VOUT[7:0]	01010111	R/W	27	0.816V	67	1.328V	A7	Reserved	E7	Reserved
				28	0.824V	68	1.336V	A8	Reserved	E8	Reserved
				29	0.832V	69	1.344V	A9	Reserved	E9	Reserved
				2A	0.840V	6A	1.352V	AA	Reserved	EA	Reserved
				2B	0.848V	6B	1.360V	AB	Reserved	EB	Reserved
				2C	0.856V	6C	1.368V	AC	Reserved	EC	Reserved
				2D	0.864V	6D	1.376V	AD	Reserved	ED	Reserved
				2E	0.872V	6E	1.384V	AE	Reserved	EE	Reserved
				2F	0.880V	6F	1.392V	AF	Reserved	EF	Reserved
				30	0.888V	70	1.400V	B0	Reserved	F0	Reserved
				31	0.896V	71	1.408V	B1	Reserved	F1	Reserved
				32	0.904V	72	1.416V	B2	Reserved	F2	Reserved
				33	0.912V	73	1.424V	B3	Reserved	F3	Reserved
				34	0.920V	74	1.432V	B4	Reserved	F4	Reserved
				35	0.928V	75	1.440V	B5	Reserved	F5	Reserved
				36	0.936V	76	1.448V	B6	Reserved	F6	Reserved
				37	0.944V	77	1.456V	B7	Reserved	F7	Reserved
				38	0.952V	78	1.464V	B8	Reserved	F8	Reserved
				39	0.960V	79	1.472V	B9	Reserved	F9	Reserved
				3A	0.968V	7A	1.480V	BA	Reserved	FA	Reserved
				3B	0.976V	7B	1.488V	BB	Reserved	FB	Reserved
				3C	0.984V	7C	1.496V	BC	Reserved	FC	Reserved
				3D	0.992V	7D	1.504V	BD	Reserved	FD	Reserved
				3E	1.000V	7E	Reserved	BE	Reserved	FE	Reserved
				3F	1.008V	7F	Reserved	BF	Reserved	FF	Reserved

REGISTER MAPS (continued)

REG0x05: AVDD1 Output Voltage Level Definition Register [Reset = 0xB1]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	AVDD1_VOUT[7:0]	10110001	R/W	Sets AVDD1 regulation target voltage. Equation: V_{AVDD1} = (1384 + 8 × d) × 1mV, where d is the decimal value of the register.

Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}
00	Reserved	40	1.896V	80	2.408V	C0	2.920V
01	Reserved	41	1.904V	81	2.416V	C1	2.928V
02	Reserved	42	1.912V	82	2.424V	C2	2.936V
03	Reserved	43	1.920V	83	2.432V	C3	2.944V
04	Reserved	44	1.928V	84	2.440V	C4	2.952V
05	Reserved	45	1.936V	85	2.448V	C5	2.960V
06	Reserved	46	1.944V	86	2.456V	C6	2.968V
07	Reserved	47	1.952V	87	2.464V	C7	2.976V
08	Reserved	48	1.960V	88	2.472V	C8	2.984V
09	Reserved	49	1.968V	89	2.480V	C9	2.992V
0A	Reserved	4A	1.976V	8A	2.488V	CA	3.000V
0B	Reserved	4B	1.984V	8B	2.496V	CB	3.008V
0C	Reserved	4C	1.992V	8C	2.504V	CC	3.016V
0D	Reserved	4D	2.000V	8D	2.512V	CD	3.024V
0E	Reserved	4E	2.008V	8E	2.520V	CE	3.032V
0F	1.504V	4F	2.016V	8F	2.528V	CF	3.040V
10	1.512V	50	2.024V	90	2.536V	D0	3.048V
11	1.520V	51	2.032V	91	2.544V	D1	3.056V
12	1.528V	52	2.040V	92	2.552V	D2	3.064V
13	1.536V	53	2.048V	93	2.560V	D3	3.072V
14	1.544V	54	2.056V	94	2.568V	D4	3.080V
15	1.552V	55	2.064V	95	2.576V	D5	3.088V
16	1.560V	56	2.072V	96	2.584V	D6	3.096V
17	1.568V	57	2.080V	97	2.592V	D7	3.104V
18	1.576V	58	2.088V	98	2.600V	D8	3.112V
19	1.584V	59	2.096V	99	2.608V	D9	3.120V
1A	1.592V	5A	2.104V	9A	2.616V	DA	3.128V
1B	1.600V	5B	2.112V	9B	2.624V	DB	3.136V
1C	1.608V	5C	2.120V	9C	2.632V	DC	3.144V
1D	1.616V	5D	2.128V	9D	2.640V	DD	3.152V
1E	1.624V	5E	2.136V	9E	2.648V	DE	3.160V
1F	1.632V	5F	2.144V	9F	2.656V	DF	3.168V
20	1.640V	60	2.152V	A0	2.664V	E0	3.176V
21	1.648V	61	2.160V	A1	2.672V	E1	3.184V
22	1.656V	62	2.168V	A2	2.680V	E2	3.192V
23	1.664V	63	2.176V	A3	2.688V	E3	3.200V
24	1.672V	64	2.184V	A4	2.696V	E4	3.208V
25	1.680V	65	2.192V	A5	2.704V	E5	3.216V
26	1.688V	66	2.200V	A6	2.712V	E6	3.224V

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}	Hex	V_{AVDD1}
				27	1.696V	67	2.208V	A7	2.720V	E7	3.232V
				28	1.704V	68	2.216V	A8	2.728V	E8	3.240V
				29	1.712V	69	2.224V	A9	2.736V	E9	3.248V
				2A	1.720V	6A	2.232V	AA	2.744V	EA	3.256V
				2B	1.728V	6B	2.240V	AB	2.752V	EB	3.264V
				2C	1.736V	6C	2.248V	AC	2.760V	EC	3.272V
				2D	1.744V	6D	2.256V	AD	2.768V	ED	3.280V
				2E	1.752V	6E	2.264V	AE	2.776V	EE	3.288V
				2F	1.760V	6F	2.272V	AF	2.784V	EF	3.296V
				30	1.768V	70	2.280V	B0	2.792V	F0	3.304V
				31	1.776V	71	2.288V	B1	2.800V	F1	3.312V
				32	1.784V	72	2.296V	B2	2.808V	F2	3.320V
D[7:0]	AVDD1_VOUT[7:0]	10110001	R/W	33	1.792V	73	2.304V	B3	2.816V	F3	3.328V
				34	1.800V	74	2.312V	B4	2.824V	F4	3.336V
				35	1.808V	75	2.320V	B5	2.832V	F5	3.344V
				36	1.816V	76	2.328V	B6	2.840V	F6	3.352V
				37	1.824V	77	2.336V	B7	2.848V	F7	3.360V
				38	1.832V	78	2.344V	B8	2.856V	F8	3.368V
				39	1.840V	79	2.352V	B9	2.864V	F9	3.376V
				3A	1.848V	7A	2.360V	BA	2.872V	FA	3.384V
				3B	1.856V	7B	2.368V	BB	2.880V	FB	3.392V
				3C	1.864V	7C	2.376V	BC	2.888V	FC	3.400V
				3D	1.872V	7D	2.384V	BD	2.896V	FD	3.408V
				3E	1.880V	7E	2.392V	BE	2.904V	FE	3.416V
				3F	1.888V	7F	2.400V	BF	2.912V	FF	3.424V

REGISTER MAPS (continued)

REG0x06: AVDD2 Output Voltage Level Definition Register [Reset = 0xB1]

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	AVDD2_VOUT[7:0]	10110001	R/W	Sets AVDD2 regulation target voltage. Equation: V_{AVDD2} = (1384 + 8 × d) × 1mV, where d is the decimal value of the register.

Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}
00	Reserved	40	1.896V	80	2.408V	C0	2.920V
01	Reserved	41	1.904V	81	2.416V	C1	2.928V
02	Reserved	42	1.912V	82	2.424V	C2	2.936V
03	Reserved	43	1.920V	83	2.432V	C3	2.944V
04	Reserved	44	1.928V	84	2.440V	C4	2.952V
05	Reserved	45	1.936V	85	2.448V	C5	2.960V
06	Reserved	46	1.944V	86	2.456V	C6	2.968V
07	Reserved	47	1.952V	87	2.464V	C7	2.976V
08	Reserved	48	1.960V	88	2.472V	C8	2.984V
09	Reserved	49	1.968V	89	2.480V	C9	2.992V
0A	Reserved	4A	1.976V	8A	2.488V	CA	3.000V
0B	Reserved	4B	1.984V	8B	2.496V	CB	3.008V
0C	Reserved	4C	1.992V	8C	2.504V	CC	3.016V
0D	Reserved	4D	2.000V	8D	2.512V	CD	3.024V
0E	Reserved	4E	2.008V	8E	2.520V	CE	3.032V
0F	1.504V	4F	2.016V	8F	2.528V	CF	3.040V
10	1.512V	50	2.024V	90	2.536V	D0	3.048V
11	1.520V	51	2.032V	91	2.544V	D1	3.056V
12	1.528V	52	2.040V	92	2.552V	D2	3.064V
13	1.536V	53	2.048V	93	2.560V	D3	3.072V
14	1.544V	54	2.056V	94	2.568V	D4	3.080V
15	1.552V	55	2.064V	95	2.576V	D5	3.088V
16	1.560V	56	2.072V	96	2.584V	D6	3.096V
17	1.568V	57	2.080V	97	2.592V	D7	3.104V
18	1.576V	58	2.088V	98	2.600V	D8	3.112V
19	1.584V	59	2.096V	99	2.608V	D9	3.120V
1A	1.592V	5A	2.104V	9A	2.616V	DA	3.128V
1B	1.600V	5B	2.112V	9B	2.624V	DB	3.136V
1C	1.608V	5C	2.120V	9C	2.632V	DC	3.144V
1D	1.616V	5D	2.128V	9D	2.640V	DD	3.152V
1E	1.624V	5E	2.136V	9E	2.648V	DE	3.160V
1F	1.632V	5F	2.144V	9F	2.656V	DF	3.168V
20	1.640V	60	2.152V	A0	2.664V	E0	3.176V
21	1.648V	61	2.160V	A1	2.672V	E1	3.184V
22	1.656V	62	2.168V	A2	2.680V	E2	3.192V
23	1.664V	63	2.176V	A3	2.688V	E3	3.200V
24	1.672V	64	2.184V	A4	2.696V	E4	3.208V
25	1.680V	65	2.192V	A5	2.704V	E5	3.216V
26	1.688V	66	2.200V	A6	2.712V	E6	3.224V

BITS	NAME	DEFAULT	TYPE	DESCRIPTION							
				Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}	Hex	V_{AVDD2}
				27	1.696V	67	2.208V	A7	2.720V	E7	3.232V
				28	1.704V	68	2.216V	A8	2.728V	E8	3.240V
				29	1.712V	69	2.224V	A9	2.736V	E9	3.248V
				2A	1.720V	6A	2.232V	AA	2.744V	EA	3.256V
				2B	1.728V	6B	2.240V	AB	2.752V	EB	3.264V
				2C	1.736V	6C	2.248V	AC	2.760V	EC	3.272V
				2D	1.744V	6D	2.256V	AD	2.768V	ED	3.280V
				2E	1.752V	6E	2.264V	AE	2.776V	EE	3.288V
				2F	1.760V	6F	2.272V	AF	2.784V	EF	3.296V
				30	1.768V	70	2.280V	B0	2.792V	F0	3.304V
				31	1.776V	71	2.288V	B1	2.800V	F1	3.312V
				32	1.784V	72	2.296V	B2	2.808V	F2	3.320V
D[7:0]	AVDD2_VOUT[7:0]	10110001	R/W	33	1.792V	73	2.304V	B3	2.816V	F3	3.328V
				34	1.800V	74	2.312V	B4	2.824V	F4	3.336V
				35	1.808V	75	2.320V	B5	2.832V	F5	3.344V
				36	1.816V	76	2.328V	B6	2.840V	F6	3.352V
				37	1.824V	77	2.336V	B7	2.848V	F7	3.360V
				38	1.832V	78	2.344V	B8	2.856V	F8	3.368V
				39	1.840V	79	2.352V	B9	2.864V	F9	3.376V
				3A	1.848V	7A	2.360V	BA	2.872V	FA	3.384V
				3B	1.856V	7B	2.368V	BB	2.880V	FB	3.392V
				3C	1.864V	7C	2.376V	BC	2.888V	FC	3.400V
				3D	1.872V	7D	2.384V	BD	2.896V	FD	3.408V
				3E	1.880V	7E	2.392V	BE	2.904V	FE	3.416V
				3F	1.888V	7F	2.400V	BF	2.912V	FF	3.424V

REG0x07: Function Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2]	WAKE_UP_EN	0	R/W	Wakeup Function Control 0 = disable wakeup function (default) 1 = enable wakeup function When wakeup function is enabled, the chip will reset DVDD1/2_EN, AVDD1/2_EN, DVDD1/2_SEQ and AVDD1/2_SEQ, when SCL pin lasts for 3.8s below logic low threshold.
D[1:0]	Reserved	00	R/W	Reserved

REGISTER MAPS (continued)

REG0x0A: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	DVDD2_SEQ[3:0]	0000	R/W	There are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shutdown start from slot7 to slot1. Power-up and shutdown of each LDO regulator can be set at any one of the slots. x000 = Controlled by I^2C register 0x0E[3:0] x001 = Slot1 x010 = Slot2 x011 = Slot3 x100 = Slot4 x101 = Slot5 x110 = Slot6 x111 = Slot7
D[3:0]	DVDD1_SEQ[3:0]	0000	R/W	

REG0x0B: Power Sequence Setting Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	AVDD2_SEQ[3:0]	0000	R/W	There are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shutdown start from slot7 to slot1. Power-up and shutdown of each LDO regulator can be set at any one of the slots. x000 = Controlled by I^2C register 0x0E[3:0] x001 = Slot1 x010 = Slot2 x011 = Slot3 x100 = Slot4 x101 = Slot5 x110 = Slot6 x111 = Slot7
D[3:0]	AVDD1_SEQ[3:0]	0000	R/W	

REG0x0E: Enable Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000	R/W	Reserved
D[3]	AVDD2_EN	0	R/W	Chip enable control register by I^2C while the register value of DVDD1/2_SEQ[3:0] and AVDD1/2_SEQ[3:0] are set to default '0000'. This register can be written to enable or disable the corresponding LDO regulator. Bit0 for DVDD1_EN Bit1 for DVDD2_EN Bit2 for AVDD1_EN Bit3 for AVDD2_EN 0 = disable (default) 1 = enable
D[2]	AVDD1_EN	0	R/W	
D[1]	DVDD2_EN	0	R/W	
D[0]	DVDD1_EN	0	R/W	

REGISTER MAPS (continued)

REG0x0F: Sequence Control Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	SEQ_SPEED[1:0]	00	R/W	Define the slot period as following: 00 = 2.00ms (default) 01 = 1.00ms 10 = 0.50ms 11 = 0.25ms
D[5:4]	SEQ_CTRL[1:0]	00	R/W	Enables power-up or shutdown of SEQ. Write and clear: 00 = Standby (default) 01 = Power-Up 10 = Shutdown 11 = Ignored
D[3]	SEQ_ON	0	R	Indicates the activation signal of SEQ. Read only: 0 = Shutdown (default) 1 = Power-Up
D[2:0]	SEQ_COUNT[2:0]	000	R	Indicates the slot number of SEQ at the moment. Read only: 000 = No LDO starts (default) 001 = Slot1 starts 010 = Slot2 starts 011 = Slot3 starts 100 = Slot4 starts 101 = Slot5 starts 110 = Slot6 starts 111 = Slot7 starts and stop counting

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

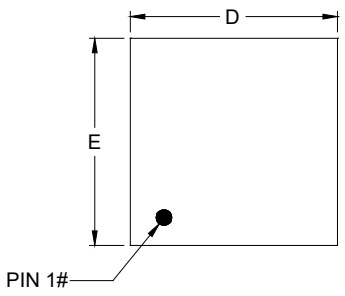
SEPTEMBER 2024 – REV.A.1 to REV.A.2	Page
Updated Typical Application Circuit	4

MAY 2024 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	5, 6

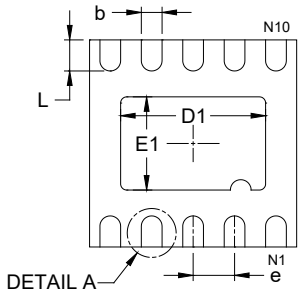
Changes from Original (MAY 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

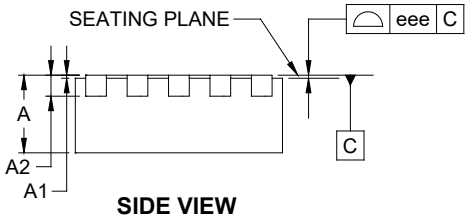
TDFN-2×2-10L



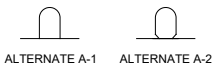
TOP VIEW



BOTTOM VIEW

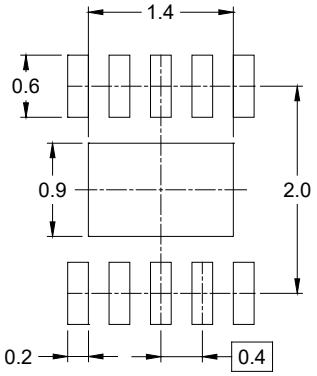


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



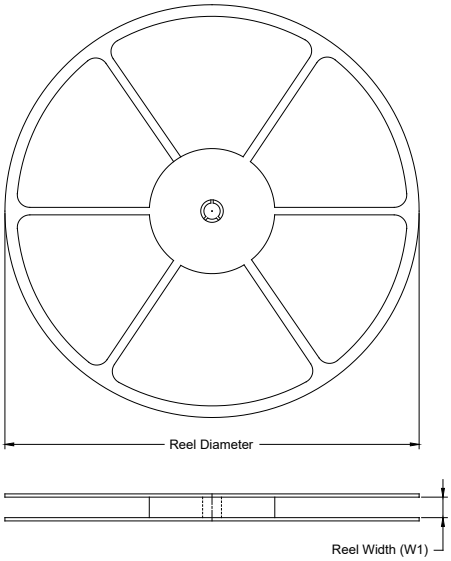
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	-	0.250
D	1.900	-	2.100
D1	1.300	-	1.500
E	1.900	-	2.100
E1	0.800	-	1.000
e	0.400 BSC		
L	0.200	-	0.400
eee	0.080		

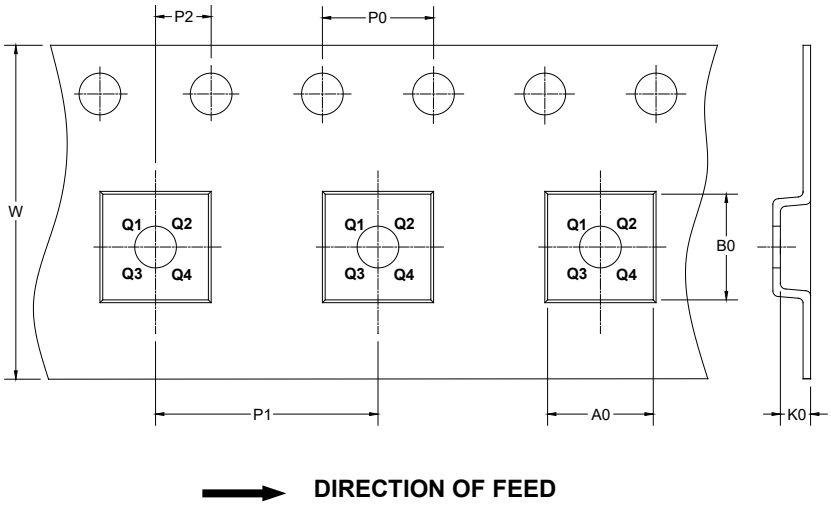
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

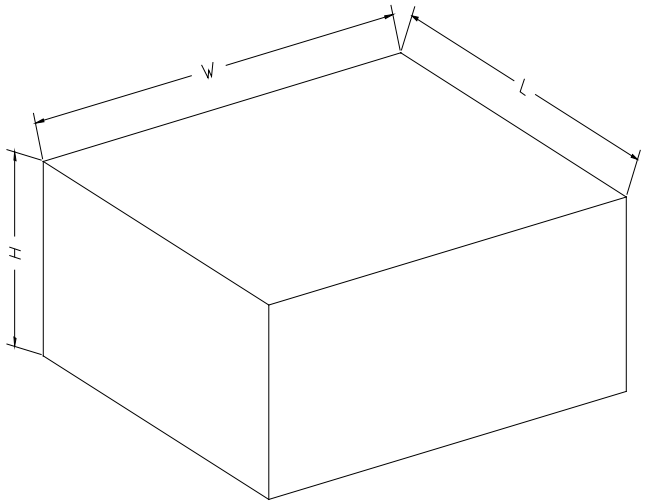
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-10L	7"	9.5	2.30	2.30	1.00	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002