SGM90116H
3-Series to 16-Series High Accuracy Battery Monitor and Protector

GENERAL DESCRIPTION

The SGM90116H is an analog front end (AFE) which is specified for general purpose monitoring and protecting of stacked Li-Ion, Li-polymer, and LiFePO4 batteries. The device can monitor 3-series to 16-series battery cells.

The device supports autonomous and host controlled cell balancing.

The device supports software configurable primary protection and secondary protection.

The device has an on-chip charge up and supports low-side NFET drivers.

The device supports 100kHz I^2C standards communication interface.

The SGM90116H is available in a Green TSSOP-38 package.

APPLICATIONS

Battery Pack Management
E-Bike and E-Scooter
Battery Powered Electric Tools and Garden Tools
Unmanned Aerial Vehicle
Industrial Power Storage Battery Pack

FEATURES

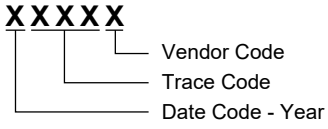
- **Monitor 3-Series to 16-Series Cells**
- **Integrated Secondary Chemical Fuse Drive Protection**
- **Two Independent ADCs**
- **High Accuracy Coulomb Counter with ±2LSB (TYP) Input Offset Error**
- **High Accuracy Cell Voltage Measurement ±2.5mV (TYP)**
- **Support Simultaneous Current and Voltage Sampling**
- **Multiple Working Modes**
- **Support Temperature Sensing Using Internal Sensor and up to 3 External Thermistors**
- **Tolerant of Random Cell Attach Sequence on Production Line**
- **Programmable LDO for External System Power**
- **Available in a Green TSSOP-38 Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM90116H	TSSOP-38	-40℃ to +85℃	SGM90116HYTS38G/TR	SGM90116H YTS38 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VC(n) - VC(n-1) ..... -0.3V to 80V
Supply Voltage, V_{BAT} ..... -0.3V to 80V
Cell Input Pins Voltage ..... -0.3V to 80V
SRN, SRP Input Voltage ..... -0.3V to 1.98V
SCL, SDA Input Voltage ..... -0.3V to V_{REGOUT}
REGSRC Input Voltage ..... -0.3V to 80V
REGOUT, ALERT Output Voltage ..... -0.3V to 6.6V
DSG Output Voltage ..... -0.3V to 20V
CHG Output Voltage ..... -0.3V to $V_{CHGCLAMP}$
Cell Balancing Current (Per Cell), I_{CB} 50mA
Package Thermal Resistance
TSSOP-38, θ_{JA} ..... 56.6℃/W
TSSOP-38, θ_{JB} ..... 30.1℃/W
TSSOP-38, θ_{JC} ..... 16.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±1500V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{BAT} ..... 6V to 72V
Cell Input Pins Voltage ..... 0V to 6.55V
SRP - SRN Input Voltage ..... -200mV to 200mV
SCL, SDA Input Voltage ..... 0V to V_{REGOUT}
TSx - VSS Input Voltage ..... 0V to 1.8V
REGSRC Input Voltage ..... 6V to 25V
CHG, DSG Output Voltage ..... 0V to 16V
REGOUT Output Voltage ..... 0V to 5V
ALERT Output Voltage ..... 0V to V_{REGOUT}
Cell Balancing Current (Per Cell), I_{CB} ..... 0mA to 50mA
External Cell Input Resistance, R_C ..... 20Ω to 100Ω
External Cell Input Capacitance, C_C ..... 0.1μF to 1μF
External Supply Filter Resistance, R_F 40Ωto 1kΩ
External Supply Filter Capacitance, C_F ..... 1μF to 10μF
Sense Resistor Filter Resistance, R_{FILT} 100Ω
ALERT Pin to VSS Resistor, R_{ALERT} 1MΩ
REGOUT Loading Capacitance, C_L 1μF
REGSRC Input Capacitance, C_I 1μF
CAP1, CAP2 (Output Capacitance), C_{CAP} 1μF
External Thermistor Nominal Resistance (103AT) at +25℃, R_{TS} 10kΩ
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

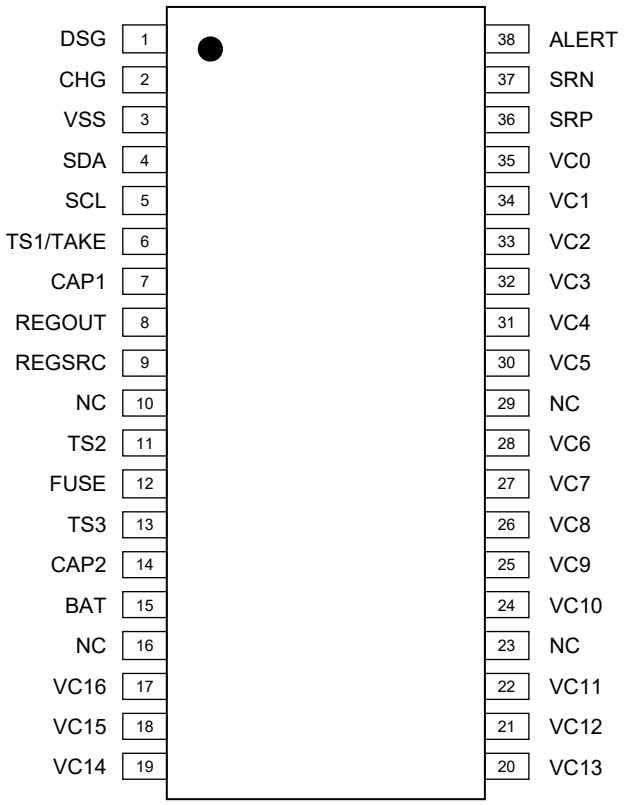
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-38

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	DSG	AO	Discharge FET Driver.
2	CHG	AO	Charge FET Driver.
3	VSS	GND	Ground.
4	SDA	DI/DO	I^2C Interface, Serial Data Input and Output.
5	SCL	DI	I^2C Interface, Serial Clock Input.
6	TS1/WAKE	AI	Thermistor Input/Wake up.
7	CAP1	AO	Internal LDO Decoupling Pin. It needs an external capacitor to be connected.
8	REGOUT	AO	1.8V/2.5V/3.0V/3.3V/5.0V Voltage Output.
9	REGSRC	AI	REG LDO Input.
10, 16, 23, 29	NC	—	Not Connected.
11	TS2	AI	Thermistor Input.
12	FUSE	AO	Fuse Blower.
13	TS3	AI	Thermistor Input.
14	CAP2	AO	Internal LDO Decoupling Pin. It needs an external capacitor to be connected.
15	BAT	AI	Primary Power Supply.
17	VC16	AI	Sense voltage input pin for the cell16 from the bottom of the stack, balance current input for the cell16 from the bottom of stack, and top-of-stack measurement point.

PIN DESCRIPTION (continued)

PIN	NAME	I/O	FUNCTION
18	VC15	AI	Sense voltage input pin for the cell15 from the bottom of the stack, balance current input for the cell15 from the bottom of stack, and return balance current for the cell16 from the bottom of stack.
19	VC14	AI	Sense voltage input pin for the cell14 from the bottom of the stack, balance current input for the cell14 from the bottom of stack, and return balance current for the cell15 from the bottom of stack.
20	VC13	AI	Sense voltage input pin for the cell13 from the bottom of the stack, balance current input for the cell13 from the bottom of stack, and return balance current for the cell14 from the bottom of stack.
21	VC12	AI	Sense voltage input pin for the cell12 from the bottom of the stack, balance current input for the cell12 from the bottom of stack, and return balance current for the cell13 from the bottom of stack.
22	VC11	AI	Sense voltage input pin for the cell11 from the bottom of the stack, balance current input for the cell11 from the bottom of stack, and return balance current for the cell12 from the bottom of stack.
24	VC10	AI	Sense voltage input pin for the cell10 from the bottom of the stack, balance current input for the cell10 from the bottom of stack, and return balance current for the cell11 from the bottom of stack.
25	VC9	AI	Sense voltage input pin for the cell9 from the bottom of the stack, balance current input for the cell9 from the bottom of stack, and return balance current for the cell10 from the bottom of stack.
26	VC8	AI	Sense voltage input pin for the cell8 from the bottom of the stack, balance current input for the cell8 from the bottom of stack, and return balance current for the cell9 from the bottom of stack.
27	VC7	AI	Sense voltage input pin for the cell7 from the bottom of the stack, balance current input for the cell7 from the bottom of stack, and return balance current for the cell8 from the bottom of stack.
28	VC6	AI	Sense voltage input pin for the cell6 from the bottom of the stack, balance current input for the cell6 from the bottom of stack, and return balance current for the cell7 from the bottom of stack.
30	VC5	AI	Sense voltage input pin for the cell5 from the bottom of the stack, balance current input for the cell5 from the bottom of stack, and return balance current for the cell6 from the bottom of stack.
31	VC4	AI	Sense voltage input pin for the cell4 from the bottom of the stack, balance current input for the cell4 from the bottom of stack, and return balance current for the cell5 from the bottom of stack.
32	VC3	AI	Sense voltage input pin for the cell3 from the bottom of the stack, balance current input for the cell3 from the bottom of stack, and return balance current for the cel4 from the bottom of stack.
33	VC2	AI	Sense voltage input pin for the cell2 from the bottom of the stack, balance current input for the cell2 from the bottom of stack, and return balance current for the cell3 from the bottom of stack.
34	VC1	AI	Sense voltage input pin for the cell1 from the bottom of the stack, balance current input for the cell1 from the bottom of stack, and return balance current for the cell2 from the bottom of stack.
35	VC0	AI	Sense voltage input pin for the cell0 from the bottom of the stack, balance current input for the cell0 from the bottom of stack, and return balance current for the cell1 from the bottom of stack.
36	SRP	AI	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
37	SRN	AI	Analog input pin connected to the internal coulomb counter peripheral for integrating a small voltage between SRP and SRN, where SRN is the bottom of the sense resistor. A charging current generates a positive voltage at SRP relative to SRN.
38	ALERT	DIO	ALERT Output and Override Input.

NOTE: AO = Analog Output, AI = Analog Input, DI = Digital Input, DO = Digital Output, DI/DO = Digital Input/Output.

ELECTRICAL CHARACTERISTICS

(V_{BAT} = 48V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
Normal Mode: VADC Off, IADC/CC Off	I_{DD}	Into BAT pin		90	185	μA
Normal Mode: VADC On, IADC/CC Off	I_{DD}	Into BAT pin		300	370	
Normal Mode: VADC Off, IADC/CC On	I_{DD}	Into BAT pin		120	235	
Normal Mode: VADC On, IADC/CC On	I_{DD}	Into BAT pin		330	430	
Normal Mode	I_{CC_REGSRC}	Into REGSRC pin		2.2	11	μA
Ship/Shutdown Mode	I_{SHIP}	Device is fully shut down, only BG and BOOT detectors are on		1.1	1.9	μA
Leakage and Offset Currents						
Cell Measurement Input Current	d_{ICELL}	Measured into VC0 ~ VC15			0.3	μA
Terminal Input Leakage	I_{LKG}				1.5	μA
Internal Power Control (Startup and Shutdown)						
Power-On Reset Threshold (1)	V_{POR}	V_{BAT} rising		4	4.7	V
Power-On Reset Hysteresis	V_{POR_HYS}	Device shuts down when $V_{BAT} < V_{POR} - V_{POR\_HYS}$		400		mV
Shutdown Voltage (1)	V_{SHUT}	V_{BAT} falling	3.1	3.6		V
Time Delay after Boot Signal on TS1/WAKE before I^2C Communications Allowed	$t_{I2CSTARTUP}$	Delay after boot sequence when I^2C communication is allowed		0.4		ms
Device Boot Startup Delay	$t_{BOOTREADY}$	Delay after boot signal when device has completed full boot-up sequence		2.3		ms
Measurement Schedule						
Cell Voltage Measurement Interval	t_{VCELL}	In normal mode, SETTLE[1:0] bits = 0		250.56		ms
		In normal mode, SETTLE[1:0] bits = 1/2/3		332.74		
		In fast mode, SETTLE[1:0] bits = 0		112.54		
		In fast mode, SETTLE[1:0] bits = 1		202.59		
		In fast mode, SETTLE[1:0] bits = 2		292.82		
		In fast mode, SETTLE[1:0] bits = 3		360.13		
Temperature Measurement Interval	t_{TEMP}	In normal mode, SETTLE[1:0] bits = 0		501.20		ms
		In normal mode, SETTLE[1:0] bits = 1/2/3		665.47		
16-Bit ADC for Cell Voltage and Temperature Measurement						
ADC Measurement Recommend Operation Range	ADC_{RANGE}	V_{CELL} measurements	0		6.55	V
		TS/Temperature measurements	0		1.8	V
ADC LSB Value	ADC_{LSB}			100		μV
ADC Cell Voltage Accuracy (2)	ADC	T_A = +25℃, V_{CELL} = 1.0V to 5.0V		±2.5		mV
		T_A = -40℃ to +60℃, V_{CELL} = 1.0V to 5.0V	-15		15	mV
		T_A = -40℃ to +85℃, V_{CELL} = 1.0V to 5.0V	-20		20	
16-Bit CC for Pack Current Measurement						
CC Input Voltage Range	CC_{RANGE}		-200		200	mV
CC LSB Value	CC_{LSB}	CC running constantly		9.3		μV
Conversion Time	tCC_{READ}	Single conversion		250.62		ms
Current Conversion Time (3)	$tCUR_{READ}$		4.88		15.616	ms
Integral Nonlinearity	CC_{INL}	16-bit, best fit over input voltage range ±200mV	-15		15	LSB
Offset Error	CC_{OFFSET}			±2		LSB
Offset Error Drift	CC_{OFFSET_DRIFT}		-15		15	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = 48V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Error	CC_{GAIN}	Over input voltage range		±0.05%		FSR
Gain Error Drift	CC_{GAIN_DRIFT}	Over input voltage range	-0.8%		0.8%	FSR
Effective Input Resistance	CC_{RIN}		0.2	0.6	1.2	MΩ
Thermistor Bias						
Pull-Up Resistance	R_{TS}	T_A = +25℃		10		kΩ
Pull-Up Resistance across Temperature	R_{TS_DRIFT}	T_A = -40℃ to +85℃	9.3		10.7	kΩ
OSC						
Internal Clock Frequency	f_{RC}	T_A = +25℃		262.144		kHz
Die Temperature						
Die Temperature Voltage	V_{DIE_TEMP25}	T_A = +25℃		0.55		V
Die Temperature Voltage Drift	$V_{DIE\_TEMP\_DRIFT}$			1.65		mV/°C
OV Threshold Range	OV_{RANGE}		0x8020	0xAB20	0xBFEO	ADC
UV Threshold Range	UV_{RANGE}		0x4000	0x65C0	0x7FFC	ADC
OV and UV Threshold Step Size	OV_{UVSTEP}			64		LSB
UV Minimum Value to Qualify	$UV_{MINQUAL}$	Below $UV_{MINQUAL}$, the cell is shorted (unused)		0x1380		ADC
OV Delay Timer Options	OV_{DELAY}	OV delay = 1s		0.6		s
		OV delay = 2s		1.8		
		OV delay = 4s		4.0		
		OV delay = 8s		7.7		
UV Delay Timer Options	UV_{DELAY}	UV delay = 1s		1.0		s
		UV delay = 4s		3.8		
		UV delay = 8s		7.8		
		UV delay = 16s		15.5		
SCD Threshold Options (4)	SCD_{RANGE}	Measured across (SRN - SRP)	22		198	mV
OCD1 Threshold Options (4)	$OCD1_{RANGE}$	Measured across (SRN - SRP)	6		102	mV
OCD2 Threshold Options (4)	$OCD2_{RANGE}$	Measured across (SRP - SRN)	4		200	mV
OCC Threshold Options (4)	OCC_{RANGE}	Measured across (SRP - SRN)	4		124	mV
SCD Threshold Step Size	SCD_{STEP}	RSNS = 0		11		mV
		RSNS = 1		22		mV
OCD1 Threshold Step Size	$OCD1_{STEP}$	RSNS = 0		3		mV
		RSNS = 1		6		mV
OCD2 Threshold Step Size	$OCD2_{STEP}$			2		mV
OCC Threshold Step Size	OCC_{STEP}			2		mV
SCD Delay Options	SCD_{DELAY}			173		µs
				199		µs
				297		µs
				482		µs
OCD1 Delay Options (4)	$OCD1_{DELAY}$		18.84		1266	ms
OCD2 Delay Options	$OCD2_{DELAY}$		4.88		374 (0x7F)	ms
OCC Delay Options (4)	OCC_{DELAY}		3.856		375.53	ms
OCD1 Voltage Offset	$OCD1_{OFFSET}$		-3.5	2	7	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = 48V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OCD2 Voltage Offset	$OCD2_{OFFSET}$		-2	2	7	mV
OCC Voltage Offset	OCC_{OFFSET}		-6	0.6	6	mV
OCD1 Scale Accuracy	$OCD1_{SCALERR}$		-16	1	16	%
OCD2 Scale Accuracy	$OCD2_{SCALERR}$		-14	1	14	%
OCC Scale Accuracy	$OCC_{SCALERR}$		-14	1.2	14	%
SCD Accuracy	SCD_{ACC}	22mV	-20	10	40	%
		> 22mV	-15	1.5	15	%
Charge and Discharge Drivers						
CHG and DSG On	V_{FETON}	V_{REGSRC} = 25V with load resistance of 10MΩ	11.2	12.5	13.6	V
		V_{REGSRC} < 12V with load resistance of 10MΩ		V_{REGSRC} - 0.9		V
CHG and DSG On Rise Time	t_{FET_ON}	V_{REGSRC} = 12V, CHG driving an equivalent load capacitance of 10nF, measured from 10% to 90% of V_{FETON}		90	120	μs
		V_{REGSRC} = 12V, DSG driving an equivalent load capacitance of 10nF, measured from 10% to 90% of V_{FETON}		120	150	
		V_{REGSRC} < 12V, CHG driving an equivalent load capacitance of 10nF, measured from 10% to 90% of V_{FETON}		100	140	
		V_{REGSRC} < 12V, DSG driving an equivalent load capacitance of 10nF, measured from 10% to 90% of V_{FETON}		125	160	
DSG Pull-Down OFF Fall Time	t_{DSG_OFF}	DSG driving an equivalent load capacitance of 10nF, measured from 90% to 10%		68		μs
CHG Pull-Down OFF Fall Time	t_{CHG_OFF}	CHG driving an equivalent load capacitance of 10nF, mesured from 90% to 10%		2500		μs
CHG Pull-Down Off-Resistance to VSS	R_{CHG_OFF}	CHG disabled, CHG held at 12V	828	990	1150	kΩ
DSG Pull-Down Off-Resistance to VSS	R_{DSG_OFF}	DSG disabled, DSG held at 12V	2.1	2.7	3.2	kΩ
Load Detection Threshold	V_{LOAD_DETECT}		400	750	1100	mV
Filter Time	t_{FILTER}	Load detection signal filter time	3		6	μs
CHG Clamp Voltage	V_{CHG_CLAMP}	If the CHG pin externally pulled high (through PACK-, if load applied), 500μA (MAX) sink current into CHG pin. With CHG_ON bit cleared.	19	20	22	V
ALERT Pin						
ALERT Output Voltage High	V_{ALERT_OH}	I_{OL} = 1mA	V_{REGOUT} × 0.75			V
ALERT Output Voltage Low	V_{ALERT_OL}	Unloaded			V_{REGOUT} × 0.25	V
ALERT Input High	V_{ALERT_IH}	V_{REGOUT} = 1.8V		1		V
		V_{REGOUT} = 3.0V		1.7		
		V_{REGOUT} = 5.0V		2.7		
ALERT Pin Weak Pull-Down Resistance when Driven Low	R_{ALERT_PD}	V_{REGOUT} = 3.3V	1.6	2.3	3.2	MΩ
Cell Balancing Driver						
Internal Cell Balancing Driver Resistance	R_{DSFET}	V_{CELL} = 3.6V	5	20	40	Ω
Cell Balancing Duty Cycle when Enabled	X_{BAL}	Every cycle		86		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{BAT} = 48V, T_A = -40℃ to +85℃, typical values are at T_A = +25℃ unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Regulator						
External LDO Voltage Options	V_{EXTLDO}	Nominal values, unloaded, across temp	1.3	1.8	1.9	V
			2.2	2.5	2.6	
			2.7	3.0	3.2	
			2.9	3.3	3.5	
			4.5	5.0	5.2	
Line Regulation	V_{EXTLDO_LN}	REGSRC pin stepped from 6V to 25V, with 10mA load, in 100μs		9.5	24	mV
Load Regulation	V_{EXTLDO_LD}	I_{REGOUT} = 0mA to 10mA		-0.12	0.5	%
External LDO Current Limit	I_{EXTLDO_LIMIT}	V_{REGOUT} = 0V	17	25.2	33	mA
Boot Detector						
Boot Threshold Voltage	V_{BOOT}	Measured at TS1/WAKE pin with device in ship mode. Below MIN, the device does not boot up. Above MAX, the device boots up.	1000			mV
Boot Threshold Application Time	t_{BOOT_MAX}	Measured at TS1/WAKE pin. Below MIN, the device does not boot up. Above MAX, the device boots up.	1000			μs

NOTES:

1. Measured at each V_{BAT}.
2. ADC values are measured when cell balancing is off.
3. Design simulation values for reference.
4. Values indicate nominal thresholds only. For minimum and maximum variation, apply OC_{OFFSET} and OCS_{CALERR}.

TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Low Logic Threshold	V_{IL}			V_{REGOUT} × 0.25	V
Input High Logic Threshold	V_{IH}	V_{REGOUT} × 0.75			V
Output Low Logic Drive	V_{OL}			0.2	V
SCL, SDA Fall Time	t_F			0.4	μs
SCL Pulse Width High	t_{HIGH}	4			μs
SCL Pulse Width Low	t_{LOW}	4.7			μs
Setup Time for START Condition	t_{SU_STA}	4.7			μs
START Condition Hold Time after which First Clock Pulse is Generated	t_{HD_STA}	4			μs
Data Setup Time	t_{SU_DAT}	250			ns
Data Hold Time	t_{HD_DAT}	0			μs
Setup Time for STOP Condition	t_{SU_STO}	4			μs
Time the Bus Must be Free before New Transmission Can start	t_{BUF}	4.7			μs
Clock Low to Data Out Valid	t_{VD_DAT}			900	ns
Data Out Hold Time after Clock Low	t_{HD_DAT}	0			ns
Clock Frequency	f_{SCL}	0		100	kHz

TIMING DIAGRAMS

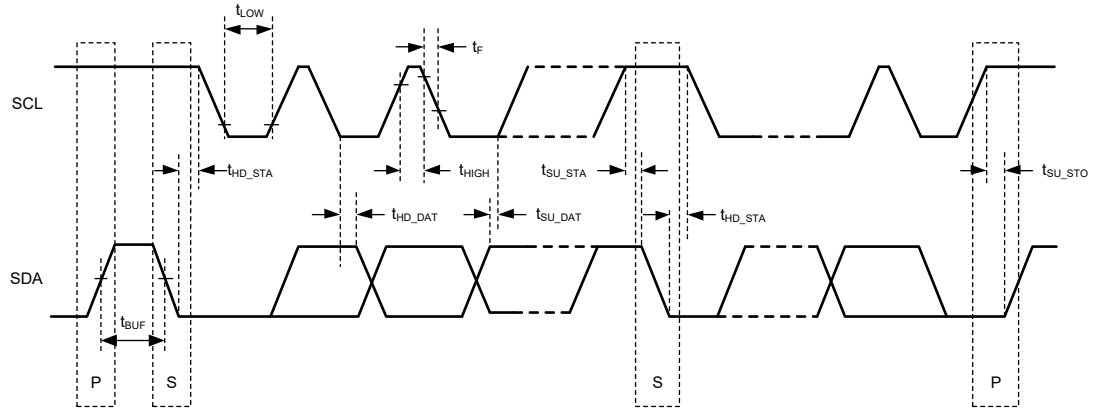
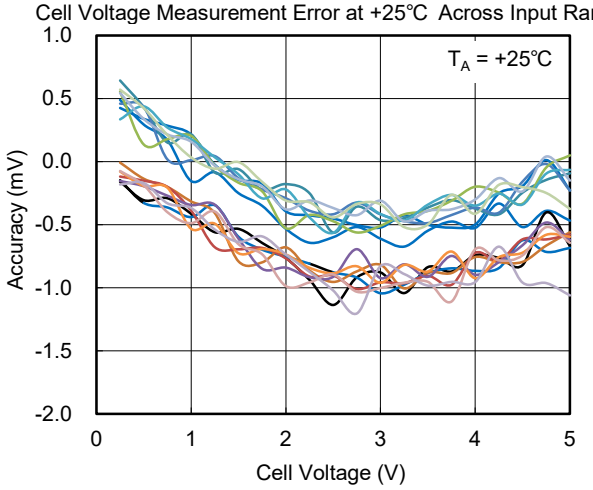


Figure 1. I²C Communications Interface Timing

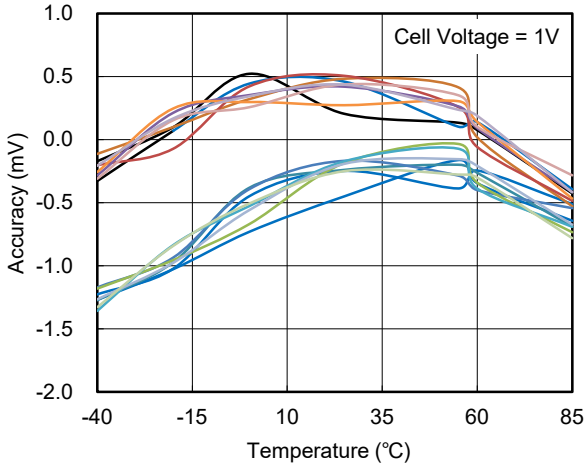
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +85℃, unless otherwise noted.

Cell Voltage Measurement Error at +25℃ Across Input Range



Cell Voltage Measurement Error vs. Temperature



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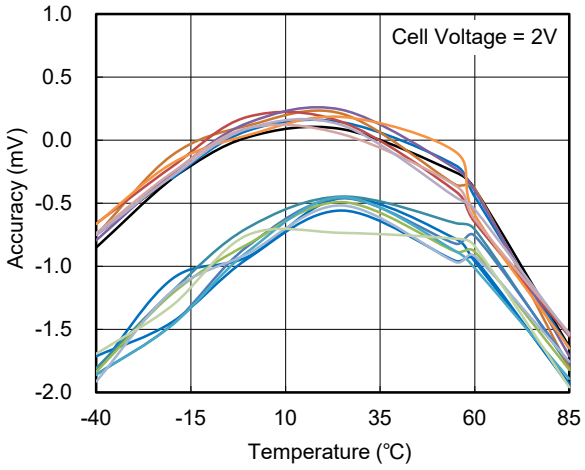
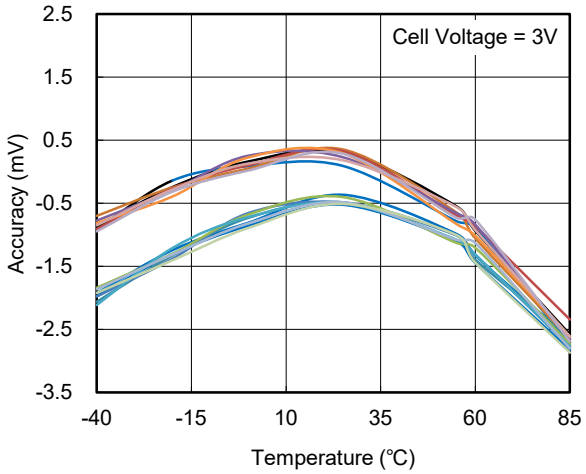
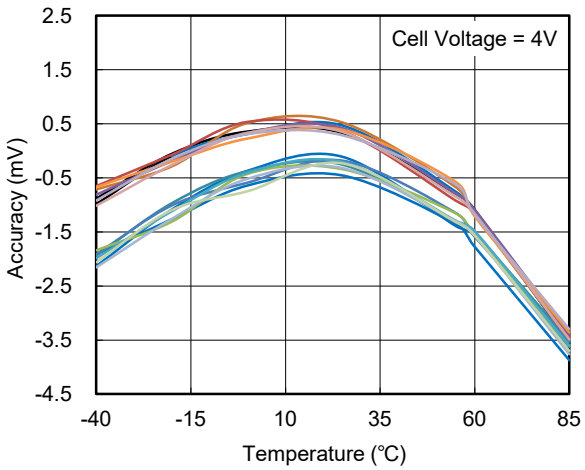


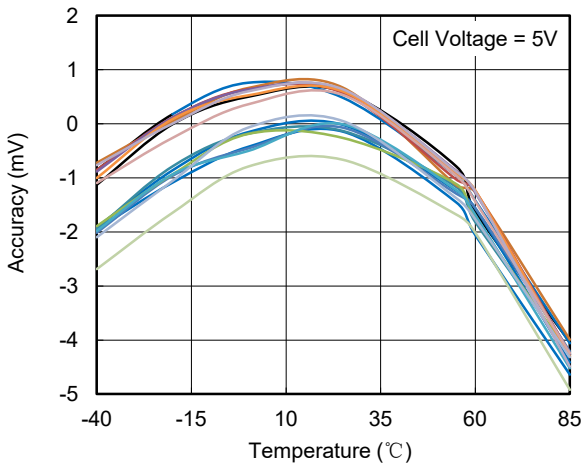
Cell Voltage Measurement Error vs. Temperature



Cell Voltage Measurement Error vs. Temperature



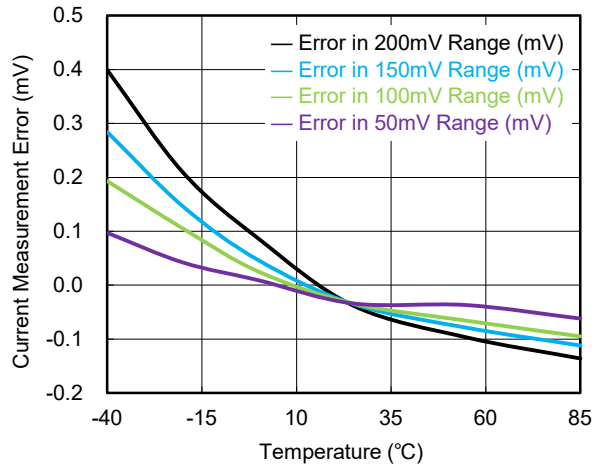
Cell Voltage Measurement Error vs. Temperature



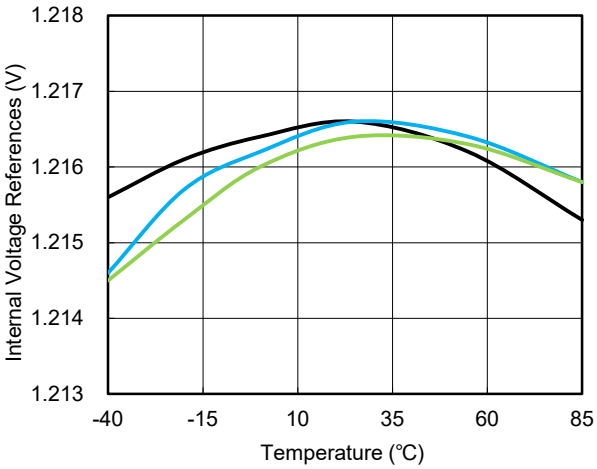
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +85℃, unless otherwise noted.

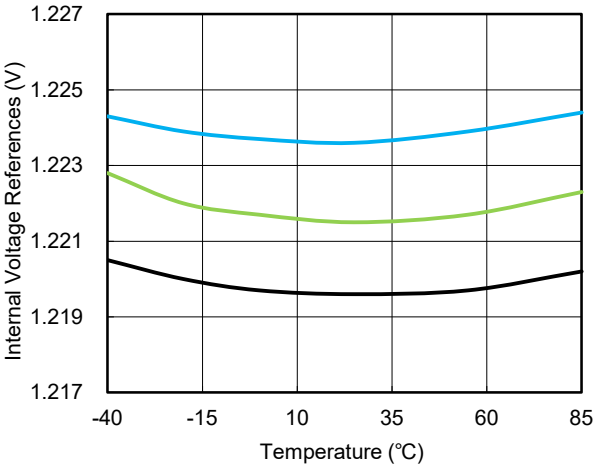
Current Measurement Error vs. Temperature



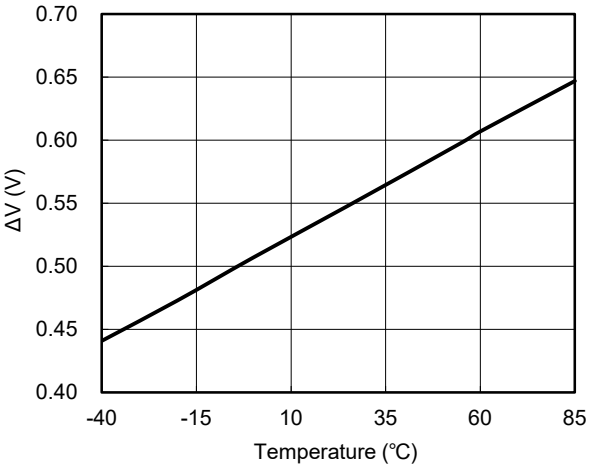
Internal Voltage References vs. Temperature (VREF1)



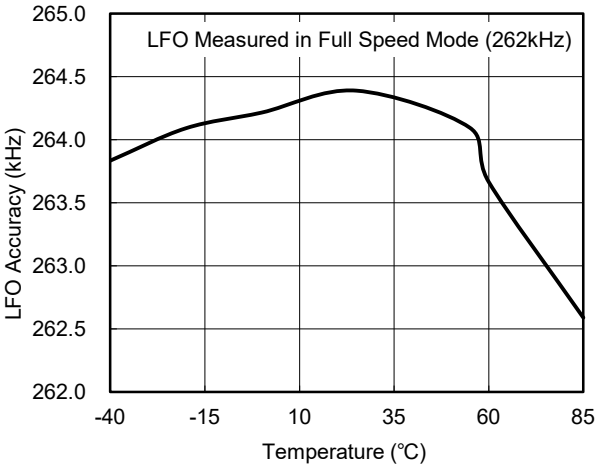
Internal Voltage References vs. Temperature (VREF2)



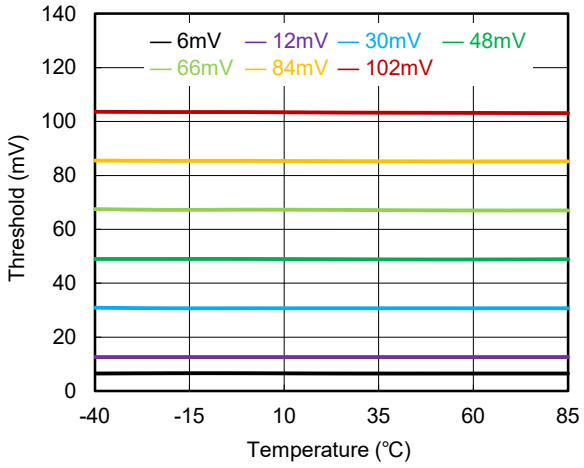
Internal Temperature Sensor (ΔV) Voltage vs. Temperature



Low Frequency Oscillator (LFO) Accuracy vs. Temperature



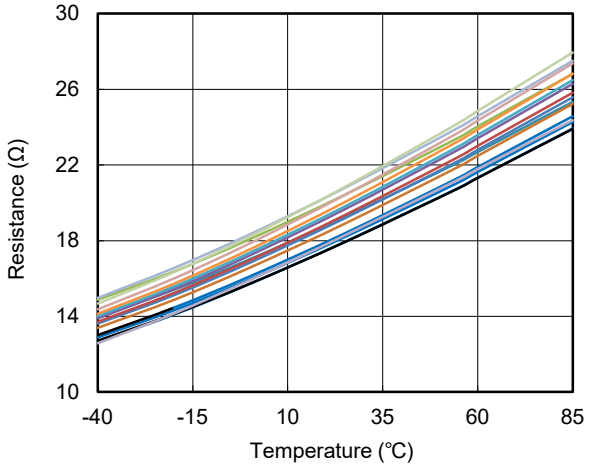
Over-Current in Discharge Protection 1 Threshold vs. Temperature



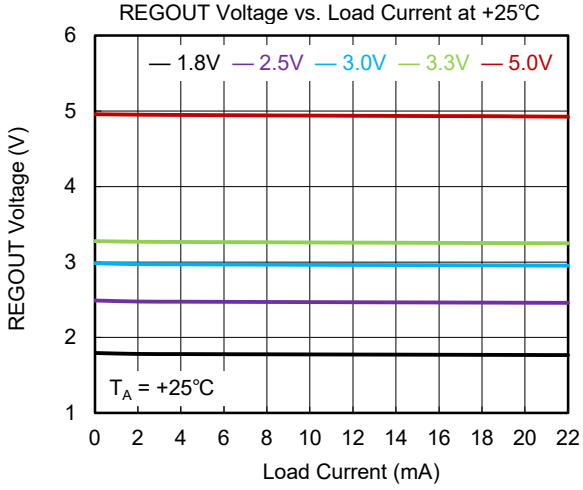
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +85℃, unless otherwise noted.

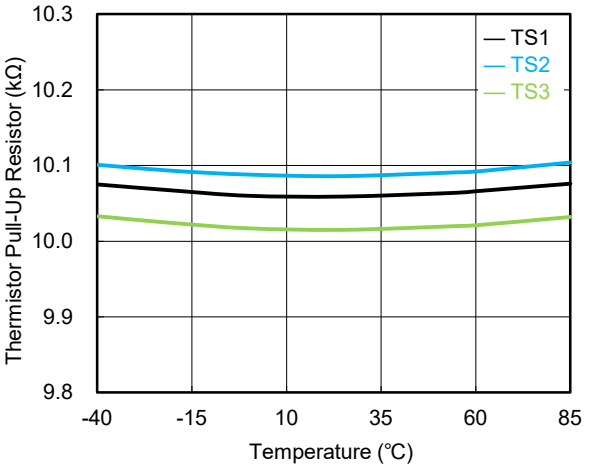
Cell Balancing Resistor vs. Temperature



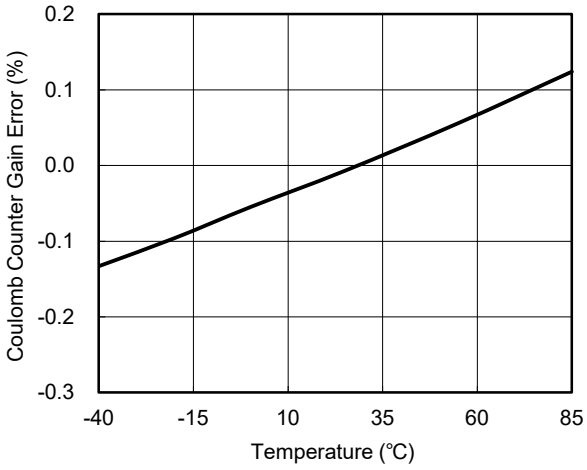
REGOUT Voltage vs. Load Current at +25℃



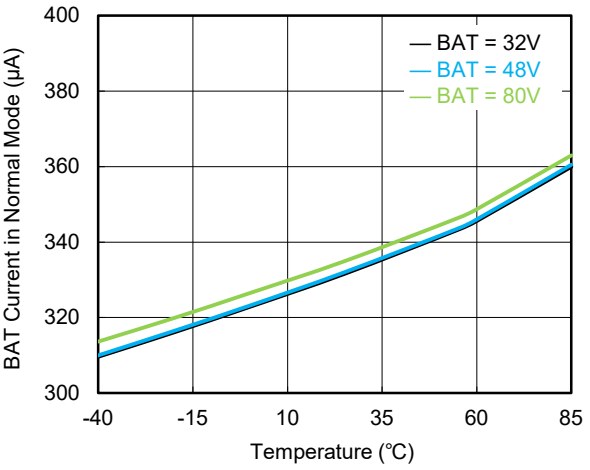
Thermistor Pull-Up Resistance vs. Temperature



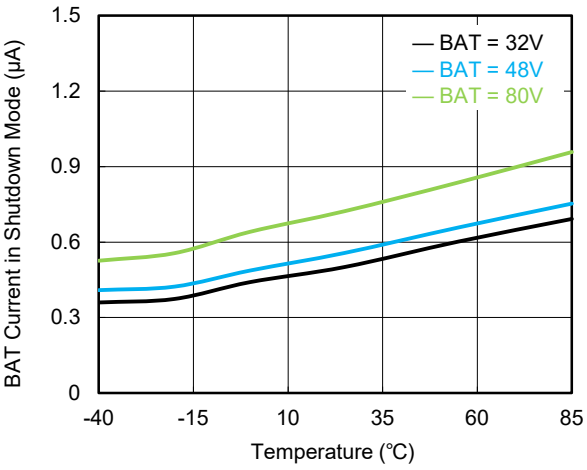
Coulomb Counter Gain Error vs. Temperature



BAT Current in Normal Mode vs.Temperature



BAT Current in Shutdown Mode vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

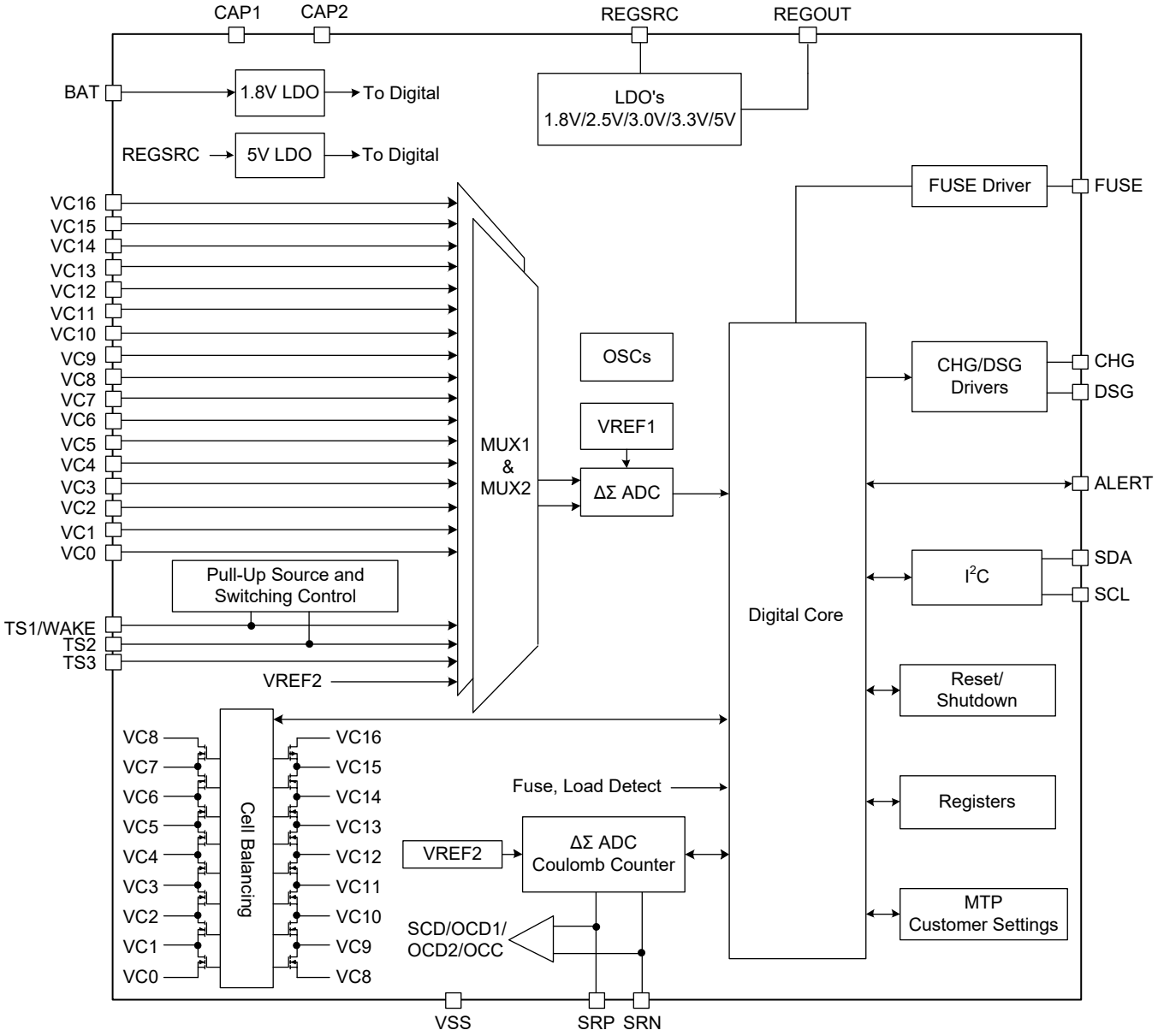


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM90116H is a multi-channel analog front end (AFE) IC targeting 3 to 16 series cells for applications such as LEV, UPS and power tools.

Two separate 16-bit ADCs provide accurate monitoring of voltage, current and temperature at both cell and pack level. The integrated post-ADC filters enable clean and stable readings to the host. Extensive protections such as over/under-voltage, over/under-current and over/under-temperature detections are readily available thanks to the precise sensing and monitoring. On-chip passive balancing up to 50mA is supported for each cell. Low-side drivers for charge/discharge FETs are also integrated to reduce BOM.

The device is programmable via on-chip I^2C controller.

Measurement Subsystem

The measurement subsystem enables the host to easily monitor cell voltages, temperatures, pack voltage, and pack current. All ADCs are trimmed by SGMICRO.

To ensure data completion a nd accuracy, the ADC and CC data are read using address auto-increment, which returns the complete value consisting of the high and low registers in the same transaction, without being interrupted or changed by other transactions.

Table 1. Normal Mode

SETTLE[1:0] Bits	Conversion Time (Per Channel)	Settle Time	Frame Time	Average
0x00	11.72ms	0.976ms	250ms	8
0x01	15.616ms	4.883ms	332ms	8
0x02	15.616ms	8.789ms	332ms	4
0x03	15.616ms	11.712ms	332ms	1

In normal conversion mode, multi-time sample average scheme is adopted for each channel during a frame. A complete conversion frame with a total of 21 channels takes about 250ms or 332ms, depending on the different settling time.

Three thermistor voltages are updated every two frames at intervals of 500ms or 664ms. Specifically, during odd frame, thermistors 3 is measured, while during the even frame, thermistor 1 and 2 are updated.

The update of the three thermistor voltages occur the same as the normal cell voltage channels.

Voltage Measurement

The SGM90116H uses a 16-bit ADC for measuring cell voltages and temperatures. This ADC measures all differential cell voltage, thermistors, die temperature, internal reference voltage, battery voltage and covers a nominal full-scale range of 0V to 6.55V with a least significant bit (LSB) value of 100μV/LSB.

To enable the ADC, set the VADC_EN bit in the SYS_CTRL1 register. This bit is auto-enabled in normal working mode, ensuring over-voltage (OV) and under-voltage (UV) protections are active.

Thermistor Temperature measurement

The device can measure up to three NTC 103AT thermistors by applying a factory-trimmed internal 10kΩ pull-up resistance to an internal 1.8V nominal regulator. The results can be read from the TSx registers.

The thermistors impedance can be calculated based on the 16-bit ADC reading from the TS1, TS2, TS3 registers and 10kΩ internal pull-up resistance using the following formulas:

$$V_{TSX} = (\text{ADC in Decimal}) \times 100\mu V/LSB \quad (1)$$

$$R_{TS} = (10000 \times V_{TSX})/(1.8 - V_{TSX}) \quad (2)$$

To convert the thermistor resistance to temperature value, please refer to the thermistor manufacturer's datasheet. When the TEMP_SEL bit is set, TS1/WAKE stores the internal die temperature value.

If TS1, TS2 and TS3 are not used as thermistor inputs, the TSx pin should be connected to ground with a 10kΩ nominal resistor.

DETAILED DESCRIPTION (continued)

Die Temperature measurement

The die temperature block produces a voltage which is proportional to the die temperature. This can reduce component count when pack thermistors are not used, and ensures the die power dissipation requirements are observed. The die temperature uses the same onboard 16-bit ADC that is used for measuring cell voltage.

To select internal die temperature measurement, set TEMP_SEL bit to 0.

To convert a DIE TEMP reading into temperature value, refer to the equations below. For more precise temperature readings from DIE TEMP, store the DIE TEMP value at room temperature during production calibration.

The equations below shows how to use the 16-bit ADC readings in TS1/WAKE when TEMPSEL = 0 to calculate the internal die temperature.

$$V_{25} = 0.54 \text{ (nominal)} \quad (3)$$

$$V_{TS1} = (\text{ADC in Decimal}) \times 100\mu V/LSB \quad (4)$$

$$TEMP_{DIE} = 25℃ + [(V_{TS1} - V_{25})/0.00175] \quad (5)$$

Stack Voltage Measurement (VC16 Pin)

After digitization, each cell voltage is added up and the summation result is stored in the BAT registers. Use the BAT_SEL bit to select either the direct stack voltage or the sum of 16 separate voltages. This sum is then divided by 16, resulting in a 16-bit value with a nominal LSB of 1.6mV. Due to direct stack voltage is measured by resistor divider connected to VC16 and the sum of 16 cells is measured by each cell, the final result has a little difference.

The following linear equation shows how to convert the 16-bit pack voltage ADC reading to an analog voltage.

$$V_{BAT} = 16 \times ADC(cell) \times 100\mu V/LSB \quad (6)$$

Cell Balance

The SGM90116H can support both internal and external passive cell balancing. The host controller decides the balancing algorithm. Internal cell balance drivers can balance up to 50mA per cell, while external options allow for higher currents.

To activate a cell balancing channel, set the corresponding bit in the CELL_BAL1, CELL_BAL2 or CELL_BAL3 register.

While multiple cells are balanced simultaneously, avoid balancing adjacent cells concurrently. This can lead to exceeding their absolute maximum conditions and is also not recommended for external balancing implementations. When using internal balancing, care should be taken to avoid exceeding package power dissipation ratings.

The host controller must ensure that no two adjacent cells are balanced simultaneously.

During cell balancing, the protection logic remains active and will not miss any protection measures while cell balancing is enabled.

Balancing occupies approximately 86% of the frame-time (See Table 1) cycle during ADC cell voltage measurement.

Current Conversion

The SGM90116H uses a low-side sense resistor to monitor pack current, which connects to the SRP and SRN pins via an external RC filter. Connect the filter so that a charging current will produce a positive voltage on SRP relative to SRN.

The device supports sense resistors of 1mΩ or less. The differential voltage between SRP and SRN is digitized by an integrated 16-bit sigma-delta ADC, which can digitize voltages over a ±200mV range.

The ADC uses multiple digital filters to optimize the measurement of instantaneous and integrated current. Two separate hardware digital filters, coulomb counting (CC) filter and current-to-voltage conversion (CUR) filter are used to get the digitized current value.

To enable one-shot mode, set CC_EN bit to 0 and CC_ONESHOT bit to 1. In one-shot mode, the CC performs a single 250ms reading and sets the CC_READY bit at the end of each reading if CC_SRC bit is set to 0. This mode is designed for non-gauging applications where the host's primary intention is to check the pack current.

DETAILED DESCRIPTION (continued)

The CUR filter generates a 16-bit current measurement used for current reporting. The CUR Filter output the current much faster than CC Filter. It will output the current results every 11.72/15.616ms in normal mode. Due to this feature, the current measurement can be synchronously measured with each cell voltage channel. If CC_SRC bit is set to 1, the CC_READY bit will represents CUR filter measurement is ready and the ALERT pin is triggered by CUR filter ready signal. CUR filter is enabled by IADC_EN bit.

The CC and CUR has a full-scale range of ±300mV, with a recommended maximum input range of ±200mV, resulting in a least significant bit (LSB) of approximately 9.3μV.

The equation below shows how to convert the 16-bit CC/CUR reading into an analog voltage when no board-level calibration has been performed:

$$\text{CC Reading (μV)} = \text{(16-bit 2's Complement Value)} \times 9.3\text{μV/LSB} \quad (7)$$

When both IADC_EN bit and CC_EN bit are set to 0, the internal 16-bit sigma-delta ADC is disabled and ONE_SHOT is not triggered.

Synchronized Voltage and Current Measurement

During normal operation, when cell voltages are sequentially digitized using a single multiplexed ADC, the current is continuously digitized by the dedicated coulomb counter ADC. This current measurement is synchronized with each cell voltage measurement, enabling its use for individual cell impedance analysis. Periodic current measurements can be read out through the digital communication interface. Additionally, measurements taken in sync with specific cell voltage readings are stored together with their associated voltage measurements for separate readout.

Protection Subsystem

Integrated hardware protections are provided to enhance safety, acting as supplements to the standard protection features within the host controller firmware. They should not be the sole means of battery pack protection. They offer additional use for FMEA purpose when the host microcontroller may not respond to any of these below protection situations.

Over-current in discharge (OCD1/2), short-circuit in discharge (SCD), and over-current in charging (OCC), are implemented using analog comparators. These continuously monitor the voltage across (SRP - SRN) while the device is in normal operation mode. If a voltage exceeding the programmed threshold is detected for a programmable delay, the alert will be triggered if the protection enable bit is set, interrupting the host microcontroller.

Cell over-voltage (COV), cell under-voltage (CUV), over-temperature in charging (OTC), under-temperature in charging (UTC), over-temperature in discharging (OTD), under-temperature in discharging (UTD), die over-temperature (OTINT), and die under-temperature (UTINT) are digital comparators based on ADC measurements and corresponding thresholds. When a measured result exceeds the threshold, a trigger flag is generated, and an alert signal will be driven high if the protection enable bit is set. Users can configure corresponding bit in PROTEN register to enable the OTC/UTC/OTD/UTD/OTINT/UTINT.

OCD1

Over-current in discharge protection (OCD1) uses a dedicated analog comparator to monitor voltage across SRN and SRP pins. When this voltage exceeds the programmable delay threshold, the OCD1 protection will be activated. The threshold can be set from 8mV to 50mV with 3mV per step (RSNS = 0) or from 17mV to 100mV with 6mV per step (RSNS = 1). The delay can be set to 8ms, 20ms, 40ms, 80ms, 160ms, 320ms, 640ms, or 1280ms. These settings are configurable through the PROTECT2 register.

If OCD1 protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the OCD1 flag, and set DSG_ON bit to 1. If the OCD1 flag is not cleared, DSG_ON bit will remain at 0.

DETAILED DESCRIPTION (continued)

OCD2

Over-current in discharge protection (OCD2) uses a dedicated analog comparator to monitor voltage across SRN and SRP pins. When this voltage exceeds the programmable delay threshold, the OCD2 protection will be activated. The threshold can be set from 4mV to 200mV with 2mV per step. The delay can be set from 3ms to 381ms with 2.93ms per step. These settings are configurable through the OCD2_THD and OCD2_DLY registers.

OCD2 function is enabled when OCD_THD[3:0] bits are not set to 0x0 and OCD2_EN bit is set to 1, the alert function and DSG control will be enabled. Otherwise, they will be ignored.

OCD2_DLY cannot be configured to 0. Otherwise, the abnormal flag will be triggered.

It is recommended to configure OCD2_DLY and OCD2_THD registers before OCD2 function is enabled.

If OCD2 protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the OCD2 flag, and set DSG_ON bit to 1. If the OCD2 flag is not cleared, DSG_ON bit will remain at 0.

SCD

Short-circuit discharge (SCD) protection uses a dedicated analog comparator to monitor voltage across SRN and SRP pins. When this voltage exceeds the programmable delay threshold, the SCD protection will be activated. The threshold can be set from 22mV to 100mV with 11mV per step (RSNS = 0), or from 44mV to 200mV with 22mV per step (RSNS = 1). Additionally, the delay can be set to 80μs, 105μs, 200μs or 400μs. These settings are configurable through the PROTECT1 register.

If SCD protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the SCD flag and set DSG_ON bit to 1. If the SCD flag is not cleared, DSG_ON bit will remain at 0.

OCC

Over-current charge protection (OCC) uses a dedicated analog comparator to monitor the voltage across SRN and SRP pins. When this voltage exceeds the programmable delay threshold, the OCC protection will be activated. The threshold can be set from 4mV to 124mV with 2mV per step. And the delay can be set from 3ms to 381ms with 2.93ms per step. OCC_THD and OCC_DLY registers are used to configure these parameters.

OCC function is enabled when OCC_THD[5:0] bits are not set to 0x0 and OCC_EN bit is set to 1, the alert function and CHG control will be enabled. Otherwise, they will be ignored.

If OCC protection is detected, the CHG FET will be automatically turned off. To turn on the CHG FET, users must clear the OCC flag, and set CHG_ON bit to 1. If the OCC flag is not cleared, CHG_ON bit will remain at 0.

COV

Cell over-voltage protection (COV) is digitally managed by comparing cell voltage readings against the 8-bit programmed threshold stored in the OV_TRIP register.

The OV threshold is direct mapping of 8 bits of the 16-bit ADC reading, with the upper 2 MSB preset to 10 and lower 6LSB preset to 100000. This corresponds to the 10-XXXX-XXXX-100000 OV trip level. The programmable OV threshold ranges approximately from 3.28V to 4.91V, but the exact value may change due to the linear equation used for ADC value mapping.

The COV triggers an alert signal if the over-voltage condition persists for a programmable delay, selectable as 1s, 2s, 4s or 8s through the DLY[1:0] bits of PROTECT3 register.

To calculate the accurate OV_TRIP register value, use the following steps:

- Determine the desired OV
- Calculate the full 16-bit ADC value required to meet the desired OV trip threshold
- Remove the upper 2 MSB and Lower 6LSB from the full 16-bit value, retaining only the remaining 8 bits. Achieve this by shifting the OV_TRIP_FULL binary value 6bits to the right and removing the 2MSB.
- Write OV_TRIP to the corresponding register.

OV protection is enabled when VADC is enabled. Make sure that the VADC_EN bit is set to 1 when OV protections are needed.

If OV protection is detected, the CHG FET will be automatically turned off. To turn on the CHG FET, users must clear the COV flag, and set CHG_ON bit to 1. If the COV flag is not cleared, CHG_ON bit will remain at 0.

DETAILED DESCRIPTION (continued)

The cell that triggered the COV flag can be checked by the SYS_STAT6 and SYS_STAT6 registers.

CUV

Cell under-voltage protection (CUV) is digitally managed by comparing cell voltage readings against an 8-bit programmed threshold in the UV_TRIP register.

The UV threshold is a direct mapping of 8 bits of the 16-bit ADC reading, with upper 2 MSB are set to 01, and lower 6LSB are set to 000000. This corresponds to the 01-XXXX-XXXX-000000 UV trip level. The programmable UV threshold ranges approximately from 1.64V to 3.27V, while the exact value may change due to the linear equation used for ADC value mapping.

The CUV triggers an alert signal if the under-voltage condition persists for a programmable delay, selectable as 1s, 4s, 8s or 16s through the UV_DLY[1:0] bits of PROTECT3 register.

To short the cell pins when the cells are not required, $UV_{MINQUAL}$ is preset in the factory, with a default value of 0x1380, corresponding to 499mV.

- Determine the desired UV
- Calculate the full 16-bit ADC value required to meet the desired UV trip threshold
- Remove the upper 2 MSB and Lower 6LSB from the full 16-bit value, retaining only the remaining 8 bits. Achieve this by shifting the UV_TRIP_FULL binary value 6 bits to the right and removing the 2 MSB.
- Write UV_TRIP to the corresponding register.

UV protection is enabled when VADC is enabled. Make sure that the VADC_EN bit is set to 1 when UV protection is needed.

If UV protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the CUV flag, and set DSG_ON bit to 1. If the CUV flag is not cleared, DSG_ON bit will remain at 0.

The cell that triggered the CUV flag can be checked by the SYS_CTRL4 and SYS_CTRL5 registers.

OTC

Over-temperature charge protection (OTC) is initiated by comparing the measured die temperature voltage with a threshold while in charge mode. If the voltage on any of the TS1/TS2/TS3 pins exceeds the threshold within a programmable delay, the OTC protection will be triggered. The threshold can be set by OTC_THD_HI/OTC_THD_LO registers, while the OTC_DLY is used to set the programmable delay.

OTC threshold high 8 bits are stored in a temporary register after OTC_THD_HI register is configured, and the threshold value is updated after OTC_THD_LO register is configured. OTC_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure OTC_DLY and OTC threshold register before OTC function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

OTC function is enabled when [OTC_THD] bit is not set to 0x0 and [OTC_EN] bit is set to 1. The alert function and CHG control will be enabled. Otherwise, they will be ignored.

If OTC protection is detected, the CHG FET will be automatically turned off. To turn on the CHG FET, users must clear the OTC flag, and set CHG_ON bit to 1. If the OTC flag is not cleared, CHG_ON bit will remain at 0.

UTC

Under-temperature charge protection (UTC) is initiated by comparing the measured die temperature voltage with a threshold while in charge mode. If the voltage on any of the TS1/TS2/TS3 pins is lower than the threshold within a programmable delay, the UTC protection will be triggered. The threshold can be set by UTC_THD_HI/UTC_THD_LO register, while the UTC_DLY register is used to set the programmable delay.

UTC threshold high 8 bits are stored in a temporary register after UTC_THD_HI register is configured, and the threshold value is updated after UTC_THD_LO register is configured. UTC_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure UTC_DLY and UTC threshold registers before UTC function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

DETAILED DESCRIPTION (continued)

UTC function is enabled when UTC_THD bits are not set to 0x0 and UTC_EN bit is set to 1, the alert function and CHG control will be enabled. Otherwise, they will be ignored.

If UTC protection is detected, the CHG FET will be automatically turned off. To turn on the CHG FET, users must clear the UTC flag, and set CHG_ON bit to 1. If UTC flag is not cleared, CHG_ON bit will remain at 0.

OTD

Over-temperature discharge protection (OTD) is initiated by comparing the measured die temperature voltage with a threshold while in discharge mode. If the voltage on any of the TS1/TS2/TS3 pins exceeds the threshold within a programmable delay, the OTD protection will be triggered. The threshold can be set by OTD_THD_HI/OTD_THD_LO register, while the OTD_DLY register is used to set the programmable delay.

OTD threshold high 8 bits are stored in a temporary register after OTD_THD_HI configured, and the threshold value is updated after OTD_THD_LO register is configured. OTD_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure OTD_DLY and OTD threshold register before OTD function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

OTD function is enabled when OTD_THD[15:0] bits are not set to 0x0 and OTD_EN bit is set to 1, the alert function and DSG control will be enabled. Otherwise, they will be ignored.

If OTD protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the OTD flag, and set DSG_ON bit to 1. If OTD flag is not cleared, DSG_ON bit will remain at 0.

UTD

Under-temperature discharge protection (UTD) is initiated by comparing the measured die temperature voltage with a threshold while in discharge mode. If the voltage on any of the TS1/TS2/TS3 pins is lower than the threshold within a programmable delay, the UTD protection will be triggered. The threshold can be set by UTD_THD_HI/UTD_THD_LO register, while the UTD_DLY register is used to set the programmable delay.

UTD threshold high 8 bits are stored in a temporary register after UTD_THD_HI register is configured, and the threshold value is updated after UTD_THD_LO register is configured. UTD_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure UTD_DLY and UTD threshold register before UTD function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

UTD function is enabled when UTD_THD[15:0] bits are not set to 0x0 and UTD_EN bit is set to 1, the alert function and DSG control will be enabled. Otherwise, they will be ignored.

If UTD protection is detected, the DSG FET will be automatically turned off. To turn on the DSG FET, users must clear the UTD flag, and set DSG_ON bit to 1. If UTD flag is not cleared, DSG_ON bit will remain at 0.

OTINT

Die temperature over-temperature protection is initiated by comparing the measured die temperature voltage with threshold. If the voltage exceeds the threshold within a programmable delay, the OTINT protection will be triggered. The threshold can be set by OTINT_THD_HI/OTINT_THD_LO register, while the OTINT_DLY register is used to set the programmable delay.

OTINT threshold high 8 bits are stored in a temporary register after OTINT_THD_HI configured, and the threshold value is updated after OTINT_THD_LO register is configured. OTINT_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure OTINT_DLY and OTINT threshold register before OTINT function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

OTINT function is enabled when OTINT_THD[15:0] bits are not set to 0x0 and OTINT_EN bit is set to 1, the alert function and DSG/CHG control will be enabled; otherwise, they will be ignored.

DETAILED DESCRIPTION (continued)

If OTINT protection is detected, the DSG/CHG FET will be automatically turned off. To turn on the DSG/CHG FET, users must clear the OTINT flag, and set DSG_ON/CHG_ON bit to 1. If OTINT flag is not cleared, DSG_ON/CHG_ON bit will remain at 0.

UTINT

Die temperature under-temperature protection is initiated by comparing the measured die temperature voltage with threshold. If the voltage is lower than the threshold within a programmable delay, the UTINT protection will be triggered. The threshold can be set by UTINT_THD_HI/UTINT_THD_LO register, while the UTINT_DLY register is used to set the programmable delay.

UTINT threshold high 8 bits are stored in a temporary register after UTINT_THD_HI configured, and the threshold value is updated after UTINT_THD_LO register is configured. UTINT_DLY cannot be configured to 0 or abnormal flag will be triggered. It is recommended to configure UTINT_DLY and UTINT threshold register before UTINT function is enabled.

Default protection thresholds and delays are loaded from the NVM preset area during chip regular power-up.

UTINT function is enabled when UTINT_THD[15:0] bits are not set to 0x0 and UTINT_EN bit is set to 1, the alert function and DSG/CHG control will be enabled. Otherwise, they will be ignored.

If UTINT protection is detected, the DSG/CHG FET will be automatically turned off. To turn on the DSG/CHG FET, users must clear the UTINT flag, and set DSG_ON/CHG_ON bit to 1. If UTINT flag is not cleared, DSG_ON/CHG_ON bit will remain at 0.

OVRD_ALERT

The ALERT pin can also be driven by an external second-level protection IC. When the ALERT pin is forced high by an external IC while the internal output is low for a programmable delay, the device will recognize this as an OVRD_ALERT. This event triggers an automatic disabling of both CHG/DSG FET drivers. However, the device cannot recognize the ALERT signal input as high when it is already forcing the ALERT signal high due to another condition.

HWD

The SGM90116H integrates a hardware watchdog protection that triggers a fault when no communication is received for a programmable delay defined by HWD_DLY. The HWD_DLY delay is programmable and can range from 32s to 4096s, with 16 seconds per step. When a HWD fault is triggered, the device will turn off both the DSG FET and CHG FET. HWD_DLY = 0 will disable this function.

Control Subsystem

FET Driving (CHG and DSG)

The SGM90116H provides two low-side FET drivers, CHG and DSG, which control NCH power FETs or can be used as signals to enable various other circuits, such as a high-side NCH charge pump circuit.

Both DSG and CHG drivers have a fast pull-up to nominally 12V when enabled. DSG uses a fast pull-down to VSS when disabled, while CHG uses a high-impedance (nominally 1MΩ) pull-down path when disabled.

An additional internal clamp circuit ensures that the CHG pin does not exceed a maximum of 12V. The power path for the CHG and DSG pull-up circuit originates from the REGSRC pin instead of BAT.

To enable the CHG FET, set the CHG_ON bit to 1. To disable it, set the CHG_ON bit to 0. Similarly, the discharge FET can be controlled through the DSG_ON bit.

Certain fault conditions or power state transitions will clear the state of the CHG/DSG FET controls.

The host microcontroller is responsible for initiating all protection recovery. To resume FET operation after a fault condition, the host microcontroller must first clear the corresponding status bit in the SYS_STAT register, which will reset the ALERT pin, and then manually re-enable the CHG and/or DSG bits. Certain faults, such as COV or CUV, may immediately re-trigger if such a condition still persists. The SGM90116H does not automatically set either CHG_ON or DSG_ON to 1 under any conditions.

DETAILED DESCRIPTION (continued)

Table 2. CHG, DSG Response under Various System Events

EVENT	CHG_ON Bit	DSG_ON Bit
COV Fault	Set to 0	—
CUV Fault	—	Set to 0
SCD Fault	—	Set to 0
OCD1 Fault	—	Set to 0
OCD2 Fault	—	Set to 0
OCC Fault	Set to 0	—
OTC Fault	Set to 0	—
UTC Fault	Set to 0	—
OTD Fault	—	Set to 0
UTD Fault	—	Set to 0
OTINT Fault	Set to 0	Set to 0
UTINT Fault	Set to 0	Set to 0
HWD Fault	Set to 0	Set to 0
ALERT Override	Set to 0	Set to 0
Enter Ship Mode from Normal	Set to 0	Set to 0

Load Detection

When CHG_ON bit is disabled, the load detection circuit on the CHG pin becomes active.

When the high impedance (approximately 1MΩ) pull-down path holds the CHG pin to VSS, the load detection circuit detects whether the CHG pin is externally pulled high. This action can determine whether the PACK- pin (located outside the AFE) keeps at a high voltage level, which is particularly useful when a load is connected and the power FETs are off. The LOAD_PRESETN bit in the SYS_CTRL1 register can read the status of load detection circuit.

After an OCD or SCD fault, the DSG FET will be disabled, and the CHG FET should also be disabled to activate the load detection circuit. The host microcontroller can periodically pull the LOAD_PRESENT bit to decide the state of the PACK- pin and to decide the time when the load is removed from LOAD_PRESENT = 0.

The load detection integrates an internal digital filter. The width of the filter is 6ms. If the load detection signal width succeeds the filter's width, the load detection signal will be set.

Alert

The ALERT pin acts as an active-high digital interrupt signal that can be connected to a GPIO port of the host microcontroller. This signal is an OR logic of all bits in the SYS_STAT register.

To clear the alert signal, the corresponding source bit in the SYS_STAT register must be cleared by writing a "1" to that bit. This action will automatically clear the ALERT pin once all bits are reset.

In cases where the source of the alert signal persists, the clear operation may temporarily clean the alert signal, but it will re-toggle in the next sample edge.

LDO over-temperature alert cannot be cleared until the over-temperature condition no longer exists.

The ALERT pin can also be driven externally. For instance, the pack may include a secondary over-voltage protector IC. If the ALERT pin is externally forced high while it is low, the device interprets this as an OVRD_ALERT fault and sets the OVRD_ALERT bit. This results in an automatic disabling of both CHG and DSG FET drivers. However, the device cannot recognize an ALERT signal input as high if it is already being forced high due to another condition.

An internal 2ms filter is included to detect the secondary over-voltage signal. If the ALERT output is low while the external protector IC forces the pin to be high, a secondary over-voltage fault is detected.

Output LDO

An adjustable output voltage regulator LDO is provided to power additional components in the battery pack, like the host microcontroller or LEDs. The LDO is configured during the production test process using NVM and supports options of 1.8V, 2.5V, 3.0V, 3.3V, and 5.0V. The host can modify LDO_CFG[2:0] bits to adjust the output voltage.

For efficient power distribution and reduced package power dissipation, a cascade small-signal FET must be added in the external path between BAT and REGSRC.

FUSE

The SGM90116H employs a fuse blower logic. The duration of the fuse blower can be configured using the FUSE_BT register. The fuse blower logic can be enabled by setting the FUSE_SET bit in the REG_CFG register. This logic becomes disabled either when the FUSE_BT time elapses or when the FUSE_CLR bit is set in the REG_CFG register.

DETAILED DESCRIPTION (continued)

Charge and Discharge Detection

The SGM90116H detects charge and discharge operations by detecting the "SRP-SRN" voltage. If the voltage is positive, then a charge operation is detected. The OTC/UTC protection scheme is operated if it is enabled. Conversely, if the voltage is negative, then a discharge operation is detected. The OTD/UTD protection scheme is operated if it is enabled.

Communication Subsystem

The AFE implements a standard 100kHz I^2C interface and acts as a slave device. The I^2C device address is 7-bit and is factory programmed.

A write transaction is shown in Figure 3. Block writes are allowed by sending additional data bytes before the STOP. The I^2C block will auto-increment the register address after each data byte.

When enabled, the CRC is calculated as follows:

In a single-byte write transaction, the CRC is calculated over the slave address, register address, and data.

In a block write transaction, the CRC for the first data byte is calculated over the slave address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the slave detects a bad CRC, the I^2C slave will not acknowledge (NCK) the CRC, which causes the I^2C slave to go to an idle state.

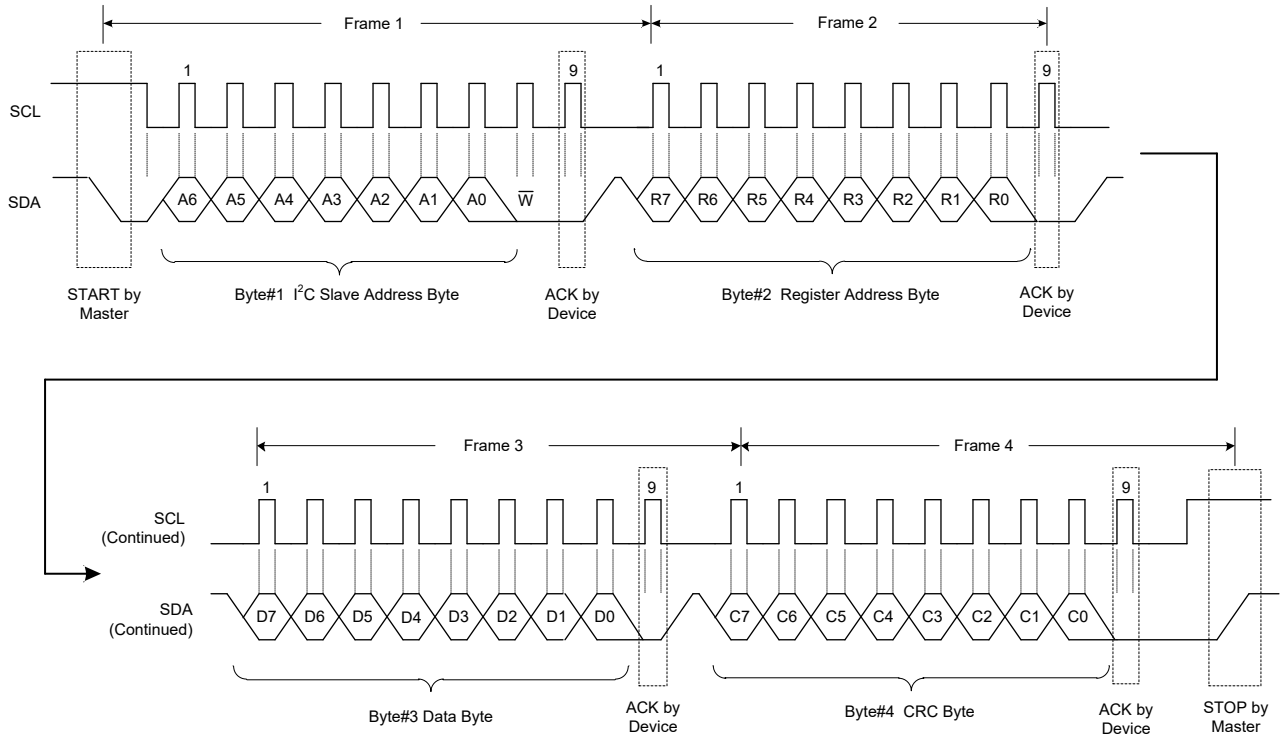


Figure 3. I^2C Write Format

DETAILED DESCRIPTION (continued)

Figure 4 shows a read transaction using a Repeated Start.

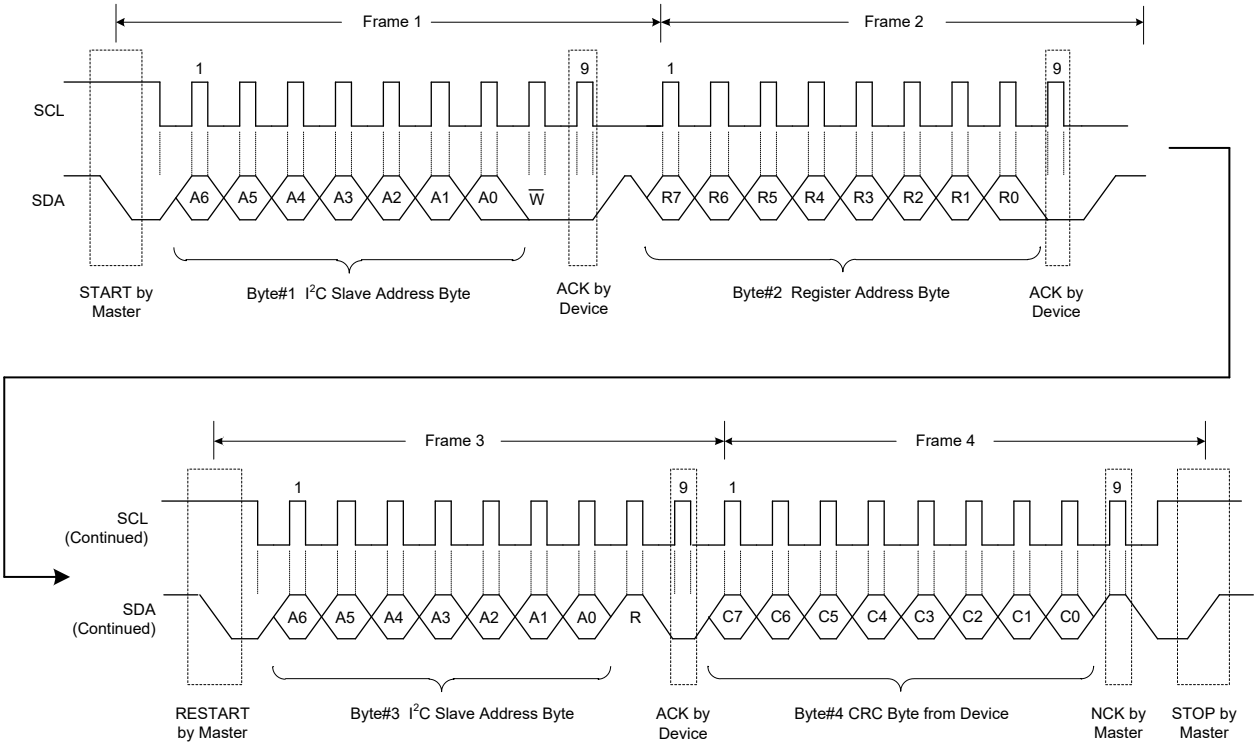


Figure 4. I²C Read Format with Repeated Start

DETAILED DESCRIPTION (continued)

Figure 5 shows a read transaction where a repeated START is not used, for example if not available in hardware. For a block read, the master ACK's each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte.

When enabled, the CRC for a read transaction is calculated as follows:

In a single-byte read transaction, the CRC is calculated after the second start and uses the slave address and data byte.

In a block read transaction, the CRC for the first data byte is calculated after the second start and uses the slave address and data byte. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the master detects a bad CRC, the I²C master will not acknowledge the CRC, which causes the I²C slave to go to an idle state.

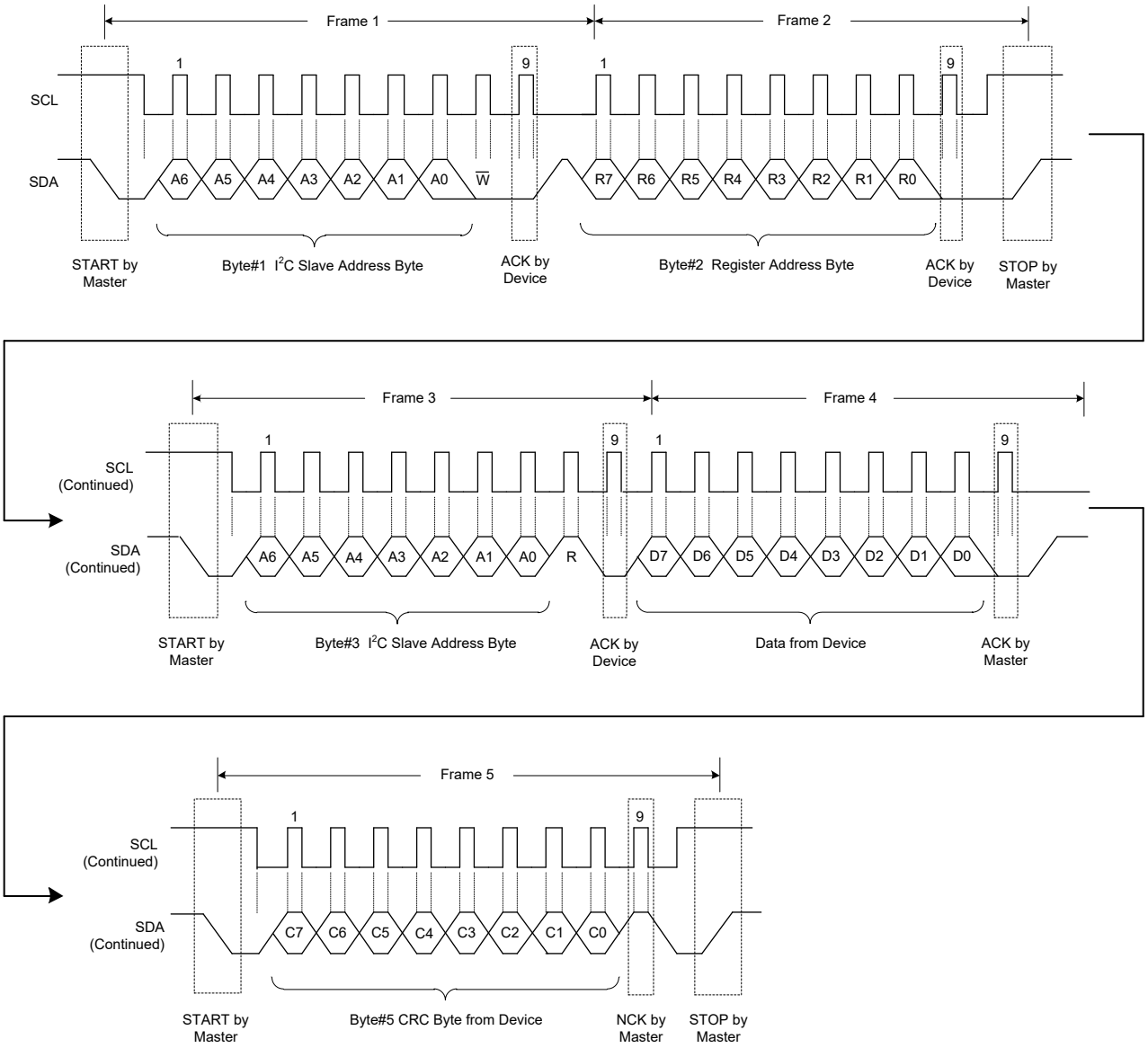


Figure 5. I²C Read Format without Repeated Start

OPERATION MODE

The SGM90116H supports two operation modes: normal mode and ship mode.

Normal Mode

In normal mode, all blocks are enabled, and the device consumes the highest current. To save power, certain blocks/functions such as VADC, IADC and CC may be disabled. OV and UV run continuously as long as the ADC is enabled. The OCD and SCD comparators cannot be disabled in this mode.

The host initiates the transition from normal to ship mode, which requires consecutive writes to two bits in the SYS_CTRL1 register.

Ship Mode

Ship mode is the basic and lowest power mode that SGM90116H supports. It is automatically entered during initial pack assembly and after every POR event. When the device is in normal mode, the host controller can enter ship mode through a specific sequence of I^2C commands.

In ship mode, only a minimum of blocks are turned on, including the BG power supply and primal boot detector. To wake from ship mode to normal mode, the WAKE pin must be pulled greater than V_{BOOT}, which triggers the device boot-up sequence.

WAKE pin should be connected to ground via 2 cascaded diodes. Please refer to the typical application (Figure 6) for detailed around circuits.

To enter ship mode from normal mode, the SHUT_A and SHUT_B bits in the SYS_CTRL1 register must be consecutively written in a specific sequence:

Write #1: SHUT_A = 0, SHUT_B = 1

Write #2: SHUT_A = 1, SHUT_B 0

Note that SHUT_A and SHUT_B should each be in a 0 state before executing the shutdown command above. If this specific sequence is entered into the device, the device transitions into ship mode. Any other sequence written to the SHUT_A and SHUT_B bits or incorrect entry of either of the two patterns will prevent the device from entering ship mode.

The device will enter ship mode during a POR event, but this is not a recommended method of ship mode entry. If the supply voltage falls below V_{SHUT} and then back up above V_{POR}, the device defaults into the SHIP mode state. This is similar to an initial pack assembly condition. To exit ship mode into normal mode, the device must follow the standard boot sequence by applying a voltage greater than the V_{BOOT} threshold on the TS1/WAKE pin.

TYPICAL APPLICATIONS

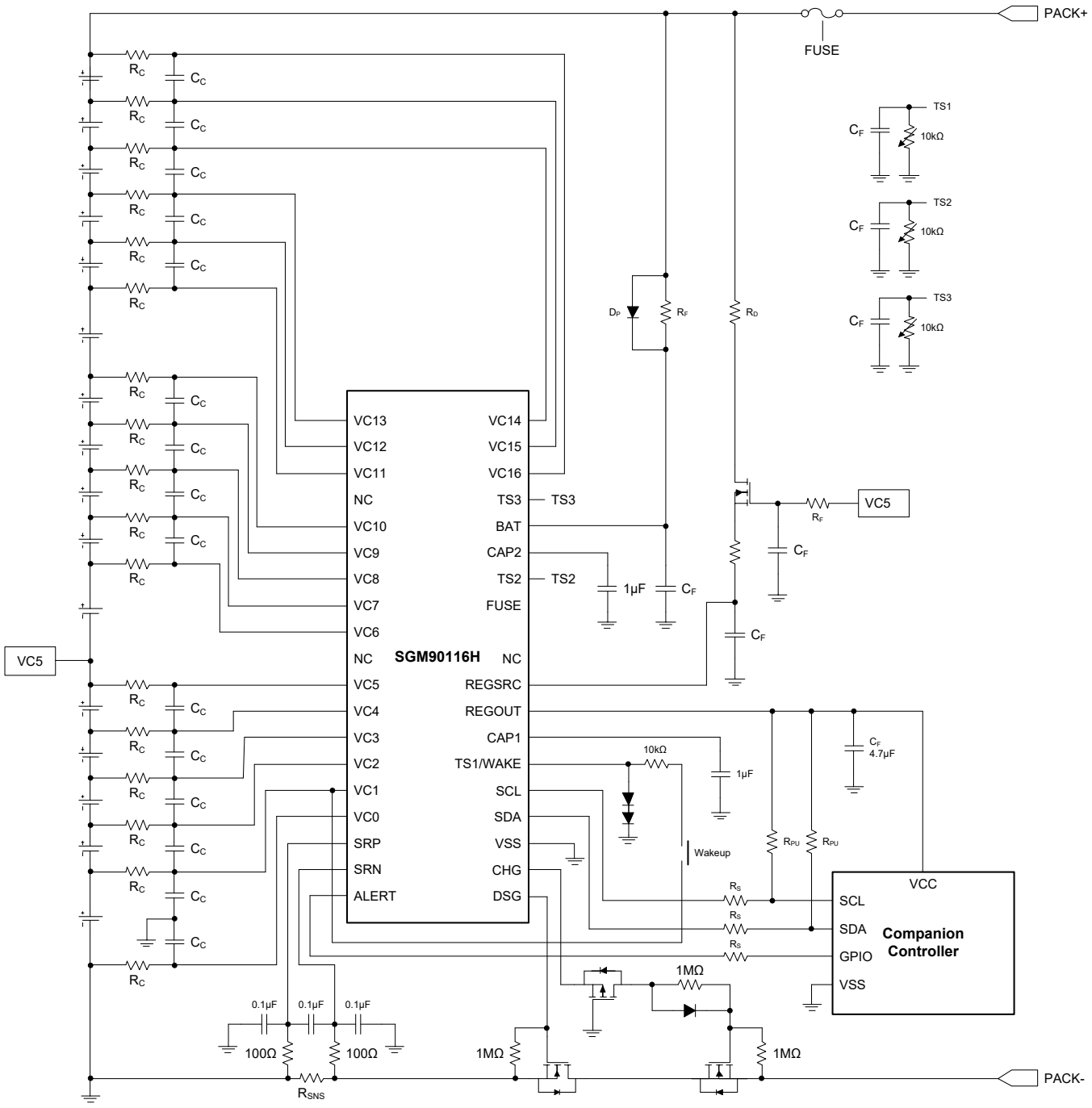


Figure 6. Typical Application

REGISTER DESCRIPTION

Summary Register Map

NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
SYS_STAT	0x00	CC_READY	RSVD	DEV_READY	OVRD_ALERT	UV	OV	SCD	OCD1
CELL_BAL1	0x01	RSVD			CB[5:1]				
CELL_BAL2	0x02	RSVD			CB[10:6]				
CELL_BAL3	0x03	RSVD		CB[16:11]					
SYS_CTRL1	0x04	LOAD_PRESENT	RSVD	IADC_EN	VADC_EN	TEMP_SEL	BAT_SEL	SHUT_A	SHUT_B
SYS_CTRL2	0x05	RSVD	CC_EN	CC_ONESHOT	SETTLE[1:0]		CC_SRC	DSG_ON	CHG_ON
PROTECT1	0x06	RSNS	RSVD		SCD_DLY[1:0]		SCD_THD[2:0]		
PROTECT2	0x07	RSVD	OCD_DLY[2:0]			OCD_THD[3:0]			
PROTECT3	0x08	UV_DLY[1:0]		OV_DLY[1:0]		RSVD			
OV_TRIP	0x09	OV_THD[7:0]							
UV_TRIP	0x0A	UV_THD[7:0]							
SYNC_STATE	0x0B	RSVD			VCHNL[4:0]				
VC1_HI	0x0C	ADC[15:8]							
VC1_LO	0x0D	ADC[7:0]							
VC2_HI	0x0E	ADC[15:8]							
VC2_LO	0x0F	ADC[7:0]							
VC3_HI	0x10	ADC[15:8]							
VC3_LO	0x11	ADC[7:0]							
VC4_HI	0x12	ADC[15:8]							
VC4_LO	0x13	ADC[7:0]							
VC5_HI	0x14	ADC[15:8]							
VC5_LO	0x15	ADC[7:0]							
VC6_HI	0x16	ADC[15:8]							
VC6_LO	0x17	ADC[7:0]							
VC7_HI	0x18	ADC[15:8]							
VC7_LO	0x19	ADC[7:0]							
VC8_HI	0x1A	ADC[15:8]							
VC8_LO	0x1B	ADC[7:0]							
VC9_HI	0x1C	ADC[15:8]							
VC9_LO	0x1D	ADC[7:0]							
VC10_HI	0x1E	ADC[15:8]							
VC10_LO	0x1F	ADC[7:0]							
VC11_HI	0x20	ADC[15:8]							
VC11_LO	0x21	ADC[7:0]							
VC12_HI	0x22	ADC[15:8]							
VC12_LO	0x23	ADC[7:0]							
VC13_HI	0x24	ADC[15:8]							
VC13_LO	0x25	ADC[7:0]							
VC14_HI	0x26	ADC[15:8]							
VC14_LO	0x27	ADC[7:0]							
VC15_HI	0x28	ADC[15:8]							
VC15_LO	0x29	ADC[7:0]							
BAT_HI	0x2A	ADC[15:8]							
BAT_LO	0x2B	ADC[7:0]							
TS1_HI	0x2C	ADC[15:8]							
TS1_LO	0x2D	ADC[7:0]							
TS2_HI	0x2E	ADC[15:8]							
TS2_LO	0x2F	ADC[7:0]							

REGISTER DESCRIPTION (continued)

NAME	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
TS3_HI	0x30	ADC[15:8]							
TS3_LO	0x31	ADC[7:0]							
CC_HI	0x32	ADC[15:8]							
CC_LO	0x33	ADC[7:0]							
CUR_HI	0x34	CUR_ADC[15:8]							
CUR_LO	0x35	CUR_ADC[7:0]							
VC16_HI	0x40	ADC[15:8]							
VC16_LO	0x41	ADC[7:0]							
REF_HI	0x44	ADC[15:8]							
REF_LO	0x45	ADC[7:0]							
SYS_STAT2	0x48	OTINT	UTINT	OTD	UTD	OTC	UTC	OCC	OCD2
SYS_STAT3	0x49	RSVD					OTP	OVF	HWD
SYS_STAT4	0x4A	CUV_F16	CUV_F15	CUV_F14	CUV_F13	CUV_F12	CUV_F11	CUV_F10	CUV_F9
SYS_STAT5	0x4B	CUV_F8	CUV_F7	CUV_F6	CUV_F5	CUV_F4	CUV_F3	CUV_F2	CUV_F1
SYS_STAT6	0x4C	COV_F16	COV_F15	COV_F14	COV_F13	COV_F12	COV_F11	COV_F10	COV_F9
SYS_STAT7	0x4D	COV_F8	COV_F7	COV_F6	COV_F5	COV_F4	COV_F3	COV_F2	COV_F1
SYS_STAT8	0x4E	RSVD	UTC_F3	UTC_F2	UTC_F1	RSVD	OTC_F3	OTC_F2	OTC_F1
SYS_STAT9	0x4F	RSVD	UTD_F3	UTD_F2	UTD_F1	RSVD	OTD_F3	OTD_F2	OTD_F1
REG_CFG	0x5E	FUSE_SET	FUSE_CLR	EN_2LVL	RSVD			LDO_CFG[2:0]	
PROT_EN	0x5F	OTINT_EN	UTINT_EN	UTD_EN	OTD_EN	UTC_EN	OTC_EN	OCC_EN	OCD2_EN
OCD2_THD	0x60	RSVD	OCD2_THD[6:0]						
OCD2_DLY	0x61	OCD2_DLY[7:0]							
OCC_THD	0x62	RSVD		OCC_THD[5:0]					
OCC_DLY	0x63	OCC_DLY[7:0]							
OTC_THD_HI	0x64	OTC_THD[15:8]							
OTC_THD_LO	0x65	OTC_THD[7:0]							
OTC_DLY	0x66	OTC_DLY[7:0]							
OTD_THD_HI	0x67	OTD_THD[15:8]							
OTD_THD_LO	0x68	OTD_THD[7:0]							
OTD_DLY	0x69	OTD_DLY[7:0]							
UTC_THD_HI	0x6A	UTC_THD[15:8]							
UTC_THD_LO	0x6B	UTC_THD[7:0]							
UTC_DLY	0x6C	UTC_DLY[7:0]							
UTD_THD_HI	0x6D	UTD_THD[15:8]							
UTD_THD_LO	0x6E	UTD_THD[7:0]							
UTD_DLY	0x6F	UTD_DLY[7:0]							
OTINT_THD_HI	0x70	OTINT_THD[15:8]							
OTINT_THD_LO	0x71	OTINT_THD[7:0]							
OTINT_DLY	0x72	OTINT_DLY[7:0]							
UTINT_THD_HI	0x73	UTINT_THD[15:8]							
UTINT_THD_LO	0x74	UTINT_THD[7:0]							
UTINT_DLY	0x75	UTINT_DLY[7:0]							
HWD_DLY	0x76	HWD_DLY[7:0]							
FUSE_BT	0x77	FUSE_BT[7:0]							
MANU_ID_HI	0x7A	MANU_ID[15:8]							
MANU_ID_LO	0x7B	MANU_ID[7:0]							

REGISTER DESCRIPTION (continued)

Bit Types:
R: Read only
W: Write only
R/W: Read/Write
W1C: Write 1 to clear

Detailed Registers

0x00: SYS_STAT Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	CC_READY	R/W	0	If CC_SRC = 0, a fresh coulomb counter reading is available. If CC_SRC = 1, a fresh current reading is available. Note that if this bit is not cleared between two adjacent CC readings, it will remain latched to 1 and can only be cleared by the host. 0 = Fresh CC/CUR reading is not available or this bit is cleared by host. 1 = Fresh CC/CUR reading is available. Remain latched high until cleared.
D[6]	RSVD	R/W	0	Reserved
D[5]	DEV_RDY	R/W	1	Device Ready Bit. The host should wait the device ready bit change to 0 and can start monitor function.
D[4]	OVRD_ALERT	R/W	0	External pull-up on the ALERT pin indicator. Only active when ALERT pin is not already being driven high by the AFE itself. 0 = No external override detected 1 = External override detected. Remain latched high until cleared by host.
D[3]	UV	R/W	0	Under-voltage fault event indicator. 0 = No UV fault is detected 1 = UV fault is detected. Remain latched high until cleared by the host.
D[2]	OV	R/W	0	Over-voltage fault event indicator. 0 = No OV fault is detected 1 = OV fault is detected. Remain latched high until cleared by the host.
D[1]	SCD	R/W	0	Short-Circuit During Discharge Fault Event Indicator. 0 = No SCD fault is detected 1 = SCD fault is detected. Remain latched high until cleared by the host.
D[0]	OCD1	R/W	0	Over-Current During Discharge Fault (OCD1) Event Indicator. 0 = No OCD1 fault is detected 1 = OCD1 fault is detected. Remain latched high until cleared by the host.

0x01: CELL_BAL1 Resister

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:5]	RSVD	R/W	000	Reserved
D[4:0]	CB[5:1]	R/W	00000	Cell5 to cell1 balancing on, high enable.

0x02: CELL_BAL2 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:5]	RSVD	R/W	000	Reserved
D[4:0]	CB[10:6]	R/W	00000	Cell10 to cell6 balancing on, high enable.

0x03: CELL_BAL3 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:6]	RSVD	R/W	00	Reserved
D[5:0]	CB[16:11]	R/W	000000	Cell16 to cell11 balancing on, high enable.

REGISTER DESCRIPTION (continued)

0x04: SYS_CTRL1 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	LOAD_PRESENT	R/W	0	Valid only when CHG_ON = 0. When the CHG pin voltage is detected higher than VLOAD_DETECT, Bit [7] will be active high, external load is present. This bit is read-only and will be automatically cleared when load is removed. 0 = CHG pin < V_{LOAD_DETECT} or CHG_ON = 1 1 = CHG pin > V_{LOAD_DETECT} or CHG_ON = 0
D[6]	RSVD	R/W	0	Reserved
D[5]	IADC_EN	R/W	0	IADC Enable, Active-High. 0 = Disable current monitor 1 = Enable current monitor
D[4]	VADC_EN	R/W	0	VADC Enable, Active-High. 0 = Disable voltage and temperature ADC readings (also disable OV protection) 1 = Enable voltage and temperature ADC readings (also enable OV protection)
D[3]	TEMP_SEL	R/W	0	TS1_HI and TS1_LO Temperature Source. 0 = Store internal die temperature in TS1_HI and TS1_LO 1 = Store TS1/WAKE thermistor reading in TS1_HI and TS1_LO
D[2]	BAT_SEL	R/W	0	BAT_HI and BAT_LO Source. 0 = sum of all battery cells 1 = direct capture VC16 pin voltage
D[1]	SHUT_A	R/W	0	Shutdown commands from host microcontroller. Must be written in a specific sequence, shown below = start from SHUT_A = 0, SHUT_B = 0 write #1 = SHUT_A = 0, SHUT_B = 1 write #2 = SHUT_A = 1, SHUT_B = 0
D[0]	SHUT_B	R/W	0	

0x05: SYS_CTRL2 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSVD	R/W	0	Reserved and should be kept at 0.
D[6]	CC_EN	R/W	0	Coulomb counter continuous operation enable command. If set high, CC_ONESHOT bit is ignored. 0 = Disable CC continuous readings 1 = Enable CC continuous readings and ignore CC_ONESHOT state
D[5]	CC_ONESHOT	R/W	0	Trigger Single Coulomb Counter Conversion Command. After set this bit, the coulomb counter will convert one time, and then turned back off. If CC_SRC set to 0, the CC_READY bit will be set to 1 after the coulomb counter conversion finished. 0 = No action 1 = Enable single CC reading (only valid if CC_EN = 0 and CC_READY = 1)
D[4:3]	SETTLE[1:0]	R/W	00	Settle Time: the settle time for each slot in normal mode 0x0 = 0.976ms settle time, filter average 8 times, total conversion time is 250ms 0x1 = 4.883ms settle time, filter average 8 times, total conversion time is 332ms 0x2 = 8.789ms settle time, filter average 4 times, total conversion time is 332ms 0x3 = 11.719ms settle time, no average, total conversion time is 332ms
D[2]	CC_SRC	R/W	0	CC FLAG Source 0 = column counting conversion ready as CC_READY source 1 = current conversion ready as CC_READY source
D[1]	DSG_ON	R/W	0	Discharge FET driver or discharge signal control. 0 = DSG is off 1 = DSG is on
D[0]	CHG_ON	R/W	0	Charge FET driver control. 0 = CHG is off 1 = CHG is on

REGISTER DESCRIPTION (continued)

0x06: PROTECT1 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSNS	R/W	0	Allow for doubling the OCD and SCD threshold simultaneously.
D[6:5]	RSVD	R/W	00	Reserved
D[4:3]	SCD_DLY[1:0]	R/W	0	Short-circuit in discharge delay setting. 0x0 = 80μs 0x1 = 105μs 0x2 = 200μs 0x3 = 400μs
D[2:0]	SCD_THD[2:0]	R/W	0	Shout-circuit in discharge threshold setting. 0x0 = 44mV (RSNS = 1), 22mV (RSNS = 0) 0x1 = 66mV (RSNS = 1), 33mV (RSNS = 0) 0x2 = 88mV (RSNS = 1), 44mV (RSNS = 0) 0x3 = 110mV (RSNS = 1), 55mV (RSNS = 0) 0x4 = 132mV (RSNS = 1), 66mV (RSNS = 0) 0x5 = 154mV (RSNS = 1), 77mV (RSNS = 0) 0x6 = 176mV (RSNS = 1), 88mV (RSNS = 0) 0x7 = 198mV (RSNS = 1), 99mV (RSNS = 0)

0x07: PROTECT2 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSVD	R/W	0	Reserved
D[6:4]	OCD_DLY[2:0]	R/W	0	Over-Current in Discharging Delay Setting. 0x0 = 8ms 0x1 = 20ms 0x2 = 40ms 0x3 = 80ms 0x4 = 160ms 0x5 = 320ms 0x6 = 640ms 0x7 = 1280ms
D[3:0]	OCD_THD[3:0]	R/W	0	Over-Current in Discharge Threshold. 0x0 = 12mV (RNS = 1), 6mV (RNS = 0) 0x1 = 18mV (RNS = 1), 9mV (RNS = 0) 0x2 = 24mV (RNS = 1), 12mV (RNS = 0) 0x3 = 30mV (RNS = 1), 15mV (RNS = 0) 0x4 = 36mV (RNS = 1), 18mV (RNS = 0) 0x5 = 42mV (RNS = 1), 21mV (RNS = 0) 0x6 = 48mV (RNS = 1), 24mV (RNS = 0) 0x7 = 54mV (RNS = 1), 27mV (RNS = 0) 0x8 = 60mV (RNS = 1), 30mV (RNS = 0) 0x9 = 66mV (RNS = 1), 33mV (RNS = 0) 0xA = 72mV (RNS = 1), 36mV (RNS = 0) 0xB = 78mV (RNS = 1), 39mV (RNS = 0) 0xC = 84mV (RNS = 1), 42mV (RNS = 0) 0xD = 90mV (RNS = 1), 45mV (RNS = 0) 0xE = 96mV (RNS = 1), 48mV (RNS = 0) 0xF = 102mV (RNS = 1), 51mV (RNS = 0)

0x08: PROTECT3 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:6]	UV_DLY[1:0]	R/W	0	Under-voltage delay setting. 0x0 = 1s 0x1 = 4s 0x2 = 8s 0x3 = 16s
D[5:4]	OV_DLY[1:0]	R/W	0	Over-voltage delay setting. 0x0 = 1s 0x1 = 2s 0x2 = 4s 0x3 = 8s
D[3:0]	RSVD	R/W	0000	Reserved

REGISTER DESCRIPTION (continued)

0x09: OV_TRIP Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OV_THD[7:0]	R/W	10101100	Middle 8 bits of the direct ADC mapping of the desired OV protection threshold, with upper 2 MSB set to 10 and lower 6LSB set to 100000. The equivalent OV threshold is mapped to: 10_OV_THD<7:0>_100000. By default, OV_TRIP is configured to 0xAC setting.

0x0A: UV_TRIP Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UV_THD[7:0]	R/W	10010111	Middle 8 bits of the direct ADC mapping of the desired UV protection threshold, with upper 2 MSB set to 01 and lower 6LSB set to 000000. The equivalent UV threshold is mapped to: 01_UV_THD<7:0>_000000. By default, UV_TRIP is configured to 0x97 setting.

0x0B: SYNC_STATE Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:5]	RSVD	R	000	Reserved
D[4:0]	VCHNL[4:0]	R	00000	0x00 = Empty Channel 0x09 = EXTS3 0x0A = EXTS2 0x0B = EXTS1 0x0C = EXTS0 0x0D = Die Temperature 0x0E = Internal V_{REF} Channel 0x0F = V_{BAT} Channel 0x10 = V_{CELL1} 0x11 = V_{CELL2} 0x12 = V_{CELL3} 0x13 = V_{CELL4} 0x14 = V_{CELL5} 0x15 = V_{CELL6} 0x16 = V_{CELL7} 0x17 = V_{CELL8} 0x18 = V_{CELL9} 0x19 = V_{CELL10} 0x1A = V_{CELL11} 0x1B = V_{CELL12} 0x1C = V_{CELL13} 0x1D = V_{CELL14} 0x1E = V_{CELL15} 0x1F = V_{CELL16}

0x0C ~ 0x29 (x = 1,2,3….15): VCx_HI and VCx_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	VCx_HI[15:8]	R	00000000	Voltage readout for Cell0 to Cell15. Always returned as an atomic value if both high and low registers are read in the same transaction.
D[7:0]	VCx_LO[7:0]	R	00000000	

0x2A ~ 0x2B: BAT_HI and BAT_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	BAT_HI[15:8]	R	00000000	Battery voltage readout for BAT or sum of cell voltage.
D[7:0]	BAT_LO[7:0]	R	00000000	

REGISTER DESCRIPTION (continued)

0x2C ~ 0x2D: TS1_HI and TS1_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	TS1_HI[15:8]	R	00000000	Die Temperature. Thermistor Voltage Readout for TS1. Determined by TEMP_SEL bit of SYS_CTRL1 register.
D[7:0]	TS1_LO[7:0]	R	00000000	

0x2E ~ 0x2F: TS2_HI and TS2_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	TS2_HI[15:8]	R	00000000	Thermistor Voltage Readout for TS2.
D[7:0]	TS2_LO[7:0]	R	00000000	

0x30 ~ 0x31: TS3_HI and TS3_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	TS3_HI[15:8]	R	00000000	Thermistor Voltage Readout for TS3.
D[7:0]	TS3_LO[7:0]	R	00000000	

0x32 ~ 0x33: CC_HI and CC_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	CC_HI[15:8]	R	00000000	Coulomb Counter Readout.
D[7:0]	CC_LO[7:0]	R	00000000	

0x34 ~ 0x35: CUR_HI and CUR_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	CUR_HI[15:8]	R	00000000	Current Readout.
D[7:0]	CUR_LO[7:0]	R	00000000	

0x40 ~ 0x41: VOLT16_HI and VOLT16_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	VOLT_HI[15:8]	R	00000000	Cell16 Voltage Readout.
D[7:0]	VOLT_LO[7:0]	R	00000000	

0x44 ~ 0x45: REF_HI and REF_LO Registers

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[15:8]	REF_HI[15:8]	R	00000000	Reference Voltage Readout for VREF2.
D[7:0]	REF_LO[7:0]	R	00000000	

REGISTER DESCRIPTION (continued)

0x48: SYS_STAT2 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	OTINT	R/W1C	0	Internal temperature sensor over-temperate fault event indicator. 0 = No OTINT fault is detected 1 = OTINT fault is detected. Remain latched high until cleared by the host.
D[6]	UTINT	R/W1C	0	Internal temperature sensor under-temperate fault event indicator. 0 = No UTINT fault is detected 1 = UTINT fault is detected. Remain latched high until cleared by the host.
D[5]	OTD	R/W1C	0	Thermistor over-temperate during discharging fault event indicator. 0 = No OTD fault is detected 1 = OTD fault is detected. Remain latched high until cleared by the host.
D[4]	UTD	R/W1C	0	Thermistor under-temperate during discharging fault event indicator. 0 = No UTD fault is detected 1 = UTD fault is detected. Remain latched high until cleared by the host.
D[3]	OTC	R/W1C	0	Thermistor over-temperate during charging fault event indicator. 0 = No OTC fault is detected 1 = OTC fault is detected. Remain latched high until cleared by the host.
D[2]	UTC	R/W1C	0	Thermistor under-temperate during charging fault event indicator. 0 = No UTC fault is detected 1 = UTC fault is detected. Remain latched high until cleared by the host.
D[1]	OCC	R/W1C	0	Over-current during charging fault event indicator. 0 = No OCC fault is detected 1 = OCC fault is detected. Remain latched high until cleared by the host.
D[0]	OCD2	R	0	Over-Current during Discharge fault (OCD2) event indicator. 0 = No OCD2 fault is detected 1 = OCD2 fault is detected. Remain latched high until cleared by the host.

0x49: SYS_STAT3 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:3]	RSVD	R/W1C	00000	Reserved
D[2]	OTP	R	0	Internal LDO over-temperature protection.
D[1]	OVF	R/W1C	0	Calculation overflow. 0 = No overflow happened 1 = Calculation overflow happened
D[0]	HWD	R/W1C	0	Hardware Watchdog fault event indicator. 0 = No HWD fault is detected 1 = HWD fault is detected. Remain latched high until cleared by the host.

0x4A: SYS_STAT4 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	CUV_F[16:9]	R	00000000	Cellx CUV Status (x = 9 ~ 16).

0x4B: SYS_STAT5 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	CUV_F[8:1]	R	00000000	Cellx CUV Status (x = 1 ~ 8).

0x4C: SYS_STAT6 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	COV_F[16:9]	R	00000000	Cellx COV Status (x = 9 ~ 16).

0x4D: SYS_STAT7 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	COV_F[8:1]	R	00000000	Cellx COV Status (x = 1 ~ 8).

REGISTER DESCRIPTION (continued)

0x4E: SYS_STAT8 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSVD	R	0	Reserved
D[6:4]	UTC_F[3:1]	R	000	NTC Under-Temperature in Charging Fail, x = (1 ~ 3)
D[3]	RSVD	R	0	Reserved
D[2:0]	OTC_F[3:1]	R	000	NTCx Over-Temperature in Charging Fail (x = 1 ~ 3)

0x4F: SYS_STAT9 Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSVD	R	0	Reserved
D[6:4]	UTD_F[3:1]	R	000	NTC Under-Temperature in Discharging Fail, x = (1 ~ 3)
D[3]	RSVD	R	0	Reserved
D[2:0]	OTD_F[3:1]	R	000	NTCx Over-Temperature in Discharging Fail (x = 1 ~ 3)

0x5E: REG_CFG Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	FUSE_SET	W1C	0	FUSE Blower Enable
D[6]	FUSE_CLR	W1C	0	FUSE Blower Disable
D[5]	EN_2LVL	W1C	0	OVRD ALERT Enable
D[4:3]	RSVD	R/W	00	Reserved
D[2:0]	LDO_CFG[2:0]	R/W	010	REGOUT Voltage Select. 0x0 = 1.8V 0x1 = 2.5V 0x2 = 3.0V (default) 0x3 = 3.3V 0x4 = 5.0V

0x5F: PROT_EN Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	OTINT_EN	R/W	0	OTINT_EN bit. 1 = Enabled. 0 = Disabled.
D[6]	UTINT_EN	R/W	0	UTINT_EN bit. 1 = Enabled. 0 = Disabled.
D[5]	UTD_EN	R/W	0	UTD_EN bit. 1 = Enabled. 0 = Disabled.
D[4]	OTD_EN	R/W	0	OTD_EN bit. 1 = Enabled. 0 = Disabled.
D[3]	UTC_EN	R/W	0	UTC_EN bit. 1 = Enabled. 0 = Disabled.
D[2]	OTC_EN	R/W	0	OTC_EN bit. 1 = Enabled. 0 = Disabled.
D[1]	OCC_EN	R/W	0	OCC_EN bit. 1 = Enabled. 0 = Disabled.
D[0]	OCD2_EN	R/W	0	OCD2_EN bit. 1 = Enabled. 0 = Disabled.

REGISTER DESCRIPTION (continued)

0x60: OCD2_THD Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7]	RSVD	R/W	0	Reserved
D[6:0]	OCD2_THD[6:0]	R/W	0000000	When OCD2_THD is not 0x0, OCD2 is enabled, and OCD2 value is from 2 to 100 with 2mV per step.

0x61: OCD2_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OCD2_DLY[6:0]	R/W	0000000	OCD2 value is from 1 to 127 with 2.93ms per step.

0x62: OCC_THD Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:6]	RSVD	R/W	00	Reserved
D[5:0]	OCC_THD[5:0]	R/W	000000	When OCC_THD is not 0x0, OCC is enabled, and OCC value is from 2 to 62, with 2mV per step.

0x63: OCC_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OCC_DLY[7:0]	R/W	00000000	OCC value is from 1 to 127 with 2.93ms per step, the delay value should not be set to 0.

0x64: OTC_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTC_THD[15:8]	R/W	00000000	OTC_THD 8 MSB, when OTC_THD is not 0x0, OTC is enabled.

0x65: OTC_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTC_THD[7:0]	R/W	00000000	When OTC_THD is not 0x0, OTC is enabled.

0x66: OTC_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTC_DLY[7:0]	R/W	00000000	OTC value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

0x67: OTD_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTD_THD[15:8]	R/W	00000000	OTD_THD 8 MSB, when OTD_THD is not 0x0, OTD is enabled.

0x68: OTD_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTD_THD[7:0]	R/W	00000000	When OTD_THD is not 0x0, OTD is enabled.

REGISTER DESCRIPTION (continued)

0x69: OTD_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTD_DLY[7:0]	R/W	00000000	OTD value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

0x6A: UTC_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTC_THD[15:8]	R/W	00000000	UTC_THD 8 MSB, when UTC_THD is not 0x0, UTC is enabled.

0x6B: UTC_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTC_THD[7:0]	R/W	00000000	When UTC_THD is not 0x0, UTC is enabled.

0x6C: UTC_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTC_DLY[7:0]	R/W	00000000	UTC value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

0x6D: UTD_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTD_THD[15:8]	R/W	00000000	UTD_THD 8 MSB, when UTD_THD is not 0x0, UTD is enabled.

0x6E: UTD_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTD_THD[15:8]	R/W	00000000	UTD_THD 8 MSB, when UTD_THD is not 0x0, UTD is enabled.

0x6F: UTD_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTD_DLY[7:0]	R/W	00000000	UTD value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

0x70: OTINT_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTINT_THD[15:8]	R/W	00000000	OTINT_THD 8 MSB, when OTINT_THD is not 0x0, OTINT is enabled.

0x71: OTINT_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTINT_THD[7:0]	R/W	00000000	When OTINT_THD is not 0x0, OTINT is enabled.

0x72: OTINT_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	OTINT_DLY[7:0]	R/W	00000000	OTINT value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

REGISTER DESCRIPTION (continued)

0x73: UTINT_THD_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTINT_THD[15:8]	R/W	00000000	UTINT_THD 8 MSB, when UTINT_THD is not 0x0, UTINT is enabled.

0x74: UTINT_THD_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTINT_THD[7:0]	R/W	00000000	When UTINT_THD is not 0x0, UTINT is enabled.

0x75: UTINT_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	UTINT_DLY[7:0]	R/W	00000000	UTINT value is from 1 to 255 with 0.976s per step, the delay value should not be set to 0.

0x76: HWD_DLY Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	HWD_DLY[7:0]	R/W	00000000	HWD value is from 1 to 255, with 15.6s per step, Delay time is (HWD_DLY + 1) × 16.

0x77: FUSE_BT Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	FUSE_BT[7:0]	R/W	00000000	FUSE Blower Time is set from 1 to 255 with 0.976s per step.

0x7A: MANU_ID_HI Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	MANU_ID_HI	R	00000000	0x53

0x7B: MANU_ID_LO Register

BITS	BIT NAME	TYPE	RESET	DESCRIPTION
D[7:0]	MANU_ID_LO	R/W	00000000	0x41

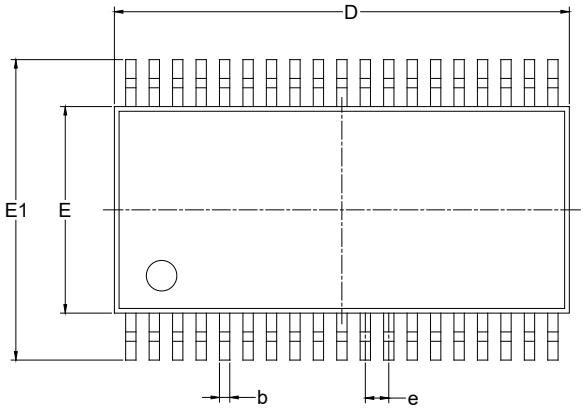
REVISION HISTORY

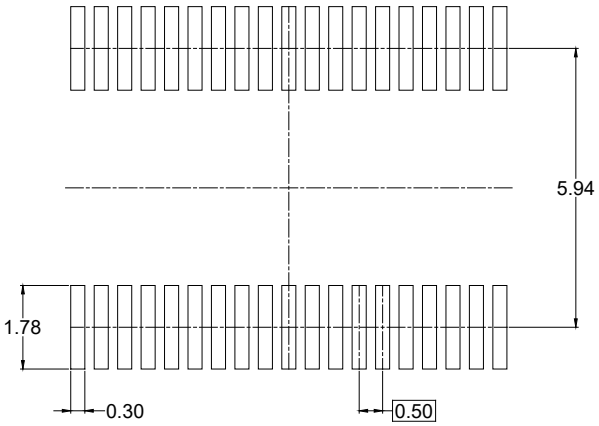
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

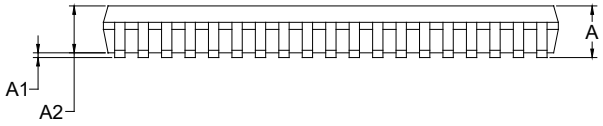
PACKAGE OUTLINE DIMENSIONS

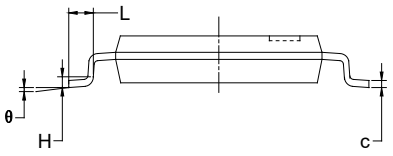
TSSOP-38





RECOMMENDED LAND PATTERN (Unit: mm)



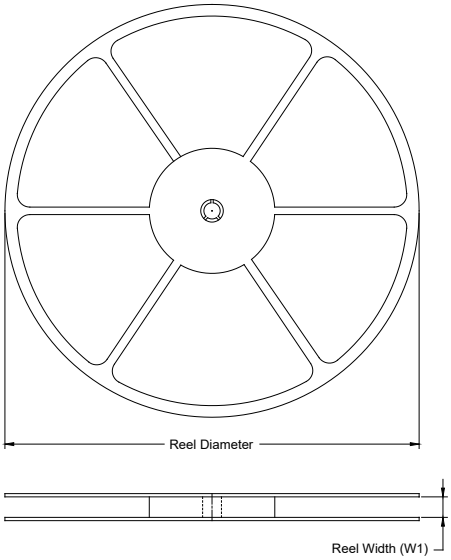


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.500 BSC		0.020 BSC	
H	0.250 TYP		0.010 TYP	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

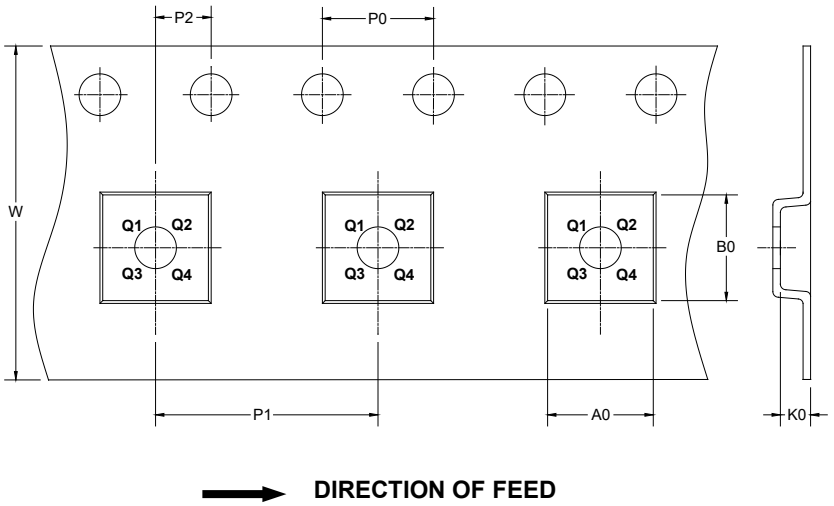
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

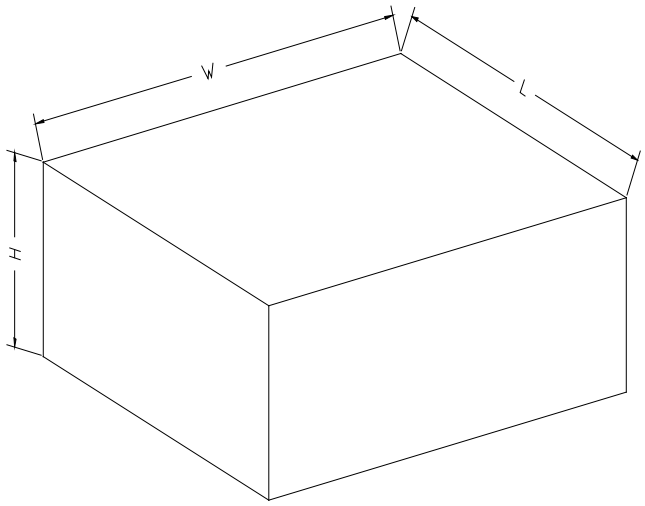
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-38	13"	16.4	6.80	10.25	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002