74LVC139A
Dual 2-Line to 4-Line Decoder/Demultiplexer

GENERAL DESCRIPTION

The 74LVC139A is a dual 2-line to 4-line decoder/ demultiplexer, which can decode two binary weighted address inputs to four mutually exclusive outputs.

The nA0 and nA1 are two binary address inputs that determine which of the four normally high outputs ($n\overline{Y}0$ to $n\overline{Y}3$) of the device will in low-state. Each decoder has an enable input of $1\overline{E}$ and $2\overline{E}$ respectively. All of the outputs are in a high-state except the case that $1\overline{E}$ and $2\overline{E}$ are low. The outputs are enabled only when all $1\overline{E}$ and $2\overline{E}$ are active. When the device operates as a 1-line to 4-line demultiplexer, one of the active-low enable inputs is used as data input. Both 3.3V and 5V devices can drive inputs, enabling this device to operate as translator in a mixed 3.3V and 5V system environment.

All inputs support Schmitt-Trigger action, which allows the circuit to tolerate slower input rise and fall times.

The 74LVC139A is available in Green SOIC-16 and TSSOP-16 packages. It operates over a temperature range of -40℃ to +125℃.

FUNCTION TABLE

CONTROL INPUT	INPUTS		OUTPUTS			
$n\overline{E}$	nA0	nA1	$n\overline{Y}0$	$n\overline{Y}1$	$n\overline{Y}2$	$n\overline{Y}3$
H	*X*	*X*	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High Voltage Level

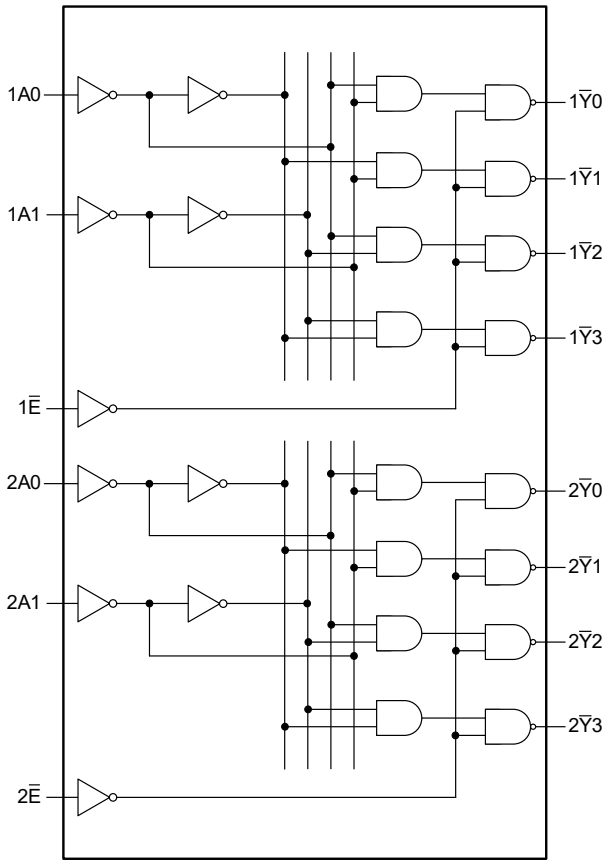
L = Low Voltage Level

X = Don't Care

FEATURES

- **Wide Supply Voltage Range: 1.2V to 3.6V**
- **Inputs Accept Voltages Higher than the Supply Voltage and up to 5.5V**
- **CMOS Low Power Dissipation**
- **Direct Interface with TTL Levels**
- **Dual Individual 2-Line to 4-Line Decoders**
- **Support Demultiplexing Function**
- **Capable of Multifunction**
- **Outputs are Mutually Exclusive**
- **Output Drive Capability: 50Ω Transmission Lines at +125℃**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-16 and TSSOP-16 Packages**

LOGIC DIAGRAM

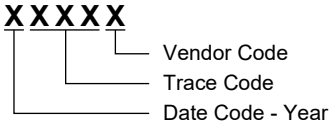


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC139A	SOIC-16	-40℃ to +125℃	74LVC139AXS16G/TR	1NQXS16 XXXXX	Tape and Reel, 2500
	TSSOP-16	-40℃ to +125℃	74LVC139AXTS16G/TR	1NS XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.5V to 6.5V
Input Voltage Range, V_I (1) ..... -0.5V to 6.5V
Output Voltage Range, V_O (1) .....-0.5V to V_{CC} + 0.5V
Input Clamp Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamp Current, I_{OK} (V_O > V_{CC} or V_O < 0V).....±50mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}) .....±50mA
Continuous Current through V_{CC} or GND.....±100mA
Junction Temperature (2).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (3) (4)
HBM.....±4000V
CDM .....±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} ..... 1.65V to 3.6V
Data Retention Only, V_{CC} ..... 1.2V to 3.6V
Input Voltage Range, V_I..... 0V to 5.5V
Output Voltage Range, V_O.....0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.65V to 2.7V..... 20ns/V (MAX)
V_{CC} = 2.7V to 3.6V..... 8ns/V (MAX)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

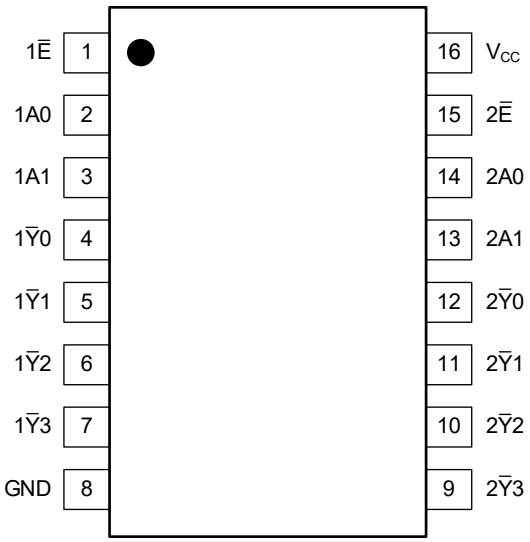
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



SOIC-16/TSSOP-16

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	1$\overline{E}$	Enable Input Pin 1 (Active-Low).
2, 3	1A0, 1A1	Address Inputs.
4, 5, 6, 7	1$\overline{Y}$0, 1$\overline{Y}$1, 1$\overline{Y}$2, 1$\overline{Y}$3	Data Outputs.
8	GND	Ground.
12, 11, 10, 9	2$\overline{Y}$0, 2$\overline{Y}$1, 2$\overline{Y}$2, 2$\overline{Y}$3	Data Outputs.
14, 13	2A0, 2A1	Address Inputs.
15	2$\overline{E}$	Enable Input Pin 2 (Active-Low).
16	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V	Full	1.08			V
		V_{CC} = 1.65V to 1.95V	Full	0.65 × V_{CC}			
		V_{CC} = 2.3V to 2.7V	Full	1.70			
		V_{CC} = 2.7V to 3.6V	Full	2.00			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V	Full			0.12	V
		V_{CC} = 1.65V to 1.95V	Full			0.35 × V_{CC}	
		V_{CC} = 2.3V to 2.7V	Full			0.70	
		V_{CC} = 2.7V to 3.6V	Full			0.80	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 3.6V, I_{OH} = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.005		V
		V_{CC} = 1.65V, I_{OH} = -4mA	Full	1.45	1.56		
		V_{CC} = 2.3V, I_{OH} = -8mA	Full	2.05	2.18		
		V_{CC} = 2.7V, I_{OH} = -12mA	Full	2.39	2.54		
		V_{CC} = 3.0V, I_{OH} = -18mA	Full	2.55	2.78		
		V_{CC} = 3.0V, I_{OH} = -24mA	Full	2.45	2.70		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65V to 3.6V, I_{OL} = 100μA	Full		0.005	0.05	V
		V_{CC} = 1.65V, I_{OL} = 4mA	Full		0.07	0.20	
		V_{CC} = 2.3V, I_{OL} = 8mA	Full		0.11	0.25	
		V_{CC} = 2.7V, I_{OL} = 12mA	Full		0.16	0.30	
		V_{CC} = 3.0V, I_{OL} = 24mA	Full		0.30	0.55	
Input Leakage Current	I_I	V_{CC} = 3.6V, V_I = 5.5V or GND	Full		±0.05	±2	μA
Supply Current	I_{CC}	V_{CC} = 3.6V, V_I = V_{CC} or GND, I_O = 0A	Full		0.05	10	μA
Additional Supply Current	ΔI_{CC}	Per input pin, V_{CC} = 2.7V to 3.6V, V_I = V_{CC} - 0.6V, I_O = 0A	Full		0.05	20	μA
Input Capacitance	C_I	V_{CC} = 0V to 3.6V, V_I = GND to V_{CC}	+25℃		4		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃ and V_{CC} = 1.2V, 1.8V, 2.5V, 2.7V and 3.3V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	nAn to n$\overline{Y}$n, see Figure 2	V_{CC} = 1.2V	+25℃		10.7		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	5.0	14.4	
			V_{CC} = 2.3V to 2.7V	Full	0.5	3.4	8.0	
			V_{CC} = 2.7V	Full	0.5	3.7	7.4	
			V_{CC} = 3.0V to 3.6V	Full	0.5	3.4	6.7	
		n$\overline{E}$ to n$\overline{Y}$n, see Figure 3	V_{CC} = 1.2V	+25℃		7.4		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	4.1	10.9	
			V_{CC} = 2.3V to 2.7V	Full	0.5	2.9	6.4	
			V_{CC} = 2.7V	Full	0.5	3.1	6.2	
			V_{CC} = 3.0V to 3.6V	Full	0.5	3.0	5.7	
Output Skew Time (3)	$t_{SK(O)}$	V_{CC} = 3.0V to 3.6V		Full			1.2	ns
Power Dissipation Capacitance (4)	C_{PD}	V_I = GND to V_{CC}	V_{CC} = 1.65V to 1.95V	+25℃		13		pF
			V_{CC} = 2.3V to 2.7V	+25℃		14		
			V_{CC} = 3.0V to 3.6V	+25℃		15		

NOTES:

1. Specified by design and characterization, not production tested.

2. t_{PD} is the same as t_{PLH} and t_{PHL}.

3. It refers to the skew between any two outputs of the same package that switch in the same direction. The parameter is guaranteed by design.

4. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

where:

f_i = Input frequency in MHz.

f_o = Output frequency in MHz.

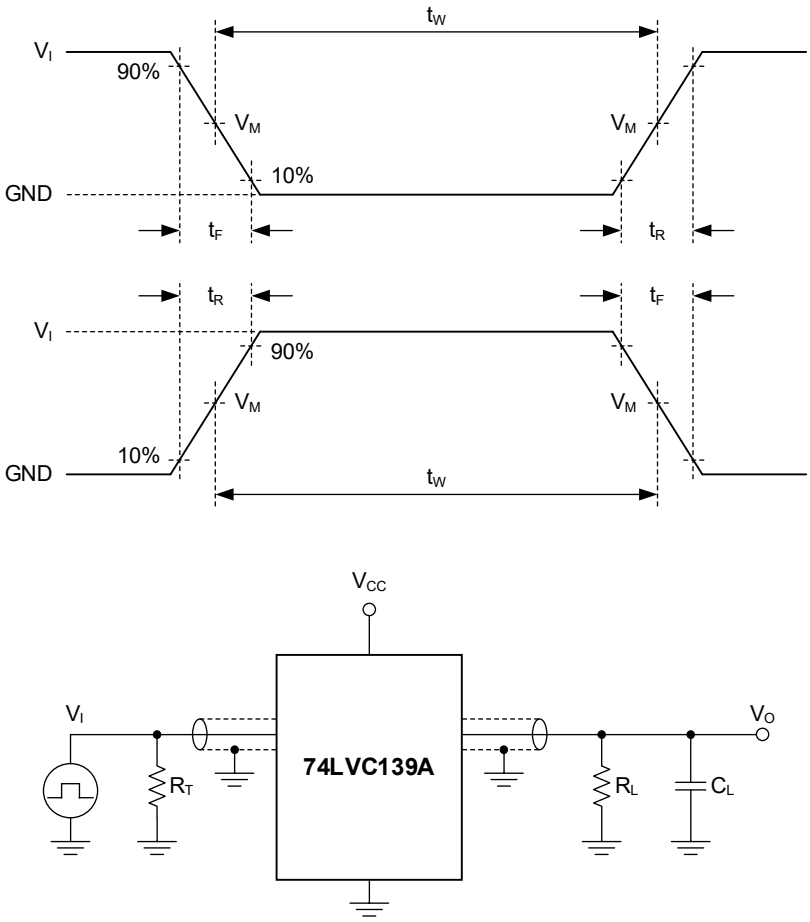
C_L = Output load capacitance in pF.

V_{CC} = Supply voltage in Volts.

N = Number of inputs switching.

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

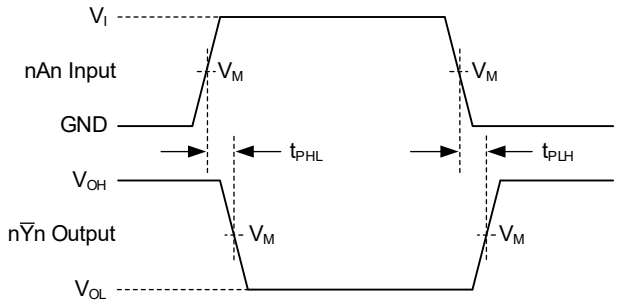
R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

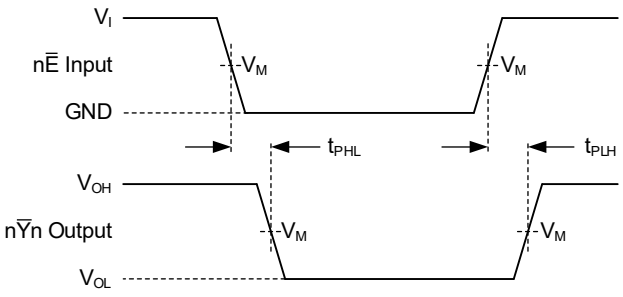
SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_R, t_F	C_L	R_L
1.2V	V_{CC}	≤ 2.0ns	30pF	1kΩ
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω
2.7V	2.7V	≤ 2.5ns	50pF	500Ω
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Address Input (nAn) to Output (nȲn) Propagation Delay Times



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable Input (nĒ) to Output (nȲn) Propagation Delay Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
1.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
1.65V to 1.95V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.3V to 2.7V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.7V	2.7V	1.5V	1.5V
3.0V to 3.6V	2.7V	1.5V	1.5V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

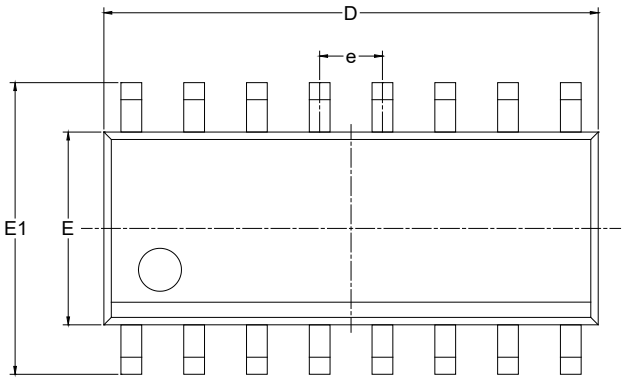
REVISION HISTORY

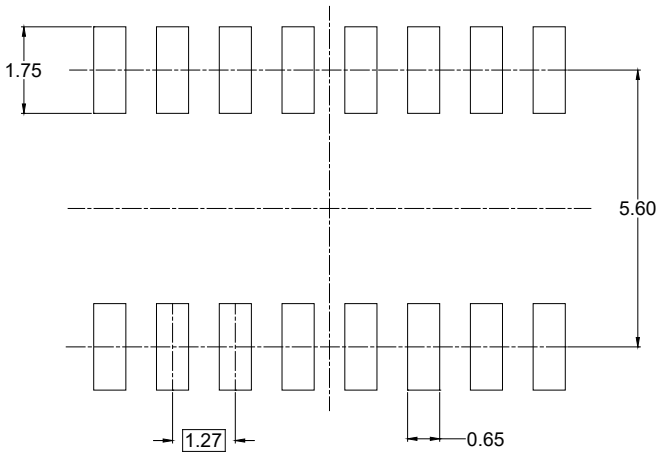
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (JULY 2025)	Page
Changed from product preview to production data	All

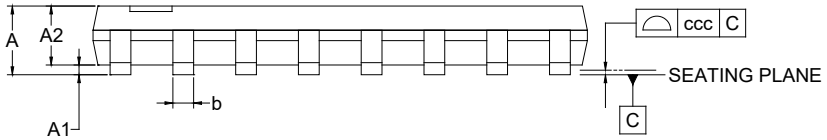
PACKAGE OUTLINE DIMENSIONS

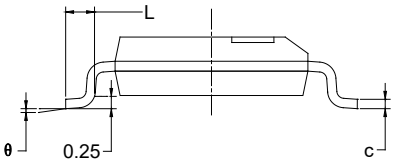
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



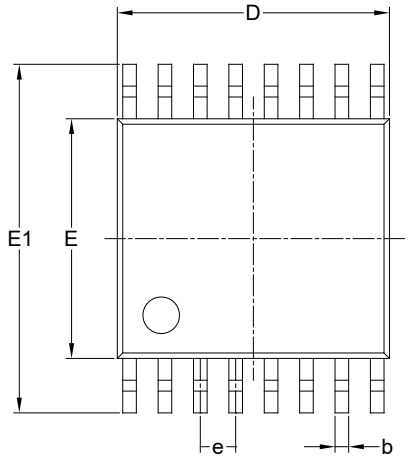


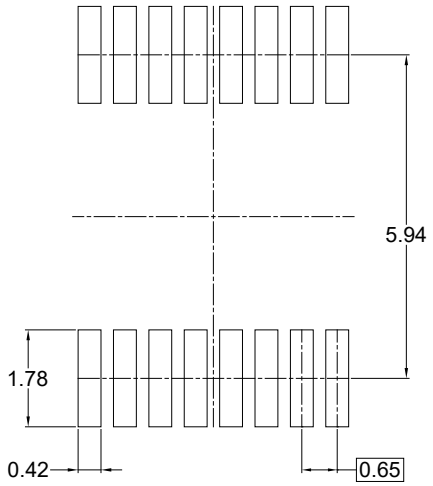
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

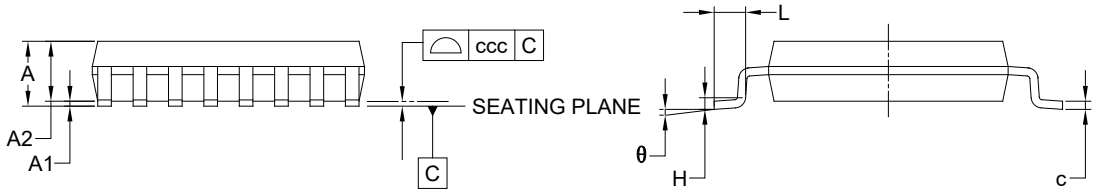
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

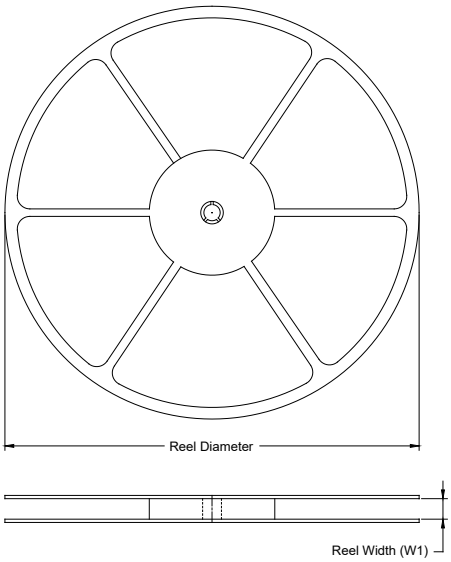


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

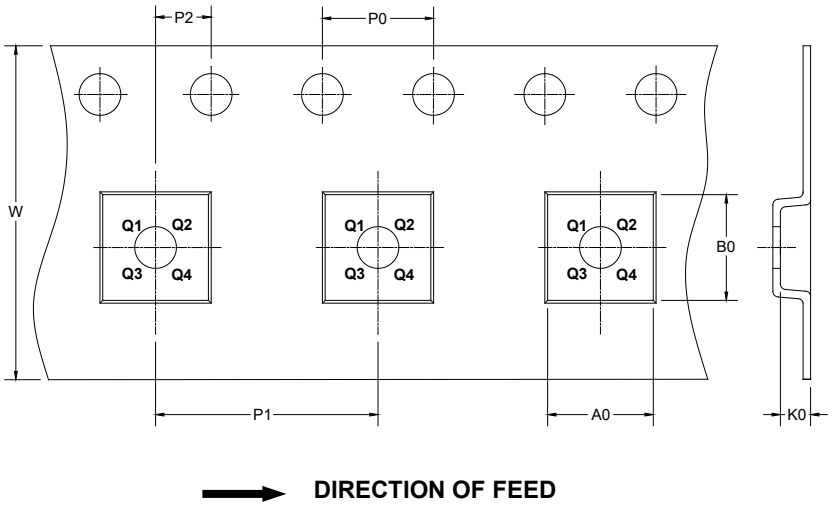
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



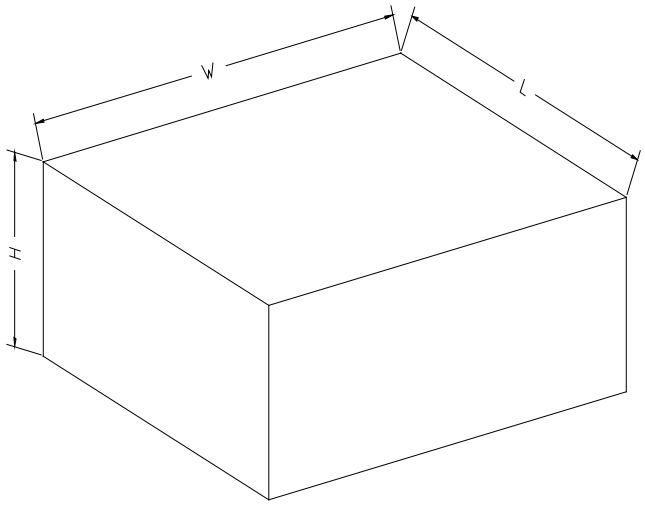
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002