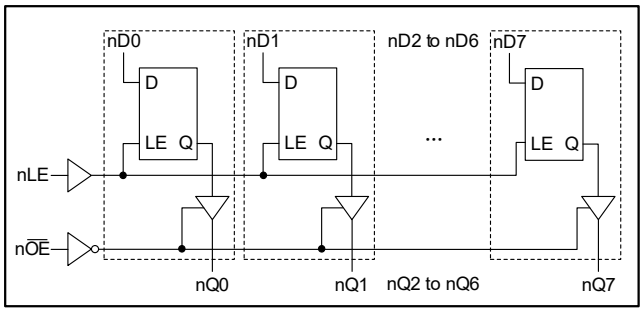
74LVCN16373
16-Bit D-Type Transparent Latch with 3-State Outputs

GENERAL DESCRIPTION

The 74LVCN16373 is a 16-bit D-type transparent latch with 3-state outputs that is designed for 1.2V to 3.6V V_{CC} operation. It features separate D-type inputs for each latch and 3-state outputs for bus-oriented applications. Each 8-bit latch is equipped with a latch enable (nLE) input and an output enable ($n\overline{OE}$) input. Both 3.3V and 5V devices can drive inputs. When the device is disabled, the outputs can accept voltages up to 5.5V, allowing this device to operate in a mixed 3.3V and 5V system environment.

The device includes two 8-bit D-type transparent latches with 3-state outputs. When nLE is high, data at the nDn inputs goes into the latches. In this case, the latches are transparent, that is to say, the latch outputs vary with corresponding D-type inputs each time. When $n\overline{OE}$ is low, data of eight latches can be used at the nQn outputs. When $n\overline{OE}$ is high, the outputs are in high-impedance state. $n\overline{OE}$ input has no influence on the state of the latches.

LOGIC DIAGRAM



FEATURES

- **Supply Voltage Range: 1.2V to 3.6V**
- **Input and Output Interface Capability to 5V System Environment**
- **+24mA/-24mA Output Current**
- **Direct Interface with TTL Levels**
- **Outputs in High-Impedance State when V_{CC} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-48 Package**

FUNCTION TABLE

CONTROL INPUT			INTERNAL LATCHES	OUTPUT
$n\overline{OE}$	nLE	nDn		nQn
L	H	L	L	L
L	H	H	H	H
L	L	l	L	L
L	L	h	H	H
H	L	l	L	Z
H	L	h	H	Z

H = High Voltage Level

h = High Voltage Level One Setup Time before the High-to-Low Transition of nLE

L = Low Voltage Level

l = Low Voltage Level One Setup Time before the High-to-Low Transition of nLE

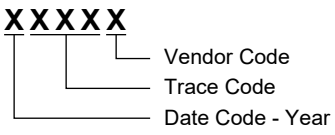
Z = High-Impedance State

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVCN16373	TSSOP-48	-40℃ to +125℃	74LVCN16373XTS48G/TR	74LVCN16373 XTS48 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 6.5V
Input Voltage Range, V_I (2) ..... -0.5V to 6.5V
Output Voltage Range, V_O (2)
High-State or Low-State..... -0.5V to MIN(6.5V, V_{CC} + 0.5V)
High-Impedance State ..... -0.5V to 6.5V
Input Clamping Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)... ±50mA
Continuous Output Current, I_O ..... ±50mA
Continuous Current through V_{CC} or GND..... ±100mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....7000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Function Supply Voltage Range, V_{CC}.....1.2V to 3.6V
Operating Supply Voltage Range, V_{CC}.....1.65V to 3.6V
Input Voltage Range, V_I .....0V to 5.5V
Output Voltage Range, V_O
High-State or Low-State..... 0V to V_{CC}
High-Impedance State .....0V to 5.5V
Output Current, I_O ..... ±24mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.2V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 3.6V ..... 10ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

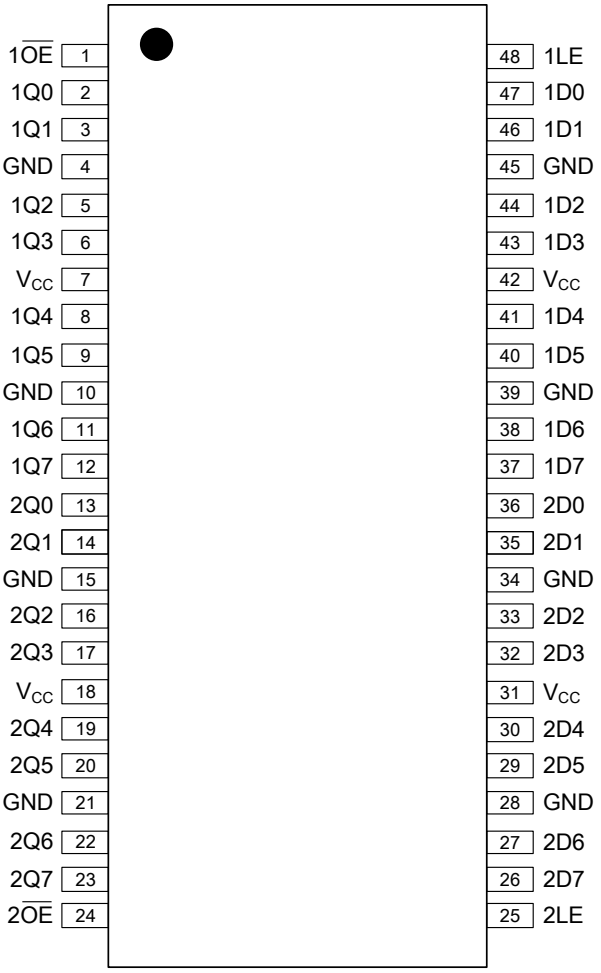
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-48

PIN DESCRIPTION

PIN	NAME	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37	1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	Data Inputs.
36, 35, 33, 32, 30, 29, 27, 26	2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	Data Inputs.
1, 24	1$\overline{OE}$, 2$\overline{OE}$	Output Enable Inputs (Active-Low).
48, 25	1LE, 2LE	Latch Enable Inputs (Active-High).
2, 3, 5, 6, 8, 9, 11, 12	1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	Data Outputs.
13, 14, 16, 17, 19, 20, 22, 23	2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	Data Outputs.
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground.
7, 18, 31, 42	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V	Full	1.08			V
		V_{CC} = 1.65V to 1.95V	Full	0.65 × V_{CC}			
		V_{CC} = 2.3V to 2.7V	Full	1.7			
		V_{CC} = 2.7V to 3.6V	Full	2.0			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V	Full			0.12	V
		V_{CC} = 1.65V to 1.95V	Full			0.35 × V_{CC}	
		V_{CC} = 2.3V to 2.7V	Full			0.7	
		V_{CC} = 2.7V to 3.6V	Full			0.8	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 3.6V, I_O = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.003		V
		V_{CC} = 1.65V, I_O = -4mA	Full	1.43	1.54		
		V_{CC} = 2.3V, I_O = -8mA	Full	2.03	2.18		
		V_{CC} = 2.7V, I_O = -12mA	Full	2.36	2.55		
		V_{CC} = 3.0V, I_O = -18mA	Full	2.53	2.80		
		V_{CC} = 3.0V, I_O = -24mA	Full	2.35	2.73		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65V to 3.6V, I_O = 100μA	Full		0.002	0.05	V
		V_{CC} = 1.65V, I_O = 4mA	Full		0.07	0.20	
		V_{CC} = 2.3V, I_O = 8mA	Full		0.11	0.28	
		V_{CC} = 2.7V, I_O = 12mA	Full		0.16	0.35	
		V_{CC} = 3.0V, I_O = 24mA	Full		0.30	0.55	
Input Leakage Current	I_I	V_{CC} = 3.6V, V_I = 5.5V or GND	Full		±0.01	±2	μA
Off-State Output Current	I_{OZ}	V_{CC} = 3.6V, V_I = V_{IH} or V_{IL}, V_O = 5.5V or GND	Full		±0.01	±2	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 5.5V	Full		0.01	5	μA
Supply Current	I_{CC}	V_{CC} = 3.6V, V_I = V_{CC} or GND, I_O = 0A	Full		1.3	20	μA
Additional Supply Current (1)	ΔI_{CC}	Per input pin, V_{CC} = 2.7V to 3.6V, V_I = V_{CC} - 0.6V, I_O = 0A,	Full		0.1	80	μA
Input Capacitance	C_I		+25℃		6		pF

NOTE:

1. It is the increase in supply current for per input at the specified voltage level except V_{CC} or GND.

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	nDn to nQn, see Figure 2	V_{CC} = 1.2V	+25℃		28.4		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	6.8	14.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.7	7.0	
			V_{CC} = 2.7V	Full	0.5	4.4	6.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.2	6.0	
		nLE to nQn, see Figure 3	V_{CC} = 1.2V	+25℃		27.2		
			V_{CC} = 1.65V to 1.95V	Full	0.5	8.8	15.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	5.2	8.5	
			V_{CC} = 2.7V	Full	0.5	4.8	7.5	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.4	7.0	
Enable Time (2)	t_{EN}	$n\overline{OE}$ to nYn, see Figure 4	V_{CC} = 1.2V	+25℃		15.6		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	8.0	14.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.4	7.0	
			V_{CC} = 2.7V	Full	0.5	3.2	7.0	
			V_{CC} = 3.0V to 3.6V	Full	0.5	2.8	6.5	
Disable Time (2)	t_{DIS}	$n\overline{OE}$ to nYn, see Figure 4	V_{CC} = 1.2V	+25℃		12.0		ns
			V_{CC} = 1.65V to 1.95V	Full	0.5	6.8	12.0	
			V_{CC} = 2.3V to 2.7V	Full	0.5	4.4	7.0	
			V_{CC} = 2.7V	Full	0.5	4.0	7.0	
			V_{CC} = 3.0V to 3.6V	Full	0.5	4.0	6.5	
Pulse Width	t_W	nLE high, see Figure 3	V_{CC} = 1.65V to 1.95V	Full	3.3			ns
			V_{CC} = 2.3V to 2.7V	Full	3.3			
			V_{CC} = 2.7V	Full	3.3			
			V_{CC} = 3.0V to 3.6V	Full	3.3			
Setup Time	t_{SU}	nDn to nLE, see Figure 5	V_{CC} = 1.65V to 1.95V	Full	1.5			ns
			V_{CC} = 2.3V to 2.7V	Full	1.5			
			V_{CC} = 2.7V	Full	2.0			
			V_{CC} = 3.0V to 3.6V	Full	2.0			
Hold Time	t_H	nDn to nLE, see Figure 5	V_{CC} = 1.65V to 1.95V	Full	2.0			ns
			V_{CC} = 2.3V to 2.7V	Full	2.0			
			V_{CC} = 2.7V	Full	1.2			
			V_{CC} = 3.0V to 3.6V	Full	1.2			

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Power Dissipation Capacitance (3)	C_{PD}	Per input, V_I = GND to V_{CC}	V_{CC} = 1.65V to 1.95V	+25℃		12		pF
			V_{CC} = 2.3V to 2.7V	+25℃		13		
			V_{CC} = 3.0V to 3.6V	+25℃		14		

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

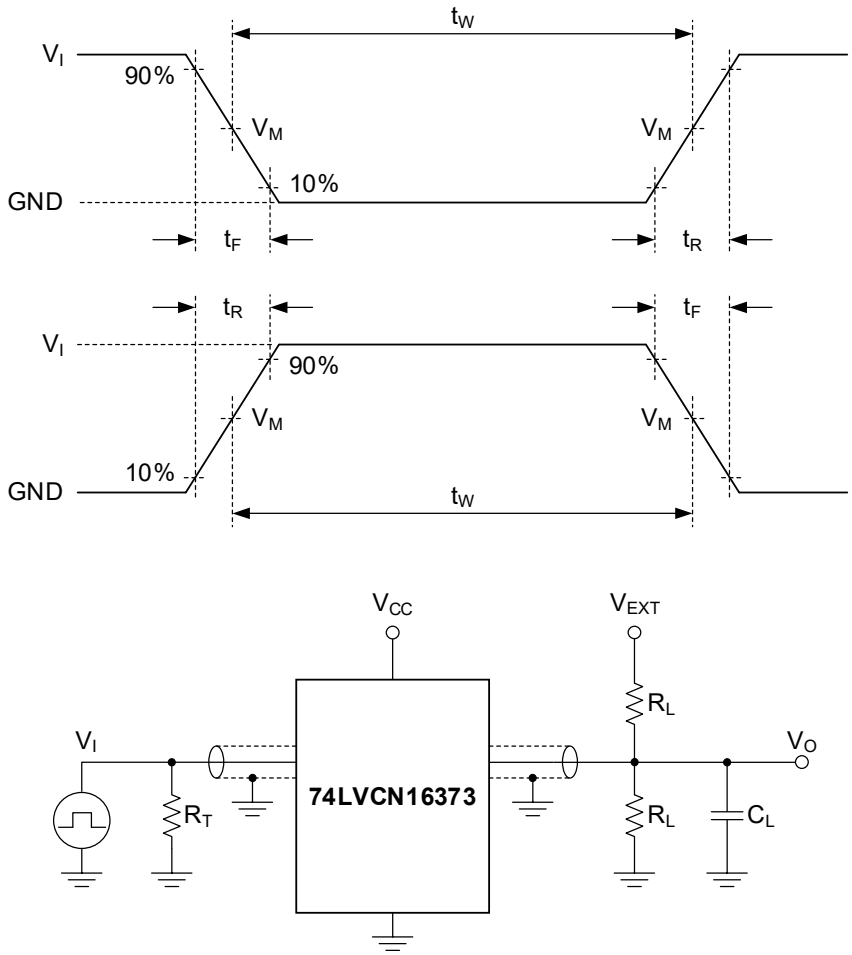
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

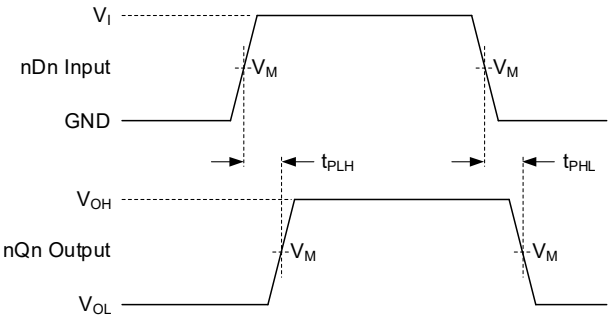
V_{EXT}: External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

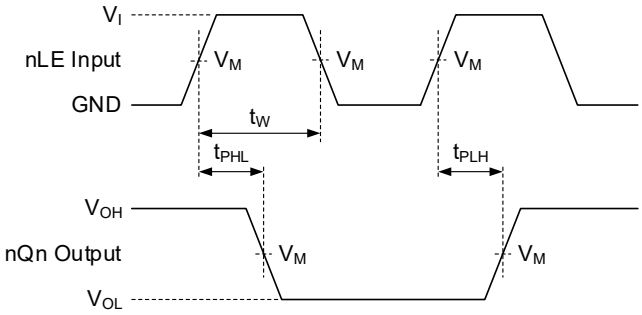
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open	2 × V_{CC}	GND
1.65V to 1.95V	V_{CC}	≤ 2.0ns	30pF	1kΩ	Open	2 × V_{CC}	GND
2.3V to 2.7V	V_{CC}	≤ 2.0ns	30pF	500Ω	Open	2 × V_{CC}	GND
2.7V	2.7V	≤ 2.5ns	50pF	500Ω	Open	2 × V_{CC}	GND
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω	Open	2 × V_{CC}	GND

WAVEFORMS



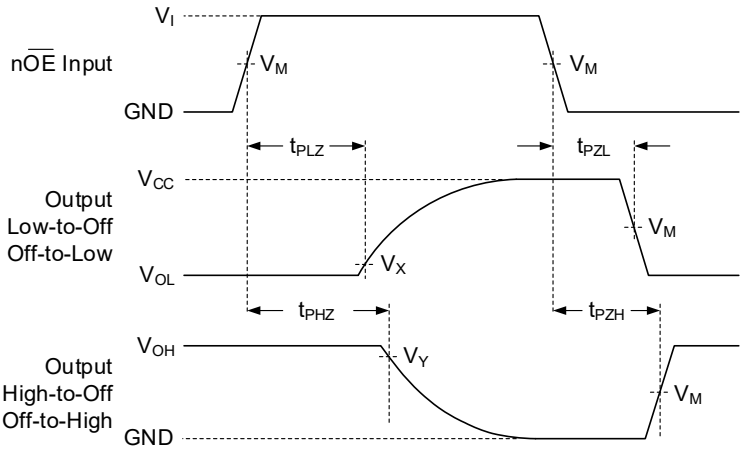
Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input nDn to Output nQn Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

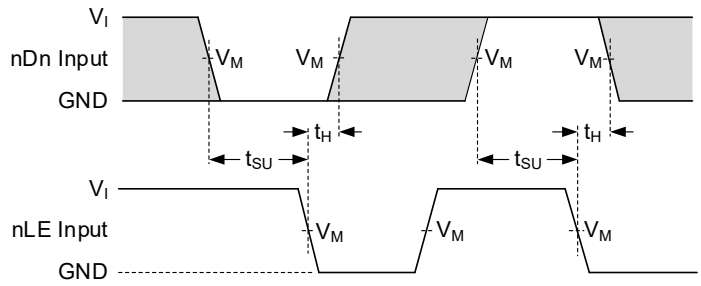
Figure 3. The Latch Enable Input to Output Propagation Delays and Pulse Width



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and Disable Times

WAVEFORMS (continued)



Test conditions are given in Table 1.

Measurement points are given in Table 2.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Data Setup and Hold Times for nDn Input to nLE Input

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
1.2V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
1.65V to 1.95V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
2.3V to 2.7V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15V	V_{OH} - 0.15V
2.7V	2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V
3.0V to 3.6V	2.7V	1.5V	1.5V	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

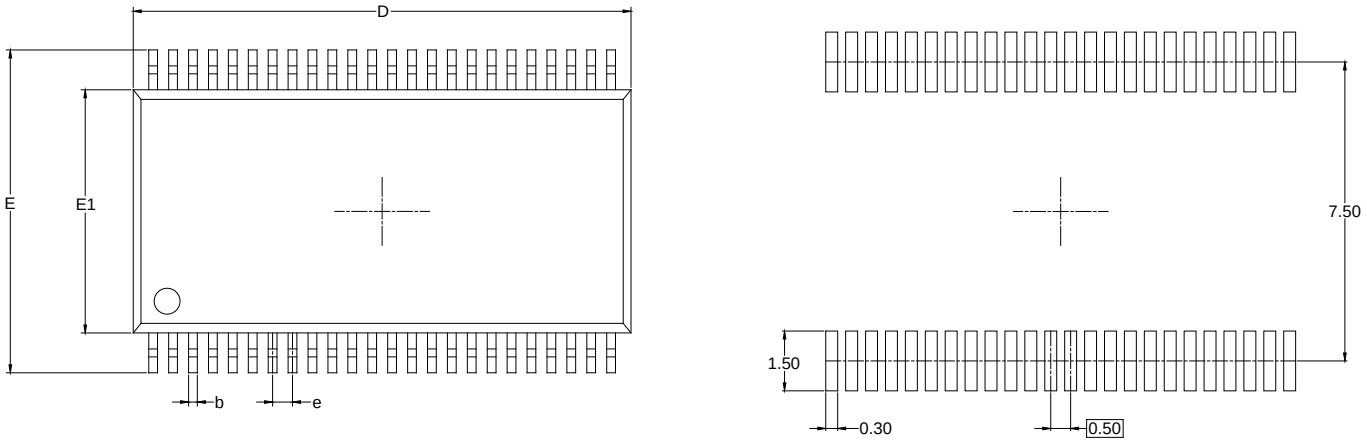
JANUARY 2024 – REV.A.1 to REV.A.2	**Page**
Updated Dynamic Characteristics section	5

NOVEMBER 2021 – REV.A to REV.A.1	**Page**
Updated HBM value in Absolute Maximum Ratings section	2

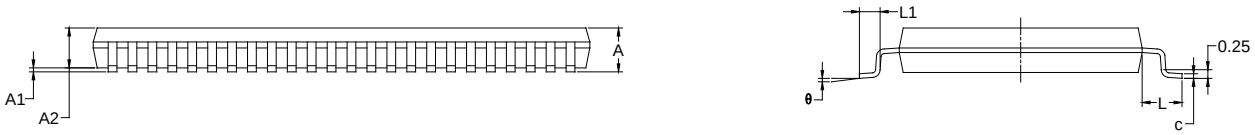
Changes from Original (MARCH 2021) to REV.A	**Page**
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TSSOP-48



RECOMMENDED LAND PATTERN (Unit: mm)

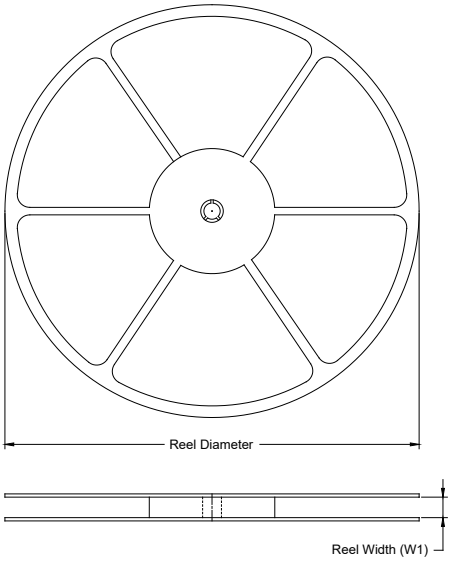


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
b	0.18		0.26
c	0.15		0.19
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50 BSC		
L	1.00 REF		
L1	0.45		0.75
θ	0°		8°

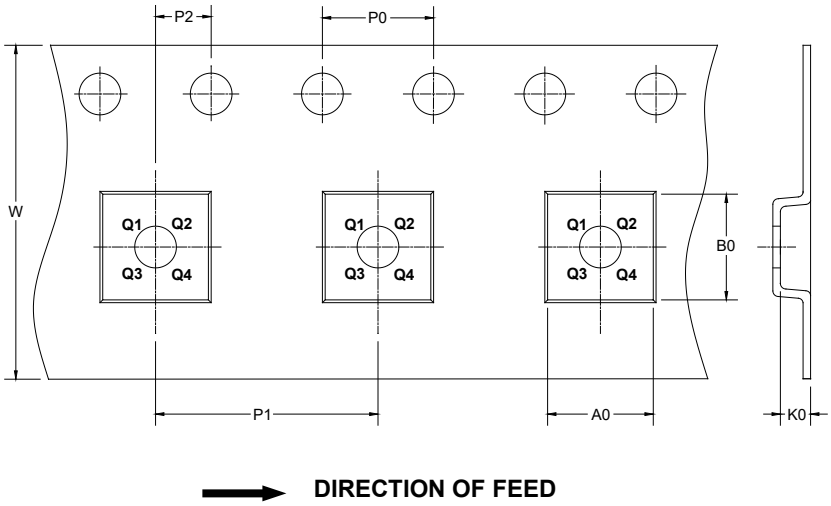
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

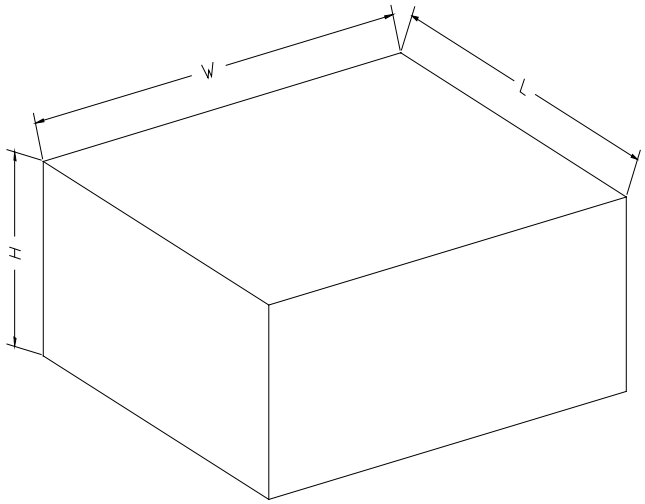
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-48	13”	24.4	8.60	13.00	1.80	4.0	12.0	2.0	24.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002