SGM25120
16V, 20A, 1.9mΩ R_{DSON}, Hot-Swap Intelli-Fuse Solution

GENERAL DESCRIPTION

The SGM25120 is a hot-plug protection device providing dual-directional protection: it safeguards its output circuit from input-induced transients while simultaneously shielding its input from harmful short circuits and transient events originating from the output side.

The device includes an IMON option that generates a voltage proportional to the power supply current through the power supply device, which is set by the resistance of IMON pin to ground. An integrated high-efficiency charge pump drives the gate of the power MOSFET, enabling ultra-low-loss power delivery through enhanced power device with an extremely low on-resistance of 1.9mΩ to turn on.

During start-up, the output slew rate control mechanism, implemented via an external capacitor on the SS pin effectively suppresses inrush current. A dynamic current limiting unit, based on FET detection topology and combined with a precision resistor from the ILIM pin to the ground, supports programmable load current thresholds.

Full protection features include damaged MOSFET detection, current limit, thermal shutdown, over-voltage protection, and under-voltage protection.

The SGM25120 is available in a Green TLGA-4×4-24AL package.

APPLICATIONS

Hot Swap
PC Cards
Disk Drives
Servers
Networking
Laptops

FEATURES

- **Input Voltage Range: 2.7V to 16V**
- **Output Current: 20A (MAX)**
- **Integrated Switch with 1.9mΩ R_{DSON}**
- **IMON Accuracy: ±1.5% at T_J = +25℃, I_{OUT} = 15A**
- **VIN/VOUT/Temperature Monitor**
- **Built-In MOSFET Driver**
- **3.3V LDO Output**
- **PG Detector and Indication**
- **PG De-Asserts Low when V_{IN} = 0V**
- **Fault Signal Output**
- **Integrated Current Sensing with Sense Output**
- **Programmable Over-Current Limit**
- **Programmable Short-Circuit Current Limit**
- **Pin Programmable Input Over-Voltage Protection Threshold (OV)**
- **Pin Programmable OCP Fault Regulation Time**
- **Adjustable Soft-Start (SS)**
- **Output Short-Circuit Protection (SCP)**
- **Over-Temperature Protection (OTP)**
- **Built-In Fuse Health Reporting**
- **Available in a Green TLGA-4×4-24AL Package**

TYPICAL APPLICATION

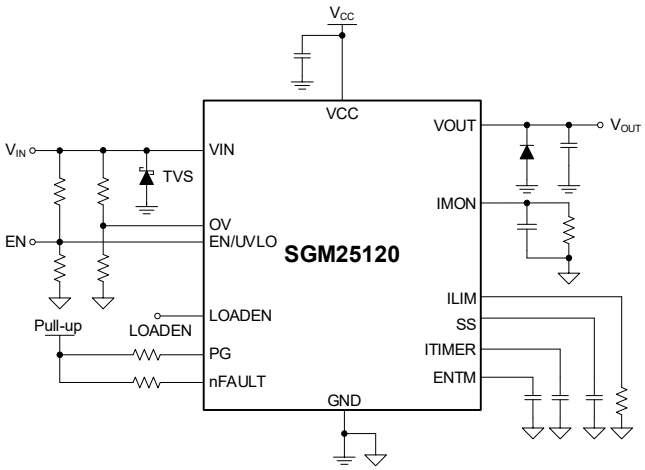


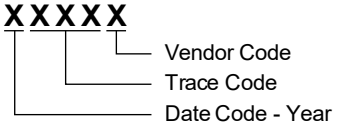
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25120	TLGA-4×4-24AL	-40℃ to +125℃	SGM25120XTLAN24G/TR	SGM25120 XTLAN24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- DC ..... -0.3V to 20V
- 1μs 24V

Output Voltage
- V_{OUT} ..... -0.3V to 20V
- V_{OUT} (200ns) ..... -1.5V

All Other Pins ..... -0.3V to 4.2V

Package Thermal Resistance
- TLGA-4×4-24AL, θ_{JA} ..... 30.2℃/W
- TLGA-4×4-24AL, θ_{JB} ..... 3.1℃/W
- TLGA-4×4-24AL, $\theta_{JC\ (TOP)}$ ..... 22.9℃/W
- TLGA-4×4-24AL, $\theta_{JC\ (BOT)}$ ..... 2.2℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.7V to 16V
Operating Junction Temperature ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

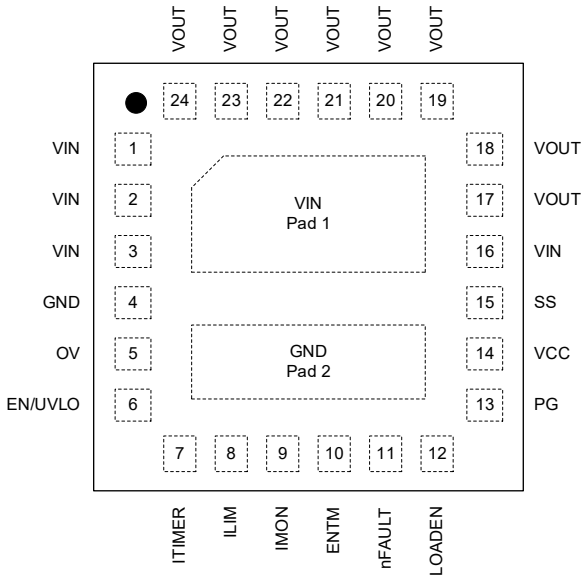
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TLGA-4×4-24AL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2, 3, 16, Pad 1	VIN	Input Power Supply for Main Power.
4, Pad 2	GND	Ground.
5	OV	Over-Voltage Enable Input. The over-voltage lockout threshold is programmed by the resistor divider from the VIN pin to the OV terminal to GND. Turn off the internal MOSFET by pulling OV high. If this function is not used, the OV pin must be connected to GND.
6	EN/UVLO	Enable Input or Under-Voltage Lockout. Asserting EN/UVLO pin high enables the device. As a UVLO pin, the UVLO threshold is configured using an external resistor divider. Do not leave this pin floating.
7	ITIMER	Timer Set. Fault timeout period and the hot plug insertion time delay are set by an external capacitor.
8	ILIM	Current Limit Set. Connect a resistor R_{ILIM} from this pin to GND to set the overload current limit threshold. The over-current limit is determined by the current through the ILIM pin. The current through the power FET is sensed proportionally and compared to ILIM. The fault timer is activated until it times out and the power FET is disabled when the sensed current reaches the over-current limit.
9	IMON	Output Current Monitor. This pin delivers a voltage proportional to power supply output current. The gain of the IMON output voltage is configured by grounding the resistor (R_{IMON}). When in used, a capacitor exceeding 10nF must be connected in parallel with R_{IMON} to ensure stability.
10	ENTM	LOADEN Blanking Time Set. The blanking time of LOADEN can be set by connecting an external capacitor. As soon as EN is activated, the timer is started and LOADEN is disabled. When EN is low or a fault occurs, the switch will trip. However, LOADEN low does not operate during the blanking time.
11	nFAULT	Fault Event Indicator. Active-low open-drain output. It is asserted during over-current, over-voltage, over-temperature, FET health or short-circuit fault condition. Pull nFAULT pin up to an external power supply through a 10kΩ to 100kΩ resistor.
12	LOADEN	Load Enable Input. When driven to a logic-high state, LOADEN is used to turn off the power switch, however, recycling the switch cannot be accomplished by simply turning on LOADEN only.
13	PG	Power Good. Open-drain output. PG pin is pulled up to the external power supply via a 10kΩ to 100kΩ resistor. A high PG level indicates a power good condition.
14	VCC	LDO Regulator. The internal 3.3 V LDO regulator provides the output voltage. A 1μF decoupling capacitor must be placed adjacent to the VCC and GND pins to ensure stable power delivery.
15	SS	Soft-Start. An external capacitor on the SS pin configures the output voltage soft-start timing. At start-up, the internal circuitry regulates the output voltage's slew rate. Leaving SS floating forces the soft-start interval to its shortest possible duration (1ms).
17 - 24	VOUT	Output Voltage which is Controlled by IC. A Schottky diode must be connected between VOUT and GND to ensure suppression of reverse voltage spikes during operation.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = V_{LOADEN} = 2V, V_{OV} = 0V, R_{ILIM} = 12kΩ, ITIMER = IMON = ENTM = nFAULT = open. Typical values are at T_J = +25℃ and V_{IN} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current							
Quiescent Current	I_Q	Intelli-Fuse on, no load			0.5	0.75	mA
		Fault latch off			0.3	0.56	
		Intelli-Fuse off with $V_{EN/UVLO}$ = 0V	V_{IN} = 12V		0.18	0.36	
			V_{IN} = 16V		0.20	0.41	
VCC							
VCC Regulator Output Voltage	V_{CC}	I_{VDD33} = 0mA		3.25	3.40	3.55	V
		I_{VDD33} = 10mA			3.37		
		I_{VDD33} = 20mA			3.36		
VCC Under-Voltage Lockout Threshold	V_{CCTH_R}	Rising		2.25	2.42	2.59	V
	V_{CCTH_F}	Falling		2.10	2.27	2.44	
VCC Under-Voltage Lockout Threshold Hysteresis	V_{CCHYS}				150		mV
VIN							
VIN Under-Voltage Lockout Threshold	V_{INTH_R}	Rising		2.35	2.53	2.69	V
	V_{INTH_F}	Falling		2.02	2.34	2.66	
VIN Under-Voltage Lockout Threshold Hysteresis	V_{INHYS}				190		mV
EN/UVLO							
EN/UVLO Input Threshold	V_{EN_R}	Rising		1.13	1.22	1.31	V
	V_{EN_F}	Falling		1.01	1.10	1.19	
EN/UVLO Hysteresis	V_{EN_HYS}				120		mV
EN/UVLO Blanking Time	t_{BLANK}	EN/UVLO recycling. High level trig mode			1.3		ms
OV							
OV Input Threshold	V_{OV_R}	Rising		1.13	1.22	1.31	V
	V_{OV_F}	Falling		1.06	1.14	1.22	V
Hysteresis	V_{OV_HYS}				80		mV
Power FET							
On-Resistance	R_{DSON}	T_J = +25℃, I_{OUT} = 2A	V_{IN} = 12V		1.9	2.5	mΩ
			V_{IN} = 2.7V		1.9	2.5	
		T_J = +125℃, I_{OUT} = 2A	V_{IN} = 12V		2.5	3.5	
			V_{IN} = 2.7V		2.5	3.5	
Off-State Leakage Current	I_{OFF}	V_{IN} = 16V, power FET off, T_J = +25℃				0.58	μA
		V_{IN} = 16V, power FET off				15	
ENTM							
ENTM Rising Threshold	V_{ENTM_R}			1.14	1.22	1.32	V
Charge Current	I_{ENTM}			0.50	1.0	1.55	μA
LOADEN							
LOADEN Low-Level Voltage	V_{LOADEN_L}					0.80	V
LOADEN High-Level Voltage	V_{LOADEN_H}			2.00			V
Thermal Shutdown							
Over-Temperature Threshold	T_{SD}				148		℃

ELECTRICAL CHARACTERISTICS (continued)

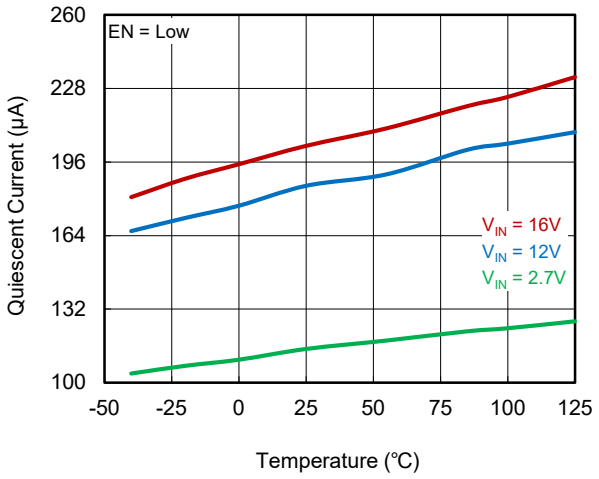
(T_J = -40℃ to +125℃, V_{IN} = 12V, $V_{EN/UVLO}$ = V_{LOADEN} = 2V, V_{OV} = 0V, R_{ILIM} = 12kΩ, ITIMER = IMON = ENTM = nFAULT = open. Typical values are at T_J = +25℃ and V_{IN} = 12V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IMON							
IMON Sense Gain	I_{MON}/I_{FET}	I_{OUT} = 15A	T_J = +25℃	19.70	20.0	20.30	μA/A
			T_J = -40℃ to +125℃	19.60	20.0	20.39	
		I_{OUT} > 4A	T_J = +25℃	19.40	20.0	21.28	
			T_J = -40℃ to +125℃	19.20	20.0	21.55	
IMON Sense Offset		I_{OUT} > 4A	T_J = +25℃	-0.65		0.65	μA
			T_J = -40℃ to +125℃	-0.9		0.9	
Current Limit							
ILIM Voltage	V_{ILIM}			0.57	0.6	0.63	V
OC Internal Current Sensing Gain		1/10 of IMON gain			2		μA/A
Current Limit at Normal Operation	I_{OC_NOR}	T_J = +25℃	R_{ILIM} = 12kΩ	-7%	25 (1)	7%	A
			R_{ILIM} = 20kΩ	-6%	15	6%	
		R_{ILIM} = 12kΩ		-16%	25 (1)	16%	
		R_{ILIM} = 20kΩ		-13.8%	15	14.2%	
Current Limit at Soft-Start	I_{OC_SS}	V_{OUT} < 90%V_{IN}	I_{OC_NOR} < 20A		I_{OC_NOR}		A
			I_{OC_NOR} ≥ 20A		20		
OC Regulation Time at Soft-Start	t_{OC_REG}				1.5		ms
Short-Circuit Current Limit	I_{SC}				50		A
Short-Circuit Protection Response Time (1)	t_{SC}				200		ns
ITIMER							
Upper Threshold Voltage	V_{ITIMER_H}			1.12	1.22	1.32	V
Insertion Delay Charge Current	I_{INSRT}			3.25	4.00	4.75	μA
OCP Fault Timeout Charge Current	I_{FLT_ITIMER}			28.8	39.70	50.7	μA
Discharge R_{DSON}	R_{ITIMER}				10		Ω
SS							
SS Pull-Up Current	I_{SS}	V_{IN} = 12V		9.25	13.50	16.94	μA
nFAULT							
Output Low Voltage	V_{OL}	I_{SINK} = 10mA				0.35	V
Off-State Leakage Current	$I_{nFAULTLKG}$	V_{FLT} = 3.3V				1	μA
PG							
PG Threshold Voltage	V_{PGTH_R}	Rising	V_{IN} = 12V	78%	87%	95%	V_{IN}
			V_{IN} = 2.7V		V_{IN} - 0.7		V
	V_{PGTH_F}	Falling	V_{IN} = 12V	72%	75%	79%	V_{IN}
			V_{IN} = 2.7V		V_{IN} - 0.7		V
Output Low Voltage	V_{OL}	I_{SINK} = 10mA				0.35	V
Off-State Leakage Current	I_{PGLKG}	V_{PG} = 3.3V				1	μA
FET Short Detection							
FET Drain-to-Source Short Entry Threshold	$V_{OUT\_DSTH\_ENT}$	V_{IN} = 12V		78%	87%	95%	V_{IN}
		V_{IN} = 2.7V			V_{IN} - 0.7		V
FET Drain-to-Source Short Recovery Threshold	$V_{OUT\_DSTH\_EXT}$	V_{IN} = 12V		72%	75%	79%	V_{IN}
		V_{IN} = 2.7V			V_{IN} - 0.7		V
Gate to Source Short Protection Delay Time (1)	t_{GS_ST}	V_{SS} > V_{CC} - 0.7			200		ms

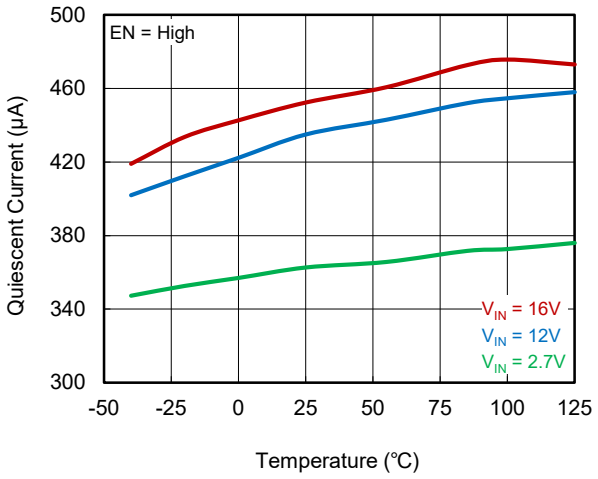
NOTE: 1. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

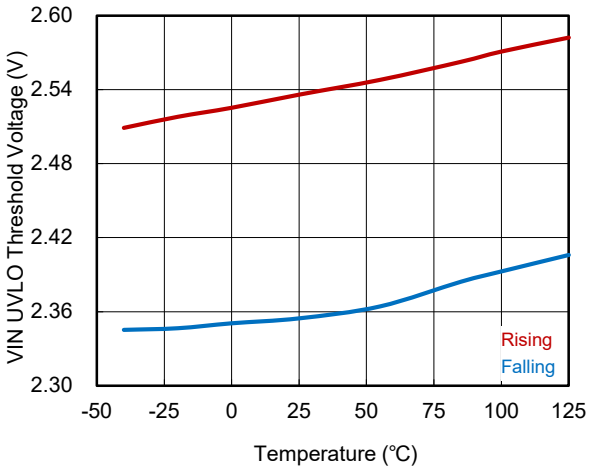
Quiescent Current vs. Temperature



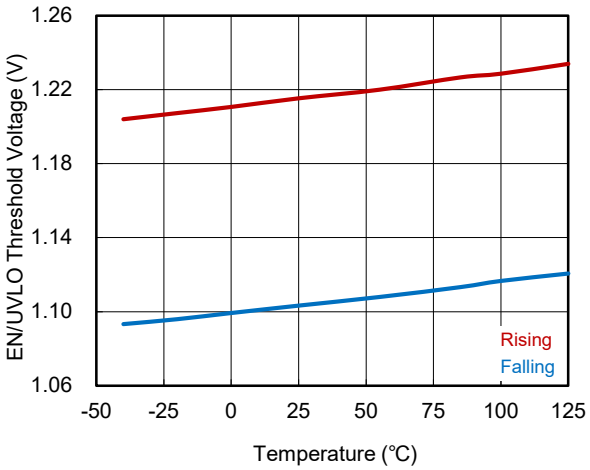
Quiescent Current vs. Temperature



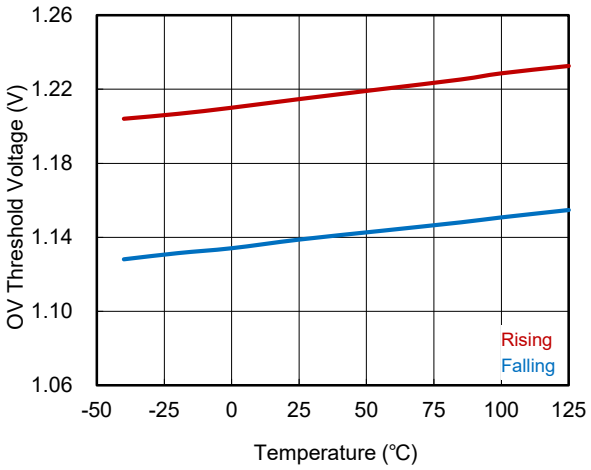
VIN UVLO Threshold vs. Temperature



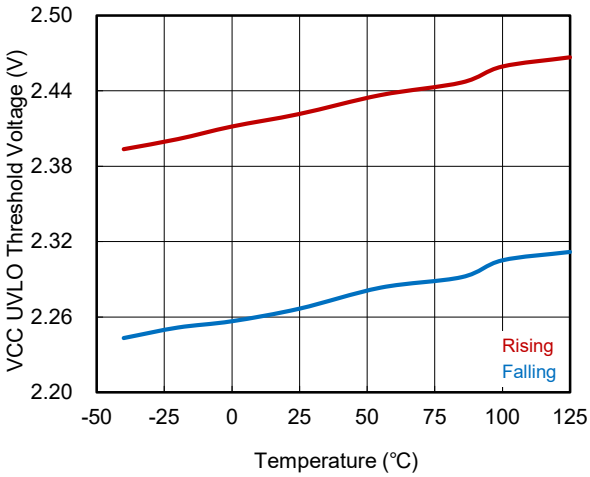
EN/UVLO Threshold vs. Temperature



OV Threshold vs. Temperature

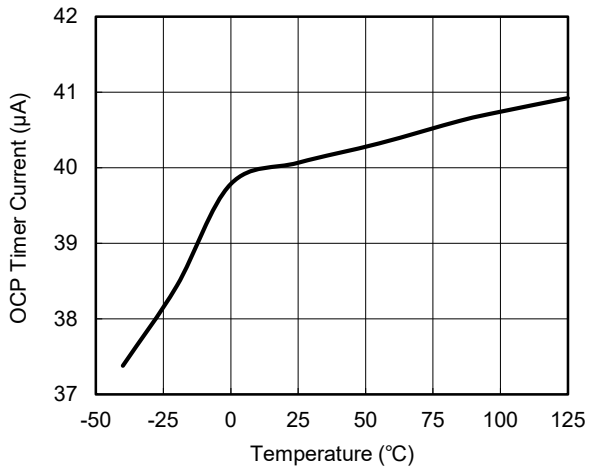


VCC UVLO Threshold vs. Temperature

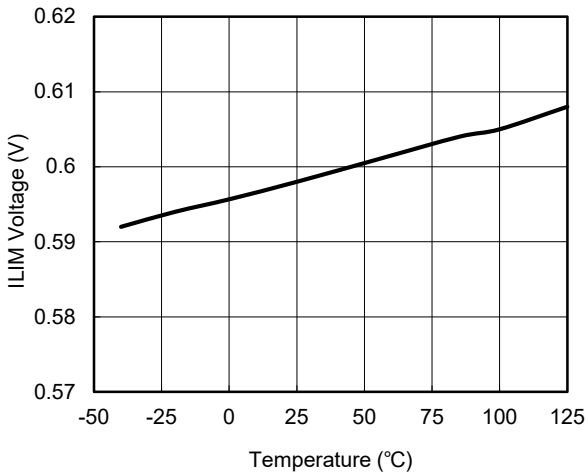


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

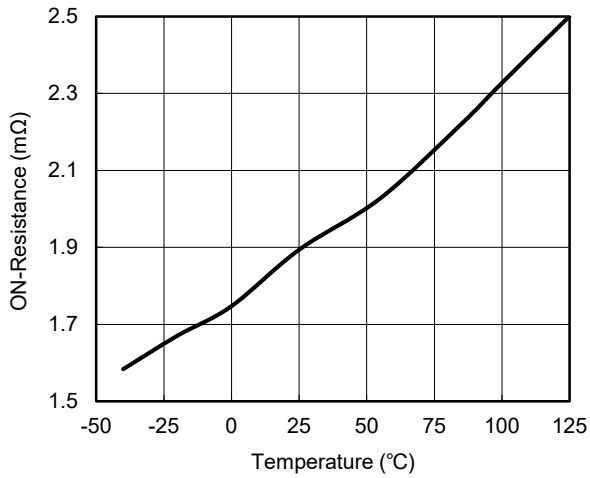
OCP Timer Current vs. Temperature



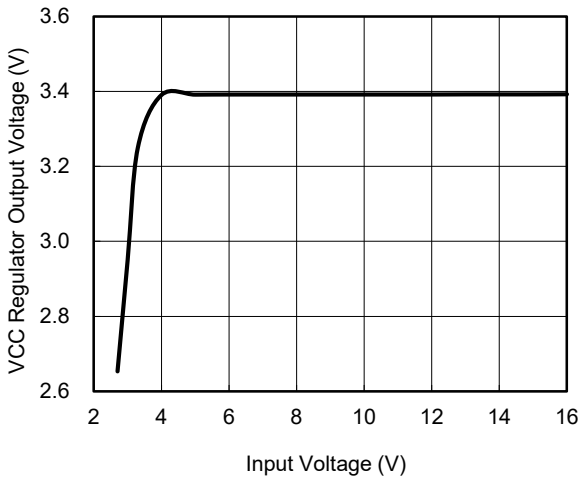
ILIM Voltage vs. Temperature



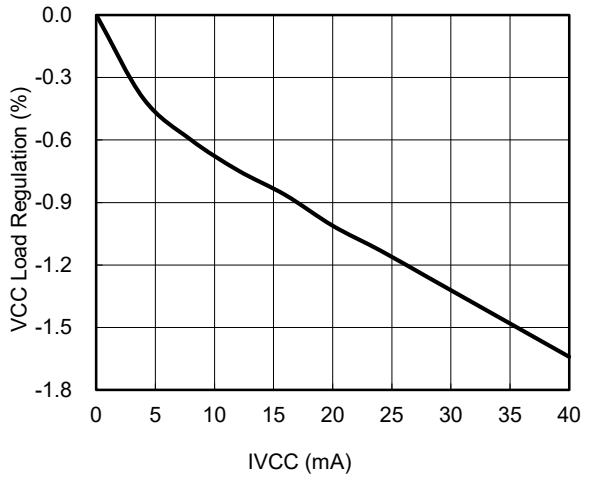
ON-Resistance vs. Temperature



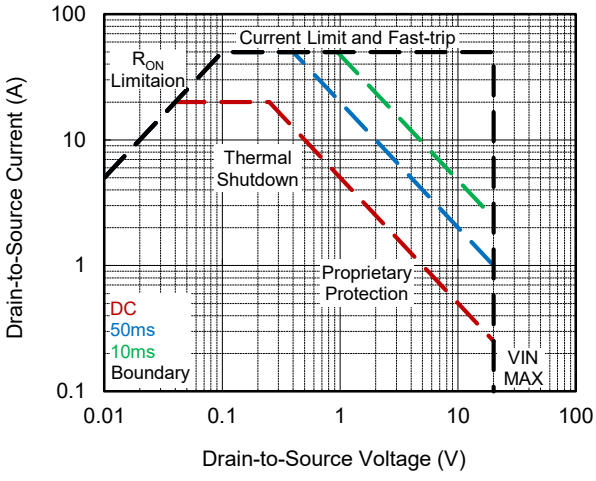
VCC Regulator Output Voltage vs. Input Voltage



VCC Load Regulation

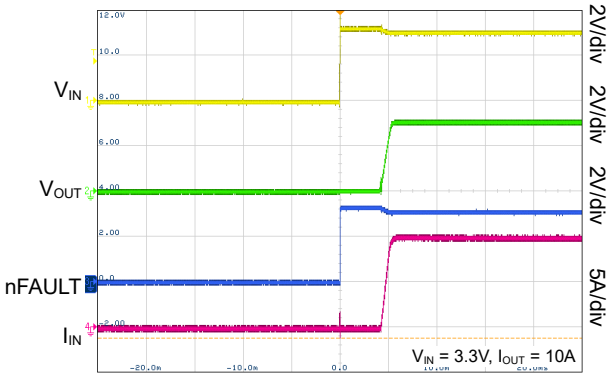


Allowed Operation Area (AOA)



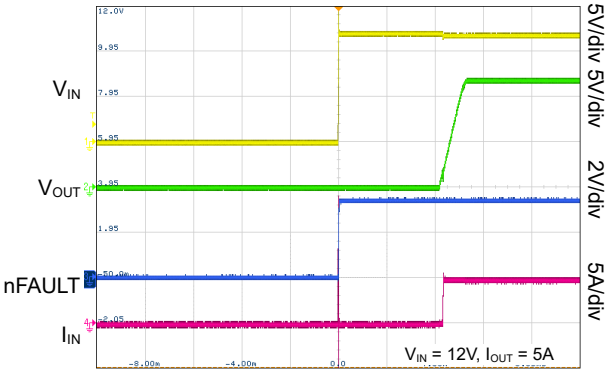
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VIN Hot Plug



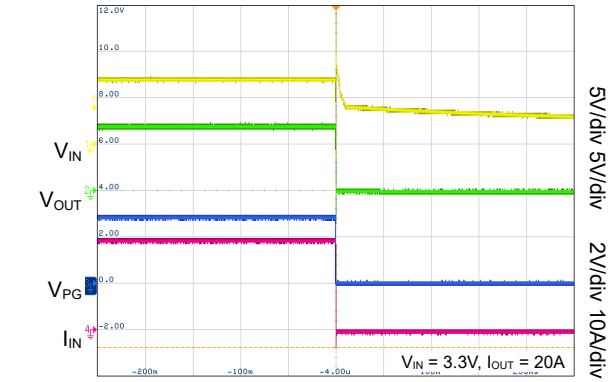
Time (5ms/div)

VIN Hot Plug



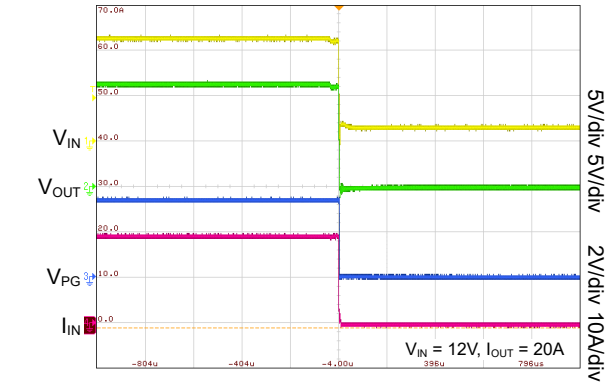
Time (2ms/div)

Shutdown through VIN



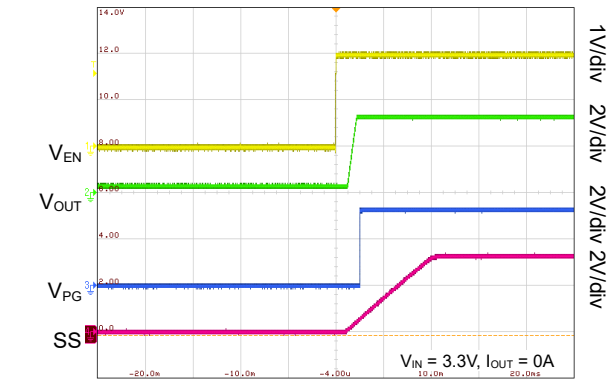
Time (50ms/div)

Shutdown through VIN



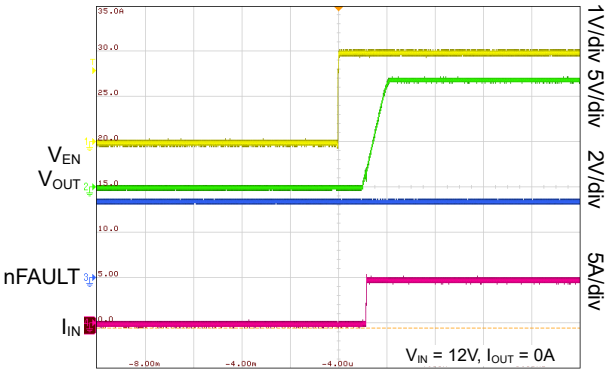
Time (200μs/div)

Start-up through EN



Time (5ms/div)

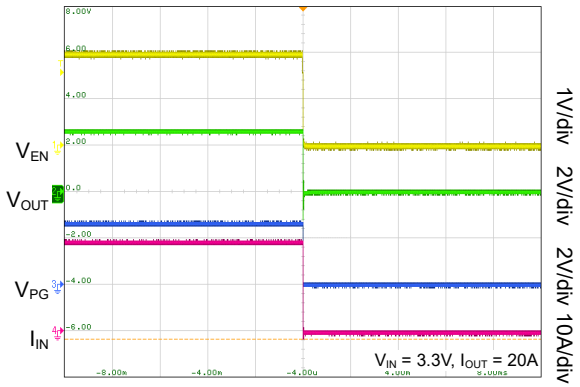
Start-up through EN



Time (2ms/div)

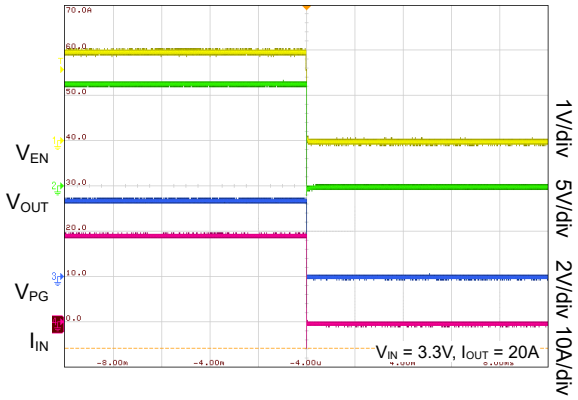
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Shutdown through EN



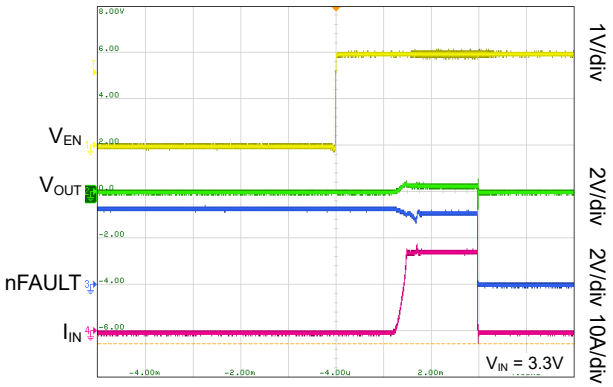
Time (2ms/div)

Shutdown through EN



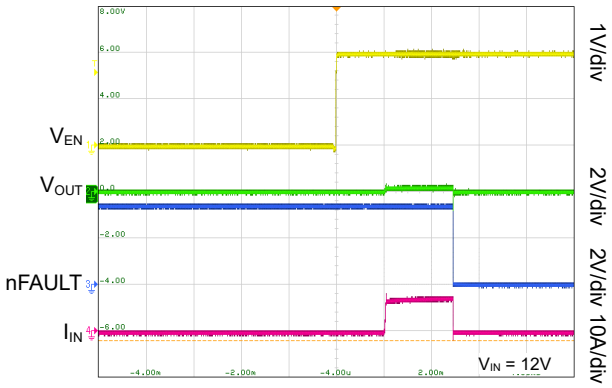
Time (2ms/div)

Short-Circuit Start-up



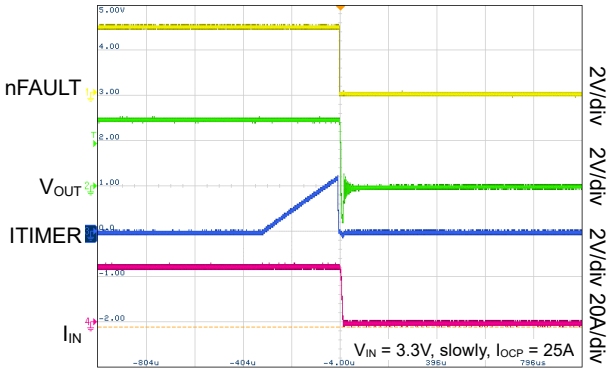
Time (1ms/div)

Short-Circuit Start-up



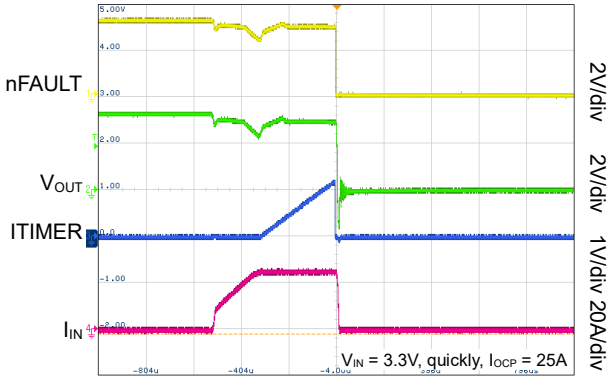
Time (1ms/div)

Over-Current Protection



Time (200μs/div)

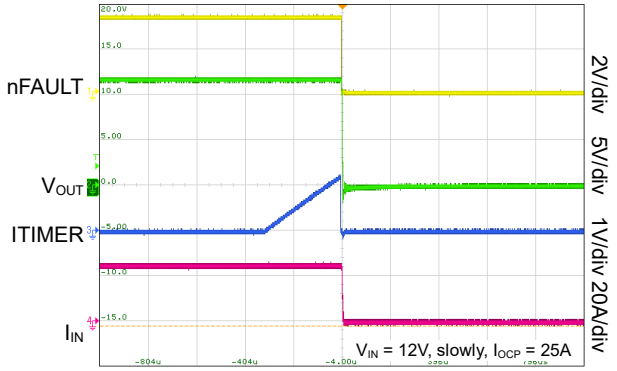
Over-Current Protection



Time (200μs/div)

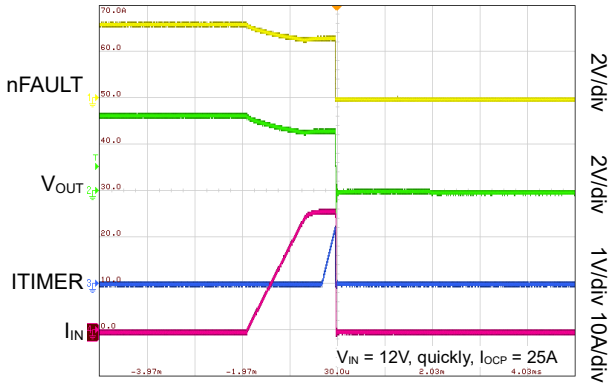
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Over-Current Protection



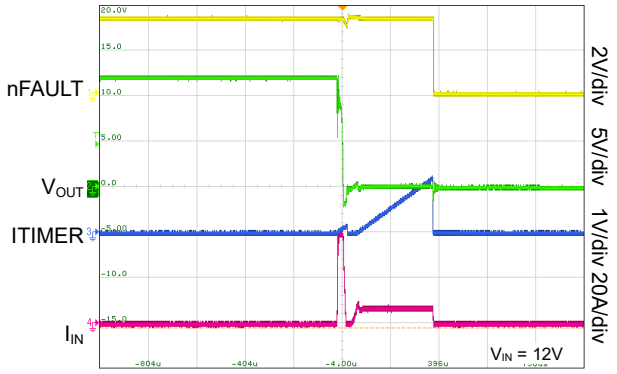
Time (200μs/div)

Over-Current Protection



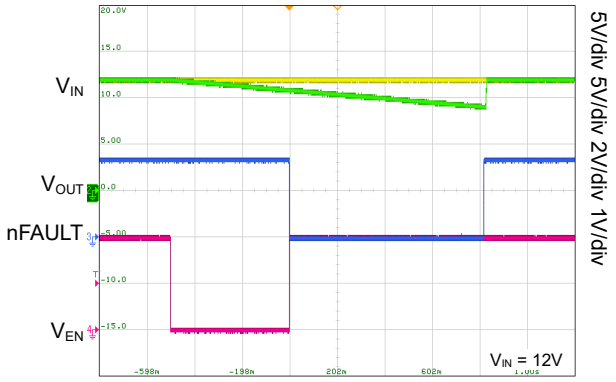
Time (1ms/div)

Short-Circuit Protection



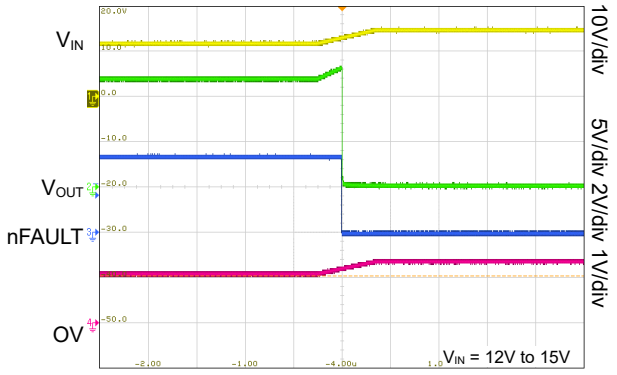
Time (200μs/div)

DS Short



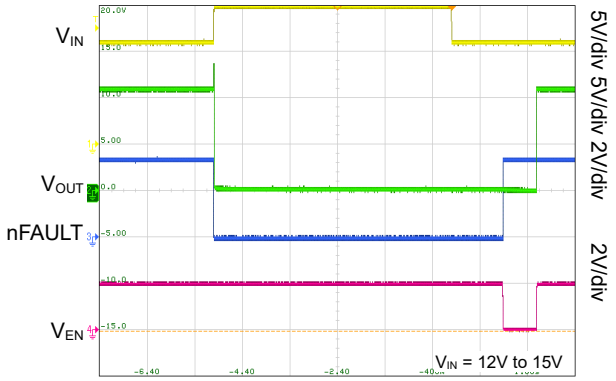
Time (200ms/div)

VIN OVP Shutdown



Time (500ms/div)

VIN OVP Shutdown



Time (1s/div)

FUNCTIONAL BLOCK DIAGRAM

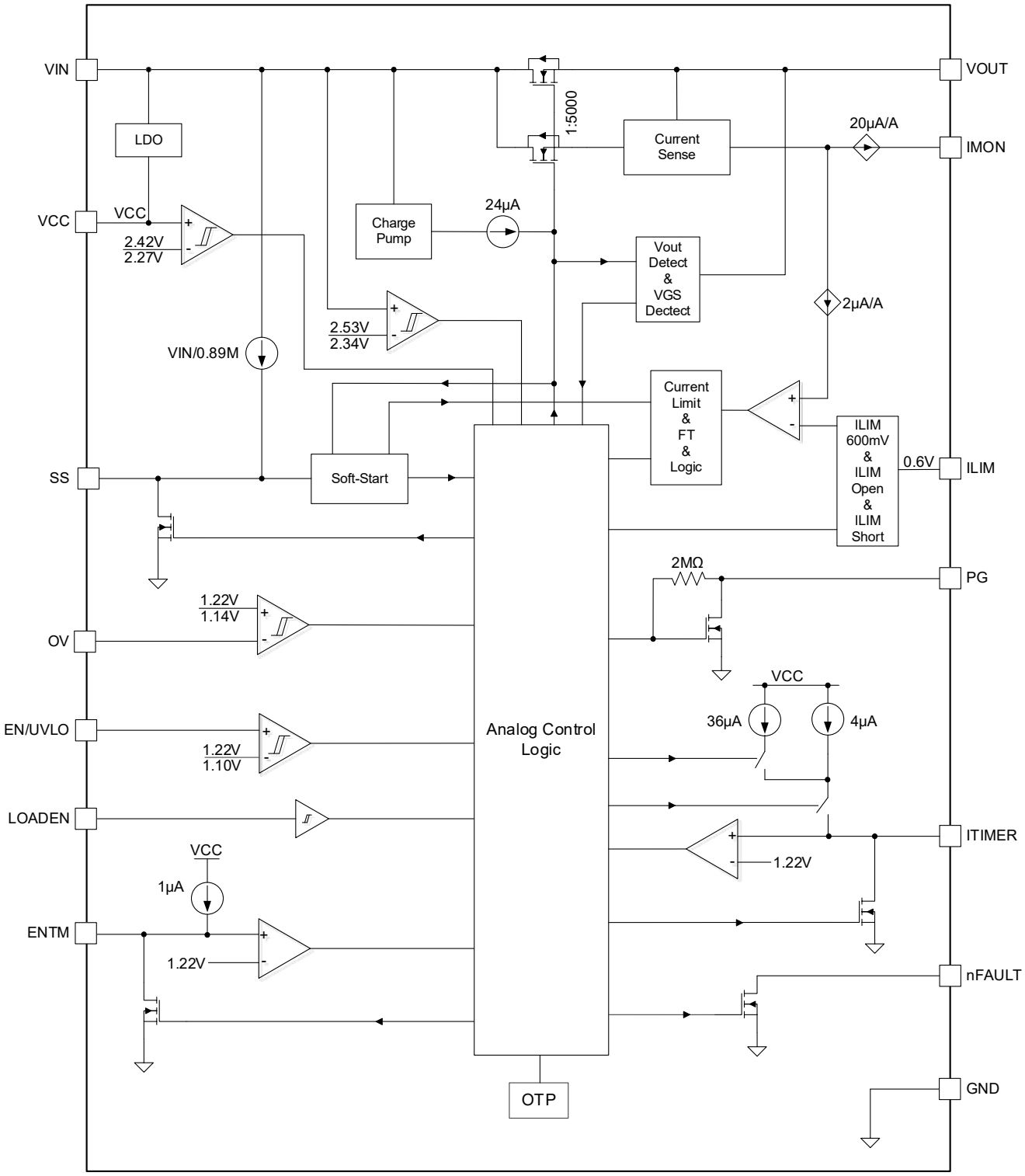


Figure 2. Block Diagram

OPERATION

The SGM25120 is a monolithic e-Fuse device with an integrated, 1.9mΩ R_{DSON} power N-MOSFET that is ideally suited for large current applications. The device supports up to 20A of continuous output current per device at room temperature and minimizes backplane voltage drop by regulating inrush current during hot-swap insertion of a circuit card into a live backplane power source.

During hot-swap operation and the device is enabled, the MOSFET gate charging process initiates only after a programmable insertion delay period. This delay is set by an external capacitor connected to the ITIMER pin, where the capacitance value determines the length of the delay. The output voltage then increases gradually as the SS (soft-start) voltage ramps up, with the slope of this ramp controlling the gate charging slew rate. After a successful start-up sequence, the device then actively monitors its load current, input voltage and protects the load from harmful over-current and over-voltage conditions. Additionally, it senses the junction temperature and shuts down the device once the temperature exceeds the safe operating conditions.

Current Limit

The SGM25120 uses an external resistor to set a constant current limit. When the monitored current reaches the programmed threshold, the internal regulator adjusts the gate voltage of the power MOSFET to maintain constant current flow.

The response time of the device is typically 200μs. Due to the response time, the output current may have a small overshoot.

While V_{OUT} < MAX (V_{IN} – 0.7V, 87% of V_{IN}). The SGM25120 is in start-up mode. During startup, the SGM25120 limits the maximum power on the power FET to 80W (TYP) to prevent over-power damage. The over-power protection lasts only 1.5ms and after 1.5ms the device will be latched off. Since high power dissipation in the MOS occurs at start-up, the junction temperature of the device increases rapidly. Once the sensed junction temperature reaches the over-temperature threshold, the IC shuts down and latches off.

During the start-up phase, the MOSFET's power dissipation remains below 80W, the soft-start current limit (I_{OC_SS}) follows the normal current limit (I_{OC_NOR}), which is determined by the external resistor-programmed current limiting value. According to the design, when I_{OC_NOR} ≥ 20A, the I_{OC_SS} is then clamped at 20A.

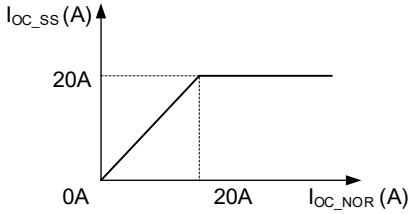


Figure 3. Start-up Current Limit to Normal Over-Current Limit

If the output voltage approaches V_{IN}, the V_{OUT} exceeds MAX (V_{IN} – 0.7V, 87% of V_{IN}), and the power FET gate voltage approaches the voltage of the internal charge pump, the device enters normal mode. When SGM25120 enters normal mode, current limiting of the device is programmed by an external resistor. The current limit can be set using Equation 1:

$$I_{LIMIT} = \frac{0.3V}{R_{ILIM}} \times 10^6 (A) \quad (1)$$

Where R_{ILIM} (Ω) is the resistor from ILIM to ground.

When an over-current event triggers, the SGM25120 initiates the fault timer. The device resumes normal operation if the output current drops below the ILIM threshold before the fault timeout period (t_{ITIMER}) expires. Conversely, if the over-current condition persists beyond $t_{ITIMER,}$ the power FET will be latched off. The duration of t_{ITIMER} can be calculate by following Equation 2:

$$t_{nFAULT} = \frac{1.22}{40} \times C_T \quad (2)$$

Where t_{FAULT} is the fault timer (ms), and C_T is the timer capacitor (nF). For instance, a 10nF capacitor corresponds to an insertion delay timer of 0.3ms.

Upon reaching the current limit threshold, the nFAULT signal is asserted low after a 4μs propagation delay to signal a fault condition.

Short-Circuit Protection (SCP)

During short-circuit events causing rapid load current rise, instantaneous current may exceed the set threshold. The power FET must disable before reaching the short-circuit threshold to prevent damage. This fast response minimizes voltage droop during faults. The short-circuit response requires about 200ns.

OPERATION (continued)

After V_{OS} falls to a low level, the SGM25120 initiates an immediate restart to prevent input voltage line transients. The gate of the FET is then charged by an internal charge pump. When V_{OUT} starts again, under persistent short-circuit conditions, the load current is regulated by the over-power protection and external current-limiting mechanisms.

The over-power protection has a higher priority than the normal current limiting value. When the current is less than twice the set current limit value, if the fault persists and the fault timer reaches 1.22V, the SGM25120 will subsequently turn off its power MOSFET (see Figure 4). When the current is greater than twice the set current limit value, if the fault continues, it will continue for 1.5ms (depends on the AOA of the device), the SGM25120 will subsequently turn off its power MOSFET.

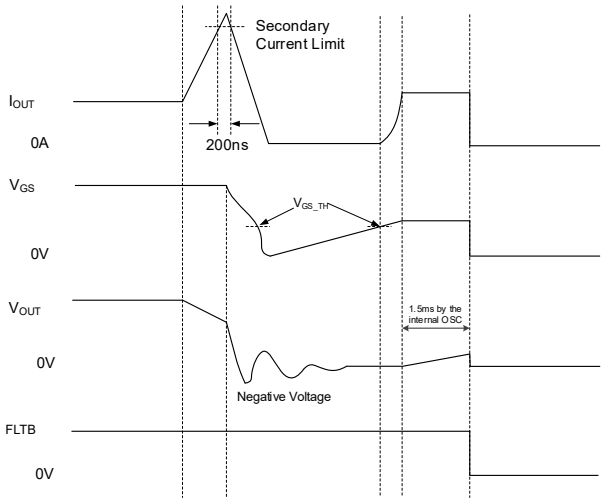


Figure 4. SCP Behavior

When a hard short arises causing the input voltage to descend below VCC abruptly, the power MOSFET's gate voltage is forcibly lowered instantaneously, independent of the secondary current limit's engagement status. Subsequently, the device initiates a secondary activation cycle while maintaining the persistent fault state.

The nFAULT asserts a low-state signal upon timer expiration if the sustained fault condition remains unresolved.

Power-Up Sequence

During hot-swap operations, inductive voltage transients may manifest at the SGM25120's supply terminal during connector mating events, primarily attributed to PCB trace inductance (L_trace) and the input capacitor's equivalent series inductance (ESL). To ensure stable rail conditions during power-up, a controlled timing sequence precedes main FET activation: the ITIMER initiates a 4μA current-limited charging path to C_T upon UVLO engagement. The timing cycle completes when the ITIMER reference potential achieves 1.22V, with C_T values derivable from Equation 3:

$$t_{DELAY} = \frac{1.22}{4} \times C_T \quad (3)$$

Where t_{DELAY} is the insertion delay time (ms), and C_T is the timer capacitor (nF). For instance, a 10nF capacitor corresponds to an insertion delay timer of 3ms.

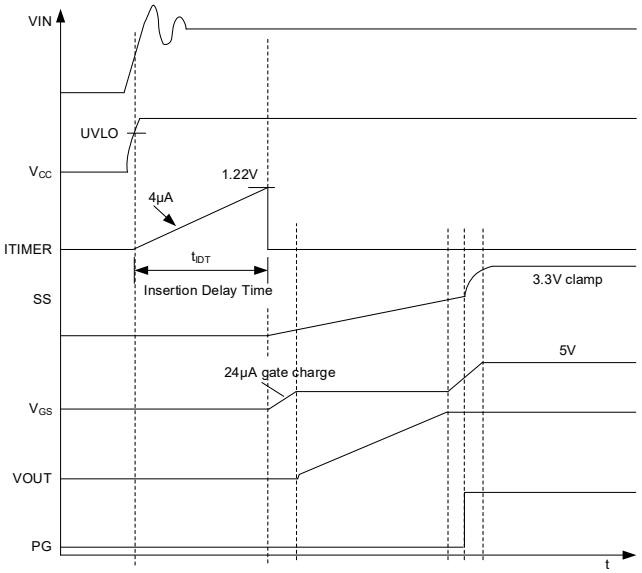


Figure 5. Power Sequence

Once VIN and VCC surpass the UVLO thresholds, the ITIMER pin uses an internal 4μA current source to charge the external C_{TMR} capacitor. The insertion delay time (t_{IDT}) is defined as the time required for the capacitor to rise from 0V to 1.22V under this charging mechanism. t_{IDT} can be configured by selecting an appropriate capacitor value for the C_{TMR} connected between the ITIMER pin and ground.

When the insertion delay period ends and EN exceeds 1.4V, the internal 24μA charge pump starts charging the MOSFET. The MOSFET conducts once its gate-source voltage (V_{GS}) surpasses the threshold (V_{GS_TH}), raising VOUT.

OPERATION (continued)

Soft-Start (SS)

SS uses a capacitor to determine the soft-start time. After the EN pin is pulled high and the startup delay period concludes, a constant current source that scales with the input voltage begins charging the SS capacitor voltage. This ensures consistent soft-start duration across varying input voltages. The output voltage's slew rate maintains tight synchronization with the SS voltage's charging profile. The SS capacitor value is determined via Equation 4:

$$C_{SS} = 9 \times \frac{t_{SS}}{R_{SS}} \quad (4)$$

Where t_{SS} is the soft-start time (ms), C_{SS} is the soft-start capacitor (nF), and R_{SS} is 0.89MΩ.

For instance, a 100nF capacitor yields an 8.9ms soft-start duration. When the load capacitance becomes excessively large, the current needed to sustain the set soft-start time surpasses the startup current threshold. Under such conditions, the voltage rise rate is governed by both the load capacitor's time constant and the current limit. Floating the SS pin generates a rapid voltage ramp-up. A 24μA current source drives the power FET's gate, where the gate charge current dictates the output voltage's rise profile. The resultant soft-start duration reaches 1ms, marking the minimal achievable output voltage ramp-up time under these parameters.

Enable and LOADEN

The enable/disable state of the SGM25120 is controlled by EN and LOADEN (see Table 1).

The exclusive switch can be enabled by setting EN = 1 during the LOADEN blanking period. After this period, EN = 1 and LOADEN = 1 must be asserted simultaneously to maintain the operation of the switch. EN = 0 Disable all working modes unconditionally. To recover from the latch failure state, restart the EN control signal or VIN power supply.

Table 1. EN/LOADEN Blanking Time

LOADEN Blanking Time Over?	EN	LOADEN	Status
N	0	0	Off
N	0	1	Off
N	1	0	On
N	1	1	On
Y	0	0	Off
Y	0	1	Off
Y	1	0	Off
Y	1	1	On

Note that LOADEN deactivates the power switch after its blanking period, but cannot re-enable it solely by cycling LOADEN. See Figure 6.

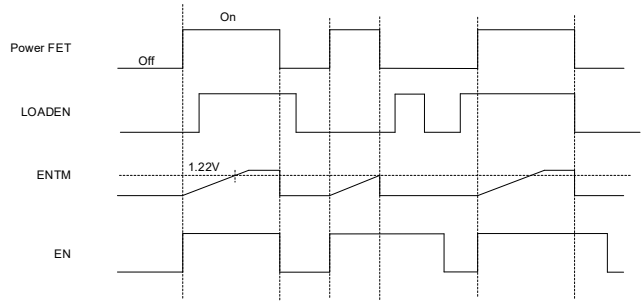


Figure 6. EN/LOADEN Timing Diagram

Upon enabling the component, the insertion delay mechanism activates. Once the delay interval completes, an internal 24μA current path is established to source charge to the power MOSFET's gate terminal. The voltage across gate-source (V_{GS}) achieves its threshold within approximately 1ms, after which the output voltage progression adheres to the soft-start (SS) defined slope profile.

LOADEN Blanking Time

When the enable signal (EN) is asserted high, LOADEN incorporates a programmable blanking time to inhibit de-assertion during the specified interval (refer to Figure 7). All fault detection functions remain enabled during startup. The power FET shuts down immediately upon fault detection. A transition of LOADEN to low during the blanking period does not deactivate the power FET switch.

Upon termination of the blanking period, LOADEN resumes standard operational control functionality.

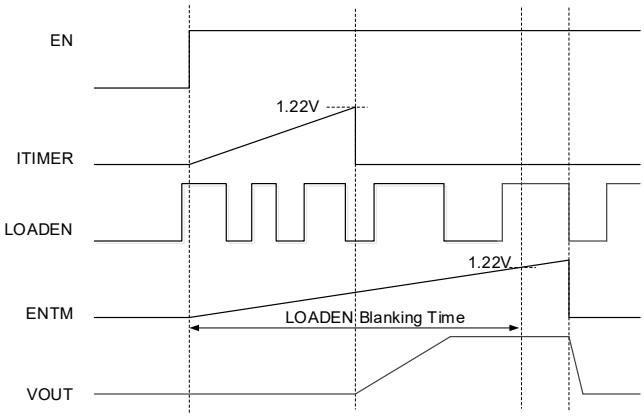


Figure 7. LOADEN Blanking Time

OPERATION (continued)

The blanking time is determined by a capacitor connected to the ENTM pin. The value of the blanking timer capacitor is calculated via Equation 5:

$$C_{ENTM} = \frac{1.1}{1.24} \times t_{LDNB} \quad (5)$$

Where t_{LDNB} (s) represents the LOADEN signal's blanking time, and C_{ENTM} (μF) the capacitor connected to the ENTM pin. For example, a 1μF capacitor results in a blanking time of 1.13s.

Connect ENTM to GND if LOADEN is not used.

Power Good (PG)

PG (Power Good) is an open-drain status monitor that asserts high when VOUT maintains regulation within specified input-referenced thresholds. This output requires a 10kΩ to 100kΩ pull-up resistor to the supply rail. During the startup sequence, PG remains in active-low state to enforce system shutdown, minimizing VOUT loading for safe power-up operation. This active-low signaling facilitates inrush current mitigation and thermal optimization during initialization phases.

The power-good signal is asserted when the device meets the following conditions, enabling the system to operate at full power.

V_{OUT} > 87% × V_{IN}, V_{GS} > 2V, V_{OUT} > V_{IN} - 0.7V

The PG signal asserts low when any of the following conditions occur:

V_{OUT} < 75% × V_{IN}, EN = 0, faults occurred

In the absence of an input signal, the PG pin remains low despite the presence of a pull-up resistor to the supply.

Fault Bar (nFAULT)

nFAULT (Fault Bar) is an open-drain fault indicator that asserts low when triggered. This output requires an external 10kΩ to 100kΩ pull-up resistor to the supply rail. The assertion occurs with 4μs maximum propagation delay from fault detection to active-low signaling.

- Over-current or output short
- Over-temperature
- Over-voltage
- VDS/VGS short

nFAULT goes high when the SGM25120 resumes normal operation. This means that the output voltage is higher than the setting voltage of the PG rising threshold, and the power FET is fully on (V_{GS} > 2V).

Fault Protections

Over-Current Protection (OCP)

Upon completion of soft-start, the SGM25120 transitions into normal operation mode. The fault timer is activated whenever the output current exceeds the programmed current limit threshold. If the output current drops below current limit before the fault timeout period expires, the device resumes normal operation. If the over-current condition persists beyond the fault timeout duration, the power FET is latched off and the nFAULT pulls down.

Intelli-Fuse OCP during Start-Up

The soft-start current limit (I_{OC_SS}) is jointly set by EFT power thresholds and external resistor values. Current is clamped at 80W MOSFET power dissipation; if over-power protection (OPP) does not trigger, resistor programming governs the limit. A 1.5ms over-current fault forces FET shutdown and nFAULT and SS pins are pulled low. See Figure 8.

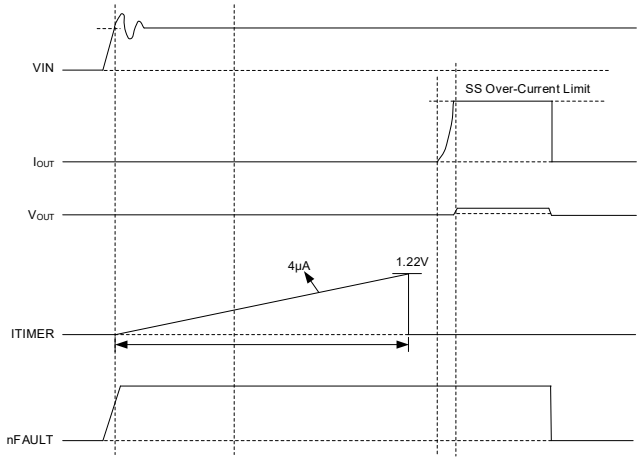


Figure 8. Soft-Start OCP Behavior

The typical OC regulation time t_{OC_REG} is 1.5ms. Actual regulation duration depends on the device's Allowed Operation Area (AOA). If over-temperature protection (OTP) triggers during soft-start OC regulation, the power FET immediately shuts down.

OPERATION (continued)

Short-Circuit Protection (SCP)

SGM25120 incorporates robust over-current protection with 50A short-circuit threshold to safeguard against critical fault conditions (e.g., output-to-ground short). When FET current surpasses this threshold, the 200ns-response gate drive cutoff mechanism instantaneously disables the power MOSFET. Post-fault, the device initiates immediate soft-start cycle re-initiation upon detecting V_{OS} drops low level to prevent input line transients. Persistent faults activate the adaptive fault timing protocol nFAULT is switched low when the integrated timer capacitor reaches 1.22V (Load current ≤ 2 × I_{LIMT}). If the load current is greater than twice the resistance setting the current limit, the fault timer is not activated, and power EFT is turned off after the device is restarted for 1.5ms.

Over-Temperature Protection (OTP)

The SGM25120 incorporates integrated junction temperature monitoring. When the temperature exceeds the thermal shutdown threshold (T_{SD} = +148℃), the power FET shuts off and nFAULT indicates low.

OCP during Normal Operation

Upon soft-start completion, the SGM25120 transitions to normal operation. When the output current exceeds the current limit (I_{LIMIT}), the fault timer (t_{OC}) activates. If the output current falls below I_{LIMIT} before the fault timeout elapses, normal operation resumes. Otherwise, if over-current persists beyond the fault timeout, the power FET is latched off permanently. The OCP fault timer (t_{OC}) value is determined by Equation 6.

$$t_{OC}(ms) = \frac{1.22}{40} \times C_{TM}(nF) \quad (6)$$

For example, a 10nF capacitor corresponds to an OCP fault timer (t_{OC}) of 0.3ms. When the output current exceeds the current limit (I_{LIMIT}), the nFAULT signal is pulled low after an 8μs delay to indicate a fault condition (see Figure 9).

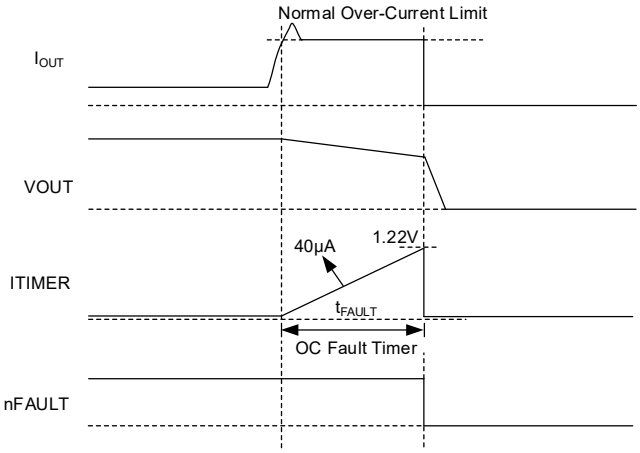


Figure 9. Normal Operation OCP Behavior

VIN Over-Voltage Protection (VIN OVP)

The SGM25120 has input over-voltage protection, and once the input voltage exceeds the set OV voltage, the power FET is turned off and the nFAULT and SS are pulled low.

DS Short Detection

When EN is high, the SGM25120 activates continuous drain-source short monitoring. If V_{OUT} > min (V_{IN} − 0.7V, 0.87 × V_{IN}) during the insertion delay period, the device immediately drives GATE low to disable the power FET while asserting nFAULT and PG low. The FET remains off until V_{OUT} < min (0.75 × V_{IN}, V_{IN} − 0.7V). Upon detecting a drain-source short during normal operation, nFAULT and PG are actively pulled low. The system automatically resumes standard functionality when the short-circuit condition is eliminated.

GS Short Detection

When these conditions are satisfied, the device detects a GS short and disables the power FET.

- V_{GATE} < V_{CP} - 0.9V
- V_{SS} > V_{CC} - 0.7V
- NO OC fault
- Delay 200ms

APPLICATION INFORMATION

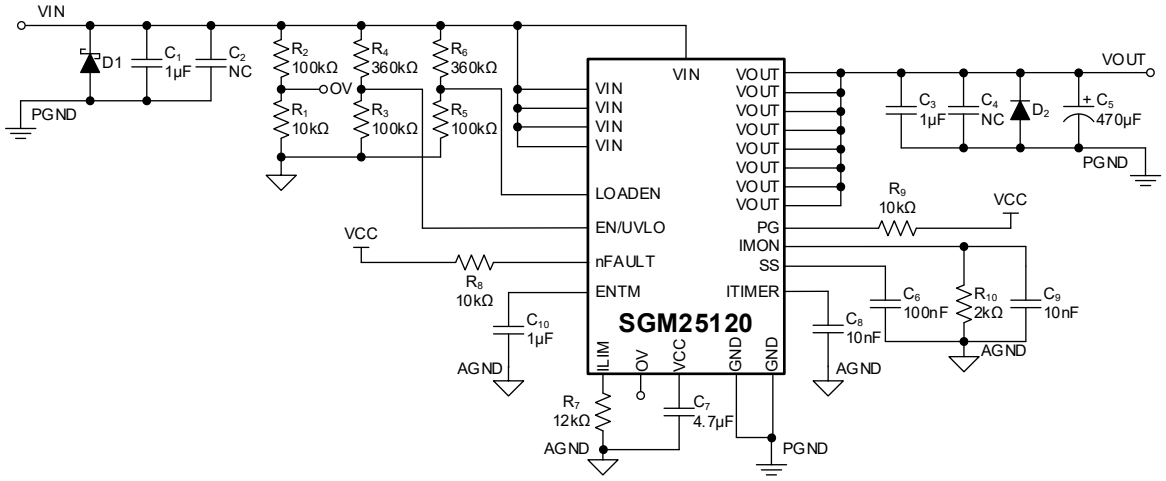


Figure 10. Typical Application Circuit

Current Limit Set (R_{SET})

The SGM25120's current limit setting must exceed the maximum expected load current in normal operation, with design margin accommodating current sense measurement tolerances. This threshold is configured through the calculation method specified in Equation 7:

$$I_{LIMIT} = \frac{0.3V}{R_{ILIM}} \times 10^6 (A) \quad (7)$$

Current Monitor Set

The SGM25120 monitors the current level through the MOSFET by sensing the voltage on the IMON pin, with a RMON resistor must be connected between this pin and GND. The IMON current can be calculated by Equation 8:

$$I_{IMON} = I_{FET} \times 20\mu A / A \quad (8)$$

Where I_{FET} is the current flowing through the MOSFET.

Then, the voltage can be achieved through the Equation 9:

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (9)$$

Using a 2kΩ R_{IMON} resistor can achieve a gain of 40mV/A. A small capacitor such as 10nF can also be placed in parallel with the RIMON resistor to smooth the indicator voltage.

PCB Layout Guidelines

To ensure optimal IC performance, careful consideration must be given to PCB layout design. The following key guidelines should be implemented:

- Position a 0.1μF or larger ceramic decoupling capacitor between VIN and GND, placing it as close as possible to the device's power pins.
- Select a low Equivalent Series Resistance (ESR) ceramic capacitor for the output stage, based on the design guidelines for capacitance value and voltage rating.
- Route the connection between the R_{ILIM} resistor and the device using the shortest possible trace lengths to minimize parasitic inductance.
- Establish a direct connection for the device's exposed thermal pad (EP) to the PCB ground plane. This can be achieved either through a solid solder joint to the ground layer or via a wide, short copper trace with minimal impedance.
- Place enough vias close to the power traces to achieve better thermal performance.

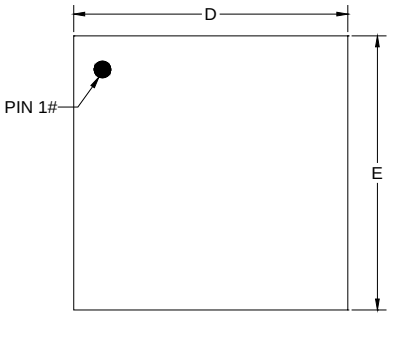
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

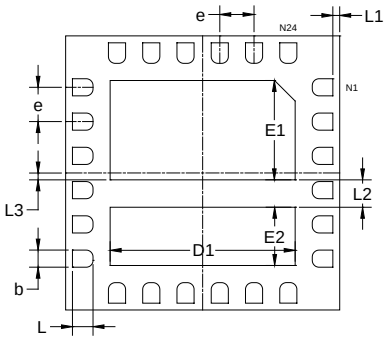
Changes from Original to REV.A (JUNE 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

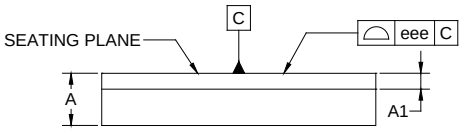
TLGA-4×4-24AL



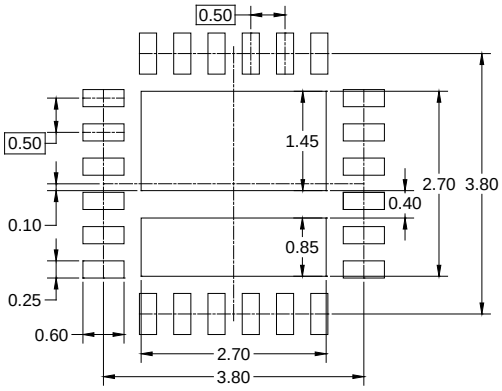
TOP VIEW



BOTTOM VIEW



SIDE VIEW



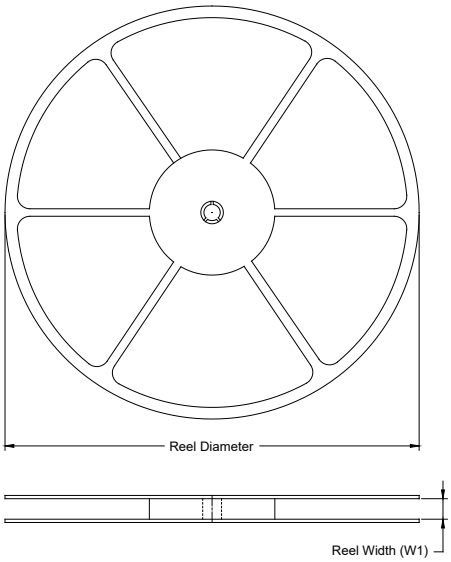
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.704	-	0.820
A1		0.232 REF	
b	0.200	-	0.300
D	3.900	-	4.100
D1	2.600	-	2.800
E	3.900	-	4.100
E1	1.350	-	1.550
E2	0.750	-	0.950
e		0.500 BSC	
L	0.250	-	0.350
L1		0.100 REF	
L2		0.400 REF	
L3		0.100 REF	
eee		0.100	

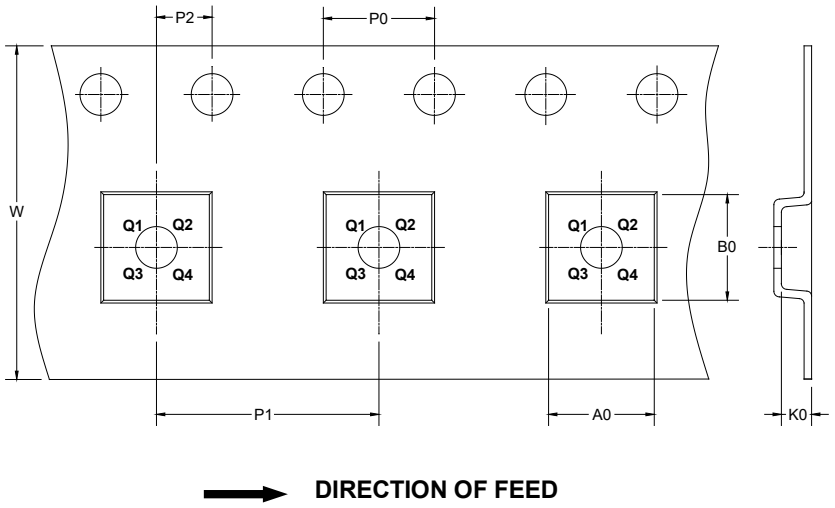
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



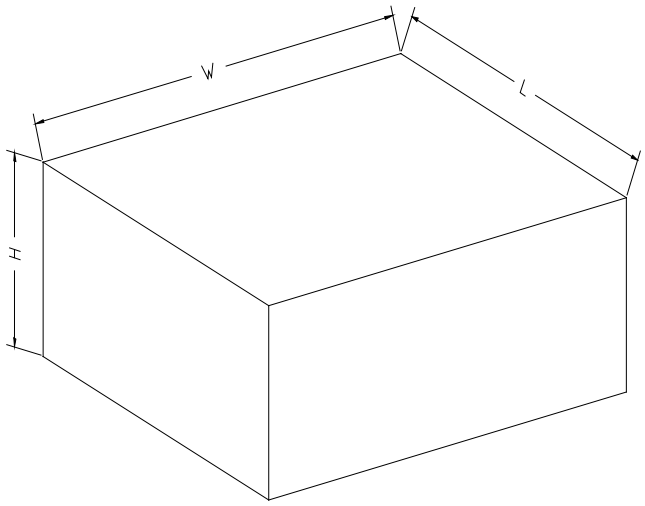
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TLGA-4×4-24AL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002