



SGM41536

Standalone 22V, 3A, 1-4 Cells

Buck Battery Charger

GENERAL DESCRIPTION

The SGM41536 is a standalone Buck charger for 1-cell to 4-cell Li-Ion or Li-polymer batteries. The charge voltage and current can be programmed by external resistors. The SGM41536 supports 4.1V to 22V input source voltage and provides 3A (MAX) charge current to 1-cell or 2-cell batteries and 2A (MAX) charge current to 3-cell or 4-cell batteries. The SGM41536 is highly integrated, including three main power switches: input reverse-blocking MOSFET (Q1, RBFET), high-side switching MOSFET (Q2, HSFET) and low-side switching MOSFET (Q3, LSFET).

Its low-impedance power path optimizes efficiency, reduces battery charging time, and extends battery life. The bootstrap diode of the high-side gate drive is also integrated to simplify the system design. The SGM41536 starts and completes the charge cycle without host control. A charge cycle automatically terminates when a full charge is detected if the device is not in thermal regulation. The charger automatically initiates a new charging cycle if the battery voltage falls below the recharge threshold.

The SGM41536 provides full protections for safety of battery charging, including battery temperature monitoring, charging safety timer, over-current and over-voltage protections, as well as pin open or short protections. When any fault occurs, the STAT pin reports the fault conditions.

The SGM41536 is available in a Green TQFN-3×3-16L package.

APPLICATIONS

Bluetooth Speakers, Drones, IP Cameras, Detachable Power Supply
Portable Internet Devices and Accessory

FEATURES

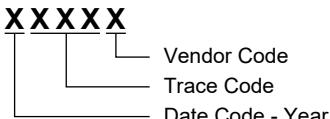
- 4.1 to 22V Operating Input Voltage Range
- 3.4V to 18V Programmable Charge Voltage
- Fully Integrated All MOSFETs, Current Sense and Loop Compensation
- 3A Maximum Charge Current for 1-2 Cells Battery
- 2A Maximum Charge Current for 3-4 Cells Battery
- High Frequency, 1.2MHz Synchronous Buck Charger
 - 92.5% Charge Efficiency at 2A from 5V Input for 1-Cell Battery
 - 92% Charge Efficiency at 2A from 9V Input for 1-Cell Battery
 - 95% Charge Efficiency at 2A from 12V Input for 2-Cell Battery
 - 96% Charge Efficiency at 1.5A from 15V Input for 3-Cell Battery
 - 96% Charge Efficiency at 1A from 20V Input for 4-Cell Battery
- Input Voltage Dynamic Power Management (VINDPM) Tracking Battery Voltage
- 5nA (TYP) Low Battery Leakage Current at 4.5V V_{BAT}
- 0.9 μ A (TYP) VBUS Supply Current in Disable Mode
- Charge Current Thermal Regulation at +120°C
- Pre-Charge Current: 10% of Fast Charge Current
- Termination Current: 10% of Fast Charge Current
- $\pm 0.64\%$ Charge Voltage Regulation
- Thermal Regulation and Thermal Shutdown
- VBUS/VBAT Over-Voltage Protection (OVP)
- Battery Charging Safety Timer
- Charge Disabled if Battery Feedback Pin FB is Open or Short
- Charge Disabled if ICHG Pin is Open or Short
- Fault Report on STAT Pin
- Available in a Green TQFN-3×3-16L Package

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41536	TQFN-3x3-16L	-40°C to +85°C	SGM41536YTQ16G/TR	03ATQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

VBUS (Converter Not Switching)	-0.3V to 28V
PMID (Converter Not Switching)	-0.3V to 28V
SW	-2V ⁽¹⁾ to 28V
BTST	-0.3V to 33V
STAT	-0.3V to 5.5V
BAT	-0.3V to 22V
BTST to SW	-0.3V to 5.5V
ICHG	-0.3V to 5.5V
REGN	-0.3V to 5.5V
POL	-0.3V to 5.5V
nEN	-0.3V to 5.5V
TS	-0.3V to 5.5V
FB	-0.3V to 22V
FB_GND	-0.3V to 22V

Output Sink Current

STAT	6mA
REGN	20mA

Package Thermal Resistance

TQFN-3x3-16L, θ_{JA}	38.9°C/W
TQFN-3x3-16L, θ_{JB}	12°C/W
TQFN-3x3-16L, θ_{JC} (TOP)	43.8°C/W
TQFN-3x3-16L, θ_{JC} (BOT)	3°C/W

Junction Temperature

Storage Temperature Range

Lead Temperature (Soldering, 10s)

ESD Susceptibility⁽²⁾⁽³⁾

HBM

CDM

NOTES:

1. -2V for 10ns transient.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBU}	4.1V to 22V
Battery Voltage Range, V_{BAT}	3.4V to 18V
Maximum Charge Current for 1-2 Cells Battery	3A
Maximum Charge Current for 3-4 Cells Battery	2A
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

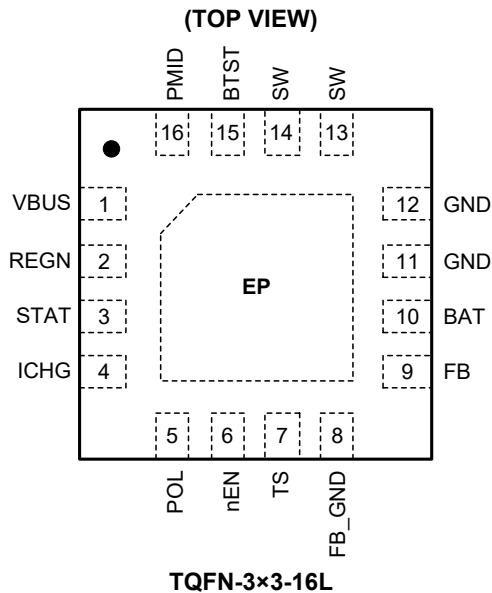
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VBUS	P	Charge Input (V_{IN}). Connect VBUS to the external DC power supply. Place a $2.2\mu F$ ceramic capacitor from VBUS pin to GND close to the device.
2	REGN	P	Gate Drive Power Supply. Power supply for internal MOSFET drivers. Place a $2.2\mu F$ ceramic capacitor from REGN pin to GND. It is recommended to place the capacitor close to REGN pin.
3	STAT	AO	Charge State Output. This is an open-drain output. Use a $1k\Omega$ resistor and LED pull-up to REGN. The state pin act as follows: During charge: low (LED ON). Charge completed or charge disabled by nEN pin: High (LED OFF). Charge fault conditions: 1Hz, 50% duty cycle pulses (LED BLINKS).
4	ICHG	AI	Charge Current Program Input. Connect a resistor between this pin and GND for programming the constant charge current by $I_{CHG} = K_{ICHG}/R_{ICHG}$ ($K_{ICHG} = 39900$). The device stops charging when this pin is pulled low to ground or left open.
5	POL	AI	nEN Pin Polarity Selection. For the standalone charger, keep this pin floating.
6	nEN	AI	Device Disable Input. When POL pin is floating, the device is enabled with nEN pin floating or pulled low and the device is disabled with nEN pin pulled high. When POL pin is pulled low, the device is enabled with nEN pin pulled high and the device is disabled with nEN pin pulled low or floating.
7	TS	AI	Temperature Sense Input. Connect TS pin to the battery negative temperature coefficient (NTC) thermistor. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charging suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC feature is not used, connect the TS pin to ground directly.
8	FB_GND	AI	Battery Voltage Feedback Ground Input. Use a low-side divider resistor R_2 to establish a connection from FB pin to this pin. This pin is in high-impedance when there is no adaptor or when the device is disabled.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
9	FB	AI	Battery Voltage Feedback Input. Use a high-side divider resistor R_1 to connect from BAT pin to this pin to program the battery charge voltage. The device stops charging when this pin is open or short. The battery charge voltage is programmed as $V_{BATREG} = 1.1 \times (1 + R_1/R_2)$.
10	BAT	AI	Battery Voltage Input. Connect this pin to the node of inductor output and positive node of the battery. It is recommended to connect a 10 μ F capacitor from this pin to GND pin.
11, 12	GND	P	Ground Pin of the Device.
13, 14	SW	P	Switching Node. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
15	BTST	P	High-side Driver Positive Supply. It is internally connected to the bootstrap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
16	PMID	P	PMID Pin. This pin is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of high-side MOSFET (HSFET). Connect a 10 μ F ceramic capacitor from PMID pin to GND and place it as close as possible to the device.
Exposed Pad	EP	—	Thermal Pad. It is the thermal pad to conduct heat from the device (not suitable for high current return). Tie externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE: AI = analog input, AO = analog output, P = power.

ELECTRICAL CHARACTERISTICS

($V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, typical values are measured at $T_J = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current						
VBUS Reverse Current from BAT/SW to VBUS	I_{VBUS_REVS}	VBUS is shorted to GND, measure VBUS reverse current, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$V_{BAT} = V_{SW} = 4.5\text{V}$		0.005	2
			$V_{BAT} = V_{SW} = 9.0\text{V}$		0.005	2.5
			$V_{BAT} = V_{SW} = 13.5\text{V}$		0.005	3
			$V_{BAT} = V_{SW} = 18\text{V}$		0.005	3
VBUS Leakage Current in Disable Mode	$I_{Q_VBUS_DIS}$	Charger is disabled, nEN is pulled high, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$V_{VBUS} = 5\text{V}, V_{BAT} = 4\text{V}$		0.9	2.5
			$V_{VBUS} = 9\text{V}, V_{BAT} = 4\text{V}$		2.7	4.25
			$V_{VBUS} = 15\text{V}, V_{BAT} = 4\text{V}$		3.4	6
			$V_{VBUS} = 20\text{V}, V_{BAT} = 4\text{V}$		4	7.5
BAT and SW Pins Leakage Current in HIZ Mode	$I_{Q_BAT_HIZ}$	$V_{BAT} = V_{SW} = 4.5\text{V}$, VBUS floating, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$			0.005	0.5
BAT and SW Pins Leakage Current in Disable Mode	$I_{Q_BAT_DIS}$	$V_{BAT} = V_{SW} = 9\text{V}$, ICHG connected to a $25\text{k}\Omega$ resistor, VBUS floating, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$			0.005	0.5
VBUS Power-Up						
VBUS Operating Range	V_{VBUS_OP}	After start-up	4.1		22	V
VBUS Power-On Reset	V_{VBUS_UVLOZ}	V_{VBUS} rising	3.3	3.58	3.85	V
VBUS Power-On Reset Hysteresis	$V_{VBUS_UVLOZ_HYS}$	V_{VBUS} falling		240		mV
A Condition to Switching	V_{VBUS_LOWV}	V_{VBUS} falling, $V_{BAT} = 3.2\text{V}$	3.5	3.7	3.95	V
A Condition to Switching, Hysteresis	$V_{VBUS_LOWV_HYS}$	V_{VBUS} rising, $V_{BAT} = 3.2\text{V}$		320		mV
Enter Sleep Mode Threshold	V_{SLEEP}	V_{VBUS} falling, $V_{VBUS} - V_{BAT}$, $V_{VBUS_LOWV} < V_{BAT} < V_{BATREG}$, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	45	100	190	mV
Exit Sleep Mode Threshold	V_{SLEEPZ}	V_{VBUS} rising, $V_{VBUS} - V_{BAT}$, $V_{VBUS_LOWV} < V_{BAT} < V_{BATREG}$, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	160	245	375	mV
VBUS Over-Voltage Rising Threshold	$V_{VBUS_OVP_RISE}$	V_{VBUS} rising, converter stops switching		22.2		V
VBUS Over-Voltage Falling Hysteresis	$V_{VBUS_OVP_HYS}$	V_{VBUS} falling, converter starts switching		425		mV
MOSFETS						
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID (Q1)	R_{DSON_Q1}	$V_{REGN} = 5\text{V}$		34	60	$\text{m}\Omega$
High-side Switching MOSFET On-Resistance between PMID and SW (Q2)	R_{DSON_Q2}	$V_{REGN} = 5\text{V}$		60	97	$\text{m}\Omega$
Low-side Switching MOSFET On-Resistance between SW and GND (Q3)	R_{DSON_Q3}	$V_{REGN} = 5\text{V}$		64	103	$\text{m}\Omega$
FB_GND MOSFET On-Resistance between FB_GND and GND	$R_{DSON_FB_GND}$				33	Ω
Battery Charger						
Charge Voltage Regulation Range	V_{BATREG_RANGE}	$V_{VBUS} = 20\text{V}$, V_{BATREG} is programmed by FB resistor divider	3.4		18	V
Battery Feedback Regulation Voltage	$V_{FB_REF_VBATREG}$	$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$, initial accuracy	1093	1100	1107	mV

ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, typical values are measured at $T_J = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Battery Charger							
Charge Current Regulation	I_{CHG}	$V_{VBUS} = 6\text{V}$, I_{CHG} set at 1.72A with $R_{I_{CHG}} = 23.2\text{k}\Omega$, initial accuracy	1.55	1.72	1.85	A	
		I_{CHG} set at 1.72A with $R_{I_{CHG}} = 23.2\text{k}\Omega$, initial accuracy	1.47	1.72	1.94		
		$V_{VBUS} = 6\text{V}$, I_{CHG} set at 1.72A with $R_{I_{CHG}} = 23.2\text{k}\Omega$, initial accuracy	0.9	1	1.1		
		I_{CHG} set at 1.0A with $R_{I_{CHG}} = 40.2\text{k}\Omega$, initial accuracy	0.86	1	1.16		
		$V_{VBUS} = 6\text{V}$, I_{CHG} set at 1.0A with $R_{I_{CHG}} = 40.2\text{k}\Omega$, initial accuracy	0.41	0.5	0.6		
		I_{CHG} set at 0.5A with $R_{I_{CHG}} = 78.7\text{k}\Omega$, initial accuracy	0.39	0.5	0.63		
Termination Current	I_{TERM}	I_{CHG} set at 1.72A with $R_{I_{CHG}} = 23.2\text{k}\Omega$, initial accuracy		184		mA	
		I_{CHG} set at 1.0A with $R_{I_{CHG}} = 40.2\text{k}\Omega$, initial accuracy		107			
		I_{CHG} set at 0.5A with $R_{I_{CHG}} = 78.7\text{k}\Omega$, initial accuracy		75			
Pre-Charge Current	I_{PRECHG}	I_{CHG} set at 1.72A with $R_{I_{CHG}} = 23.2\text{k}\Omega$, initial accuracy		172		mA	
		I_{CHG} set at 1.0A with $R_{I_{CHG}} = 40.2\text{k}\Omega$, initial accuracy		100			
		I_{CHG} set at 0.5A with $R_{I_{CHG}} = 78.7\text{k}\Omega$, initial accuracy		70			
VBAT Short Rising Threshold	$V_{BAT_SHORT_RISE}$	Short to pre-charge (per cell)	50	52.5	55	%	
VBAT Short Falling Threshold	$V_{BAT_SHORT_FALL}$	Pre-charge to battery short (per cell)	45.3	47.8	50.3	%	
Battery Short Current	I_{BAT_SHORT}	$V_{BAT} < V_{BAT_SHORT_FALL}$	22	29	37	mA	
V_{BAT_LOWV} Rising Threshold	$V_{FB_REF_LOWV_RISE}$	Pre-charge to fast charge rising, as percentage of $V_{FB_REF_VBATREG}$	68	70	72	%	
V_{BAT_LOWV} Falling Threshold	$V_{FB_REF_LOWV_FALL}$	Fast charge to pre-charge falling, as percentage of $V_{FB_REF_VBATREG}$	66	68	70	%	
Recharge Threshold	$V_{FB_REF_RECHG}$	V_{FB} falling, as percentage of $V_{FB_REF_VBATREG}$	94	96	98	%	
Input Voltage/Current Regulation							
Minimum Input Voltage Regulation	V_{INDPM_MIN}	$V_{BAT} = 3.5\text{V}$, measured at PMID pin	3.75	4.1	4.45	V	
Input Voltage Regulation	V_{INDPM}	$V_{BAT} = 4\text{V}$, measured at PMID pin, $V_{INDPM} = 1.044 \times V_{BAT} + 0.125\text{V}$	3.95	4.3	4.65	V	
		$V_{BAT} = 8\text{V}$, measured at PMID pin, $V_{INDPM} = 1.044 \times V_{BAT} + 0.125\text{V}$	8.15	8.5	8.85		
Input Current Regulation	I_{INDPM}	Initial accuracy	$T_J = +25^\circ\text{C}$	3	3.4	3.9	A
			$T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	2.75	3.4	4.15	
Battery Over-Voltage Protection							
Battery Over-Voltage Rising Threshold	$V_{FB_BAT_OVP_RISE}$	V_{BAT} rising as percentage of $V_{FB_REF_VBATREG}$, initial accuracy	103	104	105	%	
Battery Over-Voltage Falling Threshold	$V_{FB_BAT_OVP_FALL}$	V_{BAT} falling as percentage of $V_{FB_REF_VBATREG}$, initial accuracy	101	102	103	%	

ELECTRICAL CHARACTERISTICS (continued)

($V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, typical values are measured at $T_J = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter Protection						
Bootstrap Refresh Comparator Threshold	$V_{BTST_REFRESH}$	$(V_{BTST} - V_{SW})$ when LSFET refresh pulse is requested, $V_{VBUS} = 5\text{V}$	2.7	3.1	3.5	V
HSFET Cycle-by-Cycle Over-Current Limit Threshold	I_{HSFET_OCP}		5.2	6.6	7.7	A
STAT Indication						
STAT Pin Sink Current	I_{STAT_SINK}	STAT pin sink current capability, guaranteed by design	6			mA
STAT Pin Equivalent Resistance	R_{STAT}	$V_{STAT} = 0.4\text{V}$		100		Ω
STAT Pin Blink Frequency	f_{BLINK}			1		Hz
STAT Pin Blink Duty Cycle	D_{BLINK_DUTY}			50		%
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Accuracy	T_{REG}			120		$^\circ\text{C}$
Thermal Shutdown Rising Threshold	T_{SHUT}	Temperature increasing		150		$^\circ\text{C}$
Thermal Shutdown Falling Threshold		Temperature decreasing		125		$^\circ\text{C}$
Buck Mode Operation						
PWM Switching Frequency	f_{SW}	SW node frequency	1.1	1.2	1.3	MHz
Maximum PWM Duty Cycle	D_{MAX}			95		%
REGN LDO						
REGN LDO Output Voltage	V_{REGN}	$V_{VBUS} = 5\text{V}$, $I_{REGN} = 0\text{mA}$ to 16mA	4.8		5.05	V
		$V_{VBUS} = 12\text{V}$, $I_{REGN} = 16\text{mA}$	4.8	5	5.2	
ICHG Setting						
ICHG Pin Regulated Voltage	V_{ICHG}		990	1000	1010	mV
Maximum Resistance to Disable Charge	$R_{ICHG_SHORT_FALL}$				1	$\text{k}\Omega$
Minimum Resistance to Disable Charge	$R_{ICHG_OPEN_RISE}$	Guaranteed by design	550			$\text{k}\Omega$
Maximum Programmable Resistance at ICHG	R_{ICHG_MAX}				250	$\text{k}\Omega$
Minimum Programmable Resistance at ICHG	R_{ICHG_MIN}		11.7			$\text{k}\Omega$
ICHG Setting Resistor Threshold to Clamp Pre-Charge and Termination Current to 70mA and 75mA	R_{ICHG_HIGH}	$R_{ICHG} > R_{ICHG_HIGH}$	40	70	125	$\text{k}\Omega$
Charge Current Ratio	K_{ICHG}	ICHG set at 1.72A with $R_{ICHG} = 23.2\text{k}\Omega$, $I_{CHG} = K_{ICHG}/R_{ICHG}$		39900		$\text{A} \times \Omega$
		ICHG set at 1.0A with $R_{ICHG} = 40.2\text{k}\Omega$, $I_{CHG} = K_{ICHG}/R_{ICHG}$		40150		
		ICHG set at 0.5A with $R_{ICHG} = 78.7\text{k}\Omega$, $I_{CHG} = K_{ICHG}/R_{ICHG}$		40300		
Cold/Hot Thermistor Comparator						
T_{COLD} (0°C) Threshold, Charge Suspended if Thermistor Temperature is below T_1	$V_{T1\%}$	V_{TS} rising, as percentage to V_{REGN}	72	73.5	75	%
		As percentage to V_{REGN}	70	71.5	73	
T_{HOT} (45°C) Threshold, Charge Suspended if Thermistor Temperature is above T_3	$V_{T3\%}$	V_{TS} falling, as percentage to V_{REGN}	46	47.5	49	%
		As percentage to V_{REGN}	47	48.5	50	

ELECTRICAL CHARACTERISTICS (continued)

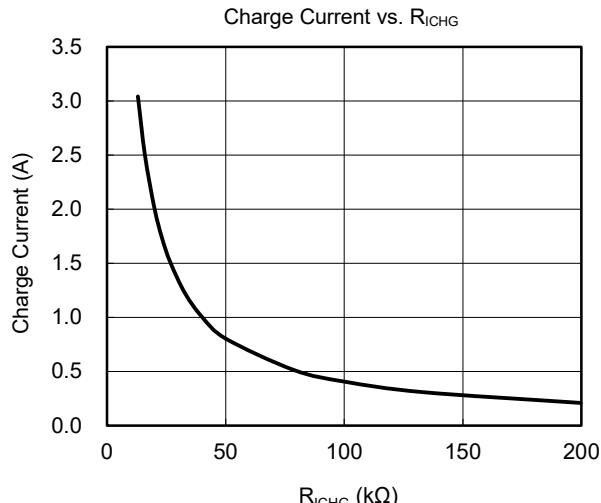
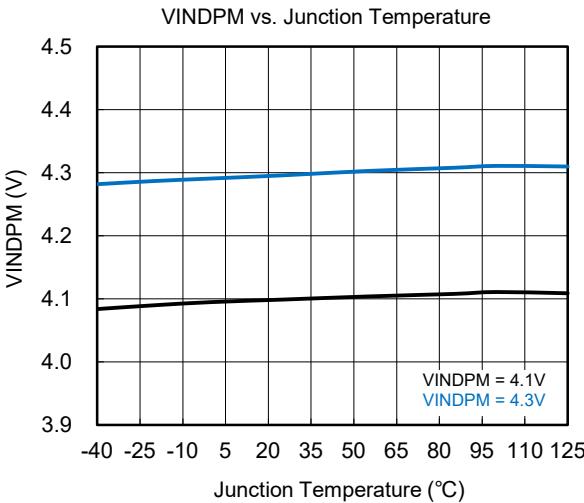
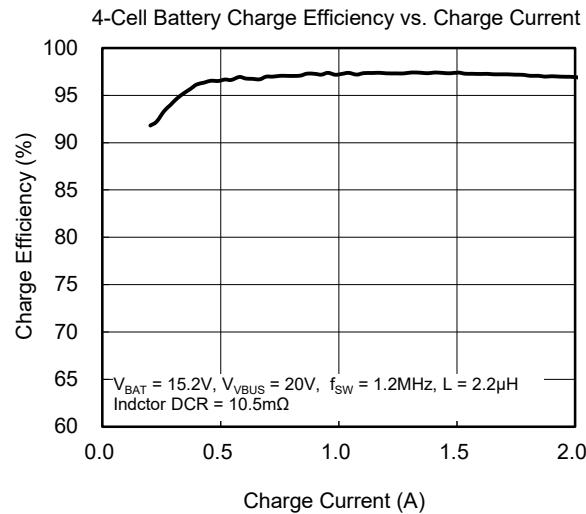
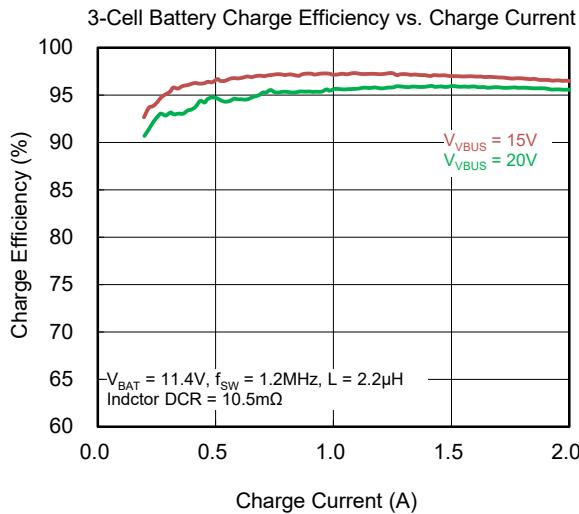
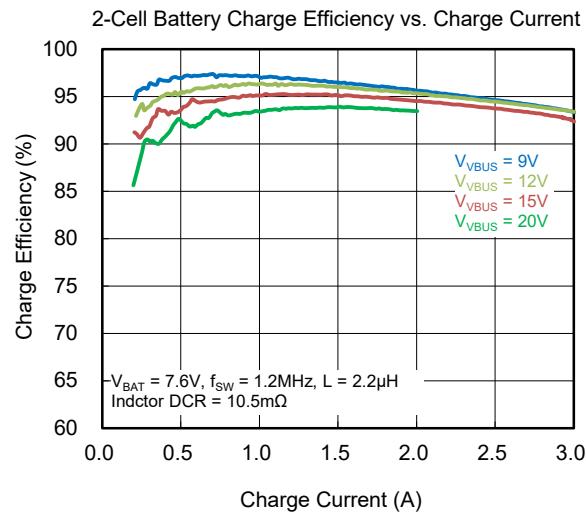
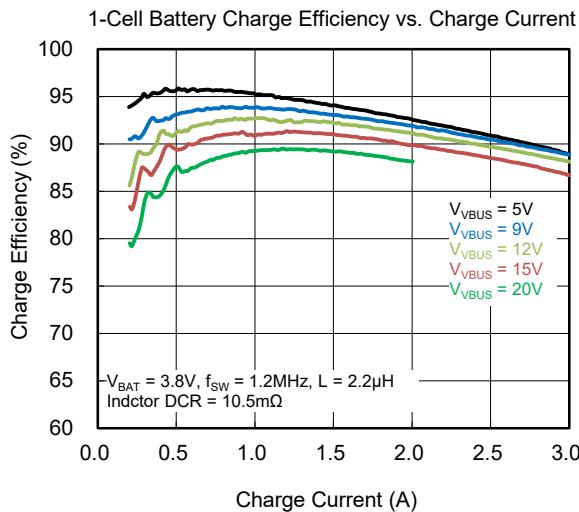
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic I/O Pin Characteristics (POL, nEN)						
Input Low Threshold	V_{ILO}	Falling			0.4	V
Input High Threshold	V_{IH}	Rising	1.2			V
High-Level Leakage Current at nEN Pin	I_{BIAS}	nEN pin is pulled up to 1.8V		0.65		μA

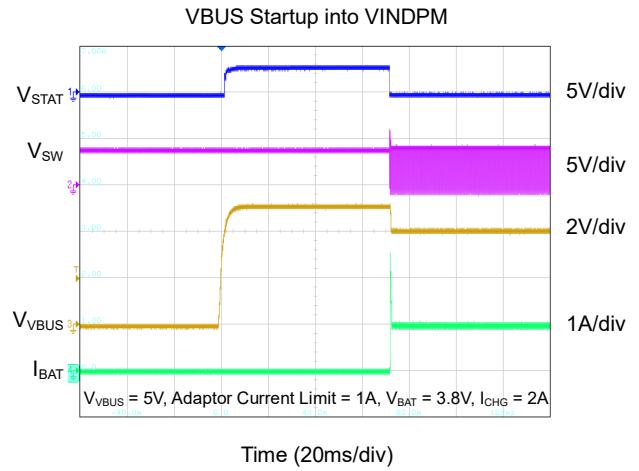
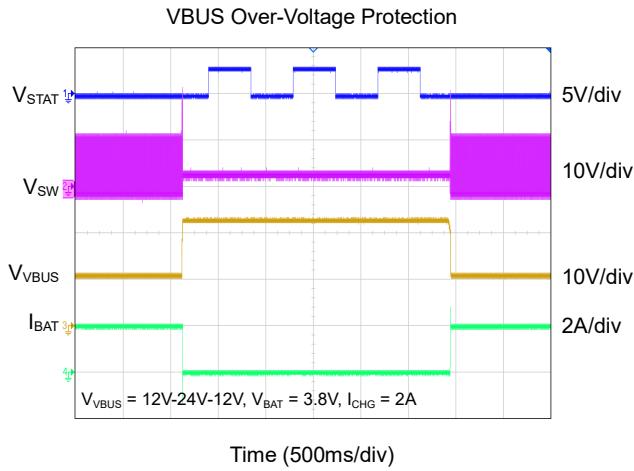
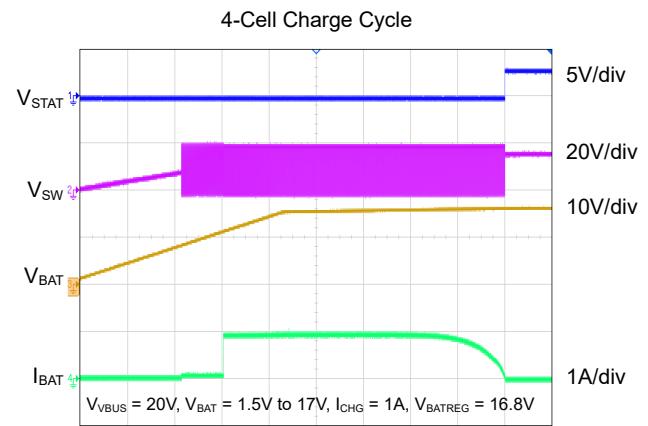
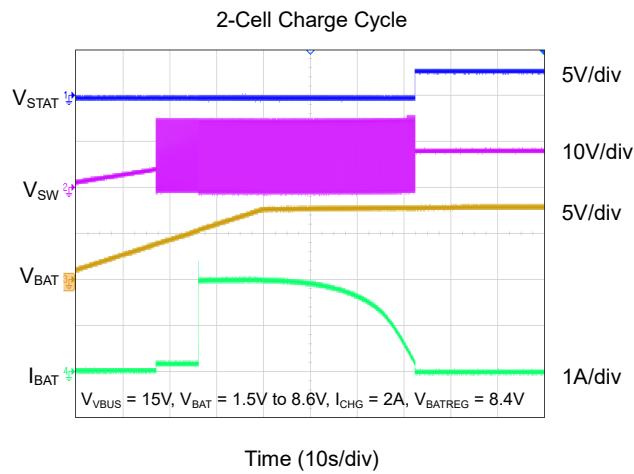
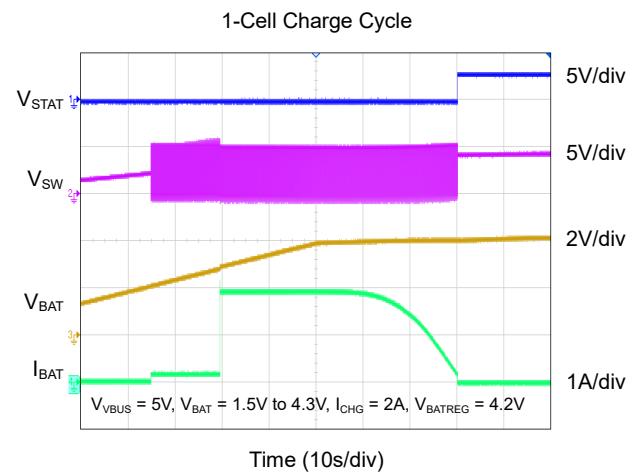
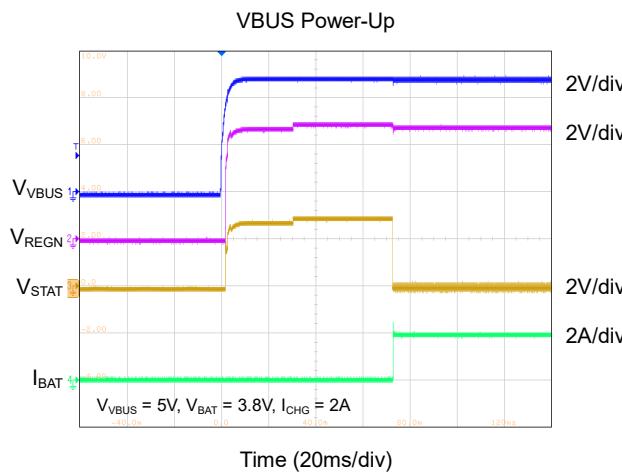
TIMING REQUIREMENTS

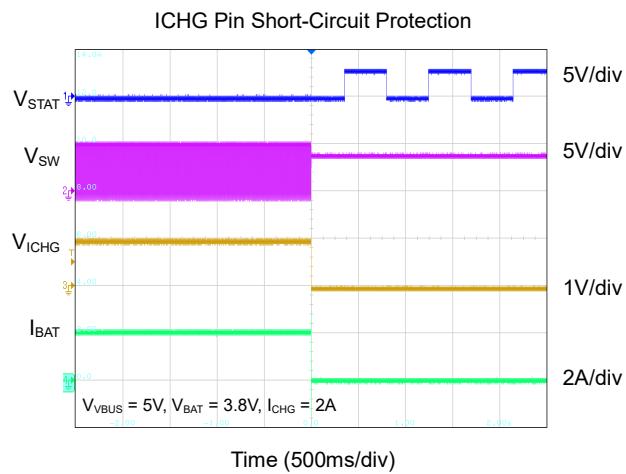
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBUS/BAT Power-Up						
Delay from Enable at nEN Pin to Charger Power-On	$t_{CHG_ON_EN}$	nEN pin voltage rising		70		ms
Delay from VBUS to Charge Start	$t_{CHG_ON_VBUS}$	nEN pin is grounded, battery present		70		ms
Battery Charger						
Charge Safety Timer	t_{SAFETY_FAST}	Fast charge safety timer		20		h
	t_{SAFETY_PRE}	Pre-charge safety timer		2		h

TYPICAL PERFORMANCE CHARACTERISTICS

Measured at $T_A = +25^\circ\text{C}$, $C_{\text{VBUS}} = 2.2\mu\text{F}$, $C_{\text{PMID}} = 10\mu\text{F}$, $C_{\text{BAT}} = 10\mu\text{F}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Measured at $T_A = +25^\circ\text{C}$, $C_{\text{VBU}} = 2.2\mu\text{F}$, $C_{\text{PMID}} = 10\mu\text{F}$, $C_{\text{BAT}} = 10\mu\text{F}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)Measured at $T_A = +25^\circ\text{C}$, $C_{\text{VBU}} = 2.2\mu\text{F}$, $C_{\text{PMID}} = 10\mu\text{F}$, $C_{\text{BAT}} = 10\mu\text{F}$, unless otherwise noted.

TYPICAL APPLICATION CIRCUIT

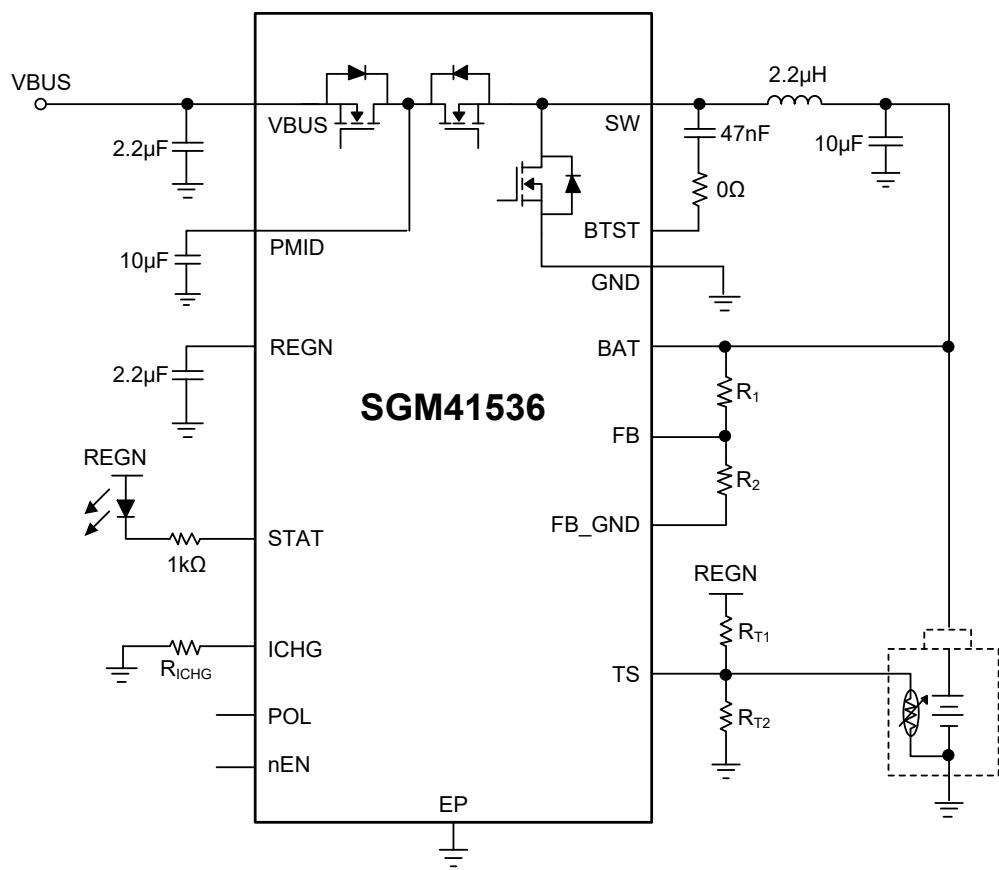


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

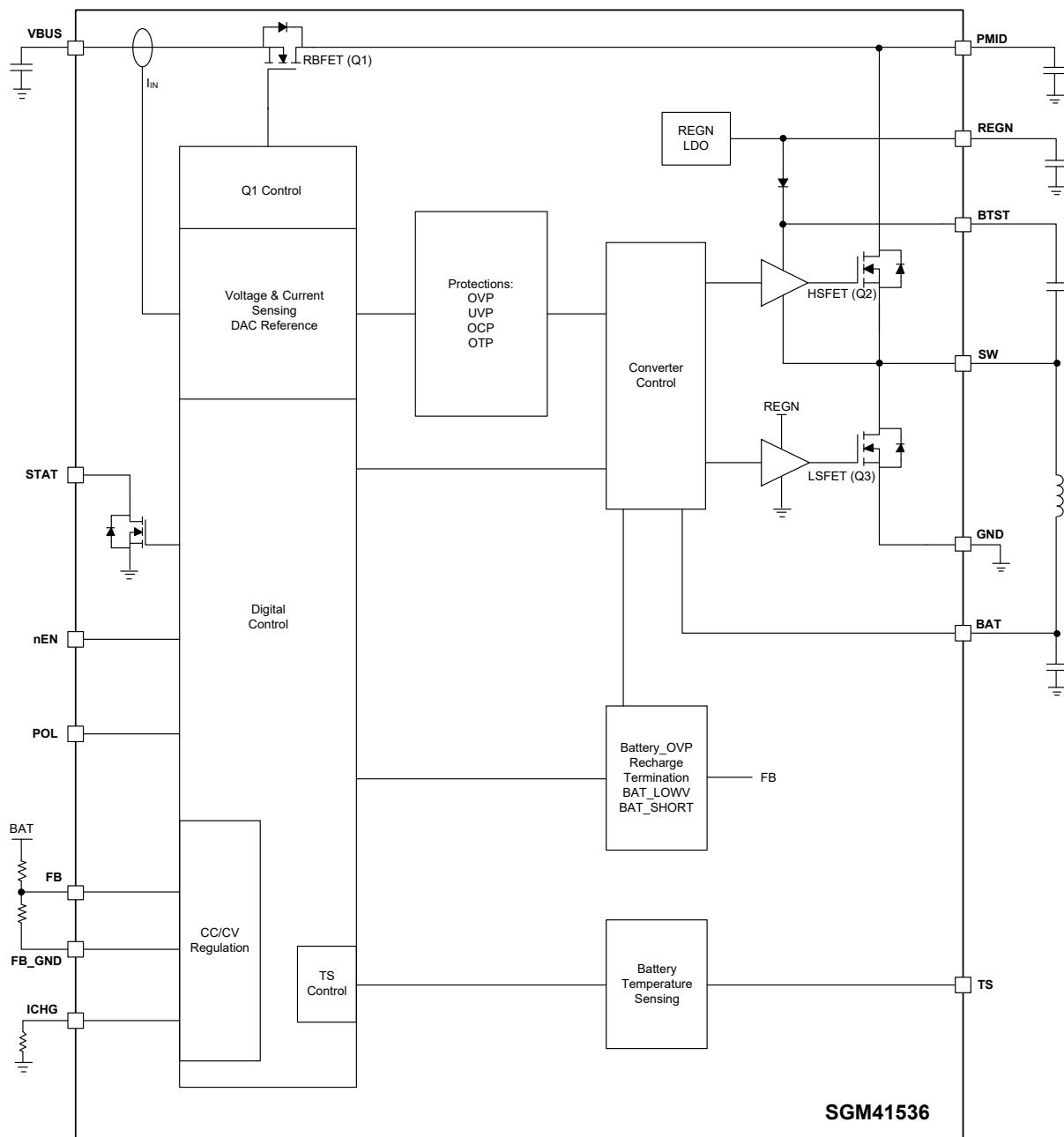


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41536 is a highly integrated Buck charger for 1-cell to 4-cell Li-Ion or Li-polymer batteries. The charge voltage and current can be programmed by external resistors. The device includes three main power switches: input reverse-blocking MOSFET (Q1, RBFET), high-side switching MOSFET (Q2, HSFET) and low-side switching MOSFET (Q3, LSFET). The bootstrap diode of the high-side gate drive is also integrated to simplify the system design.

Device Power-Up

Power-On Reset (POR)

The device can be enabled or disabled by nEN pin. The device is in disable mode and its input current is minimum from VBUS pin if the device is disabled by nEN pin. When the voltage of VBUS goes above its UVLO level ($V_{VBUS} > V_{VBUS_UVLO}$), a POR happens and activates the internal bias and comparators if the device is enabled by nEN pin.

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The STAT pin is also pulled up to REGN by a $1k\Omega$ resistor and LED. The REGN LDO enables when the following conditions are satisfied.

1. The device is enabled by nEN pin.
2. $V_{VBUS} > V_{VBUS_UVLO}$.
3. $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$.
4. After sleep comparator deglitch time.

The REGN LDO is only powered by VBUS and remains on even at fault conditions. When VBUS is removed, REGN LDO is off.

Charger Power-Up

After the REGN power-up, the charger will power up if there are no fault conditions. The charger will remain off if any of the following fault condition is satisfied.

1. $V_{VBUS} < V_{VBUS_LOWV}$.
2. $V_{VBUS} > V_{VBUS_OVP}$.
3. $V_{BAT} > V_{BAT_OVP}$.
4. ICHG pin is shorted to GND or open.
5. FB pin is shorted to GND or open.
6. Thermistor cold/hot fault on TS pin.
7. Safety timer expires.
8. Thermal shutdown.

Charger Enable and Disable by nEN Pin

When POL pin is floating, the device is enabled with nEN pin floating or pulled low and the device is disabled with nEN pin pulled high. When POL pin is pulled low, the device is enabled with nEN pin pulled high and the device is disabled with nEN pin pulled low or floating.

Device Unplugged from Input Source

The device enters the HIZ mode when the VBUS is unplugged and the leakage current from the battery to BAT pin and SW pin is less than $I_{Q_BAT_HIZ}$.

Battery Charging Management

The SGM41536 is designed for charging 1-2 cells Li-Ion or Li-polymer batteries with charge current up to 3A (MAX) and charging 3-4 cells Li-Ion or Li-polymer batteries with charge current up to 2A (MAX). The maximum input voltage is up to 22V. The charge voltage and current are programmed by external resistors at FB and ICHG pins. When the charge conditions are satisfied, a new charging cycle will start. When the charging voltage is above the recharge threshold and the current is below the termination current I_{TERM} , as well as the device is not in thermal regulation, the device will terminate the charging cycle. If the voltage of the fully charged battery drops below the recharge voltage threshold, the device will initiate charging again, and the charge safety timer will be reset.

Battery Charging Profile

The SGM41536 features a full battery charging profile with four phases. In the beginning of the cycle, the charge battery voltage (V_{BAT}) is set by external divider resistors in FB pin. The fast charge current is set by external resistor in ICHG pin. Depending on the detected status of the battery, the proper phase is selected to start or for the continuation of the charging cycle. The four phases are trickle charge, pre-charge, fast charge (constant current) and constant voltage. At each charge phase, the charge current is different as shown in Table 1.

Table 1. Charge Current Setting Based on V_{BAT}

V_{BAT} Voltage	Charge Current	Typical Value
$V_{BAT} < V_{BAT_SHORT}$	I_{BAT_SHORT}	29mA
$V_{BAT_SHORT} < V_{BAT} < V_{BAT_LOWV}$	I_{PRECHG}	10% of I_{CHG} ($I_{PRECHG} > 70mA$)
$V_{BAT} > V_{BAT_LOWV}$	I_{CHG}	Set by ICHG resistor

DETAILED DESCRIPTION (continued)

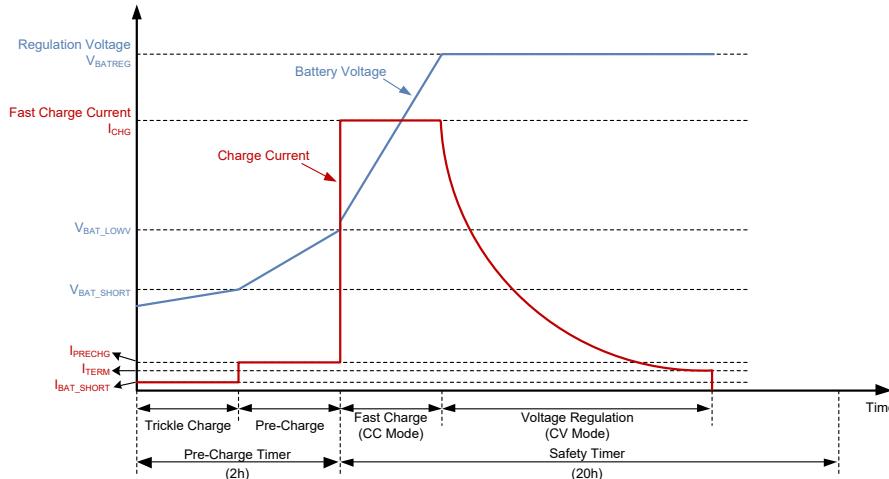


Figure 3. Battery Charging Profile

Pre-Charge

In pre-charge phase, the pre-charge current is programmed as 10% of I_{CHG} . But the pre-charge current is clamped at 70mA if $R_{ICHG} > R_{ICHG_HIGH}$.

Charging Termination

When the charging voltage is above the recharge threshold and the current is below the termination current I_{TERM} , as well as the device is not in thermal regulation, the device will terminate the charging cycle. The termination current is programmed as 10.7% of I_{CHG} . And the termination current is clamped at 75mA if $R_{ICHG} > R_{ICHG_HIGH}$.

Battery Recharge

When the charge is terminated and a charge cycle is finished, the safety timer is disabled. If the battery's voltage falls below the recharge voltage threshold ($V_{FB} < V_{FB_REF_RECHG}$), the device will recharge again and the safety timer is reset and enabled.

Charging Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. The safety timer is 20 hours if $V_{BAT} > V_{BAT_LOWV}$ and 2 hours if $V_{BAT} < V_{BAT_LOWV}$. The charge cycle will suspend if the safety timer expires. The safety timer can be reset by the following events.

1. Stop and restart the charging cycle (adaptor is re-plugged, toggle nEN pin or charged battery falls below recharge threshold).
2. The battery voltage crosses the V_{BAT_SHORT} threshold or the V_{BAT_LOWV} threshold.

The device stops switching and STAT pin is open if safety timer expires and V_{BAT} is above recharge threshold. The device stops switching and STAT pin blinks if safety timer

expires and V_{BAT} is below recharge threshold. The safety timer fault is cleared by safety timer reset.

The safety timer counts at half clock rate when the charger is under thermal regulation. The safety timer is suspended in such faults: TS fault, V_{VBUSS_OVP} , V_{BAT_OVP} , ICHG pin faults, FB pin faults and thermal shutdown. Once the fault is cleared, the safety timer resumes counting.

Thermistor Temperature Monitoring

To prevent the batteries from operating at the cold or hot temperature, the device provides the TS pin to monitor the batteries temperature. When powered on, if the voltage of the TS pin is detected to be less than 2.5% of V_{REGN} (a threshold of around 0.125V), the TS function will be disabled, resulting in the chip not having over heat or over cold protection. The normal temperature range is T_1 (T_{COLD}) to T_3 (T_{HOT}), which is programmed by R_{T1} and R_{T2} . Outside this range, charging should be stopped. The corresponding voltages sensed by NTC thermistor resistance are named V_{T1} to V_{T3} . Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. Select $T_{COLD} = 0^\circ\text{C}$ and $T_{HOT} = 45^\circ\text{C}$ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor $R_{THCOLD} = 27.28\text{k}\Omega$ and $R_{THHOT} = 4.91\text{k}\Omega$, according to Equation 1 and 2, $R_{T1} = 4.42\text{k}\Omega$ and $R_{T2} = 22.1\text{k}\Omega$ are selected.

$$R_{T2} = \frac{V_{REGN} \times R_{THHOT} \times R_{THCOLD} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T3}} \right)}{R_{THHOT} \times \left(\frac{V_{REGN}}{V_{T3}} - 1 \right) - R_{THCOLD} \times \left(\frac{V_{REGN}}{V_{T1}} - 1 \right)} \quad (1)$$

$$R_{T1} = \frac{\frac{V_{REGN}}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{THCOLD}}} \quad (2)$$

DETAILED DESCRIPTION (continued)

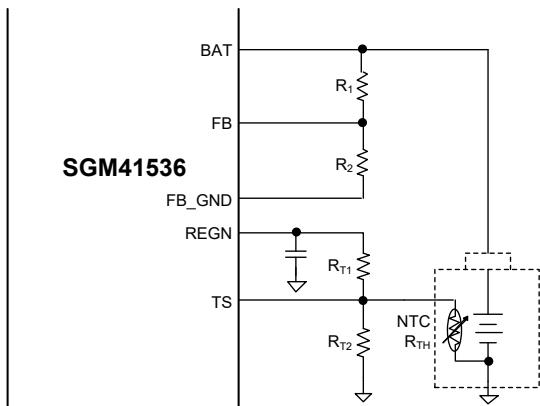


Figure 4. Battery Temperature Sensing Circuit

Charging Status Indicator (STAT)

Charging state is indicated with the open-drain STAT pin as explained in Table 2. This pin can drive a LED that is pulled up to REGN through a resistor.

Table 2. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charging complete	High (LED OFF)
Charging is disable or in HIZ mode and sleep mode	High (LED OFF)
Safety timer expiration with battery voltage above recharge threshold	High (LED OFF)
Charge is suspended due to TS cold/hot faults, VBUS_OVP, VBAT_OVP, ICHG pin faults, FB pin faults, thermal shutdown, and safety timer expiration with battery voltage below recharge threshold	Blinking at 1Hz with 50% duty cycle

Protections

Input Over-Voltage

If V_{VBUS} voltage exceeds $V_{VBUS_OVP_RISE}$, the converter switching will stop immediately and safety timer stops counting. Charger resumes normal operation when the input voltage drops back below $V_{VBUS_OVP_FALL} = V_{VBUS_OVP_RISE} - V_{VBUS_OVP_HYS}$. During V_{VBUS} OVP event, the REGN remains on and the STAT pin blinks.

Input Voltage Dynamic Power Management (VINDPM)

When the input current exceeds the current limit of the power source, the device will reduce the charge current to regulate PMID voltage and avoid crashing the power source. The VINDPM is programmed as $1.044 \times V_{BAT} + 125\text{mV}$ by dynamically tracking the battery voltage. And the actual VINDPM is clamped at V_{INDPM_MIN} at low battery voltage.

Input Current Limit

The device implements built-in input current limit and always monitors the input current. When the input current tending to

exceed the input current limit, the converter will reduce the charge current to keep the input current not exceed the limit.

Cycle-by-Cycle Current Limit

The cycle-by-cycle current limit (I_{HSFET_OCP}) is included in the device to limit the HSFET current. When the HSFET peak current triggers the current limit, the HSFET turns off immediately until the current drops below a threshold.

Thermal Regulation and Thermal Shutdown

The internal junction temperature (T_J) is constantly monitored to prevent overheating and limit the case temperature. If T_J intends to exceed T_{REG} , the device will reduce the charging current, keeping the maximum temperature within the T_{REG} (thermal regulation) limit. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the junction temperature exceeds T_{SHUT} , thermal shutdown protection arises in which the converter is turned off, meanwhile the safety timer stops counting. When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} , the converter and safety timer resume automatically.

Battery Protection

Battery Over-Voltage Protection

The over-voltage limit for the battery is about 104% (TYP) of the battery regulation voltage. The converter will immediately stop switching if a battery over-voltage occurs. During battery over-voltage event, the safety timer stops counting and STAT pin blinks, meanwhile a about 7mA pull-down current is on the BAT pin. And it resumes normal operation once the battery voltage falls below the falling threshold (typical 102% of the V_{BATREG}).

Battery Short-Circuit Protection

The device works in trickle charge phase and the charge current is decreased to I_{BAT_SHORT} if the V_{BAT} falls below the V_{BAT_SHORT} threshold.

ICHG Pin Open and Short Protection

When the ICHG pin is shorted to GND or open, the charger immediately turns off and STAT pin blinks. At power-up, if the ICHG pin is shorted to GND or open, the charge will not power up until the fault is cleared. The faults will be ignored in trickle charge phase.

FB Pin Open and Short Protection

When the FB pin is shorted to GND or floating, the charger will remain off until the fault is removed. And the fault is indicated by the STAT pin blinking.

DETAILED DESCRIPTION (continued)

Device Functional Modes

The device operates in different mode under the follow conditions, as shown in Table 3.

Table 3. Device Functional Modes

Device Mode	Conditions	REGN LDO	Charge Enabled	STAT Indicator
Disable Mode	Device is disabled (nEN = high when POL floating, nEN = low or floating when POL = GND)	Off	No	High
HIZ Mode	Device is enabled and $V_{VBUS} < V_{VBUS_UVLOZ}$	Off	No	High
Sleep Mode	Device is enabled, $V_{VBUS} > V_{VBUS_UVLOZ}$ and $V_{VBUS} < V_{BAT} + V_{SLEEPZ}$	Off	No	High
Charge Mode	Device is enabled, $V_{VBUS} > V_{VBUS_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$, no faults, charge is not terminated	On	Yes	Low
Charge Termination	Device is enabled, $V_{VBUS} > V_{VBUS_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$, no faults, charge is terminated	On	No	High
Fault Mode	VBUS_OVP, VBAT_OVP, TS cold/hot faults, thermal shutdown, safety timer fault, ICHG pin is open or short, FB pin is open or short	On	No	Blinking

APPLICATION INFORMATION

The SGM41536 is typically used as a 1-cell to 4-cell Buck batteries charger in a wide range of the input voltage. The charge voltage and current can be programmed by external resistors. The charge current is 3A (MAX) for 1-cell to 2-cell batteries and 2A (MAX) for 3-cell to 4-cell batteries.

The typical applications include a standalone charger without power path, a standalone charger with external power path and a charger with external MCU programmed charge current.

Typical Application

The typical standalone charger without power path for 1-cell to 4-cell batteries is shown in Figure 5.

Detailed Design Procedure

Charge Voltage Settings

The battery voltage is set by external divider resistors R_1 and R_2 . The battery charge voltage is programmed as $V_{BATREG} = 1.1 \times (1 + R_1/R_2)$. For 1-cell 4.2V battery, $R_1 = 56.2\text{k}\Omega$ and $R_2 = 20\text{k}\Omega$ are recommended. For 2-cell 8.4V battery, $R_1 = 133\text{k}\Omega$ and $R_2 = 20\text{k}\Omega$ are recommended. 1% or higher accuracy of resistors is recommended for R_1 and R_2 .

Charge Current Settings

The battery charge current is set by external resistor R_{ICHG} connected from ICHG pin to GND, which is expressed as below:

$$I_{ICHG} (\text{A}) = K_{ICHG} (A \times \Omega) / R_{ICHG} (\Omega) \quad (3)$$

K_{ICHG} is a coefficient that is listed in Electrical Characteristics table.

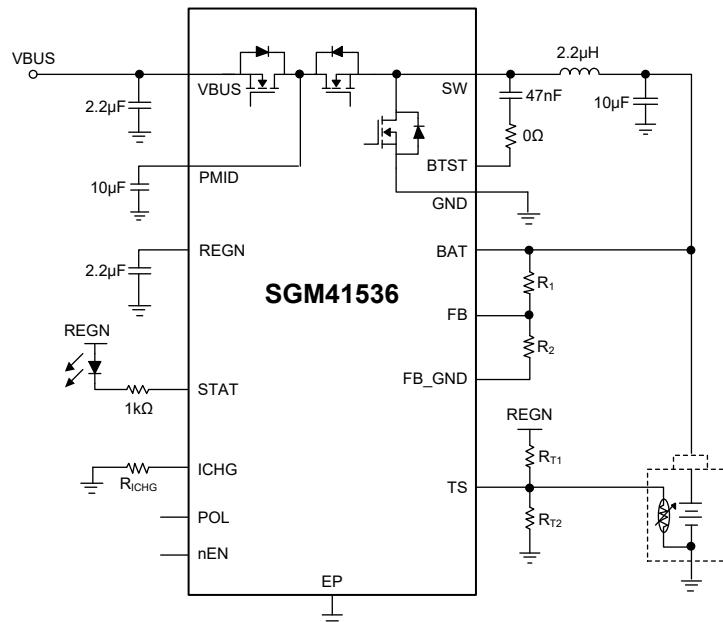


Figure 5. Typical Application Circuit without Power Path

APPLICATION INFORMATION (continued)

Input Capacitor Selection

The effective capacitance of VBUS and PMID should be enough to absorb the VBUS input switching ripple current.

The equation below shows the input capacitor RMS current I_{CIN} calculation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (6)$$

A high-quality low ESR ceramic capacitor (X5R or X7R or better dielectric grade) is recommended for input capacitor. The input capacitor voltage ripple can be calculated as follow:

$$\Delta V_{IN} = \frac{I_{CHG} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (7)$$

A 2.2μF ceramic capacitor of C_{VBUS} and a 10μF ceramic capacitor of C_{PMID} are recommended in typical application. And the voltage rating of the capacitor must be higher enough than the maximum input voltage level.

Output Capacitor Selection

The effective capacitance of output should be enough to absorb the inductor ripple current. The equation below shows the output capacitor RMS current I_{COUT} calculation:

$$I_{COUT} = \frac{\Delta I_L}{2 \times \sqrt{3}} \quad (8)$$

And the output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} \quad (9)$$

A 10μF ceramic capacitor with X5R or X7R or better dielectric grade is recommended, and the voltage rating of the capacitor must be higher enough than the fully charged battery voltage.

Typical Application with External Power Path

If the system needs to be powered up immediately from VBUS when the battery is over-discharged or dead, the application circuit in Figure 6 can be used. Q4 is an external P-MOSFET connected from system to battery. When the VBUS is removed, Q4 is turned on to power up V_{SYS} from V_{BAT} . When the VBUS is plugged in, the V_{SYS} is powered up from PMID.

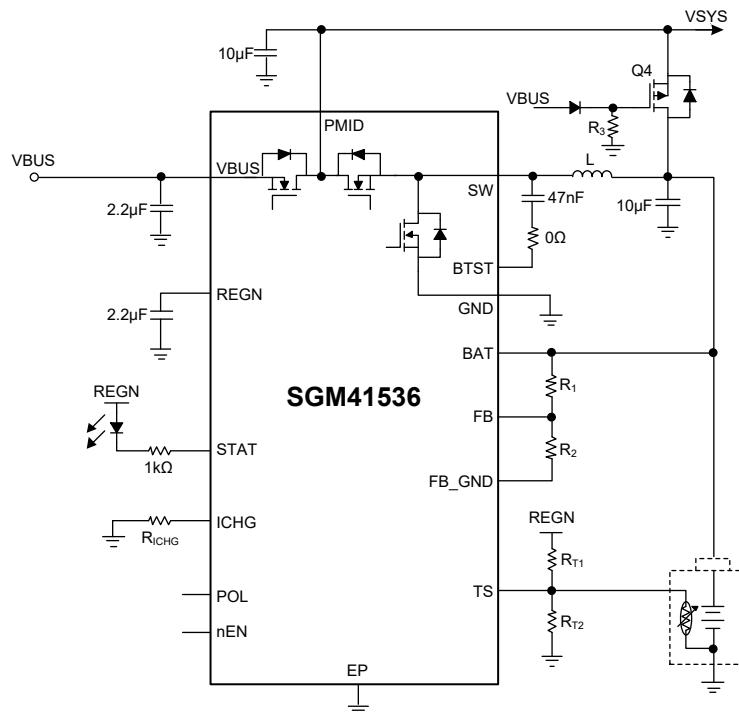


Figure 6. Typical Application Circuit with Power Path

APPLICATION INFORMATION (continued)

Typical Application with MCU Programmable Charge Current

The charge current also can be programmed by external MCU control signal in some cases. The charge current setting resistors R_{ICHG1} and R_{ICHG2} can be connected or disconnected by GPIO signal on/off as shown in Figure 7. Three-level charge current can be programmed with GPIO1 and GPIO2.

If the charge current needs to be controlled smoothly in a wide range, an average DC voltage can be generated by PWM signal to control the charge current. The charge current can be calculated as $K_{ICHG} (1V - V_{PWM})/(R_{ICHG1} + R_{ICHG2})$ and the application circuit is shown in Figure 8. V_{PWM} is average DC voltage of PWM signal output and 1V is the ICHG pin regulated voltage.

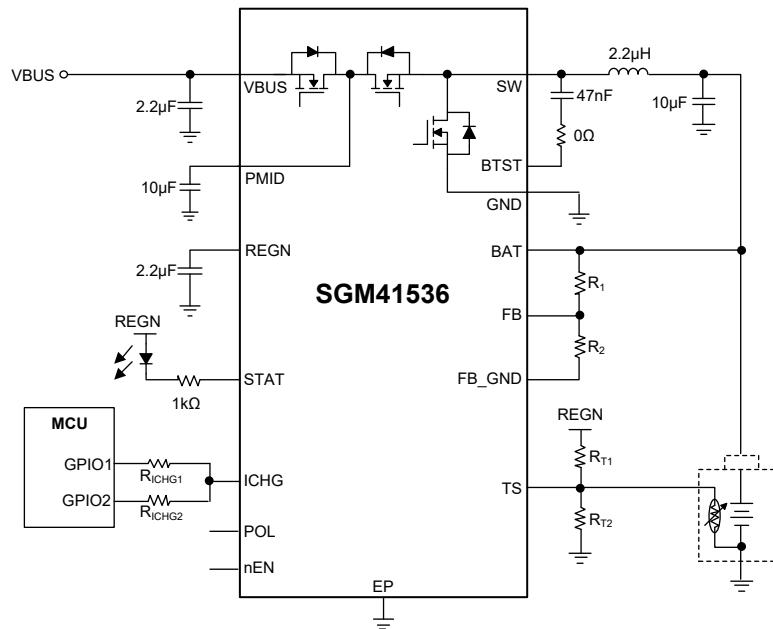


Figure 7. Typical Application Circuit with MCU Programmed Charge Current (GPIO Signal)

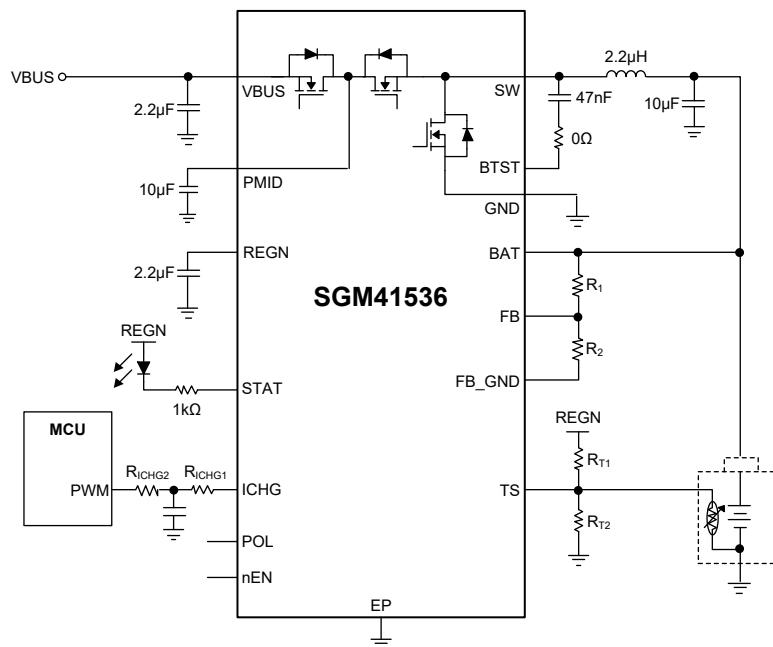


Figure 8. Typical Application Circuit with MCU Programmed Charge Current (PWM Signal)

APPLICATION INFORMATION (continued)

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.2MHz) due to sharp rise and fall of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. The following considerations can help to make a better layout.

1. Place the input capacitor between PMID and GND pins as close as possible to the chip with the shortest copper connections (avoid vias). Choose the smallest capacitor size.
2. Place the output capacitor as close as possible to BAT pin. The capacitors ground pins need to be connected to the IC ground with GND plane or short copper trace connections.
3. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection

should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin).
5. Place decoupling capacitors close to the IC pins with the shortest possible copper connections.
6. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.
7. Select proper sizes for the vias and ensure enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.
8. Route the battery feedback signal FB away from SW node.

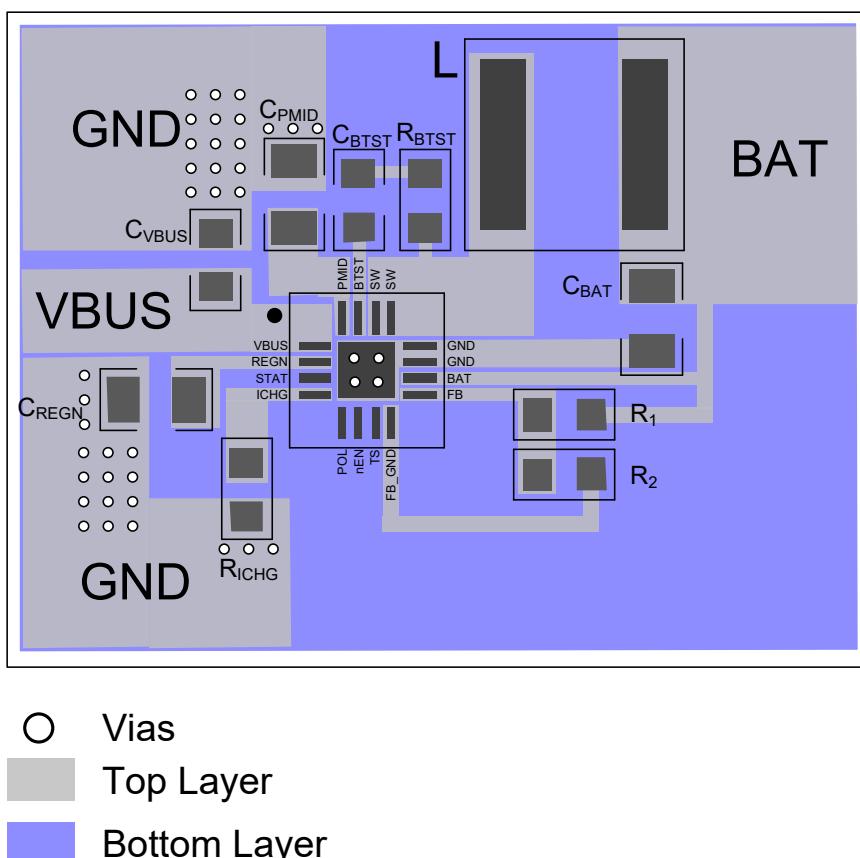


Figure 9. Layout Example

REVISION HISTORY

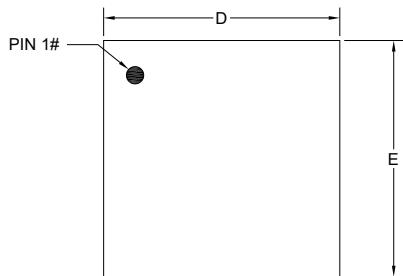
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data.....	All

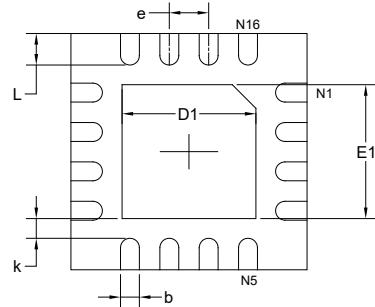
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

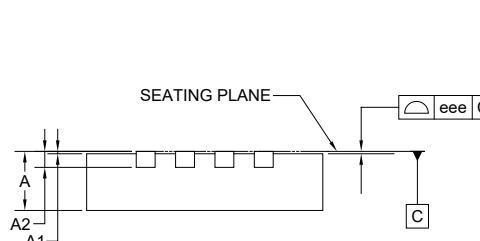
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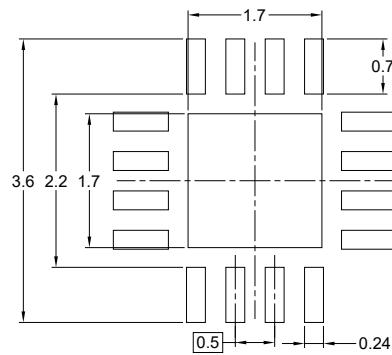
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

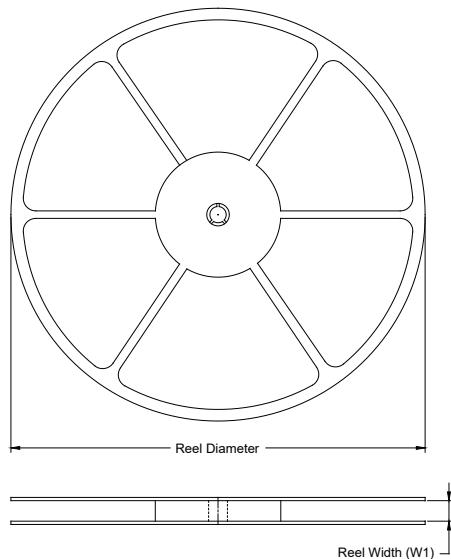
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020
eee	0.080		0.003	

NOTE: This drawing is subject to change without notice.

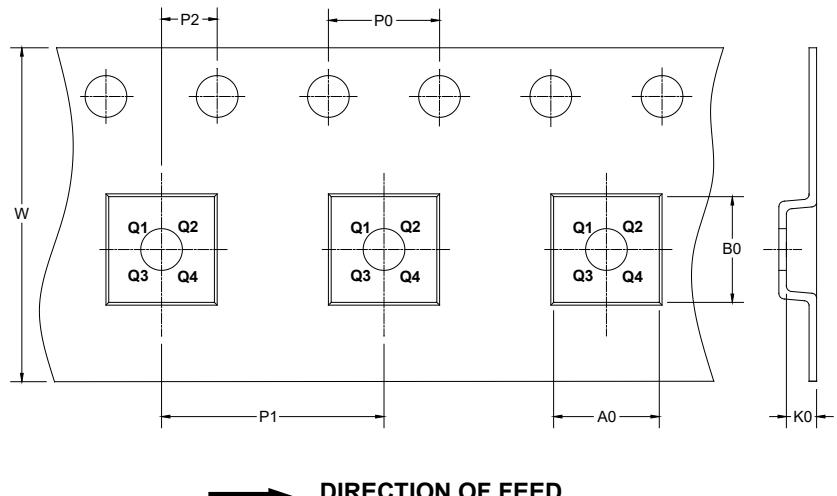
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



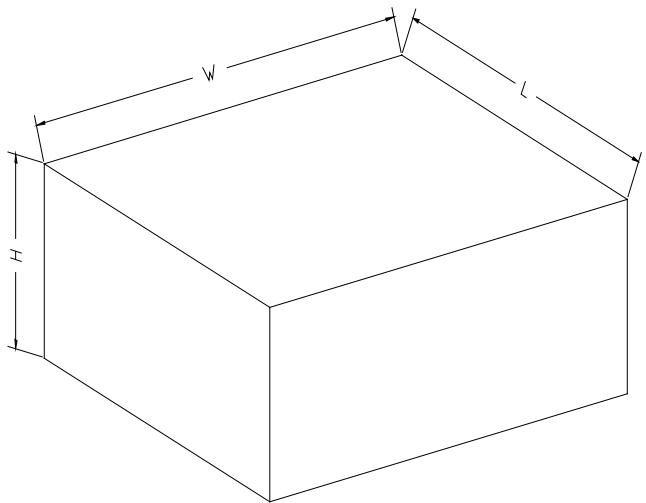
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3x3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002