SGM6620/SGM6620A
25V, 20A Synchronous Boost Converter with Stackable Multi-Phase Function

GENERAL DESCRIPTION

The SGM6620 family is a 20A valley switch current limit synchronous Boost converter designed for high power applications. The device integrates a 9.8mΩ (TYP) high-side MOSFET to maximize the efficiency and reduce overall solution size for portable applications. To further maximize the power density, the SGM6620 family supports daisy chain operation.

The device supports a wide input voltage range from 2.05V to 23V, which is suitable for various input source such as single-cell or multi-cell Lithium batteries, or USB PD3.0 input voltage range up to 20V. The SGM6620 family supports a wide programmable output voltage range from 4.5V to 25V.

The SGM6620 family uses adaptive constant on-time valley current control topology to regulate the output voltage. The device offers operation mode selection via the MODE pin. Configuring to auto PFM mode, the device consumes minimal current at light load, and automatically switches to pulse width modulation (PWM) mode in moderate to heavy load condition. Configuring to forced PWM (FPWM) mode, the device operates in PWM mode across the entire load range to maintain consistent output voltage ripple for noise sensitive applications. The switching frequency in the PWM mode is 290kHz (TYP) for SGM6620 family. The SGM6620A offers light load ultrasonic mode to clamp the PFM frequency above 30kHz (TYP). The SGM6620 family offers the flexibility to select the main low-side power FET. The device integrates an internal gate driver with 500mA sourcing current and 1A sinking current capability.

The device also integrates various protection features, such as output over-voltage protection (OVP), cycle-by-cycle over-current protection (OCP), and thermal shutdown.

The SGM6620 family is available in a Green TQFN-2.5×3-14AL package.

FEATURES

- **Wide Input Voltage Range: 2.05V to 23V**
- **Wide Output Voltage Range: 4.5V to 25V**
- **2.35V Minimum Input Voltage for Start-up**
- **10A to 20A (TYP) Programmable Valley Current Limit**
- **Device Variant:**
  - **SGM6620: 290kHz (TYP) Switching Frequency**
  - **SGM6620A: 30kHz (TYP) Switching Frequency with Ultrasonic Mode**
- **9.8mΩ (TYP) Integrated High-side FET**
- **Stackable Multi-Phase for High Output Current**
- **Synchronize to External Clock**
- **Precise EN/UVLO Threshold**
- **External Loop Compensation**
- **Protection Features:**
  - **Output Over-Voltage Protection**
  - **Cycle-by-Cycle Over-Current Protection**
  - **Thermal Shutdown**
- **Available in a Green TQFN-2.5×3-14AL Package**

APPLICATIONS

USB Type-C Power Supply
Smart Speakers

SIMPLIFIED SCHEMATIC

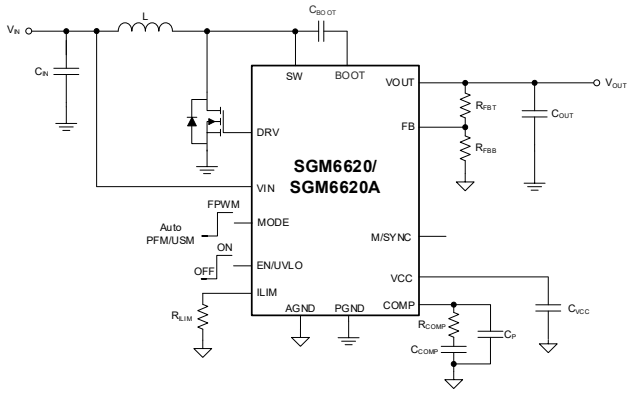


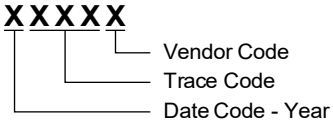
Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6620	TQFN-2.5×3-14AL	-40℃ to +125℃	SGM6620XTWP14G/TR	6620 TWP14 XXXXX	Tape and Reel, 5000
SGM6620A	TQFN-2.5×3-14AL	-40℃ to +125℃	SGM6620AXTWP14G/TR	1WJ TWP14 XXXXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN ..... -0.3V to 30V
EN/UVLO ..... -0.3V to 27V
SW, VOUT ..... -0.3V to 32V
BOOT ..... V_{SW} - 0.3V to V_{SW} + 6V
M/SYNC, MODE, VCC, COMP, FB, DRV, ILIM ... -0.3V to 6V
Package Thermal Resistance
TQFN-2.5×3-14AL, θ_{JA} ..... 56.1℃/W
TQFN-2.5×3-14AL, θ_{JB} ..... 5.6℃/W
TQFN-2.5×3-14AL, θ_{JC} ..... 39.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.05V to 23V
Output Voltage Range, V_{OUT} ..... 4.5V to 25V
Effective Inductance Range, L .... 1μH to 4.7μH, 2.2μH (TYP)
Effective Input Capacitance Range, C_{IN}
..... 4.7μF to 22μF (TYP)
Effective Output Capacitance Range, C_{OUT}
..... 10μF to 1000μF, 100μF (TYP)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

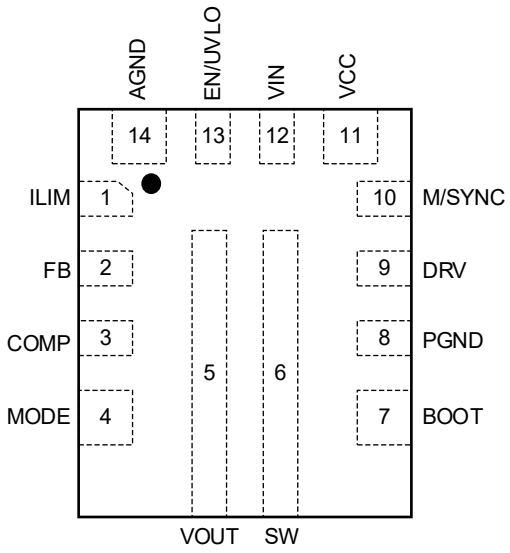
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-2.5×3-14AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	ILIM	I	Inductor Valley Current Limit Setting Pin. Connect an external resistor between this pin and the AGND pin.
2	FB	I	Voltage Feedback Pin. Use a resistor divider to set the desired output voltage.
3	COMP	O	Output of the Internal Trans-Conductance Error Amplifier. An external RC network is connected to this pin to optimize the loop stability and response time.
4	MODE	I	Mode Selection Pin. MODE = high, forced PWM. MODE = low, auto PFM, ultrasonic mode (SGM6620A), this pin must not leave floating.
5	VOUT	P	Boost Converter Output. VOUT pin is connected to the drain of the high-side MOSFET.
6	SW	P	Switch Node Pin. Connect to the drain of external low-side MOSFET and the source of the internal high-side MOSFET.
7	BOOT	O	Power Supply for the High-side MOSFET Gate Driver. A ceramic capacitor with a capacitance ranging from 0.1μF to 1μF must be connected between the BOOT pin and the SW pin.
8	PGND	G	Power Ground. Ground of low-side MOSFET.
9	DRV	O	Driver Pin. Gate driver output for low-side MOSFET.
10	M/SYNC	I	Internal or External Clock. When this pin is grounded, the device will operate at the switching frequency set internally. The switching frequency of the device is forced to set to the frequency of the external clock, when an effective clock signal is applied to this pin.
11	VCC	O	Output of the Internal Regulator. Connect a ceramic capacitor (> 2.2μF) between this pin and ground.
12	VIN	P	Power Supply Pin.
13	EN/UVLO	I	Enable Input and Under-Voltage Lockout Pin. When sets to logic high, the device is enabled. When sets to logic low, the device is disabled and turns into shutdown mode. Connecting this pin to VIN through a resistor divider can program the start-up and shutdown levels of the device.
14	AGND	G	Analog Ground.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 3.6V and V_{OUT} = 24V. All typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Input Voltage Range	V_{IN}			2.05		23	V
VIN UVLO Threshold	V_{IN_UVLO}	V_{IN} rising			2.2	2.35	V
		V_{IN} falling			1.9	2.05	
VIN UVLO Hysteresis	V_{IN_HYS}				0.3		V
Output Voltage Range	V_{OUT}			4.5		25	V
Quiescent Current	I_Q	T_J = -40℃ to +85℃, EN = high, no switching, 2.35V < V_{IN} < 23V, V_{OUT} > 1.1V_{IN}	VIN Pin		0.2	2.1	μA
			VOUT Pin		100	180	
Shutdown Current into VIN Pin	I_{SD}	T_J = -40℃ to +85℃, EN = low, no switching, 2.35V < V_{IN} < 23V			0.6	8	μA
VCC Regulated Voltage	V_{CC}	I_{VCC} = 30mA, V_{IN} = 6V, V_{OUT} = 20V			5		V
VCC UVLO Threshold	V_{CC_UVLO}	V_{CC} rising			1.95		V
		V_{CC} falling			1.8		V
EN/UVLO							
EN Logic High Threshold	V_{EN_H}	V_{CC} = 5.0V				1.15	V
EN Logic Low Threshold (Falling)	V_{EN_L}	V_{CC} = 5.0V		0.4			V
UVLO Rising Threshold at the EN/UVLO Pin	V_{UVLO}	V_{CC} = 5.0V		1.17	1.23	1.29	V
Sourcing Current at the EN/UVLO Pin	I_{UVLO_HYS}	$V_{EN/UVLO}$ = 1.3V			5.1		μA
Output							
Reference Voltage at the FB Pin	V_{REF}	PWM mode		0.985	1.0	1.015	V
Output Over-Voltage Protection Threshold	V_{OVP}	V_{OVP} rising		25.3	26.5	27.7	V
Output Over-Voltage Protection Hysteresis	V_{OVP_HYS}				1		V
Leakage Current into FB Pin	I_{FB_LKG}					50	nA
Shutdown Current into VOUT Pin	I_{OUT_SD}	T_J = -40℃ to +85℃, IC disabled, V_{OUT} = 2.35V to 25V, V_{IN} = 0V			7.6	12.7	μA
Power Switch							
High-side MOSFET On-Resistance	R_{DSON}	V_{CC} = 5.0V			9.8		mΩ
Switching Frequency	f_{SW}	SGM6620 PWM mode, V_{IN} = 3.6V, V_{OUT} = 18V			290		kHz
Ultrasonic Mode Switching Frequency	f_{USM}	SGM6620A			30		kHz
Minimum Off-Time in Boost Mode	t_{OFF_MIN}				170		ns
Minimum On-Time in Boost Mode	t_{ON_MIN}				180		ns
Low-side Gate off to High-side Gate on Deadtime	t_{DLH}				30		ns
High-side Gate off to Low-side Gate on Deadtime	t_{DHL}				11		ns
Valley Current Limit	I_{LIM}	R_{ILIM} = 20kΩ, auto PFM mode		17	20	23.5	A

ELECTRICAL CHARACTERISTICS (continued)

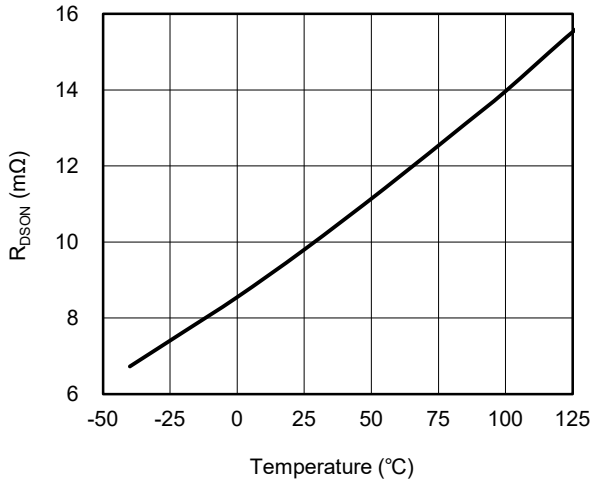
(T_J = -40℃ to +125℃, V_{IN} = 3.6V and V_{OUT} = 24V. All typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier						
Sink Current into COMP Pin	I_{SINK}	V_{FB} = V_{REF} + 400mV, V_{COMP} = 1.5V, V_{CC} = 5.0V		20		μA
Source Current into COMP Pin	I_{SOURCE}	V_{FB} = V_{REF} - 400mV, V_{COMP} = 1.5V, V_{CC} = 5.0V		20		μA
High Clamp Voltage at the COMP Pin	V_{CCLP_H}			1.8		V
Low Clamp Voltage at the COMP Pin	V_{CCLP_L}			0.6		V
Error Amplifier Transconductance	G_{EA}	V_{CC} = 5.0V		190		μA/V
Soft-Start						
Soft-Start Time of Internal Reference Voltage Ramping from 0 to V_{REF}	t_{SS}			7.5		ms
Synchronous Clock						
M/SYNC Logic High Threshold	$V_{M/SYNC\_H}$	V_{CC} = 5.0V			1.2	V
M/SYNC Logic Low Threshold (Falling)	$V_{M/SYNC\_L}$	V_{CC} = 5.0V	0.4			V
Minimum Sync Clock Pulse Width	t_{SYNC_MIN}		50			ns
Logic Interface						
MODE Logic High Threshold	V_{MODE_H}	V_{CC} = 5.0V			1.2	V
MODE Logic Low Threshold	V_{MODE_L}	V_{CC} = 5.0V	0.4			V
Thermal Shutdown	T_{SD}	T_J rising		160		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			20		℃

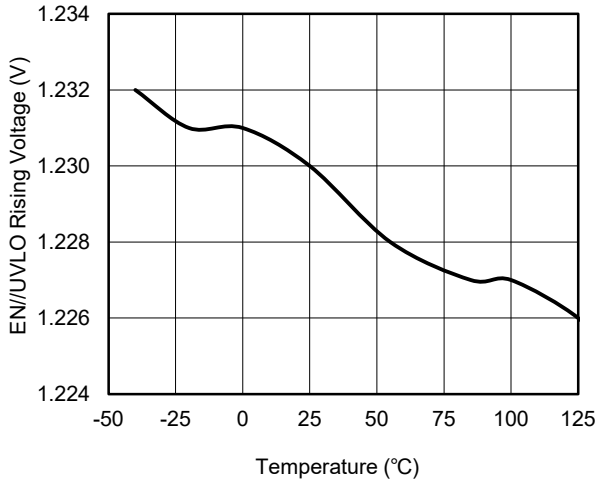
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, f_{SW}= 290kHz, unless otherwise noted.

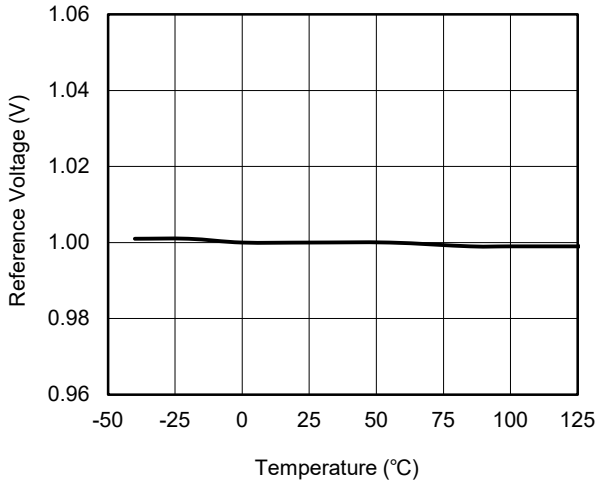
High-side MOSFET R_{DSON} vs. Temperature



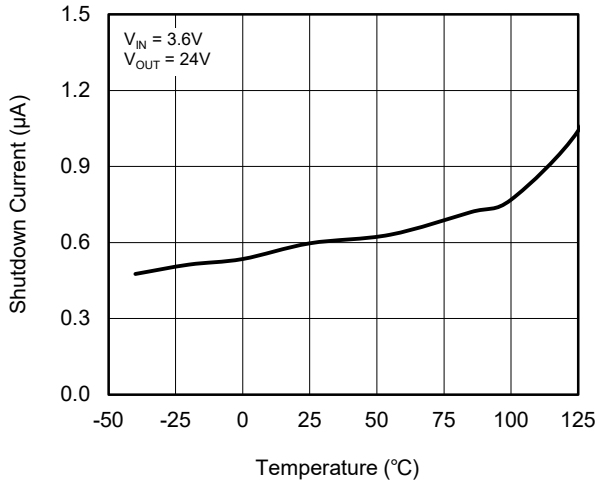
EN/UVLO Rising Voltage vs. Temperature



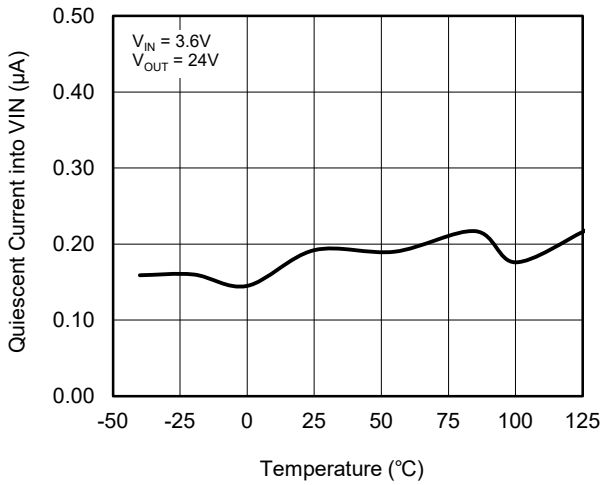
Reference Voltage vs. Temperature



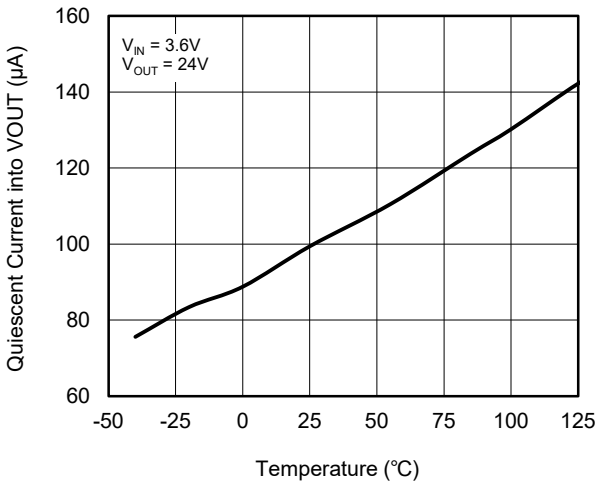
Shutdown Current vs. Temperature



Quiescent Current into VIN vs. Temperature



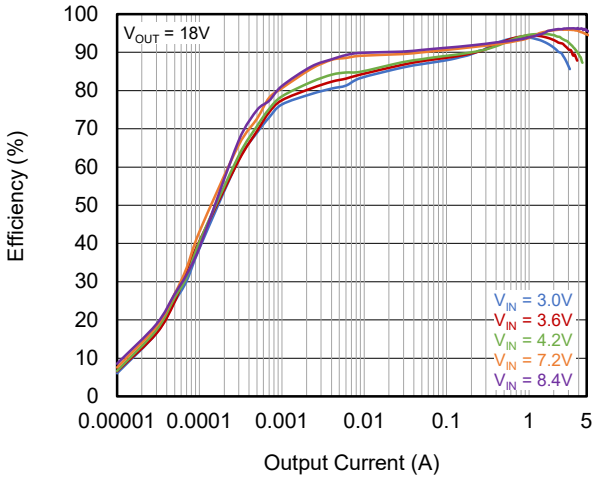
Quiescent Current into VOUT vs. Temperature



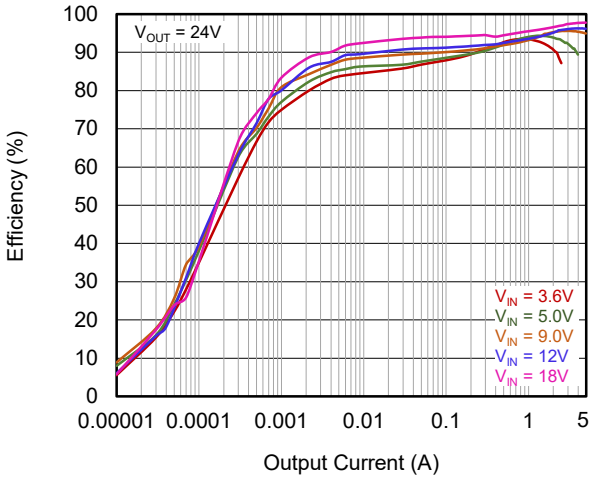
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, f_{SW}= 290kHz, unless otherwise noted.

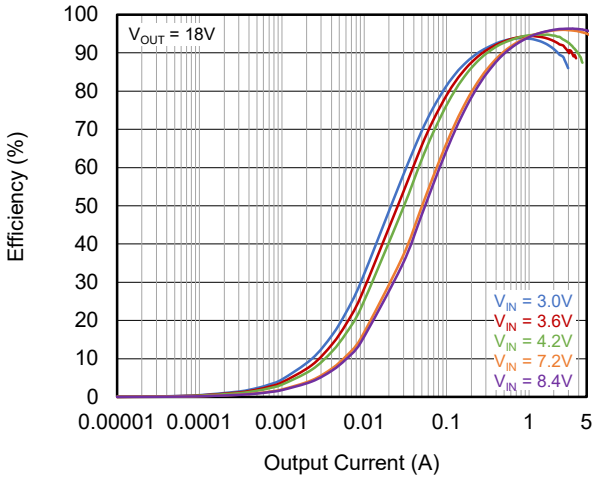
Efficiency vs. Output Current (Auto PFM Mode)



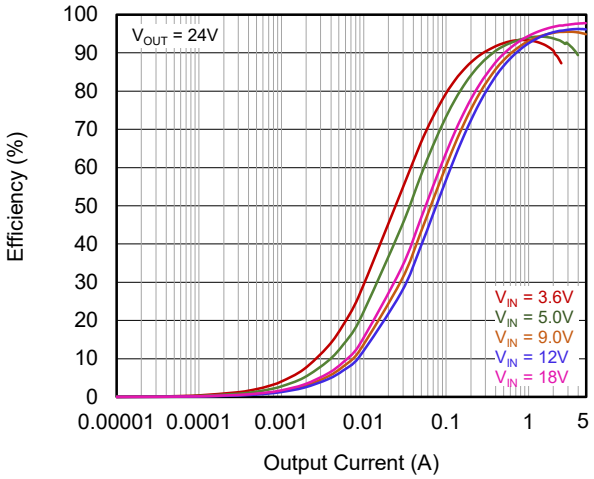
Efficiency vs. Output Current (Auto PFM Mode)



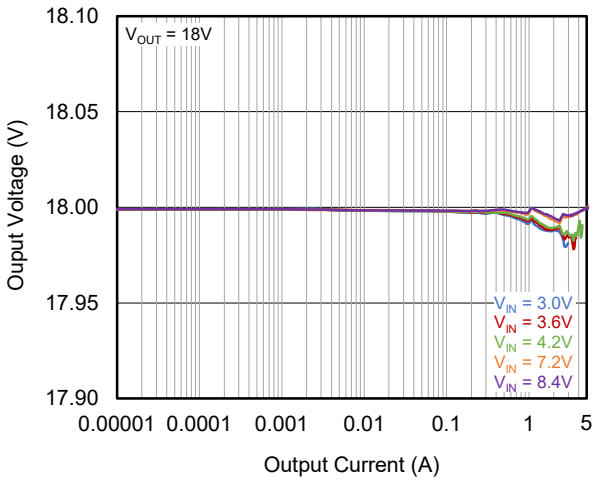
Efficiency vs. Output Current (FPWM Mode)



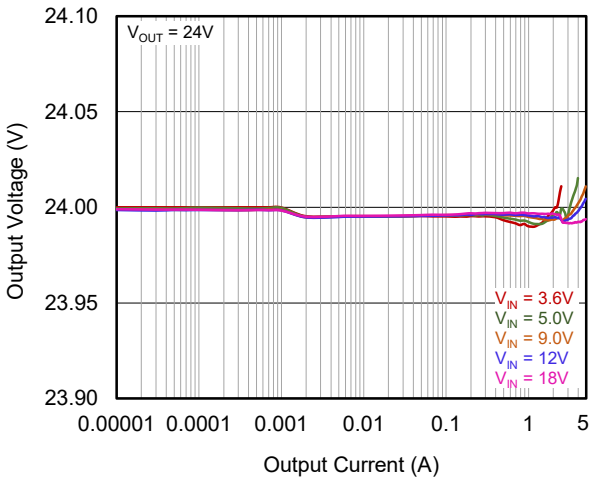
Efficiency vs. Output Current (FPWM Mode)



Output Voltage vs. Output Current (FPWM Mode)



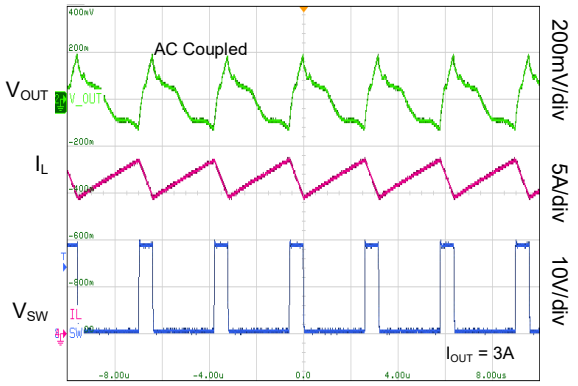
Output Voltage vs. Output Current (FPWM Mode)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

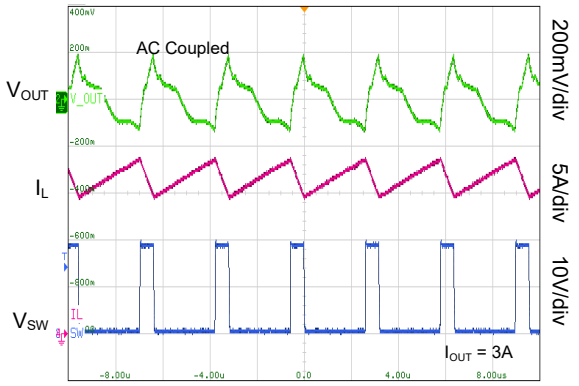
T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 18V, unless otherwise noted.

PFM Mode



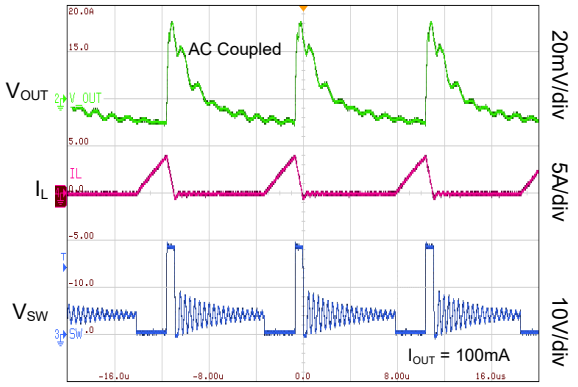
Time (2μs/div)

FPWM Mode



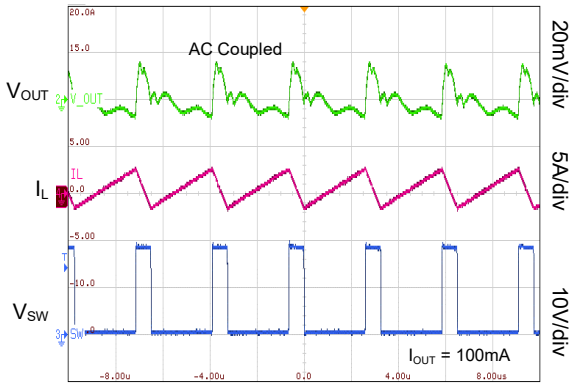
Time (2μs/div)

PFM Mode



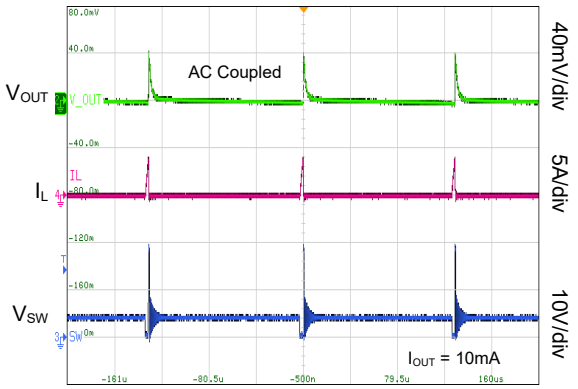
Time (4μs/div)

FPWM Mode



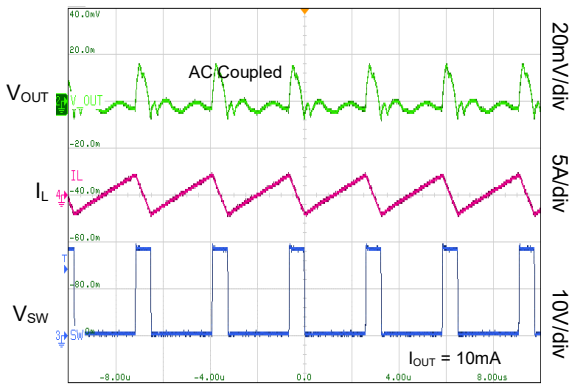
Time (2μs/div)

PFM Mode



Time (40μs/div)

FPWM Mode

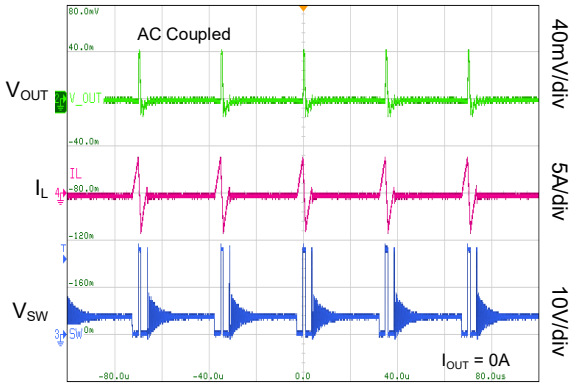


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

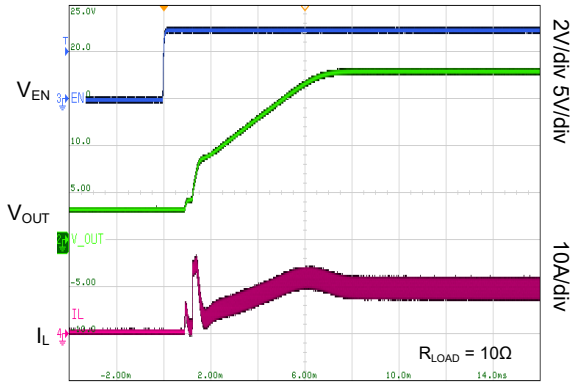
T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 18V, unless otherwise noted.

USM Mode



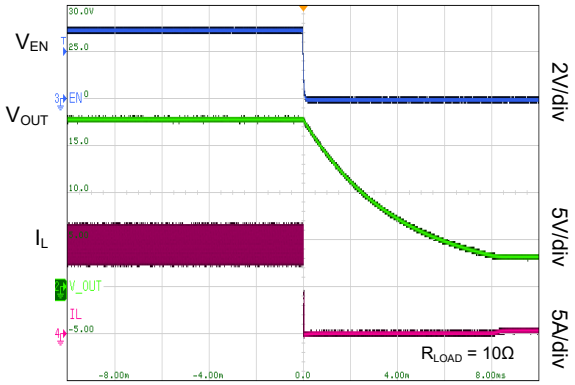
Time (20μs/div)

Start-up



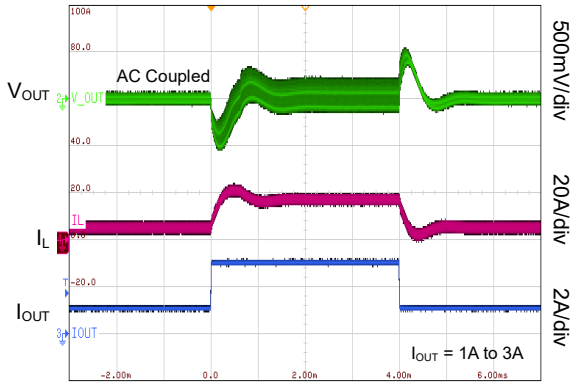
Time (2ms/div)

Shut-down



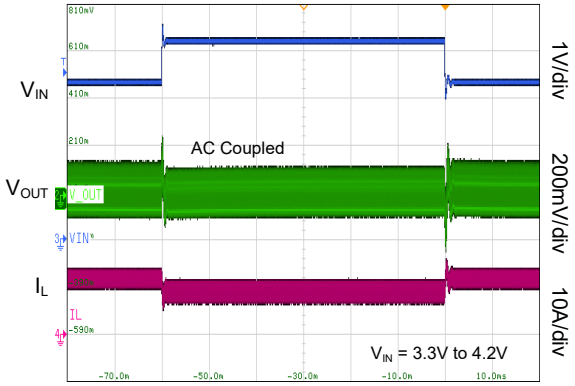
Time (2ms/div)

Load Transient



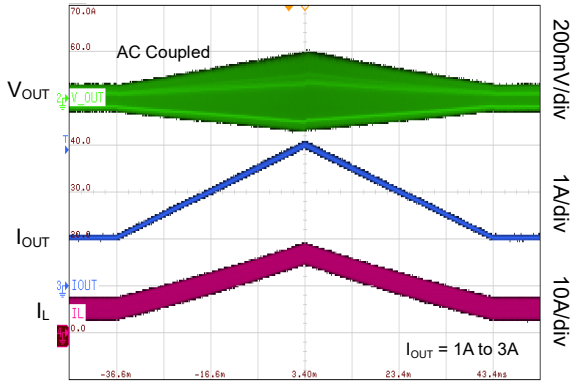
Time (1ms/div)

Line Transient



Time (10ms/div)

Load Sweep

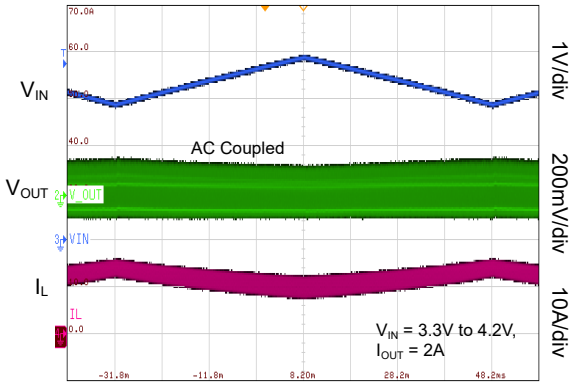


Time (10ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 18V, unless otherwise noted.

Line Sweep



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

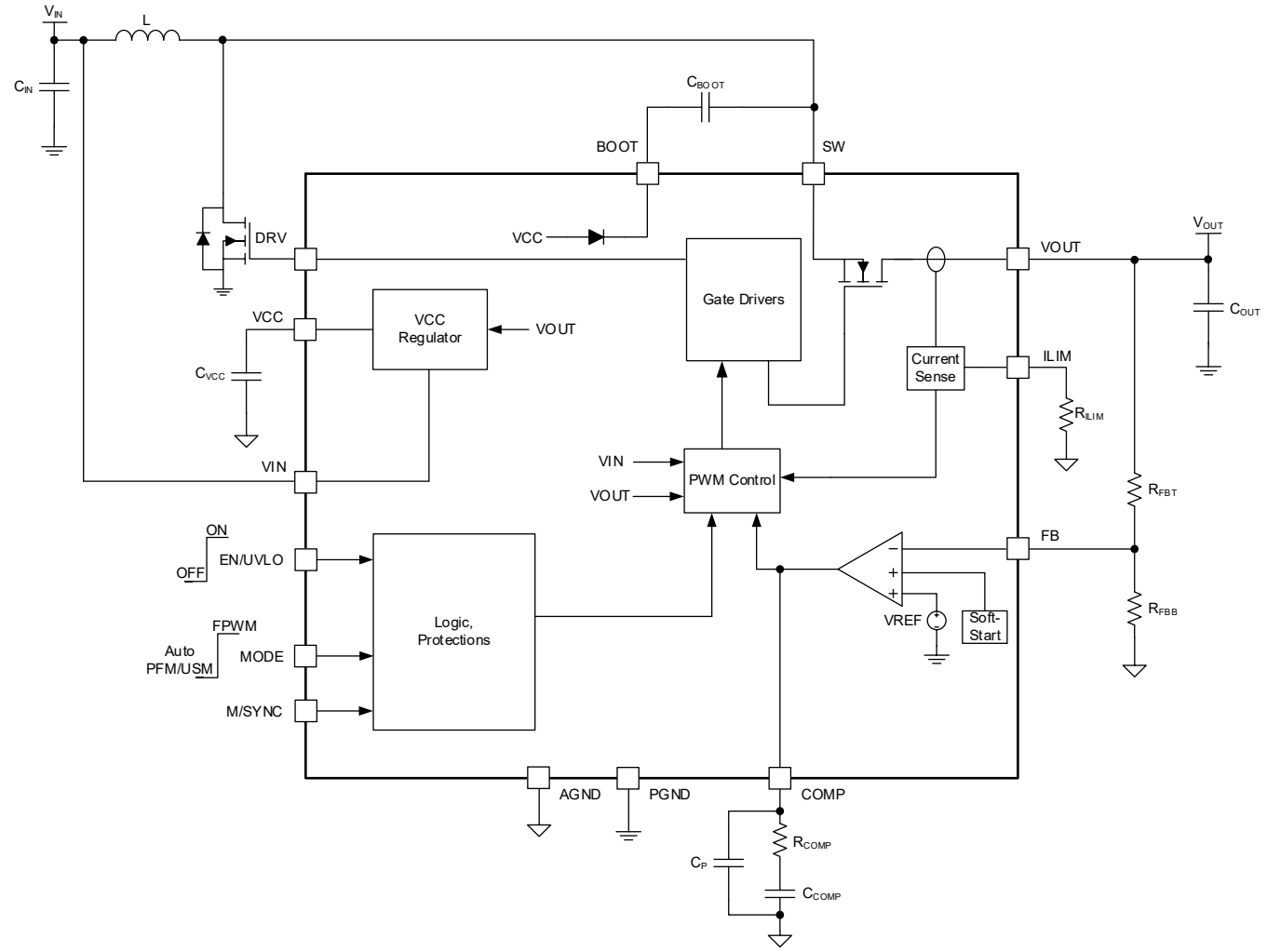


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6620 family is a high-power density, synchronous Boost converter with a 9.8mΩ (TYP) high-side MOSFET integrated to provide a high efficiency and small size solution in portable systems. The device is capable of providing an output voltage up to 25V and delivering up to 60W power from a single cell Lithium battery and 100W power from two cells Lithium batteries.

The SGM6620 family uses adaptive constant on-time valley current control topology to regulate the output voltage. In the moderate-to-heavy load condition, the SGM6620 family operates in the quasi-constant frequency pulse width modulation (PWM) mode. As conventional adaptive on-time converters, the SGM6620 family varies the on-time as a function of input and output voltage to maintain a nearly constant frequency of 290kHz (TYP). In light load condition, the device has two operation modes selected by the MODE pin. One is the pulse frequency modulation (PFM) mode, which is used to enhance efficiency under light load conditions. The other is the forced pulse width modulation (FPWM) mode, which is employed to avoid application issues arising from low switching frequency. SGM6620A offers ultrasonic mode by pulling MODE pin to logic low. Ultrasonic mode clamps the light load frequency above 30kHz (TYP), as the load increases, the load requires switching frequency above 30kHz, and the device automatically increases the PFM switching frequency. The SGM6620 family implements the cycle-by-cycle current limit to protect the device from overload conditions during Boost switching. The switch valley current limit is up to 20A (TYP). The SGM6620 family uses external loop compensation, which provides flexibility to use different inductors and output capacitors. This adaptive constant on-time valley current control scheme can achieve outstanding transient line response and load response with the requirements of small output capacitance.

To further maximize the power density, the SGM6620 family can support stackable multi-phase operation. A stackable dual-phase converter can be achieved by two SGM6620/A devices. Up to 4 pcs, SGM6620/A can be connected in parallel to meet higher power requirements. The multi-phase operation significantly reduces the peak value of the inductor current and capacitor ripple current, and increases the effective switching frequency, thereby minimizing the size of the inductor and capacitor to the greatest extent.

Feature Description

Under-Voltage Lockout (UVLO)

The SGM6620 family integrates UVLO feature to protect the device from malfunction when the input voltage is insufficient and prevent the battery from over-discharging. The SGM6620 has two functions: V_{IN_UVLO} and V_{CC_UVLO}. This lockout function causes the device to stop operating when the voltage at the VIN pin drops below the falling UVLO threshold, which is 1.9V (TYP). When the voltage of the VIN pin rises over the rising UVLO threshold 2.2V (TYP), the device starts to operate. The VCC pin also implements UVLO function. The device is disabled when V_{CC} drops below the UVLO threshold (V_{CC_UVLO}), which is 1.8V (TYP).

Enable and Programmable UVLO

The SGM6620/A has a dual-function enable and under-voltage lockout (UVLO) circuit. When the voltage at the VIN pin is higher than the input UVLO rising threshold of 2.2V (TYP) and the voltage at the EN/UVLO pin is higher than 1.15V (MAX) but lower than the enable UVLO threshold of 1.23V (TYP), the device will be enabled but remains in standby mode.

A precise UVLO voltage threshold is implemented at the EN/UVLO pin, so it can support programmable input under-voltage lockout with hysteresis. When the voltage at the EN/UVLO pin is above the UVLO threshold of 1.23V (TYP), the device is enabled. A hysteresis current (I_{UVLO_HYS}) which is sourced from the EN/UVLO pin can provide hysteresis function. It can prevent on/off chattering when the input voltage changes slowly with noise.

As shown in Figure 3, when using a resistor divider circuit, the turn-on threshold can be calculated by Equation 1.

$$V_{IN\_UVLO\_ON} = V_{UVLO} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

where, V_{UVLO} is the UVLO threshold at the EN/UVLO pin.

DETAILED DESCRIPTION (continued)

The hysteresis of UVLO is set by the resistor between the EN/UVLO pin and VIN pin, which is given by the Equation 2.

$$\Delta V_{IN\_UVLO} = I_{UVLO\_HYS} \times R_1 \quad (2)$$

where, I_{UVLO_HYS} (5.1μA, TYP) is the current sourced out of the EN/UVLO pin when the EN/UVLO voltage is above V_{UVLO}.

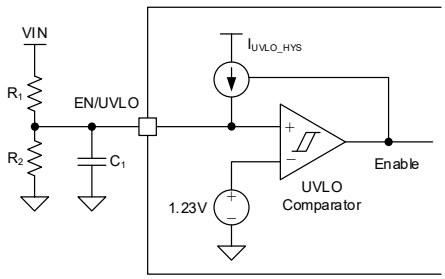


Figure 3. Programmable UVLO with Resistor Divider Circuit

By combining NMOSFET with a resistor divider, the logic enable and programmable UVLO functions can be achieved, as shown in Figure 4. The logic high-level of EN pin must exceed the sum of the enable threshold and the V_{TH} of the NMOSFET Q1. The Q1 brings about a benefit which can eliminate the leakage current from VIN to ground through the UVLO resistor divider circuit during the shutdown mode.

When EN voltage is below 0.4V, the device is disabled.

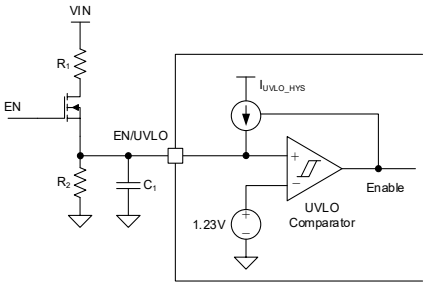


Figure 4. Logic Enable and Programmable UVLO

Enable and Start-up

The SGM6620 family has a 7.5ms (TYP) soft-start function, which can reduce inrush current during start-up. When the input voltage is valid, pulling the EN input to logic high, a constant current will charge the internal soft-start capacitor. During this period, the voltage of the capacitor will be compared with the internal reference (1.0V, TYP). The lower voltage will be input to the positive input terminal of the internal error amplifier. The output of the error amplifier (which determines the inductor valley current value) will gradually increase as the voltage of the soft-start capacitor rises. The soft-start stage is finished when the voltage of the soft-start capacitor exceeds the internal reference voltage. Pulling the EN input to logic low, the soft-start capacitor voltage will be discharged to ground.

Switching Frequency and External Clock Synchronization

The SGM6620 switches at a quasi-constant 290kHz (TYP) frequency. The SGM6620 family can synchronize with an external clock signal, which is input through the M/SYNC pin. It is suitable for applications that are sensitive to noise or involved in multiple phases. The operating switching frequency will be forced to the external clock when an external clock signal is applied to the M/SYNC pin. The external clock frequency must be within ±20% of default switching frequency, otherwise, the synchronization will fail. The external clock applied to the M/SYNC pin must meet the following requirements: the low-level voltage must be lower than 0.4V, and the high-level voltage must be higher than 1.15V. A clock signal over 50ns wide can be valid and before synchronization, the signal must have a minimum of 4 consecutive clocks.

DETAILED DESCRIPTION (continued)

Stackable Multi-Phase Operation

The stackable multi-phase operation can be supported by SGM6620 family. Two devices can realize a master/slave stackable converter. The master device M/SYNC pin should be grounded. The slave device M/SYNC pin should be connected to the drive signal of the external low-side MOSFET of the master device. Figure 5 shows the 2 pcs SGM6620/A stackable configuration. Considering for current balance and reliable phase shifting, forced PWM mode is recommended.

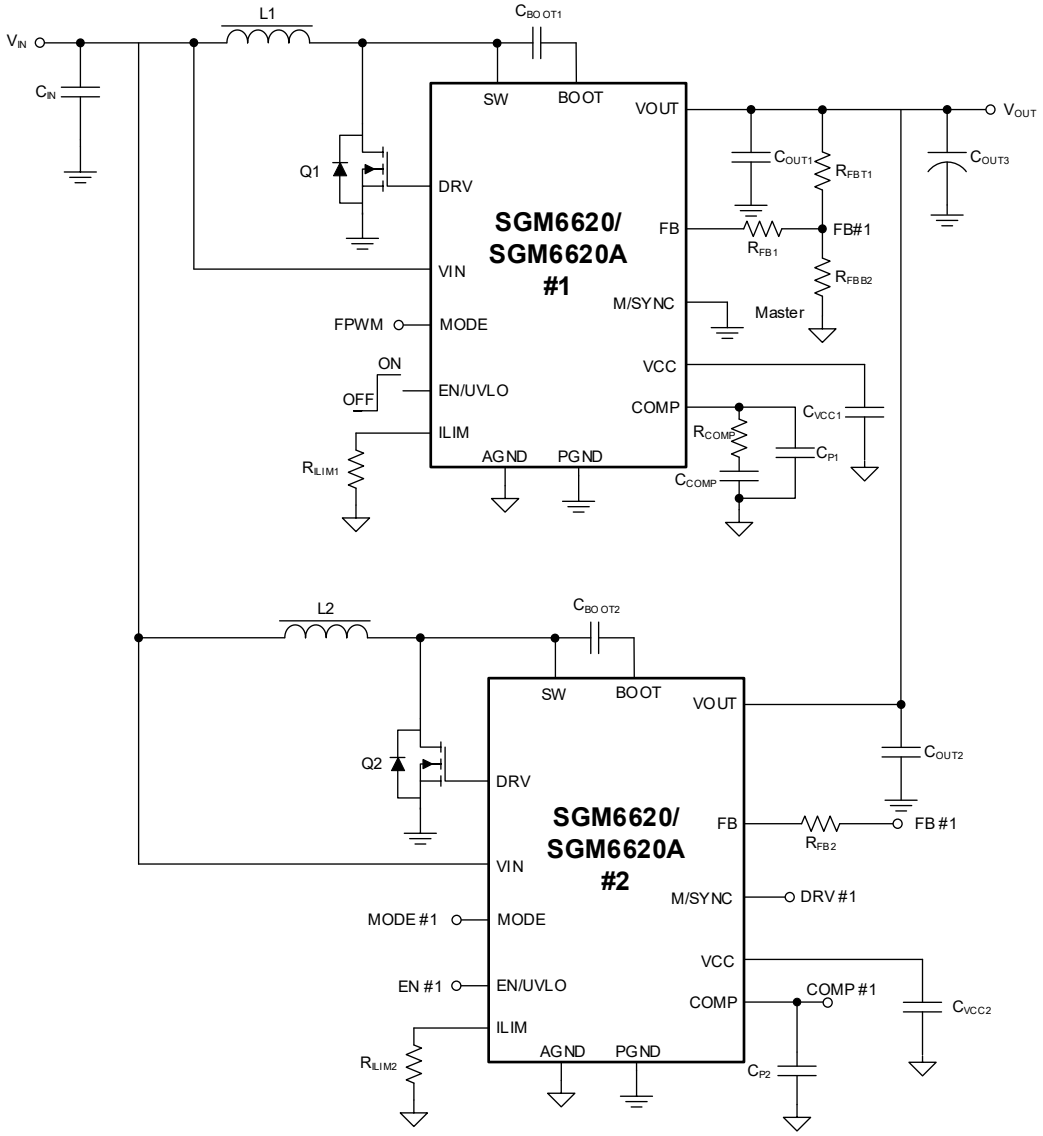


Figure 5. Dual-Phase Operation for High Power Application

DETAILED DESCRIPTION (continued)

Moreover, up to 4 pcs SGM6620/A can be connected in parallel for multi-phase operation at same switching frequency to meet higher power requirements. The multi-phase operation can significantly reduce the peak inductor current and capacitor ripple current, and increases the effective switching frequency, thereby minimizing the size of the inductor and capacitor to the greatest extent. Figure 6 shows the 4 pcs SGM6620/A stackable configuration.

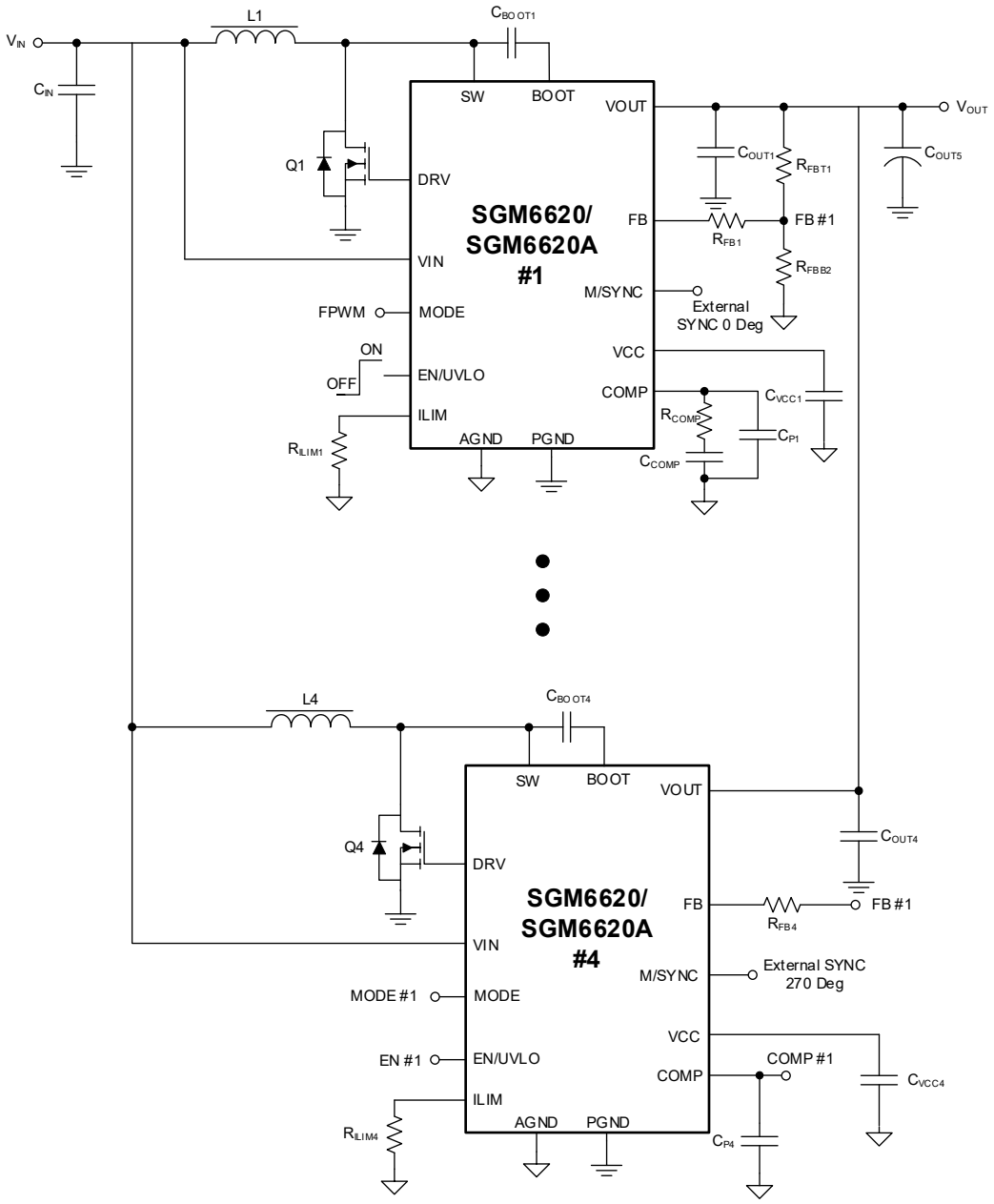


Figure 6. Multi-Phase Operation for High Power Application

DETAILED DESCRIPTION (continued)

Device Functional Modes

In the moderate to heavy load conditions, the SGM6620 family runs at 290kHz (TYP) frequency PWM mode. Under light load conditions, this device has two selectable working modes: auto PFM mode and forced PWM mode, which are designed to accommodate different application scenarios. SGM6620A offers ultrasonic mode to avoid audible noise.

The operating mode is determined by the configuration of MODE pin. The device works in auto PFM mode when the MODE pin voltage is less than logic low threshold. The device works in forced PWM mode, when the MODE pin voltage is above logic high threshold.

Forced PWM (FPWM) Mode

For FPWM option, SGM6620 family is locked in PWM mode from full load to no load. Negative inductor currents are allowed at light load to continue PWM operation. It is a tradeoff that sacrifices light load efficiency for lower output ripple, better output regulation, no audible noise and keeping switching frequency fixed. To avoid fatal negative current in the low-side switch, this current is limited at -5A. Synchronization is available over the full load range in the FPWM mode.

Auto PFM Mode

The SGM6620 family provides auto PFM operation to improve the efficiency at light loads. As the load current decreases in PWM mode, the output of the error amplifier decreases accordingly to reduce the valley inductor current, and thus it delivers less current to the load. As the load decreases further, the inductor current reaches 0A during the high-side FET on-time, the internal zero cross detect comparator triggers to turn off the high-side FET to prevent negative current flow, and waits for the next clock pulse to turn on the low-side FET. As the load current continues decreasing, the output of the error amplifier drops to the PFM threshold voltage and is clamped at this voltage, then the device operates in PFM mode. In PFM operation, the device skips pulses to deliver just enough power to the load and to maintain the output voltage in regulation.

The output voltage remains constant across various operation modes, as shown in Figure 7.

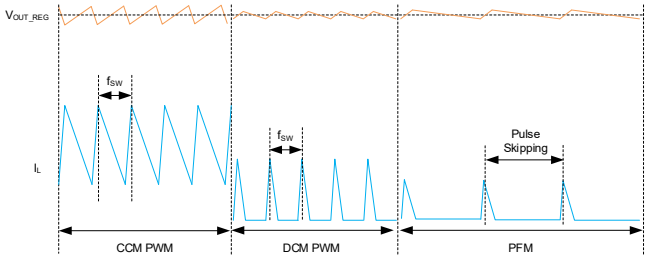


Figure 7. Auto PFM Mode Diagram

Switching Valley Current Limit

The SGM6620 family implements a cycle-by-cycle inductor valley current limit in case of over-current situation. When the internal high-side MOSFET is turned on, the inductor current is sensed by the voltage drop across the MOSFET. If the valley current limit threshold is triggered, the high-side MOSFET will turn off at once. The limit threshold can be set by an external resistor between the ILIM pin and the AGND pin, which can be calculated by Equation 3.

$$I_{VALLEY}(A) = \frac{400k\Omega}{R_{ILIM}(k\Omega)} \quad (3)$$

where, R_{ILIM} is the external resistor set between the ILIM pin and the AGND pin. I_{VALLEY} is the threshold of inductor valley current limit.

Ultrasonic Mode

The SGM6620A provides ultrasonic mode operation at light load. Pulling the MODE pin to logic low configures ultrasonic mode, and pulling the MODE pin to logic high configures FPWM mode. The SGM6620A clamps the switching frequency to 30kHz (TYP) at light load to avoid audible noise, and as the load increases, the device automatically increases the switching frequency to meet the load demand.

Over-Voltage Protection

SGM6620 family integrates over-voltage protection (OVP) to protect the device in the event of feedback resistor short-to-ground or incorrect feedback resistor value being populated. The SGM6620/A stops switching when the OVP threshold of 26.5V (TYP) is reached. When the output voltage is 1V lower than the OVP threshold, the device resumes switching.

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds 160°C (TYP), the switching will stop. The device operation will resume when the junction temperature is cooled down by 20°C (TYP).

APPLICATION INFORMATION

The SGM6620 family is capable of providing an output voltage up to 25V with the 20A valley switch current. In the moderate-to-heavy load condition, the SGM6620 family operates in the quasi-constant frequency pulse width modulation (PWM) mode. Under light load condition, the device can support two working modes. One is the pulse frequency modulation (PFM) mode, which is used to enhance efficiency; the other is the forced PWM (FPWM) mode, which is employed to avoid application issues arising from low switching frequency. This adaptive constant on-time valley current control scheme can achieve outstanding transient line response and load response with the requirements of small output capacitance. The SGM6620 family uses external loop compensation, which provides flexibility to use different inductors and output capacitors.

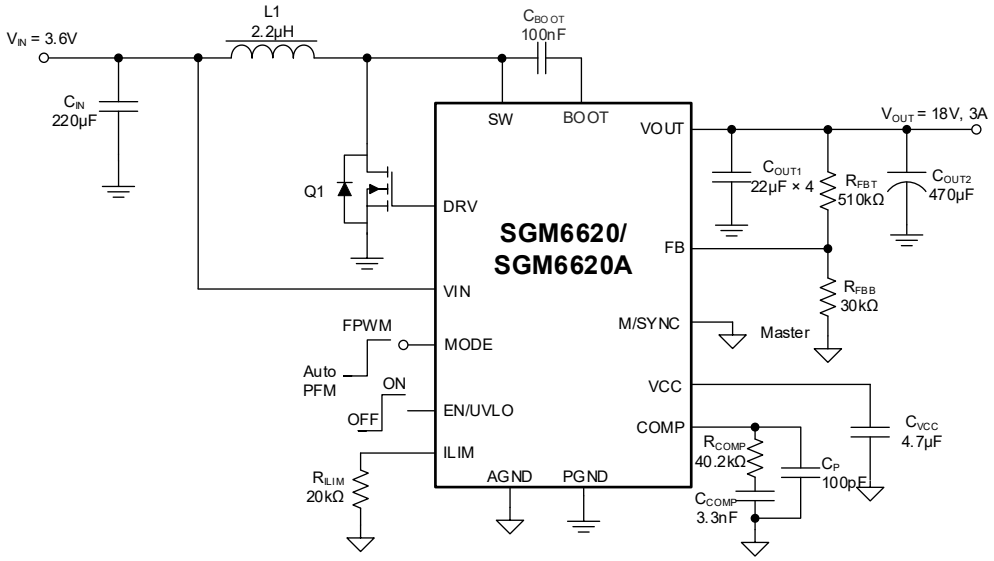


Figure 8. 3.6V V_{IN} to 18V V_{OUT} 3A Output Converter

Design Requirements

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	3.3V to 4.2V
Output Voltage	18V
Output Voltage Ripple	350mV Peak-to-Peak
Output Current Rating	3A

Detailed Design Procedure

Setting Output Voltage

A resistor divider connected between VOUT and FB pins programs the output voltage. In order to achieve the best output voltage accuracy, the recommended value for R_2 should ensure that the current flowing through R_2 is 100 times larger than the leakage current flowing into the FB pin. Lower R_2 resistance also improves the device noise immunity.

The R_1 resistance can be calculated via Equation 4:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (4)$$

APPLICATION INFORMATION (continued)

Input Capacitor Selection

Boost converter's input capacitor has continuous current throughout the entire switching cycle and a 22μF ceramic capacitor is recommended to place as close as possible between the VIN pin and GND pin. For applications where the SGM6620/A is located far away from the input source, a higher capacitance capacitor or additional "Bulk" capacitor (electrolytic or tantalum) is recommended to damp the wiring harness inductance.

Inductor Selection

Inductor is an essential element for current DC/DC switch mode power supplies regardless of topology. Inductor serves as the energy storage element for power conversion. Inductance, DC resistance and saturation current of inductor are three most important criterions for inductor selection. For general design guidance, the selected inductance should provide a peak-to-peak ripple current that is around 30% of the average inductor current at full load and nominal input voltage. The average inductor current for a Boost converter is the input current. Equation 5 shows the calculation of inductance selection.

$$L_{MIN} = \frac{V_{IN\_MIN} \times \left(V_{OUT\_MAX} - V_{IN\_MIN}\right)}{\Delta I_L \times f_{SW} \times V_{OUT\_MAX}} \quad (5)$$

where,

- V_{IN_MIN} is the minimum input voltage of Boost converter.
- V_{OUT_MAX} is the maximum output voltage of Boost converter.
- ΔI_L is the inductor current ripple.
- f_{SW} is the converter switching frequency.
- L_{MIN} is the minimum inductance needed.

The SGM6620 family is optimized to operate with inductance ranges from 2.2μH and 4.7μH. For a single cell Lithium battery application, which input voltage is below 5V and the output voltage is less than 16V, a 2.2μH inductor can meet the requirement. For multi-cell Lithium batteries application or the output voltage is over 16V, considering the inductor ripple current and negative current limit (-5A, MAX) in FPWM mode, a 3.3μH or 4.7μH inductor is recommended.

The minimal saturation current rating of the selector inductor should be higher than the worst-case peak current of the application.

Lower DCR inductor is recommended to improve the conversion efficiency of the device, especially for large load current applications. As shown in Equation 5, smaller inductance increases the peak-to-peak current, which results in higher AC core loss of the inductor. However, the tradeoff of smaller inductance parts comes with smaller footprint and larger inductance parts with same saturation current rating generally comes with larger footprint.

Bootstrap and VCC Capacitors Selection

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. A ceramic capacitor with good quality, low ESR is recommended. The capacitor must have a 10V or higher voltage rating. The BOOT capacitor is refreshed when the high-side MOSFET is off and the external low-side diode conducts.

The internal LDO in the SGM6620 family outputs a regulated voltage of 5V. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor must be above 2.2μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10V is recommended.

MOSFET Selection

The external low-side power MOSFET must choose whose V_{DS} rating can be capable of withstanding the maximum output voltage plus a transient spike. In this application, a MOSFET with 40V rated voltage is selected.

Once the operating voltage level is determined, the MOSFET can be selected by balancing the conduction loss and switching loss that are associated with MOSFET conduction resistor and total gate charge (Qg).

Please note the limitation of the dead time and confirm that the MOSFETs on the low-side and high-side will not turn on synchronously. For this high switching frequency design, a leadless package is better, as it can minimize the parasitic inductance in the driver circuit. Be careful when connecting a resistor in series to the gate, as this may shorten the actual dead time.

The gate driver current of the MOSFET in this device is powered by VCC. Please confirm that the value of the gate threshold voltage (V_{TH}) must be lower than the minimum input voltage to ensure the MOSFET is fully turned on.

APPLICATION INFORMATION (continued)

Output Capacitor Selection

The output capacitors of Boost converter dictate the output voltage ripple and load transient response. Equation 6 are used to estimate the necessary capacitance to achieve desired output voltage ripple. The DC bias effect of the ceramic capacitor should be considered when selecting the capacitors. The voltage rating of the selected capacitor should be higher than the maximum operation output voltage with > 30% margin. When using tantalum or aluminum electrolytic capacitors, the ESR must be considered to calculate the output voltage ripple.

$$C_{MIN} = \frac{I_{OUT} \times \left(V_{OUT} - V_{IN\_MIN}\right)}{f_{SW} \times \Delta V \times V_{OUT}} \quad (6)$$

where,

- V_{IN_MIN} is the minimum input voltage of the Boost converter.
- V_{OUT} is the output voltage.
- ΔV is the maximum acceptable output voltage ripple.
- I_{OUT} is the output current.
- f_{SW} is the converter switching frequency.
- C_{MIN} is the minimum capacitance needed.

Loop Stability

The compensation network of SGM6620 family is implemented externally to improve design flexibility. The SGM6620 family implements a trans-conductance error amplifier, where the COMP pin is the output of the internal error amplifier. A type-II compensation network consisting of R_{COMP}, C_{COMP} and C_P connected to the COMP pin is used to configure the loop response of SGM6620 family.

The power stage small signal loop response of peak current control can be modeled by Equation 7.

$$G_{PS}(S) = K_{COMP} \times \frac{R_{OUT} \times (1-D)}{2} \times \frac{\left(1+\frac{S}{2\pi f_{ESRZ}}\right) \times \left(1-\frac{S}{2\pi f_{RHPZ}}\right)}{1+\frac{S}{2\pi f_P}} \quad (7)$$

where,

- D is the switching duty cycle.
- R_{OUT} is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current / comp voltage), which is 25A/V.
- f_P is the pole's frequency.
- f_{ESRZ} is the zero's frequency.
- f_{RHPZ} is the right-half-plane-zero's frequency.

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \quad (8)$$

where,

- C_{OUT} is effective capacitance of the output capacitor.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (9)$$

where,

- R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_{OUT} \times (1-D)^2}{2\pi \times L} \quad (10)$$

Equation 11 shows the small signal transfer function of compensation network.

$$G_C(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1+\frac{S}{2\pi f_{COMZ}}\right)}{\left(1+\frac{S}{2\pi f_{COMP1}}\right) \times \left(1+\frac{S}{2\pi f_{COMP2}}\right)} \quad (11)$$

where

- G_{EA} is the amplifier trans-conductance.
- R_{EA} is the amplifier's output resistance.
- V_{REF} is the FB reference voltage.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the pole's frequency of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

APPLICATION INFORMATION (continued)

Once the error amplifier and power stage's poles and zeros are determined, the component value of compensation network can be designed. The designed loop crossover frequency (f_C) should be within 1/5 of the RHPZ frequency (f_{RHPZ}) or 1/10 of the switching frequency. Higher crossover frequency could improve the transient response. However, the crossover frequency could be designed to avoid instability.

With a selected f_C, use Equation12 to calculate the required R_{COMP}.

$$R_{COMP} = \frac{2\pi \times V_{OUT} \times C_{OUT} \times f_C}{(1-D) \times V_{REF} \times G_{EA} \times K_{COMP}} \quad (12)$$

where,

• f_C is the selected crossover frequency. The value of C_{COMP} can be calculated by Equation 13.

$$C_{COMP} = \frac{R_{OUT} \times C_{OUT}}{2R_{COMP}} \quad (13)$$

The value of C_P can be calculated by Equation 14.

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_{COMP}} \quad (14)$$

C_P is not needed, when applications only use ceramic capacitor or the calculated value of C_P is less than 10pF.

To measure good loop compensation design, greater than 45° of phase margin and greater than 10dB gain margin could provide good loop stability and avoid output voltage ringing during load and line transient.

Table 2. Recommended L, R_{COMP} and C_{COMP} for Different Input and Output Voltages

V_{IN} (V)	V_{OUT} (V)	L (μH)	R_{COMP} (kΩ)	C_{COMP} (nF)
3.6	5	2.2	6.2	3.3
3.6	18	3.3	40.2	3.3
3.6	25	4.7	40.2	6.8
7.2	18	3.3	40.2	3.3
7.2	25	4.7	40.2	3.3
10.8	18	3.3	34	3.3
10.8	25	4.7	30	3.3

Power Supply Recommendations

The SGM6620 family operates from a wide 2.05V to 23V input voltage. If the input power supply is located far away from the device, apart from the ceramic capacitors, additional Bulk capacitor may also be needed.

Layout Guidelines

Layout is a critical step to ensure the performance of any switch mode power supplies, in addition to component selection. Poor layout could result in system instability, EMI failure, and device damage. Thus, place the inductor, input capacitors and output capacitors as close to the IC as possible, and use wide and short traces for current carrying traces to minimize PCB parasitic inductance.

For Boost converter, the current loop of the output capacitor from VOUT pin back to the GND pin of the device should be as small as possible. The traces connected to SW node should be as short as possible. A ground plane underneath the SGM6620/A is recommended to minimize inter-plane coupling.

Due to the high power density of SGM6620/A, the current-carrying SW, VOUT, VIN and PGND pins should be connected with large copper polygon pour to ensure good thermal performance, and thermal vias on these nodes are recommended.

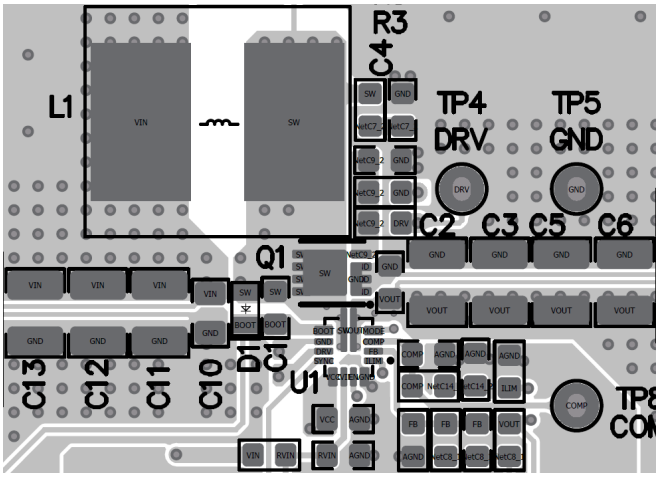


Figure 9. PCB Layout

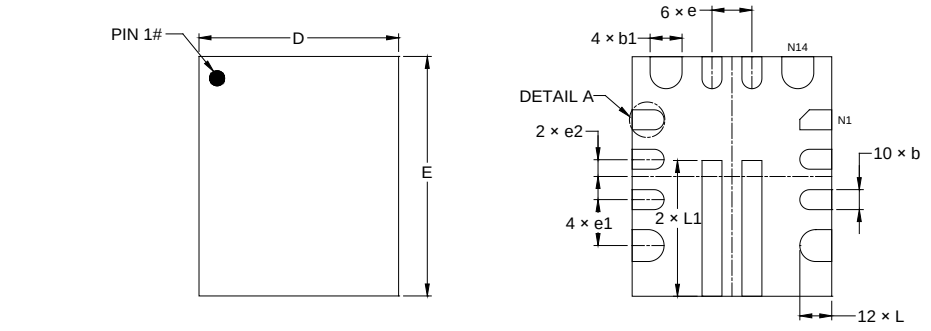
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

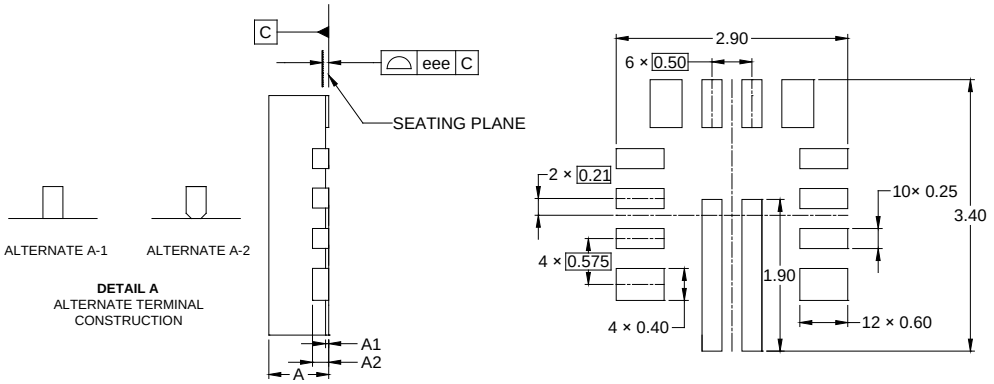
Changes from Original to REV.A (NOVEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TQFN-2.5×3-14AL



TOP VIEW **BOTTOM VIEW**



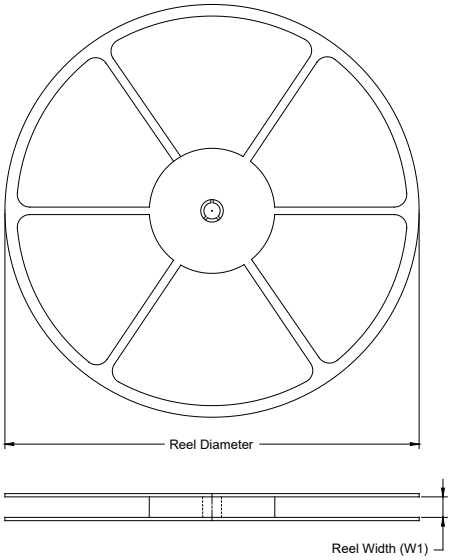
SIDE VIEW **RECOMMENDED LAND PATTERN** (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
b1	0.350	-	0.450
D	2.400	-	2.600
E	2.900	-	3.100
e		0.500 BSC	
e1		0.575 BSC	
e2		0.210 BSC	
L	0.300	-	0.500
L1	1.600	-	1.800
eee		0.080	

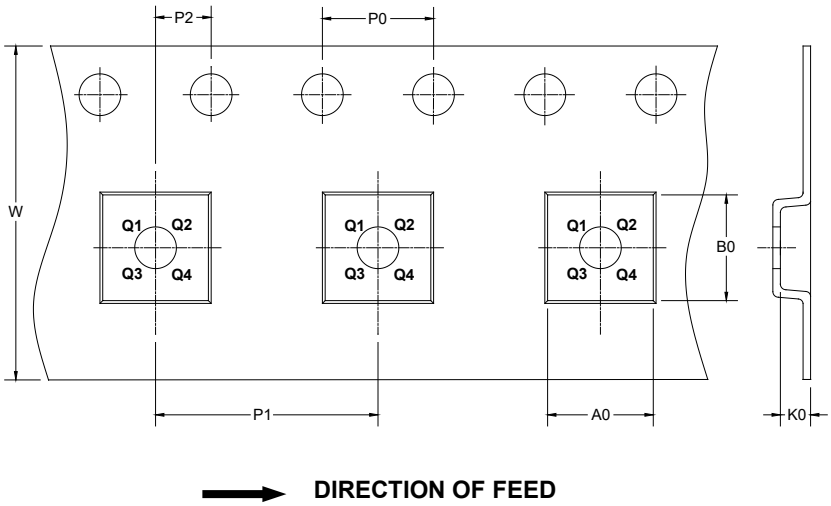
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



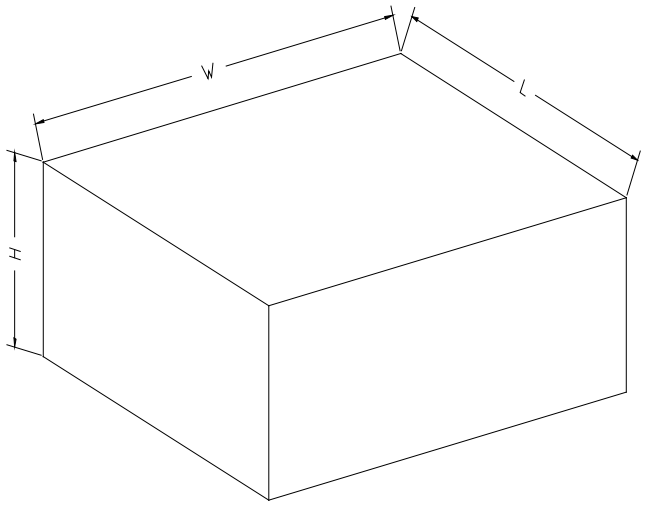
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-2.5×3-14AL	13"	12.4	2.80	3.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002