SGM5100/SGM5101
14-Bit, 10MSPS/40MSPS Low Power 3V ADCs

GENERAL DESCRIPTION

The SGM5100/SGM5101 are 14-bit 10MSPS/40MSPS, low power 3V single-channel analog-to-digital converters (ADCs) suitable for sampling high frequency and wide dynamic range signals. With 74.1dB/72.8dB SNR and 79dB/88dB SFDR for signals at the Nyquist frequency, the SGM5100/SGM5101 meet demanding requirements in imaging and communication applications.

The SGM5100/SGM5101 feature good DC performances such as ±1.7LSB (TYP) INL, ±0.65LSB (TYP) DNL and no missing codes over-temperature. Besides, the $1LSB_{RMS}$ transition noise is also a remarkable feature of the devices.

The SGM5100/SGM5101 support single-ended sampling clock input with an internal optional clock duty cycle stabilizer, which guarantees high performance for a wide range of clock duty cycles when sampling at full speed.

The SGM5100/SGM5101 are available in a Green TQFN-5×5-32DL package.

FEATURES

- **Single 3V Supply (2.7V to 3.4V)**
- **Sample Rate:**
  - **SGM5100: 10MSPS**
  - **SGM5101: 40MSPS**
- **Low Power:**
  - **SGM5100: 55.5mW (TYP)**
  - **SGM5101: 190mW (TYP)**
- **SNR:**
  - **SGM5100: 74.1dB (TYP)**
  - **SGM5101: 72.8dB (TYP)**
- **SFDR:**
  - **SGM5100: 79dB (TYP)**
  - **SGM5101: 88dB (TYP)**
- **Flexible Input: $1V_{P-P}$ to $2V_{P-P}$ Range**
- **Full Power Bandwidth S/H: 575MHz**
- **No Missing Codes**
- **Sleep and Nap Modes**
- **Support Clock Duty Cycle Stabilizer**
- **Available in a Green TQFN-5×5-32DL Package**

APPLICATIONS

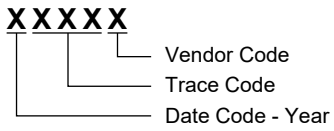
Communication Infrastructures
Medical Imaging Systems
Instrumentations

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5100	TQFN-5×5-32DL	-40℃ to +125℃	SGM5100XTVJ32G/TR	SGM5100 XTVJ32 XXXXX	Tape and Reel, 3000
			SGM5100XTVJ32SG/TR	SGM5100 XTVJ32 XXXXX	Tape and Reel, 250
SGM5101	TQFN-5×5-32DL	-40℃ to +125℃	SGM5101XTVJ32G/TR	SGM5101 XTVJ32 XXXXX	Tape and Reel, 3000
			SGM5101XTVJ32SG/TR	SGM5101 XTVJ32 XXXXX	Tape and Reel, 250

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (1)

Supply Voltage (V_{DD}) 4V

Analog Input Voltage Range (2) ..... -0.3V to (V_{DD} + 0.3V)

Digital Input Voltage Range ..... -0.3V to (V_{DD} + 0.3V)

Digital Output Voltage Range ..... -0.3V to (OV_{DD} + 0.3V)

Power Dissipation 4600mW

Package Thermal Resistance

TQFN-5×5-32DL, θ_{JA} ..... 26.9℃/W

TQFN-5×5-32DL, θ_{JB} ..... 8.6℃/W

TQFN-5×5-32DL, $\theta_{JC\ (TOP)}$ ..... 18.5℃/W

TQFN-5×5-32DL, $\theta_{JC\ (BOT)}$ ..... 1.9℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 4000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

NOTES:

1. All voltage values are referred to ground. If no special comments, GND and OGND are connected together.

2. When these pin voltages are lower than GND or higher than V_{DD}, they will be clamped by the internal protection circuits. The device can deal with the input currents of greater than 100mA below GND or above V_{DD} without latch-up.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

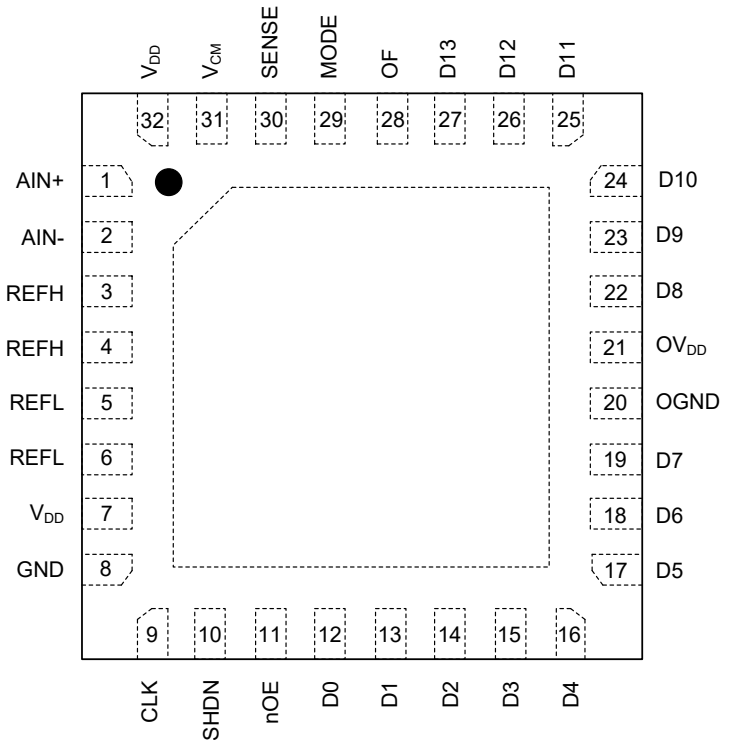
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM5100/SGM5101 (TOP VIEW)



TQFN-5×5-32DL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	AIN+	Positive Differential Analog Input Pin.
2	AIN-	Negative Differential Analog Input Pin.
3, 4	REFH	ADC Reference Input High. Connect them together and place a 0.1μF between the pins and pin 5/pin 6. Also a 2.2μF along with another 1μF ceramic chip capacitor is suggested to connect between the pin and ground.
5, 6	REFL	ADC Reference Input Low. Connect them together and place a 0.1μF between the pins and pin 3/pin 4. Also a 2.2μF along with another 1μF ceramic chip capacitor is suggested to connect between the pin and ground.
7, 32	V_{DD}	3V Power Supply. A 0.1μF bypass ceramic capacitors is suggested between this pin and ground.
8	GND	ADC Power Ground.
9	CLK	Clock Input Pin. Conversion starts on the rising edge.
10	SHDN	Shutdown Pin. Co-work with nOE pin. (0 means connecting the pin to GND and 1 means connecting the pin to V_{DD}) SHDN = 0 and nOE = 0: normal operation with the outputs enabled. SHDN = 0 and nOE = 1: normal operation with the outputs at high impedance. SHDN = 1 and nOE = 0: nap mode with the outputs at high impedance. SHDN = 1 and nOE = 1: sleep mode with the outputs at high impedance.
11	nOE	Output Enable Pin. Refer to SHDN pin function.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
12	D0	Digital Output Pin 0. This is the LSB.
13	D1	Digital Output Pin 1.
14	D2	Digital Output Pin 2.
15	D3	Digital Output Pin 3.
16	D4	Digital Output Pin 4.
17	D5	Digital Output Pin 5.
18	D6	Digital Output Pin 6.
19	D7	Digital Output Pin 7.
20	OGND	Output Ground.
21	OV_{DD}	Power Supply for Digital Output. It should be bypassed to ground with 0.1μF ceramic chip capacitor.
22	D8	Digital Output Pin 8.
23	D9	Digital Output Pin 9.
24	D10	Digital Output Pin 10.
25	D11	Digital Output Pin 11.
26	D12	Digital Output Pin 12.
27	D13	Digital Output Pin 13. This is the MSB.
28	OF	Over/Under Flow Indicator. High if an over or under flow occurs.
29	MODE	Output Format and Clock Duty Cycle Stabilizer Selection Pin. MODE = GND: offset binary output format and disables the clock duty cycle stabilizer. MODE = 1/3 V_{DD}: offset binary output format and enables the clock duty cycle stabilizer. MODE = 2/3 V_{DD}: two's complement output format and enables the clock duty cycle stabilizer MODE = V_{DD}: two's complement output format and disables the clock duty cycle stabilizer.
30	SENSE	Internal reference and a ±1V input range are selected if SENSE is connected to V_{DD}. Similarly, Internal reference and a ±0.5V input range are selected if SENSE is connected to V_{CM}. External reference and an input range of $\pm V_{SENSE}$ are selected if SENSE is connected to a voltage from 0.5V to 1V. Note that ±1V is the largest valid input range.
31	V_{CM}	1.5V Output and Input Common Mode Bias Pin. It is recommended to connect a 2.2μF bypass capacitor between the pin and ground.
Exposed Pad	—	ADC Power Ground. The exposed pad should be connected to ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, f_{SAMPLE} = 10MHz (SGM5100) or 40MHz (SGM5101), input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Converter Characteristics							
Resolution (No Missing Codes)				14			Bits
Integral Nonlinearity (1)	INL	Differential analog input	SGM5100	-8.1	±1.7	7.2	LSB
			SGM5101	-9.3	±1.7	8.5	
Differential Nonlinearity	DNL	Differential analog input	SGM5100	-0.999	±0.65	1.5	LSB
			SGM5101	-0.999	±0.65	2.2	
Offset Error (2)	E_O		SGM5100	-16	±2	33	mV
			SGM5101	-17	±2	36	
Gain Error	E_G	External reference	SGM5100	-7	±0.5	6.5	%FS
			SGM5101	-9	±0.5	10	
Offset Drift					37		μV/℃
Full-Scale Drift		Internal reference			85		ppm/℃
		External reference			80		
Transition Noise		SENSE = 1V			1		LSB_{RMS}
Analog Input							
Analog Input Range (3) (AIN+ - AIN-)	V_{IN}	2.7V < V_{DD} < 3.4V			±0.5 to ±1		V
Analog Input Common Mode (3) (AIN+ + AIN-)/2	$V_{IN(CM)}$	Differential input		1	1.5	1.9	V
		Single-ended input		0.5	1.5	2	V
Analog Input Leakage Current	I_{IN}	0V < AIN+, AIN- < V_{DD}		-1		1	μA
SENSE Input Leakage	I_{SENSE}	0V < SENSE < 1V		-3		3	μA
MODE Pin Leakage	I_{MODE}			-3		3	μA
Sample-and-Hold Acquisition Delay Time (3)	t_{AP}				0		ns
Sample-and-Hold Acquisition Delay Time Jitter (3)	t_{JITTER}				0.2		ps_{RMS}
Analog Input Common Mode Rejection Ratio	CMRR				60		dB
Full Power Bandwidth		SGM5101			575		MHz
Dynamic Accuracy (A_{IN} = -1dBFS)							
Signal-to-Noise Ratio	SNR	5MHz input	SGM5100	69.3	74.1		dB
			SGM5101		72.3		
		20MHz input	SGM5101	67.4	72.8		
		70MHz input	SGM5100		72.6		
			SGM5101		70.8		
		140MHz input	SGM5101		69		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, f_{SAMPLE} = 10MHz (SGM5100) or 40MHz (SGM5101), input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Accuracy (A_{IN} = -1dBFS)							
Spurious Free Dynamic Range (2nd or 3rd Harmonic)	SFDR	5MHz input	SGM5100	68.1	79		dB
			SGM5101		85.3		
		20MHz input	SGM5101	71	88		
		70MHz input	SGM5100		73.6		
			SGM5101		78.1		
		140MHz input	SGM5101		68.2		
Spurious Free Dynamic Range (4th Harmonic or Higher)		5MHz input	SGM5100	77.4	88.3		dB
			SGM5101		90		
		20MHz input	SGM5101	74.5	97		
		70MHz input	SGM5100		85.6		
			SGM5101		92.2		
		140MHz input	SGM5101		90		
Signal-to-Noise + Distortion	SINAD	5MHz input	SGM5100	66.7	72.6		dB
			SGM5101		72		
		20MHz input	SGM5101	66.4	72.1		
		70MHz input	SGM5100		68.6		
			SGM5101		69.7		
		140MHz input	SGM5101		63		
Intermodulation Distortion	I_{MD}	f_{IN1} = 4.3MHz, f_{IN2} = 4.6MHz	SGM5100		80		dB
		f_{IN1} = 28.2MHz, f_{IN2} = 26.8MHz	SGM5101		80		
Internal Reference Characteristics							
V_{CM} Output Voltage		I_{OUT} = 0mA		1.475	1.5	1.525	V
V_{CM} Output Tempco					25		ppm/℃
V_{CM} Line Regulation		2.7V < V_{DD} < 3.4V			0.1		mV/V
V_{CM} Output Resistance		-1mA < I_{OUT} < 1mA			2		Ω
Digital Inputs and Digital Outputs							
Logic Inputs (CLK, nOE, SHDN)							
High-Level Input Voltage	V_{IH}	V_{DD} = 3V		2			V
Low-Level Input Voltage	V_{IL}	V_{DD} = 3V				0.8	V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}		-1		1	μA
Input Capacitance (3)	C_{IN}				3		pF
Logic Outputs (OV_{DD} = 3V)							
Hi-Z Output Capacitance (3)	C_{OZ}	nOE = High			3		pF
Output Source Current	I_{SOURCE}	V_{OUT} = 0V			26		mA
Output Sink Current	I_{SINK}	V_{OUT} = 3V			30		mA
High-Level Output Voltage	V_{OH}	I_O = -10μA			2.995		V
		I_O = -200μA		2.7	2.95		
Low-Level Output Voltage	V_{OL}	I_O = 10μA			0.001		V
		I_O = 1.6mA			0.06	0.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, f_{SAMPLE} = 10MHz (SGM5100) or 40MHz (SGM5101), input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Outputs (OV_{DD} = 2.5V)						
High-Level Output Voltage	V_{OH}	I_O = -200μA		2.48		V
Low-Level Output Voltage	V_{OL}	I_O = 1.6mA		0.06		V
Logic Outputs (OV_{DD} = 1.8V)						
High-Level Output Voltage	V_{OH}	I_O = -200μA		1.78		V
Low-Level Output Voltage	V_{OL}	I_O = 1.6mA		0.08		V
Power Requirements (Input Range = $1V_{P-P}$ with Differential Drive)						
Analog Supply Voltage (4)	V_{DD}		2.7	3	3.4	V
Output Supply Voltage (4)	OV_{DD}		1.65	3	3.6	V
Supply Current	IV_{DD}	SGM5100		18.5	23	mA
		SGM5101		63.4	75	
Power Dissipation	P_{DISS}	SGM5100		55.5	69	mW
		SGM5101		190	225	
Sleep Mode Power	P_{SHDN}	SHDN = H, nOE = H, no CLK		0.05		mW
Nap Mode Power	P_{NAP}	SHDN = H, nOE = L, no CLK		6		mW

NOTES:

1. Integral nonlinearity is described as the deviation of an actual transfer function from a straight line. The deviation is measured from the center of the quantization voltage level and is noted in LSB.

2. The offset error refers to the voltage offset that is measured when the output code alternates between code equals all 0s and all 1s in two's complement output mode, with -0.5LSB being the starting point.

3. Guaranteed by design.

4. Suggested conditions.

TIMING CHARACTERISTICS

(V_{DD} = 3V, f_{SAMPLE} = 10MHz (SGM5100) or 40MHz (SGM5101), input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sampling Frequency (1)	f_S	SGM5100		1		10	MHz
		SGM5101		2		40	
CLK Low Time (2)	t_L	Duty cycle stabilizer off	SGM5100	40	50	500	ns
		Duty cycle stabilizer on		8	50	500	
		Duty cycle stabilizer off	SGM5101	12	12.5	250	
		Duty cycle stabilizer on		5	12.5	250	
CLK High Time (2)	t_H	Duty cycle stabilizer off	SGM5100	40	50	500	ns
		Duty cycle stabilizer on		8	50	500	
		Duty cycle stabilizer off	SGM5101	12	12.5	250	
		Duty cycle stabilizer on		5	12.5	250	
Sample-and-Hold Aperture Delay (2)	t_{AP}				0		ns
CLK to OF Delay (2)	t_D	C_L = 10pF		5.5	11	21.5	ns
CLK to DATA Delay (2)		C_L = 10pF		5	10	20.5	ns
Data Access Time after nOE (2)		C_L = 10pF			9.6	20	ns
BUS Relinquish Time (2)					10	15	ns
Pipeline Latency					5		Cycles

NOTES:

1. Suggested conditions.

2. Guaranteed by design.

TIMING DIAGRAM

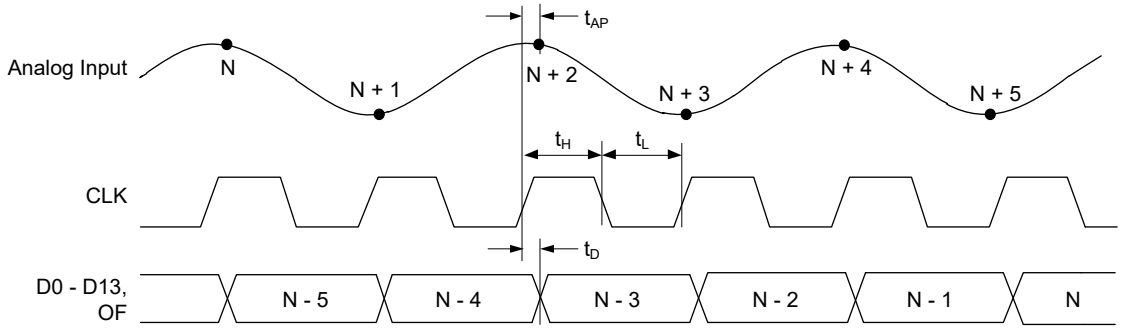
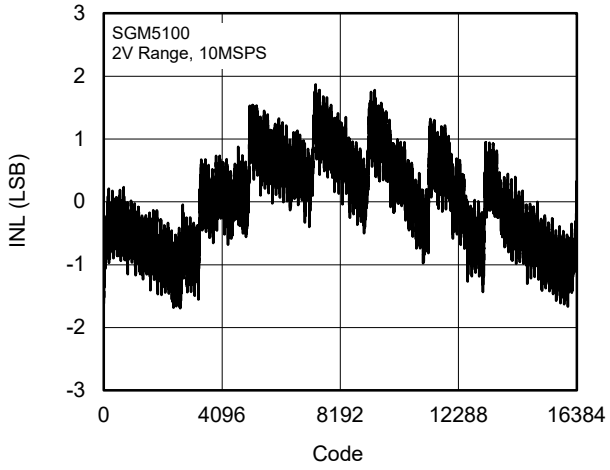


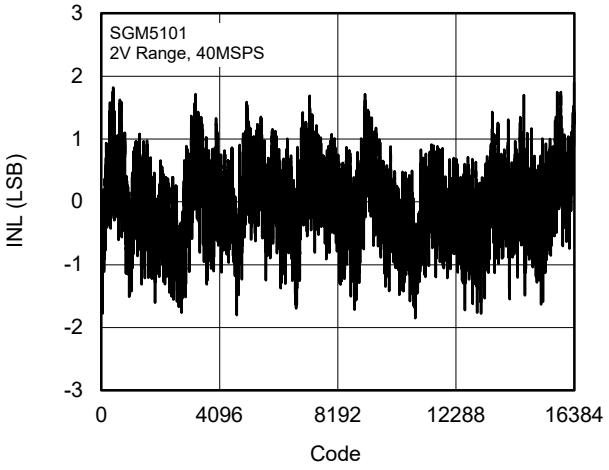
Figure 1. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

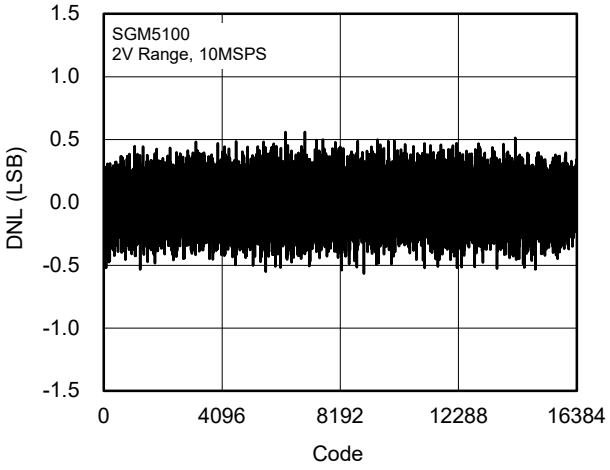
Integral Nonlinearity vs. Code



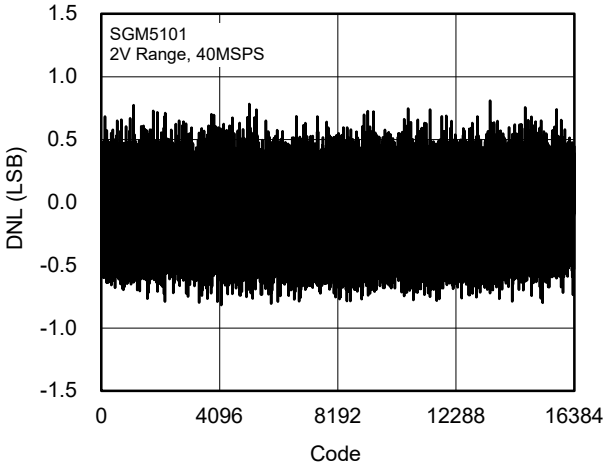
Integral Nonlinearity vs. Code



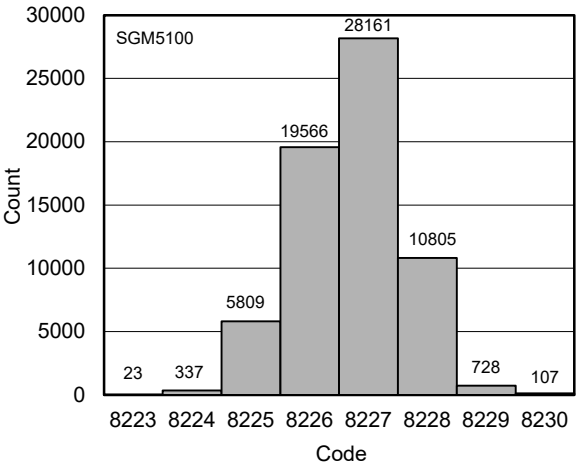
Differential Nonlinearity vs. Code



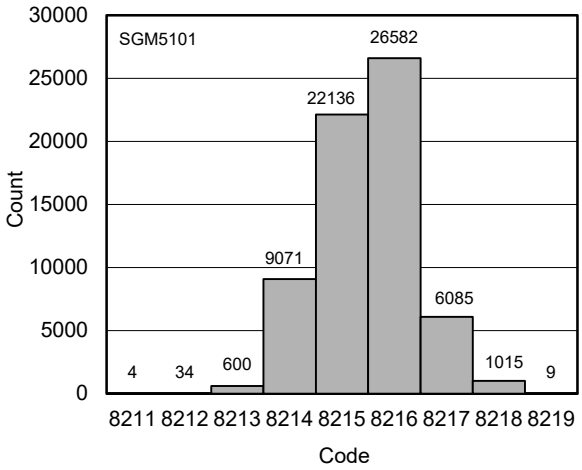
Differential Nonlinearity vs. Code



Grounded Input Histogram

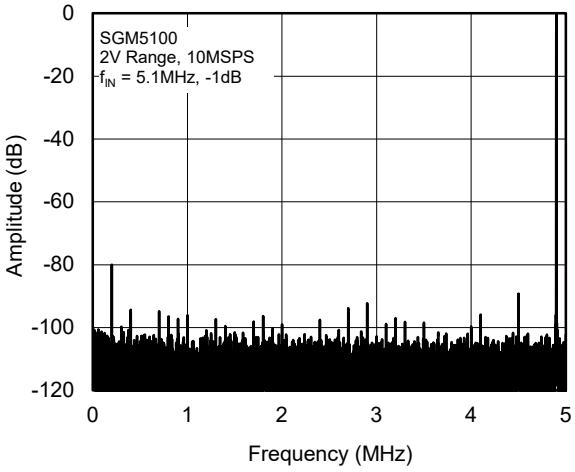


Grounded Input Histogram

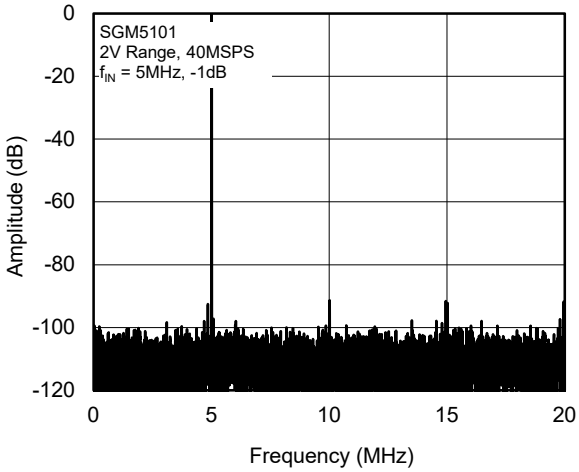


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

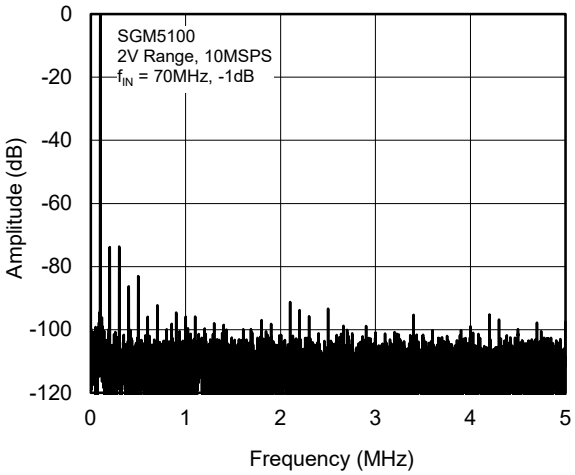
16384 Point FFT 5.1MHz



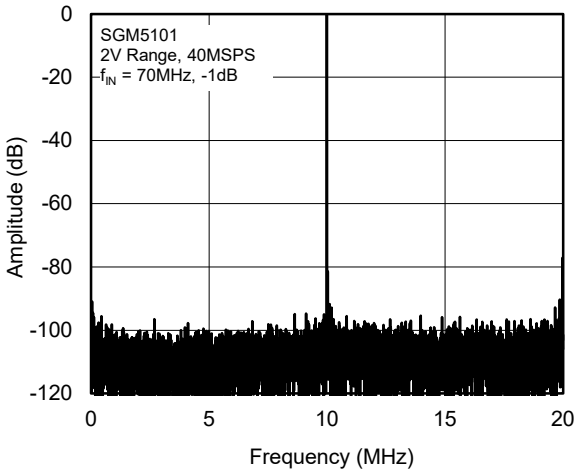
16384 Point FFT 5MHz



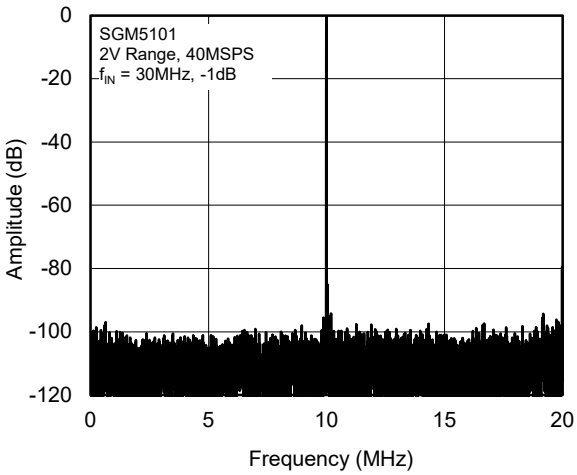
16384 Point FFT 70MHz



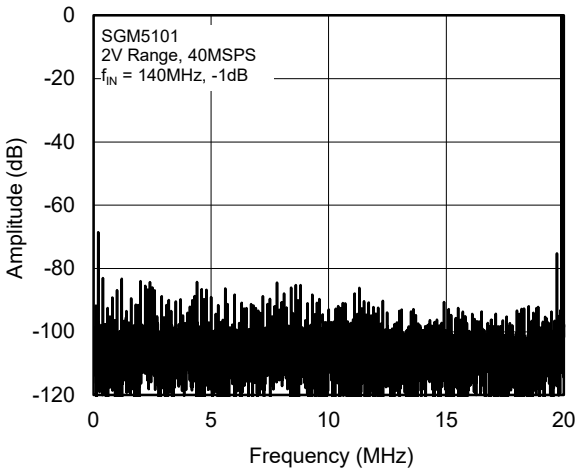
16384 Point FFT 70MHz



16384 Point FFT 30MHz

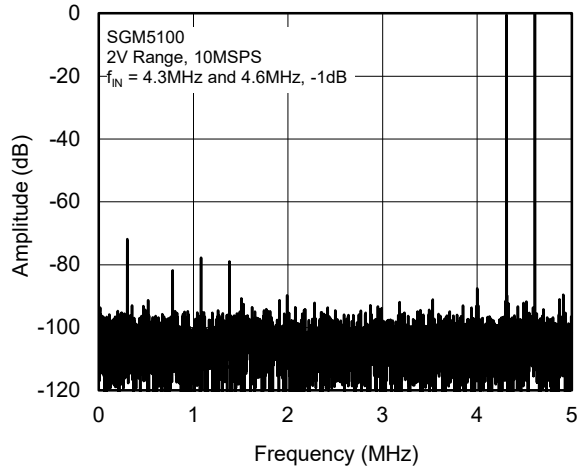


16384 Point FFT 140MHz

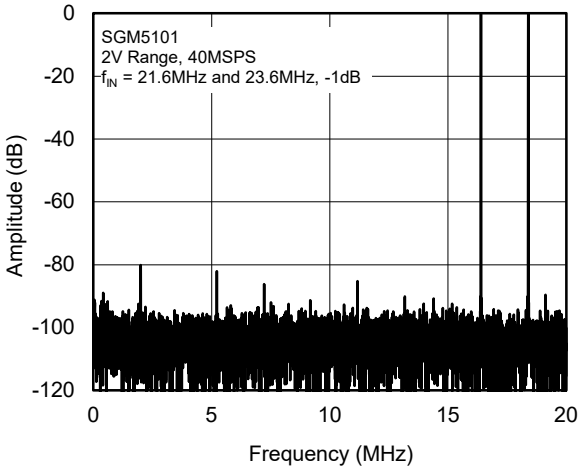


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

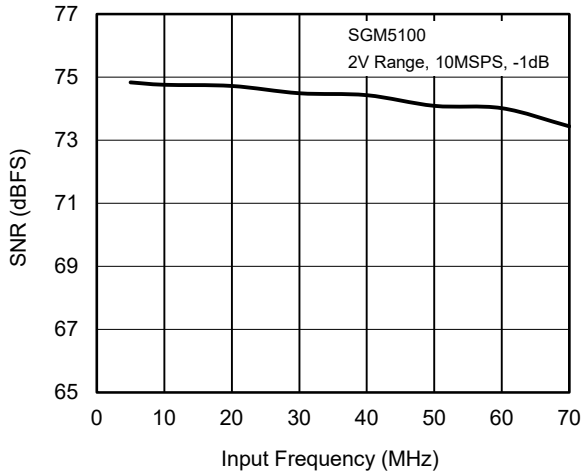
16384 Point 2-Tone FFT



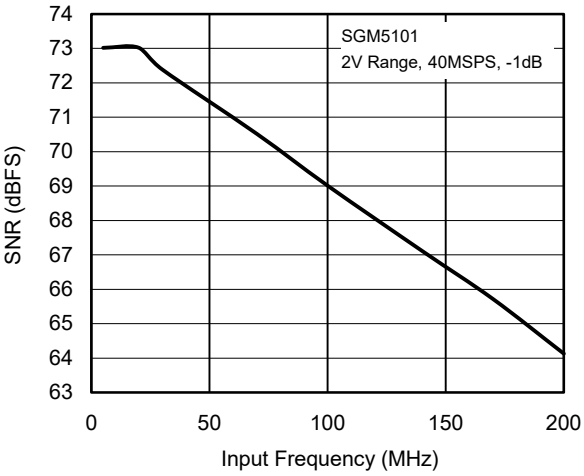
16384 Point 2-Tone FFT



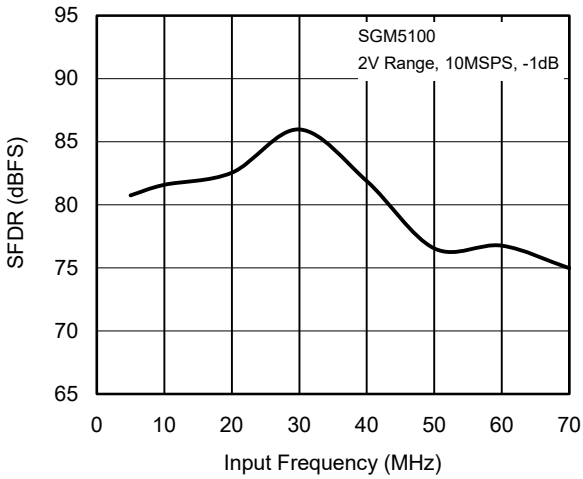
SNR vs. Input Frequency



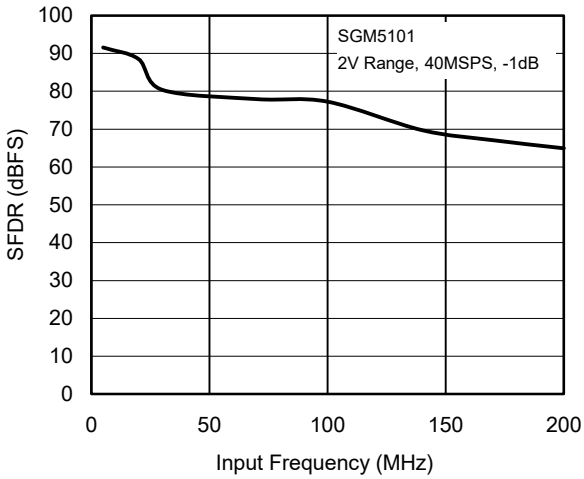
SNR vs. Input Frequency



SFDR vs. Input Frequency

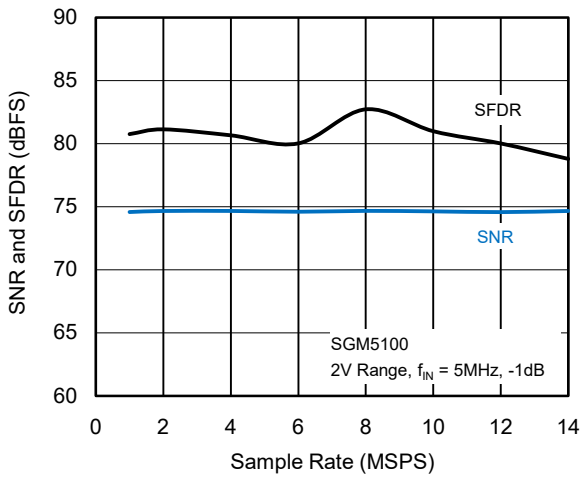


SFDR vs. Input Frequency

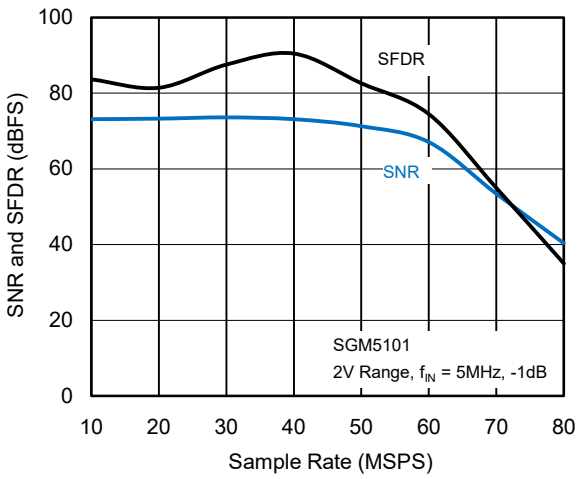


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

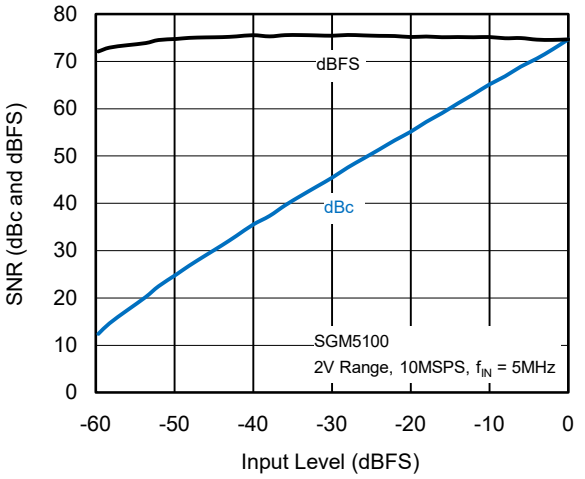
SNR and SFDR vs. Sample Rate



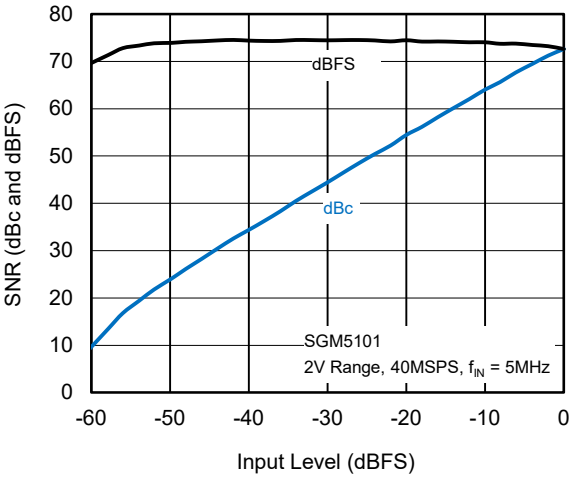
SNR and SFDR vs. Sample Rate



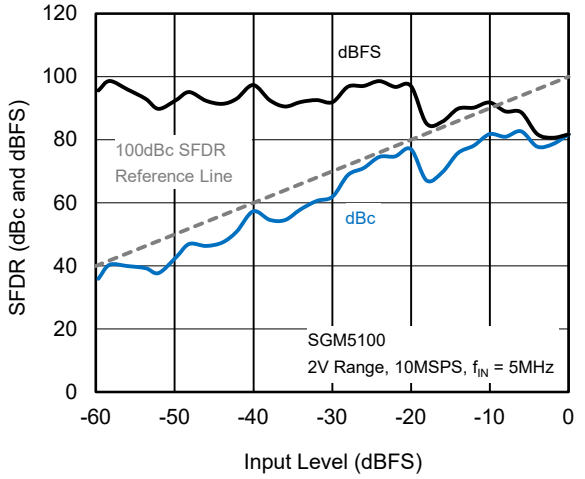
SNR vs. Input Level



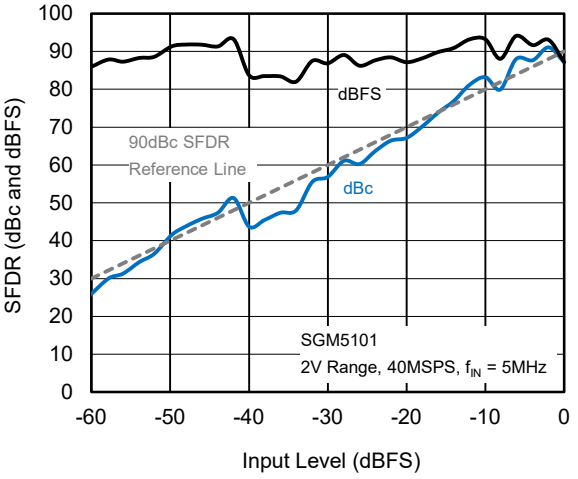
SNR vs. Input Level



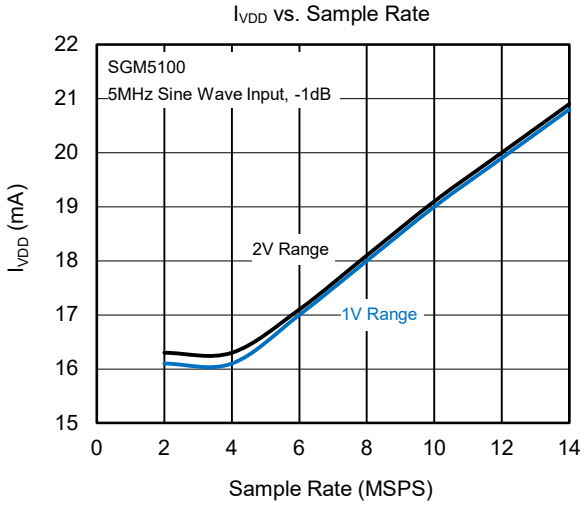
SFDR vs. Input Level

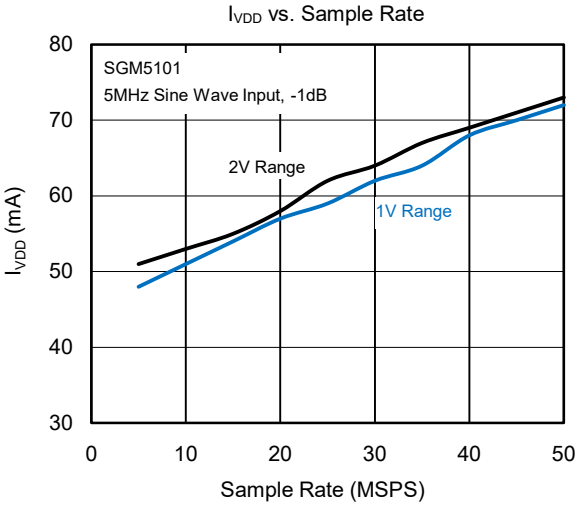


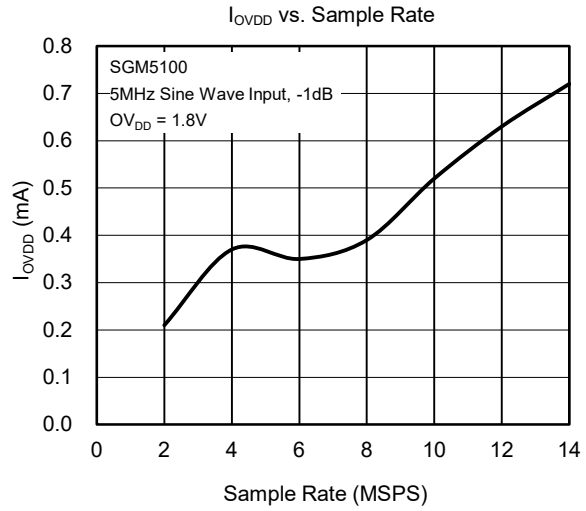
SFDR vs. Input Level

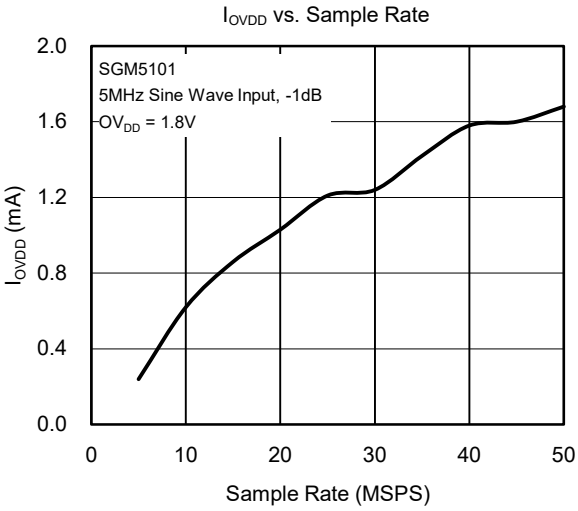


TYPICAL PERFORMANCE CHARACTERISTICS (continued)









TYPICAL APPLICATION CIRCUIT

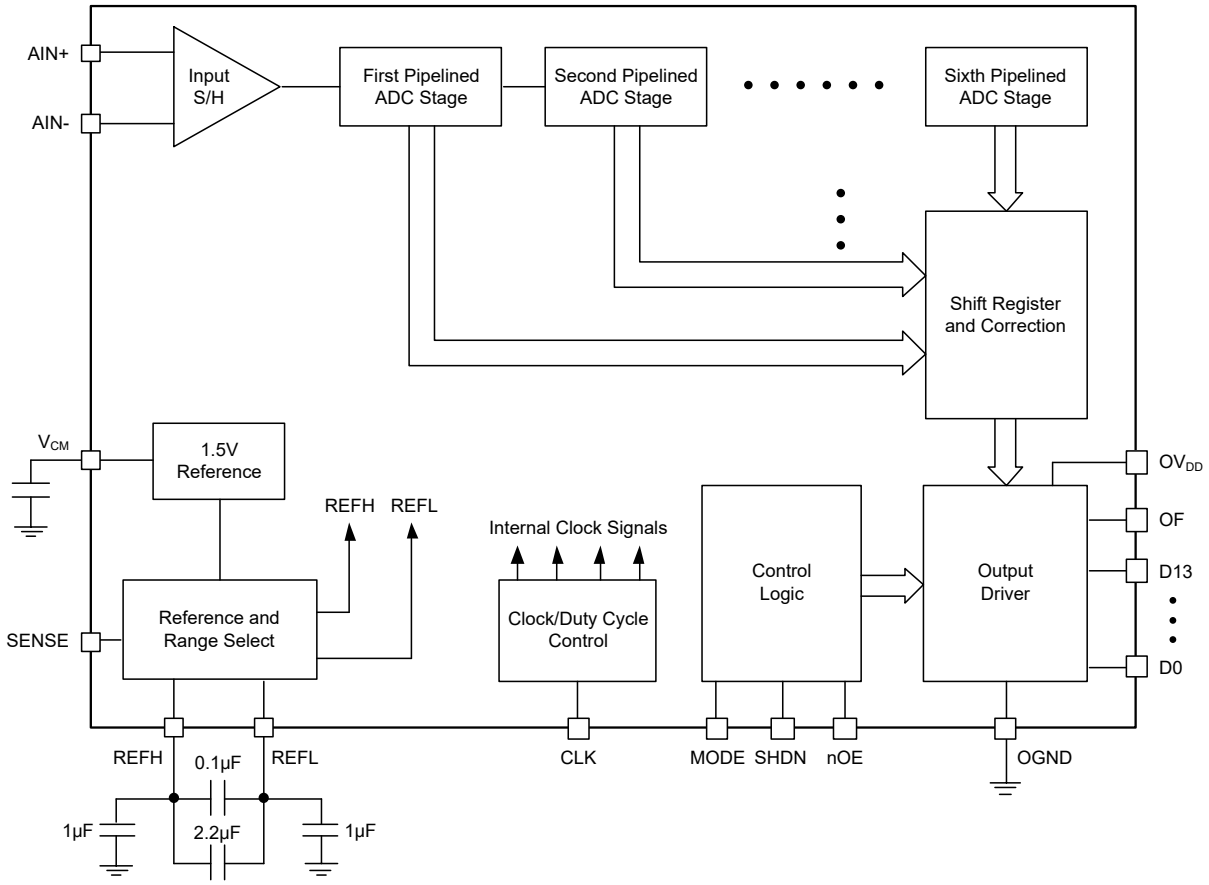


Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

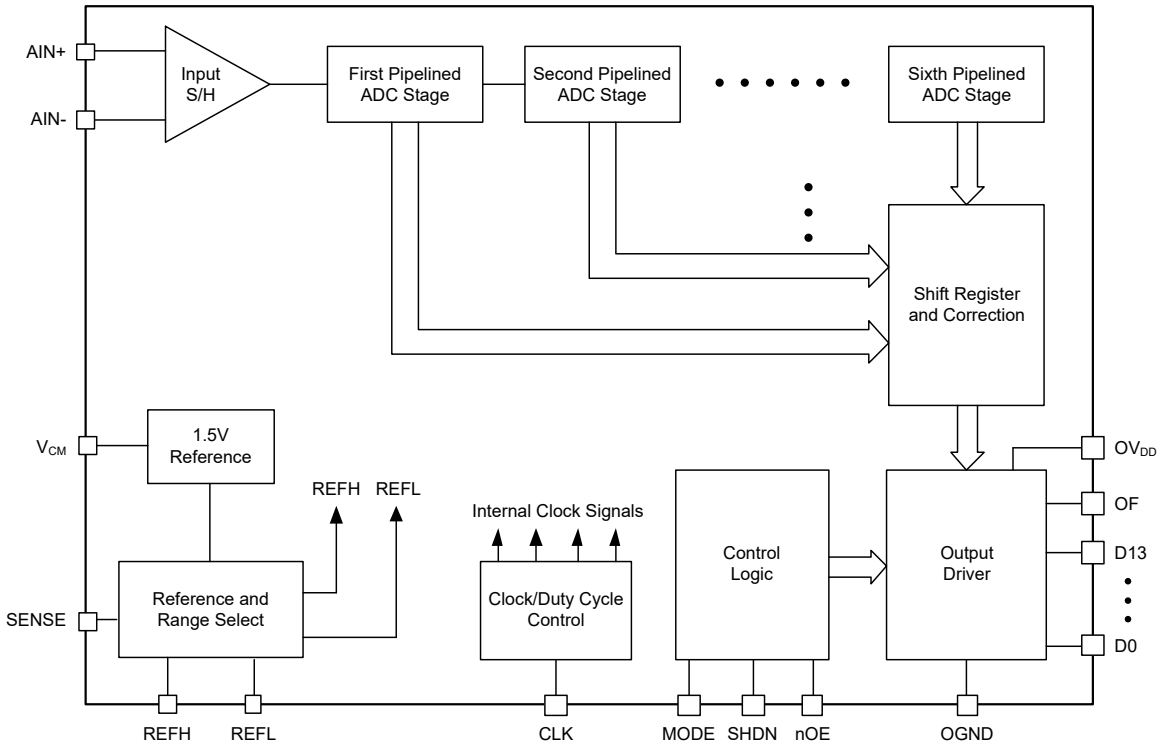


Figure 3. Block Diagram

APPLICATION INFORMATION

Dynamic Performance

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is calculated by dividing RMS amplitude of the fundamental input frequency by the RMS amplitude of noise terms. Under actual circumstances, only first ten harmonics and DC component will be excluded for SNR calculation.

Signal-to-Noise plus Distortion Ratio

The signal-to-noise plus distortion ratio (SINAD) is defined as the ratio of the RMS signal amplitude to the mean value of root sum square of all other spectral components, excluding DC. The output frequency range is limited between DC and half of the sampling frequency.

Total Harmonic Distortion

The total harmonic distortion (THD) is defined as the ratio of the equivalent RMS of all harmonics (starting from the 2nd harmonic frequency on) over the RMS amplitude of the fundamental frequency. In this datasheet, only the first 10th harmonics are taken into consideration. The THD is calculated using the following formula:

$$THD = 20\log\left(\frac{\sqrt{\sum_{2}^{\infty} V_{n\_rms}^2}}{V_{fundmental\_rms}}\right) \quad (1)$$

Where:

$V_{fundmental\_rms}$ is the RMS amplitude of the input signal (i.e. the fundamental frequency).

V_{n_rms} is the RMS amplitude of the n^{th} harmonic.

Intermodulation Distortion

The intermodulation distortion (IMD) is the measurement that describes the ratio between the RMS amplitude of input fundamental frequencies (f_1 and f_2) and the third-order intermodulation products ($2f_1 - f_2$ and $2f_2 - f_1$). It is caused by the nonlinearities or time variances in a system, which is the amplitude modulation of signals with two or even more different frequencies. In an ADC sampling system, if the input signal of ADC contains more than one frequency, the nonlinearity of ADC will result in IMD.

Two pure sine waves with close frequencies (f_1 and f_2) to the ADC can be used to evaluate the IMD. For example, when the frequencies of the two input signal are 7MHz and 8MHz, Figure 4 shows the location of the second and third-order products.

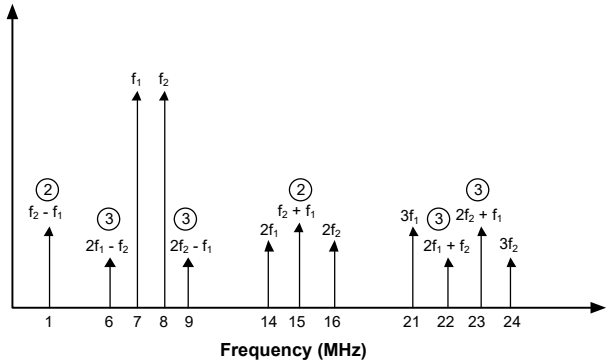


Figure 4. Locations of the Second and Third-Order Intermodulation Products when f_1 = 7MHz and f_2 = 8MHz

The frequency components at 1MHz, 14MHz, 15MHz and 16MHz are the second-order intermodulation products. The other frequency points are the third-order intermodulation products. Obviously, the third-order products are too close to the input signals to be filtered using a filter.

Spurious Free Dynamic Range (SFDR)

The SFDR is a crucial parameter that describes the relationship between the RMS amplitude of the input fundamental frequency and the amplitude of the most prominent harmonic.

Input Bandwidth

When the input signal is full-scale and the reconstructed output decreases by 3dB, in this case, the frequency of the input signal is defined as the input bandwidth.

Aperture Delay Time

The delay is the time difference between the half of rising edge of the input clock and when the sampling happens.

Aperture Delay Jitter

The aperture delay time of each single conversion is different, and the aperture jitter is the deviation of the delay time. Therefore, the delay in variation usually leads to noise when ADC converts AC signal. The signal-to-noise ratio caused by the delay jitter is expressed using the formula:

$$SNR_{Jitter} = -20\log(2\pi \times f_{in} \times t_{Jitter}) \quad (2)$$

APPLICATION INFORMATION (continued)

Converter Operation

The SGM5100/SGM5101 are CMOS pipelined multistep converters as shown in Figure 3. There are six pipelined conversion stages in the converter. Every stage contains an ADC, an interstage residue amplifier and a reconstruction DAC. The sampling process is that the ADC quantizes the input signal and the residue is generated by subtracting quantized value by the input signal. Then, the residue amplifier will amplify and output the residue. The operations of successive stages are out of phase, hence, if the residue is output by the odd stages, the residue will be acquired by the even stages, and vice versa.

The conversion from an analog input to a digital output requires five cycles as shown in Figure 1. The analog inputs should be differential to achieve optimal AC performance. To reduce the application cost, the inputs can be single-ended at the cost of a slight deterioration in harmonic suppression.

The SGM5100/SGM5101 have two operation modes, which are determined by the state of the CLK pin. The CLK input is single-ended. When the state of CLK is low, in the block "Input S/H", the input sample-and-hold capacitors directly acquire analog input, and differential sampling will be operated. The sampled input is held when the state of the CLK transits from low to high. When CLK is high, the S/H amplifier buffers the held input signal to drive the first pipelined ADC stage. When the state of CLK is high, the output of S/H amplifier is acquired. The residue of the first stage is generated and acquired by the second stage, as the CLK goes down. Meanwhile, the input signal is acquired by the S/H amplifier again. Then, the CLK rises again, and the second stage generates the corresponding residue. The third stage acquires the residue from the second stage. For the third, the fourth and the fifth stages, the same operation is implemented. The residue generated by the fifth stage is acquired by the sixth stage for producing the final result.

The additional range is implemented on the every stage except for the first one to eliminate the effect caused by the flash and amplifier offset errors. The outputs of all the stages are synchronized in digital domain, in which case the outputs can be combined appropriately before being sent to the output buffer.

Sample/Hold Operation and Input Drive

Sample/Hold Operation

The equivalent input circuit for the CMOS differential sample-and-hold is shown in Figure 5. The input signal goes through NMOS transistors to the sampling capacitors C_{SAMPLE}. All the capacitances related to the input are summed and represented by the input parasitic capacitor $C_{PARASITIC}$.

When the state of CLK is low, the input signal is connected to the sampling capacitors. The sampling capacitors will be charged and the differential input voltage is tracked by the transistors. After the CLK transits from low to high, the sampling capacitors hold the input voltage. In this mode, the transistors are open and the held voltage is transmitted to the core of ADC for further processing. When the CLK returns to low, the sampling capacitors reconnect the input signal and the new samples are acquired. Meanwhile, due to the existence of previous sample, the difference between the latest sample and last sample will lead to a charging glitch, which is proportional to the voltage variation. The amplitude of the charging glitch is determined by the difference between the last sample and the latest sample.

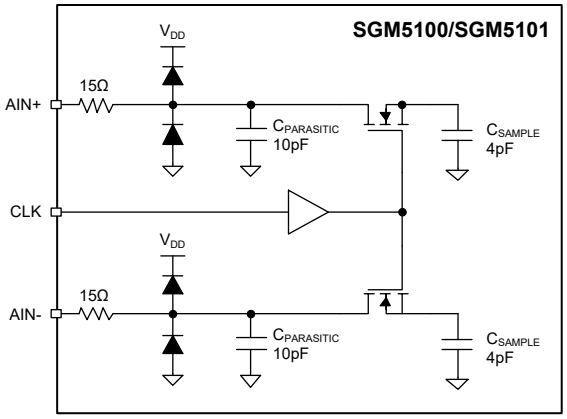


Figure 5. Equivalent Input Circuit

Single-Ended Input

The input signal can be single-ended to reduce the application costs. To operate in this mode, the AIN+ should be connected to the input signal and the AIN- must be connected to 1.5V or V_{CM}. However, it is in exchange for the deterioration of harmonic and INL, therefore, this operation mode is not recommended if the performance is required to meet the specification strictly.

Common Mode Bias

The inputs of the ADC must be driven differentially to achieve optimal performance. For the range of 2V and 1V, the swing of each input should be ±0.5V and ±0.25V respectively. The common mode bias can be provided by the pin 31 (V_{CM} output pin). The V_{CM} pin can be used to set the DC input level of a transformer or provide a reference level for the differential driven circuit of an operational amplifier. Note that a 2.2μF bypass capacitor must be connected to the V_{CM} pin.

APPLICATION INFORMATION (continued)

Input Drive Impedance

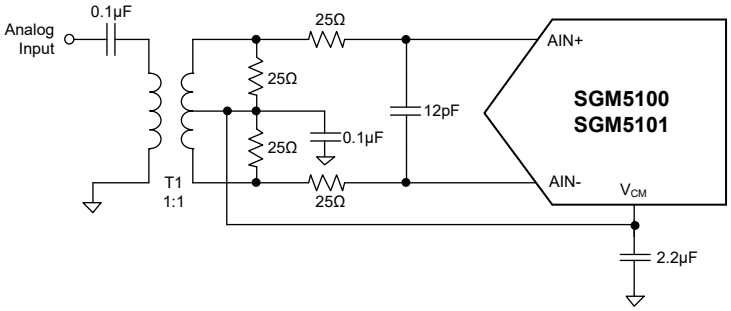
The input drive circuitry can affect the dynamic performance of the device, the effect on the second and third harmonics is the most significant. The SFDR can be influenced by the source reactance and impedance. With the falling of CLK, the sampling period starts, and the input signal is connected to the 4pF sampling capacitor by the sample-and-hold circuit. As the CLK rises, the sampling period stops. The sampling capacitor holds the sampled input. In the ideal case, the sampling capacitor should be fully charged within the sampling period $1/2F_{ENCODE}$. In the real case, it cannot be realized every time, therefore, the SFDR will degrade due to the incomplete charging. To eliminate the influence caused by the incomplete settling, the sampling glitch is designed to be as linear as possible.

It is significant to implement source match for differential inputs. If the match is not good enough, it will cause higher even order harmonics, especially the second harmonics. To achieve the best performance, the source impedance should be 100Ω or less for each input.

Input Drive Circuits

As shown in Figure 6, the SGM5100/SGM5101 are driven by an RF transformer, which contains a center tapped secondary with DC bias (V_{CM}). The input signal can be set to the optimal common voltage. It is important to terminate on the secondary of transformer, so that a common mode path for charging glitches caused by the sample-and-hold can be provided. The turns ratio of the transformer is 1:1. The ratio can be modified as long as the source impedance does not exceed 100Ω. However, the application of transformer can result in the loss of low frequency response. The performance of most small RF transformers is poor when the frequencies are below 1MHz.

As shown in Figure 7, a differential amplifier is used to convert a single-ended signal to a differential input signal. It can solve the problem with transformer. The low frequency response can be provided, however, the SFDR can also be limited when the input frequency is high due to its limited bandwidth.



NOTE: The package size of the capacitors is 0402. T1 is MA/COM ETC1-1T resistor.

Figure 6. Conversion Circuit for Converting Single-Ended to Differential

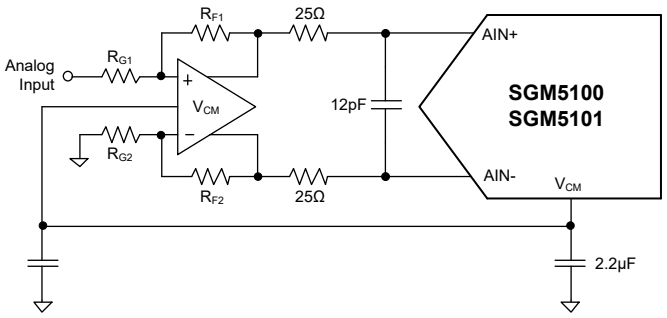


Figure 7. Differential Amplifier Circuit Used for Driving the ADC

APPLICATION INFORMATION (continued)

A single-ended analog input circuit is shown in Figure 8. The impedance match should be implemented. However, if the high performance is required, the single-ended input should be avoided.

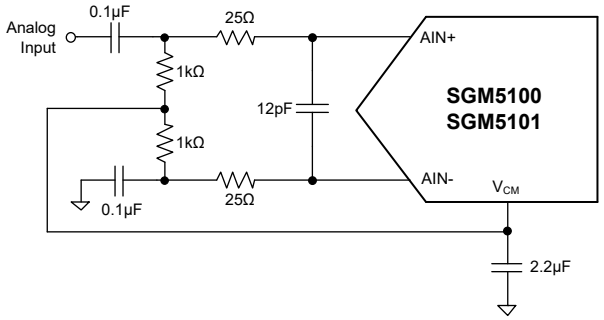
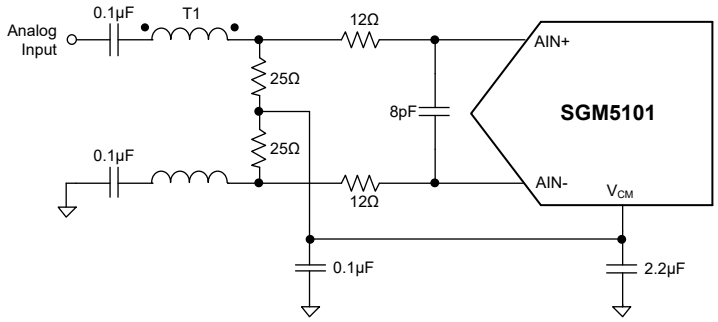


Figure 8. Single-Ended Drive Circuit

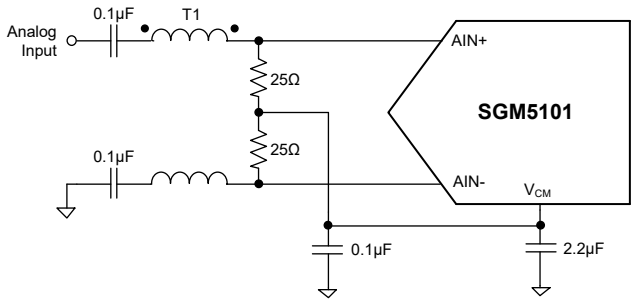
To isolate the sample-and-hold charging glitches from the drive circuitry and limit the wideband noise from the input, the 25Ω resistors and 12pF capacitor should be added.

For the SGM5101, three typical input circuits as shown Figure 9, Figure 10 and Figure 11 are recommended when the input frequency is higher than 70MHz. The flux coupled center tapped transformer can be replaced with a balun transformer, which is able to achieve better response at high frequency. The input signal can be added a 1.5V DC bias by using coupling capacitors. To maximize the ADC bandwidth, the impedance match should be implemented by adding the inductors in series as shown in Figure 11.



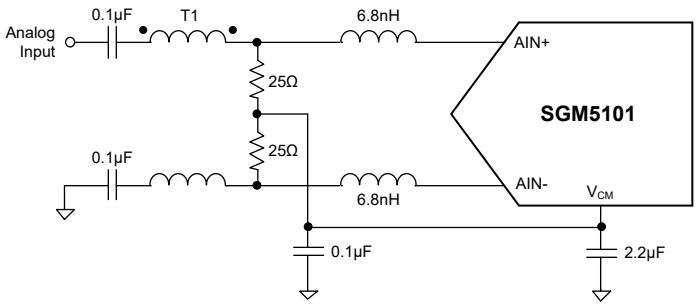
NOTE: The package size of the capacitors are 0402, T1 is MA/COM ETC1-1-13 resistor.

Figure 9. Typical Input Circuit for Input Frequencies Ranging from 70MHz to 170MHz



NOTE: The package size of the capacitors are 0402, T1 is MA/COM ETC1-1-13 resistor.

Figure 10. Typical Input Circuit for Input Frequencies Ranging from 170MHz and 300MHz



NOTE: The package size of the capacitors are 0402, T1 is MA/COM ETC1-1-13 resistor.

Figure 11. Typical Input Circuit for Input Frequencies Ranging above 300MHz

APPLICATION INFORMATION (continued)

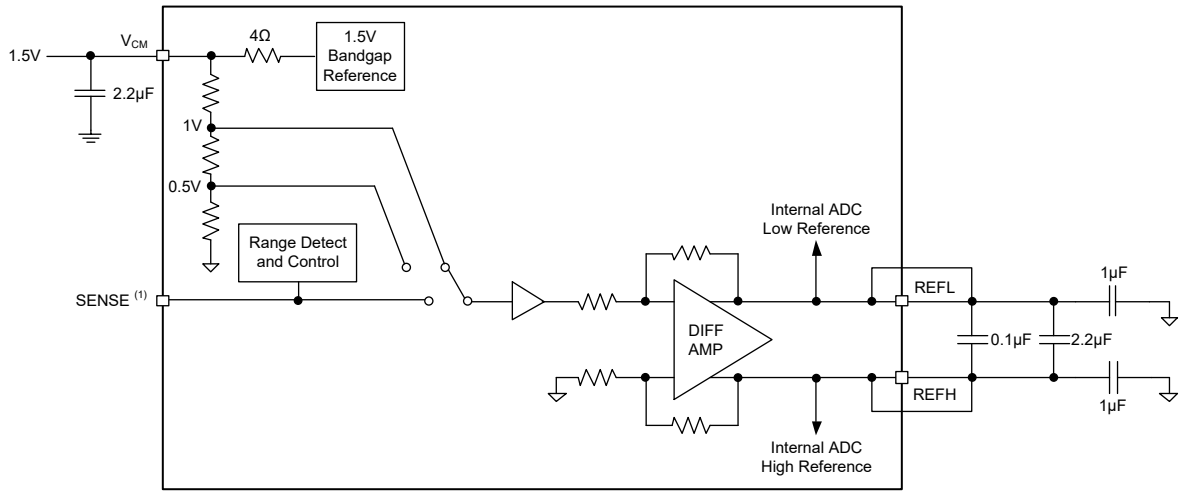
Reference Operation

The reference circuit of the device is shown in Figure 12, which includes a difference amplifier, a range detection and control unit and a 1.5V bandgap reference unit. The voltage of the internal reference can be changed by connecting the SENSE pin to different voltage level. If it is connected to V_{DD}, the reference range will be 2V (±1V). If it is connected to V_{CM}, the reference range will be 1V (±0.5V).

The 1.5V bandgap reference unit has two purposes. The first one is that it can give out a DC bias to the external input circuit to set the common mode voltage of the input. The other one is that the internal difference amplifier uses the reference to produce the differential reference voltages required by the internal ADC circuit. In addition, the output of 1.5V reference must be connected to a bypass capacitor to form a low impedance path to ground at high frequency.

The high and low references of ADC are generated by the difference amplifier. The references must be connected to the external bypass capacitors due to the internal high-speed switching circuits. The package inductance is reduced by using multiple output pins. The bypass capacitors are required to be connected following Figure 12.

As shown in Figure 13, there are two external resistors can be modified to obtain the target voltage within the reference range. The SENSE pin can be connected directly to an external reference or between the voltage divider resistors. The logic level is not suitable for driving the SENSE pin. The appropriate input of SENSE pin should be as close to the converter as possible. If the driven source of the SENSE pin is external, a 1μF bypass ceramic capacitor should be connected to the pin as close as possible.



NOTE:
1. Connect SENSE pin to V_{DD} for 2V range, connect SENSE pin to V_{CM} for 1V range.
For SGM5100, Range = 2 × V_{SENSE} when V_{SENSE} is between 0.5V and 1V.
For SGM5101, Range = 2 × V_{SENSE} when V_{SENSE} is between 0.5V and (1.1 × V_{CM})/1.5.

Figure 12. Equivalent Reference Circuit

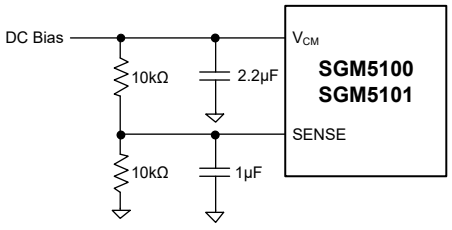


Figure 13. 1.5V Reference Range

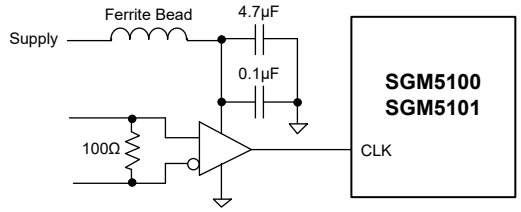
APPLICATION INFORMATION (continued)

Input Range

The selection of input range is dependent on the specific application. If the SFDR is the most significant parameter, the input range should be 1V, but the drawback is that the SNR will be decreased by 5.8dB. In contrast, if the SNR is the key point, the input range can be 2V, which can achieve the highest SNR and keep a good SFDR.

Driving the Clock Input

For the SGM5100, a signal at CMOS or TTL level can be used to directly drive the CLK. Before the CLK pin, a low-jitter CMOS converter and a differential clock can also be used (see Figure 14).



NOTE: To implement LVDS, FIN1002 or FIN1018 should be used. To implement PECL, AZ100ELT21 or similar components should be used.

Figure 14. Using PECL or LVDS as the Input of CLK

For the SGM5101, the input of CLK can be CMOS or TTL level. Another option is to use a sinusoidal clock and a low-jitter squaring circuit prior to the CLK pin (see Figure 15).

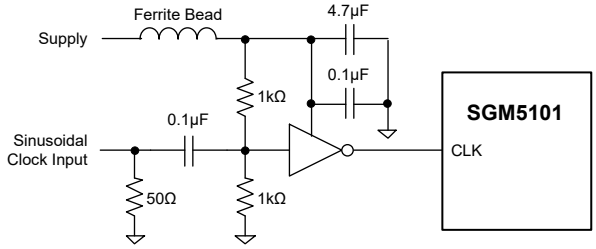


Figure 15. Using Sinusoidal as the Input of Single-Ended CLK (SGM5101)

The quality of CLK and the analog input can both affect how well the SGM5100/SGM5101 suppress noise. The presence of any noise on the CLK will cause extra aperture jitter, which will be combined with the inherent ADC aperture jitter.

For the applications such as digitizing input with high frequency which are sensitive to jitter. The amplitude should be as large as possible. In addition, if the CLK of ADC is sinusoidal, the CLK signal should be filtered to suppress the wideband noise and distortion.

For the SGM5101, when the jitter is crucial in certain applications, for instance, when the input frequencies are high frequencies, it is recommended to utilize the highest amplitude possible. Additionally, if the ADC is synchronized with a sinusoidal signal, it is advisable to apply filtering to the CLK signal. This filtering will help decrease wideband noise and distortion products that are produced by the source.

Figure 14 and Figure 16 indicate two other methods to convert a differential clock to the single-ended clock. A transformer will not result in the increment of phase noise.

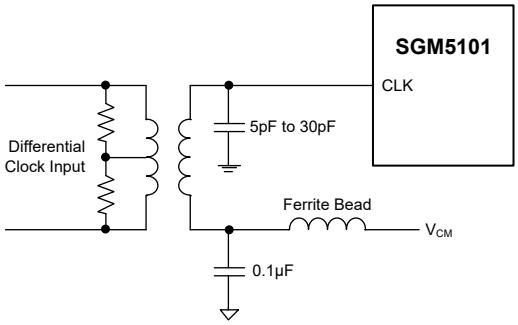


Figure 16. Using a Transformer to Drive LVDS or PECL CLK (SGM5101)

The transformer can have a termination that is suitable for the signal used. Considering the lower voltage differential signals, it is best to use a transformer with a 1:4 impedance ratio. If the differential signals come from a different plane, the center tap should be bypassed to ground via a capacitor near the ADC. A 10Ω to 20Ω series resistor may be needed to serve as a low pass filter to reduce the high frequency noise which could be induced into the clock line by nearby digital signals, and a dampening mechanism for reflections if a capacitor is used at the input. As this could lead to peaking and it may be necessary according to the length of the transmission line.

APPLICATION INFORMATION (continued)

Maximum and Minimum Conversion Rates

The maximum conversion rates for the SGM5100/SGM5101 are 10MSPS (SGM5100) and 40MSPS (SGM5101), respectively. In order to ensure the normal operation of the ADC, the duty cycle of the CLK should be 50% and the error should be within ±5%.

For the SGM5101, if the duty cycle of the input CLK is not 50%, an optional duty cycle stabilizer can be used to improve the CLK. The operation process of the duty cycle stabilizer unit is that only the rising edge of CLK is used, and the falling edge is ignored. The internal falling edge generated by phase-locked loop is used. Therefore, the stabilizer can make the duty cycle of internal clock a constant of 50, when the duty cycle of input clock is in the range from 40% to 60%. If the CLK signal is disconnected for a long period, it takes a hundred cycles for the PLL to lock onto the input CLK. The MODE pin needs to be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using a voltage divider to enable the stabilizer.

The pipelined ADC relies on the capacitors with the small value to store the input signal. The capacitors may discharge due to the junction leakage. Therefore, the drop of the sample-and-hold circuits determines the minimum operating frequency of ADC. For the SGM5100/SGM5101, the sampling rate must be higher than 1MSPS.

Digital Outputs

The conversion between the analog input voltage, the digital data bits, and the overflow bit is demonstrated in Table 1.

Table 1. Output Codes vs. Input Voltage

AIN+ - AIN- (2V Range)	OF	D13 - D0	
		Offset Binary	Two's Complement
> +1.000000V	1	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	0	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	0	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	0	10 0000 0000 0001	00 0000 0000 0001
0.000000V	0	10 0000 0000 0000	00 0000 0000 0000
-0.000122V	0	01 1111 1111 1111	11 1111 1111 1111
-0.000244V	0	01 1111 1111 1110	11 1111 1111 1110
-0.999878V	0	00 0000 0000 0001	10 0000 0000 0001
-1.000000V	0	00 0000 0000 0000	10 0000 0000 0000
< -1.000000V	1	00 0000 0000 0000	10 0000 0000 0000

Digital Output Buffers

The equivalent circuit for a single output buffer is depicted in Figure 17. The power for the output buffer comes from OV_{DD} and OGND, which are separate from the power and ground of the ADC.

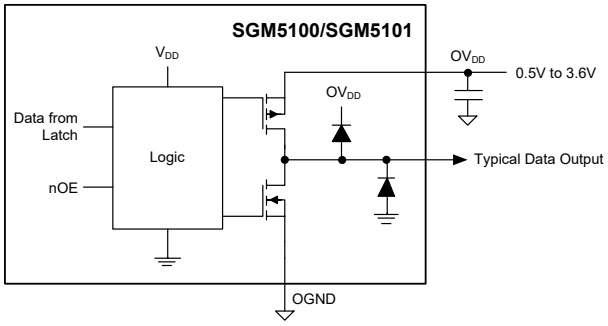


Figure 17. Digital Buffer at the Output Stage

When using high-speed/high-resolution converters like the SGM5100/SGM5101, it is important to take the impact of the digital output loading on performance into consideration. To prevent any potential interaction between the digital outputs and the sensitive input circuitry, it is recommended to minimize the capacitive load on the digital outputs. One way to achieve this is to buffer the output using a device like the ALVCH16373 CMOS latch. For optimal operation at full speed, it is recommended to keep the capacitive load below 10pF.

Additionally, using the lower OV_{DD} voltages can also help to reduce interference caused by the digital outputs.

Data Format

There are two data formats for the SGM5100/SGM5101. The parallel digital output can be set to offset binary or two's complement format by using the MODE pin. When the MODE pin is connected to GND or $1/3V_{DD}$, the output format is offset binary. On the other hand, when the MODE pin is connected to $2/3V_{DD}$ or V_{DD}, the output format is two's complement. To determine the logic states, an external resistor divider can be utilized. The logic states for the MODE pin are demonstrated in Table 2.

Table 2. MODE Pin Function

MODE Pin	Output Format	Clock Duty Cycle Stabilizer
0	Offset Binary	Off
$1/3V_{DD}$	Offset Binary	On
$2/3V_{DD}$	Two's Complement	On
V_{DD}	Two's Complement	Off

APPLICATION INFORMATION (continued)

Overflow Bit

If the output of OF is a logic high, it indicates that the converter is in a state of either being overranged or underranged.

Output Driver Power

The output drivers can be separated from the analog circuitry by separating output power from ground pins. It is important to connect the power supply OV_{DD} of the digital output buffers to the same power supply as the logic being driven. For instance, if the ADC is connected to a DSP operating with 1.8V power supply, the OV_{DD} should also be connected to that same 1.8V supply.

The OV_{DD} can operate at any voltage in the range of 1.65V to 3.6V. The OGND should be strictly 0V (GND). The logic outputs will vary between OGND and OV_{DD}.

Output Enable

For the SGM5100, the data outputs can be turned off using the output enable (nOE) pin. When nOE is set to a high state, all data outputs, excluding OF, are disabled. The Hi-Z state of the outputs is designed to multiplex the data bus of several SGM5100s.

For the SGM5101, the data outputs can be turned off using the output enable (nOE) pin. When nOE is set to high, all data outputs, excluding OF, are disabled. However, during high-speed operation, the time required to access the data and release the bus is too slow to enable or disable the outputs. The Hi-Z state of the outputs is meant to be used when there is no activity for a long period.

Sleep and Nap Modes

To conserve power, the converter can be put into sleep or nap modes. The normal operation is achieved by connecting SHDN to GND. The sleep mode is activated by connecting SHDN to V_{DD} and nOE to V_{DD}, which turns off all circuitry including the reference, resulting in a power dissipation of around 0.05mW. The recharging and stabilization of the reference capacitors after exiting the sleep mode cause a brief delay before the output data becomes valid again, which typically takes only milliseconds. On the other hand, the nap mode is achieved by connecting SHDN to V_{DD} and nOE to GND, the typical power consumption is about 6mW. During the nap mode, the on-chip reference circuit remains active, resulting in the quicker restoration compared to the sleep mode, which usually requires 100 clock cycles. During the sleep and nap modes, the digital outputs are turned off and set to high impedance state.

Grounding and Bypassing

For the optimal performance, it is necessary to have a printed circuit board that has a clean and continuous ground plane for the SGM5100/SGM5101. It is recommended to use a multilayer board with an internal ground plane. When designing the layout for the printed circuit board, it is important to keep the digital and analog signal lines as separate as possible. It is crucial to avoid putting any digital track alongside an analog signal track or placing it underneath the ADC.

To ensure the optimal performance, it is recommended to use high-quality ceramic bypass capacitors for the V_{DD}, OV_{DD}, V_{CM}, REFH and REFL pins. These capacitors should be placed as close to the pins as possible. Pay particular attention to the 0.1μF capacitor between REFH and REFL pins, which should be placed as near to the device as possible, ideally within 1.5mm or less. It is recommended to use a ceramic capacitor of size 0402 for this purpose. The larger 2.2μF capacitor between REFH and REFL pins can be placed at a slightly greater distance. Additionally, it is important to keep the traces connecting the pins and bypass capacitors short and wide.

To reduce capacitance and noise interference, it is recommended to align the differential inputs of the SGM5100/SGM5101 and keep them close. Additionally, it is recommended to keep the input traces as short as possible.

Heat Transfer

The majority of the heat produced by the SGM5100 /SGM5101 is transferred from the die to the printed circuit board through the exposed pad on the bottom side and the package leads. To ensure the optimal electrical and the thermal efficiency, it is important to solder the exposed pad to a sizable grounded pad on the PCB. It is important to ensure that all ground pins are correctly connected to a sufficiently sized ground plane.

APPLICATION INFORMATION (continued)

Clock Sources for Undersampling

As the input frequency increases, undersampling amplifies the need for a clock source, making the impact of clock jitter or phase noise more pronounced.

If the absolute clock frequency accuracy is not a major concern and only one ADC is needed, it is possible to use a 3V canned oscillator from vendors like Saronix or Vectron. This oscillator should be placed near the ADC and directly connected to it. In the case of a distance existing between the oscillator and the ADC, it is recommended to employ source termination to minimize any potential ringing, even if the distance is relatively short. It is important to prevent the clock from exceeding the power supplies, as it will negatively impact performance. Avoid using a narrow band filter on the clock signal unless the clock source is sinusoidal, as this can introduce phase noise due to the rise and fall time artifacts present in the typical digital clock signals.

The most accurate oscillators produce single-ended sinusoidal outputs, and using a filter near the converter can be advantageous for these devices. To minimize round-trip reflection times and the vulnerability of the traces between the filter and the ADC, it is recommended to place this filter in close proximity to the ADC. When dealing with close-in phase noise sensitivity, it is crucial to have a highly stable power supply for the oscillators and any buffers. Fluctuations in the supply can result in phase noise due to variations in propagation delay.

Although these clock sources can be considered digital devices, the key is not to power them with a digital power source. If the clock drives digital devices such as an FPGA at the same time, it is recommended to place the oscillator or any clock fan-out devices close to the ADC, and prioritize the routing to the ADC. To avoid any disruption caused by high frequency noise from the FPGA on the clock fan-out device's substrate, it is important to implement series termination at the driver for the clock signals going to the FPGA. In order to utilize an FPGA as a configurable divider, it is necessary to synchronize the signal by employing the original oscillator. Both the retiming flip-flop and the oscillator should be placed near the ADC, and powered by a stable and noise-free source.

It is recommended to use differential clock distribution in cases where there are multiple ADCs or when the clock source is located far away. It is beneficial to reduce EMI and prevent noise from digital sources, which can be radiated or propagated through the waveguides in multilayer PCBs. It is recommended to place the differential pairs in proximity to each other and away from the other signals. Both sides of the differential pair should have the copper protection, with a spacing of at least three times the distance between the traces. Additionally, the vias for grounding should be utilized, with a maximum separation of 1/4 inch.

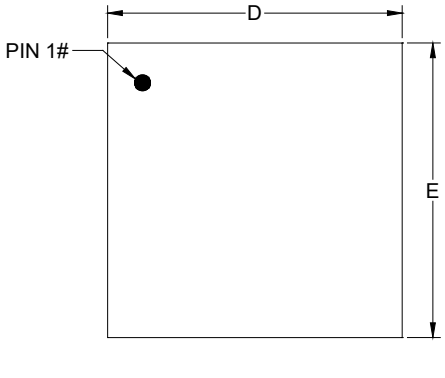
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

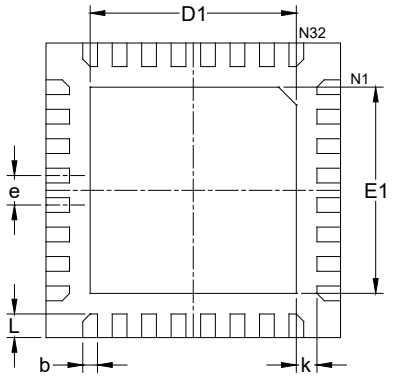
Changes from Original (JULY 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

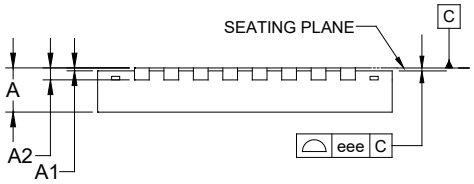
TQFN-5×5-32DL



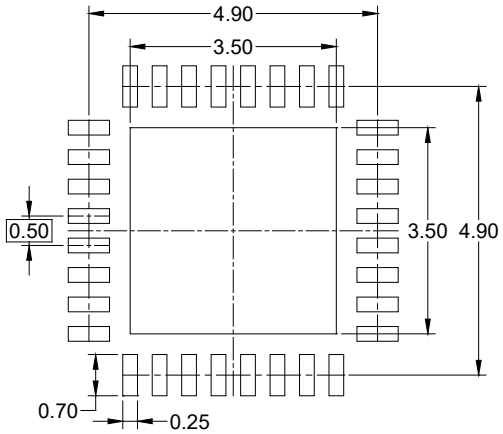
TOP VIEW



BOTTOM VIEW



SIDE VIEW



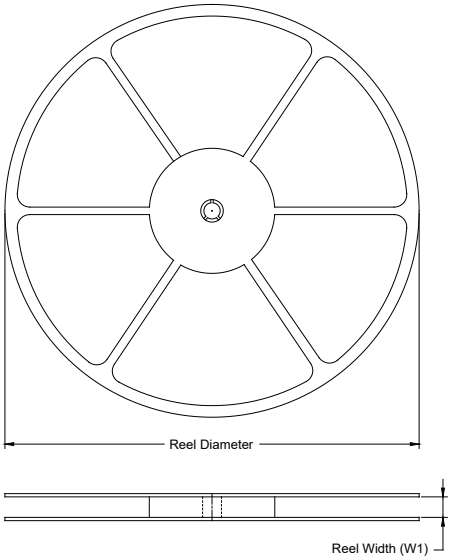
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.100
A2		0.203 REF	
b	0.180	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.400	3.500	3.600
E1	3.400	3.500	3.600
e		0.500 BSC	
k		0.350 REF	
L	0.300	-	0.500
eee		0.080	

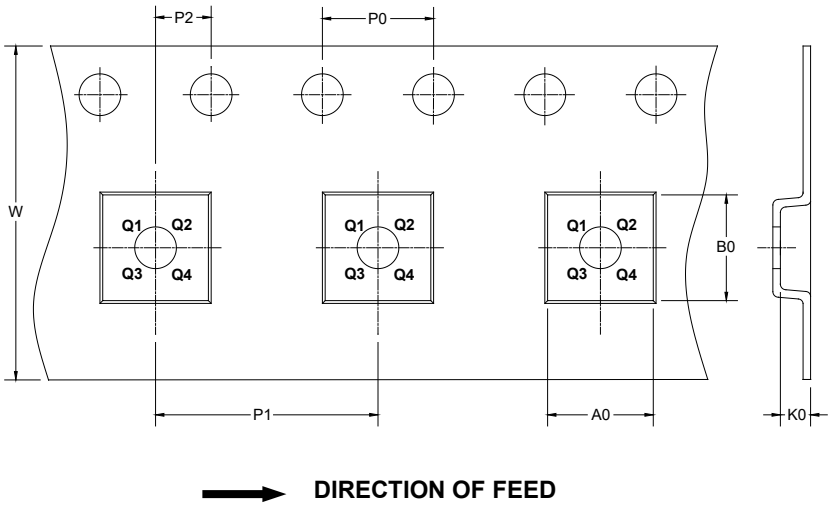
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



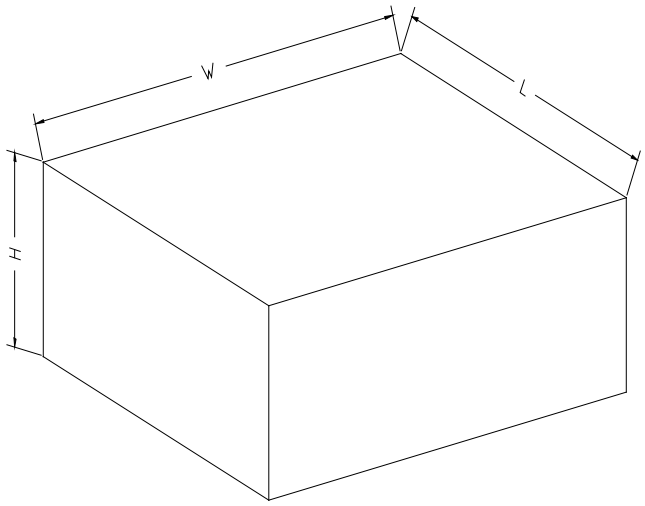
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32DL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002