SGM2528
5A, 12V Electronic Fuse (eFuse) with Thermal Shutdown

GENERAL DESCRIPTION

The SGM2528 is a compact electronic fuse (eFuse) with a complete set of protection functions. The wide operating voltage range is specifically designed for many popular DC buses. The SGM2528 provides excellent accuracy, making it very suitable for many system protection applications.

It provides accurate over-voltage (OV) and under-voltage lockout (UVLO) protections, which ensure tight supervision of bus voltages and eliminate the need for supervisor circuits. The over-voltage (OV) protection will clamp the eFuse output at a fixed level during input voltage surges. During the input voltage transient, the internal FET remains on, which allows the load to continue to operate. If the transient duration remains long, the accumulated heat will cause the eFuse thermal shutdown. Once in thermal shutdown, latch-off and auto-retry thermal options are available.

The SGM2528 is available in a Green TDFN-3×3-10L package.

FEATURES

- **Wide Input Voltage Range from 9V to 18V with Surge up to 30V**
- **Extremely Low $R_{DS(ON)}$ for the Integrated Protection Switch: 26mΩ (TYP)**
- **3-State EN/FAULT Pin, Bidirectional Interface**
- **Programmable Soft-Start Time**
- **Programmable Current Limit up to 5A**
- **Thermal Shutdown Options:**
  - **SGM2528A: Thermal Latch-Off with V_{CLAMP}**
  - **SGM2528B: Thermal Auto-Retry with V_{CLAMP}**
  - **SGM2528C: Thermal Latch-Off without V_{CLAMP}**
- **Fault Output for Thermal Shutdown**
- **Accurate Under-Voltage Lockout**
- **Accurate Over-Voltage Clamp (SGM2528A and SGM2528B)**
- **Available in a Green TDFN-3×3-10L Package**

APPLICATIONS

Hard Drives

PCIE SSD

Motherboard Power Management

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2528A	TDFN-3×3-10L	-40℃ to +125℃	SGM2528AXTD10G/TR	SGM 2528AD XXXXX	Tape and Reel, 4000
SGM2528B	TDFN-3×3-10L	-40℃ to +125℃	SGM2528BXTD10G/TR	SGM 2528BD XXXXX	Tape and Reel, 4000
SGM2528C	TDFN-3×3-10L	-40℃ to +125℃	SGM2528CXTD10G/TR	SGM 2528CD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X XXX X

- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Operating Input Voltage Range [(1)]

V_{CC} to GND .... -0.3V to 25V

Transient (100ms) .... -0.6V to 25V

Surge (8μs/20μs) 30V

Other Pins Voltage Range

SOURCE, I_{LIMIT} to GND .... -0.3V to 25V

dV/dt, EN/FAULT to GND .... -0.3V to 5.5V

Package Thermal Resistance

TDFN-3×3-10L, θ_{JA} .... 90℃/W

TDFN-3×3-10L, θ_{JB} .... 54℃/W

TDFN-3×3-10L, θ_{JC} .... 52℃/W

Junction Temperature .... +150℃

Storage Temperature Range .... -65℃ to +150℃

Lead Temperature (Soldering, 10s) .... +260℃

ESD Susceptibility

HBM 2000V

CDM 1000V

NOTE: 1. Negative voltages can be withstood by the device without damage as long as the power dissipation is limited to the power rating allowed by the package.

RECOMMENDED OPERATING CONDITIONS

Operating Input Voltage Range

Steady-State .... -0.3V to 18V

Operating Junction Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

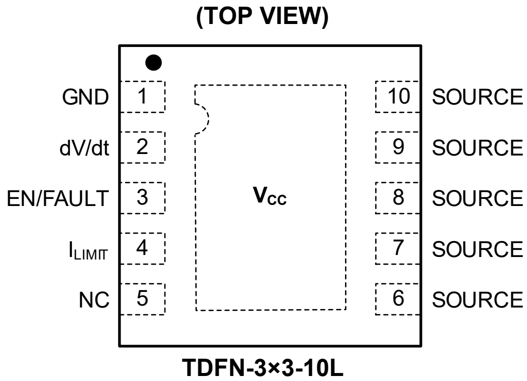
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Ground.
2	dV/dt	Internal dV/dt Circuit. Leaving this pin open will allow the device to ramp up in 2ms. An external capacitor between this pin and GND will set the slew rate according to the application requirements.
3	EN/FAULT	Enable or Fault Pin. This pin is a 3-state, bidirectional interface. Asserting EN/FAULT pin high enables the device. When the thermal shutdown occurs, the device sinks current from EN/FAULT, and pulls the pin low to alert the host (this pin is used as output port).
4	I_{LIMIT}	Current Limit Pin. This pin is used to set the overload and short-circuit current limit levels by placing a resistor.
5	NC	No Connection.
6 - 10	SOURCE	Power Output Pins.
Exposed Pad	V_{CC}	Power Input Pin. Power input and supply voltage of the device.

ELECTRICAL CHARACTERISTICS

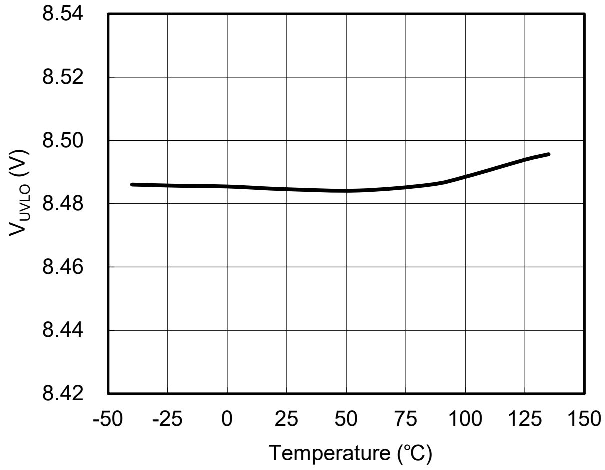
(T_J = +25℃, V_{CC} = 12V and dV/dt pin is open, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power FET						
Delay Time	t_{DLY}	Enabling of chip to I_D = 100mA with 1A resistive load		386		μs
Kelvin On-Resistance	$R_{DS(ON)}$	T_J = +25℃	21	26	31	mΩ
		T_J = +135℃		38		
Off-State Output Voltage	V_{OFF}	V_{CC} = 18V, V_{GS} = 0V, R_L = ∞		20	200	mV
Continuous Current	I_D			5		A
Thermal Latch						
Shutdown Temperature	T_{SD}			158		℃
Thermal Hysteresis	T_{HYS}	Decrease in die temperature for turn-on; does not apply to latch-off options.		22		℃
Under/Over-Voltage Protection						
Output Clamping Voltage	V_{CLAMP}	Over-voltage protection, V_{CC} = 18V	14.5	15	15.5	V
Under-Voltage Lockout	V_{UVLO}	Turn on, voltage going high	8.2	8.5	8.8	V
UVLO Hysteresis	V_{HYS}			0.83		V
Current Limit						
Kelvin Short-Circuit Current Limit	$I_{LIM\text{-}SC}$	R_{LIMIT} = 77Ω, V_{CC} - V_{SOURCE} = 1V	0.5	0.95	1.4	A
Kelvin Overload Current Limit	$I_{LIM\text{-}OL}$	R_{LIMIT} = 77Ω		3		A
dV/dt Circuit						
Output Voltage Ramp Time	t_{SLEW}	Enable to V_{OUT} = 11.7V	1.3	2	2.8	ms
Maximum Capacitor Voltage	V_{MAX}				5.3	V
EN/FAULT Pin						
Logic Level Low	$V_{IN\text{-}LOW}$	Output disabled	0.45	0.55	0.65	V
Logic Level Mid	$V_{IN\text{-}MID}$	Thermal fault, output disabled	1.35	1.45	1.55	V
Logic Level High	$V_{IN\text{-}HIGH}$	Output enabled	2.5	2.62	2.75	V
High State Maximum Voltage	$V_{IN\text{-}MAX}$		4.9	5.1	5.3	V
Logic Low Sink Current	$I_{IN\text{-}LOW}$	$V_{EN/FAULT}$ = 0V		-15	-22	μA
Power Supply						
Quiescent Current	I_Q	Operating		110	140	μA
		Shutdown		48		

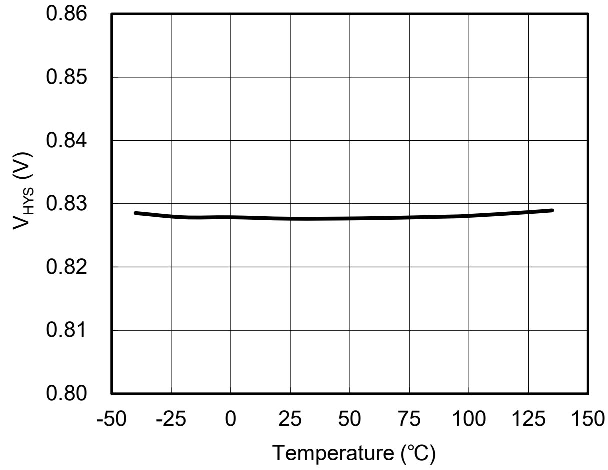
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

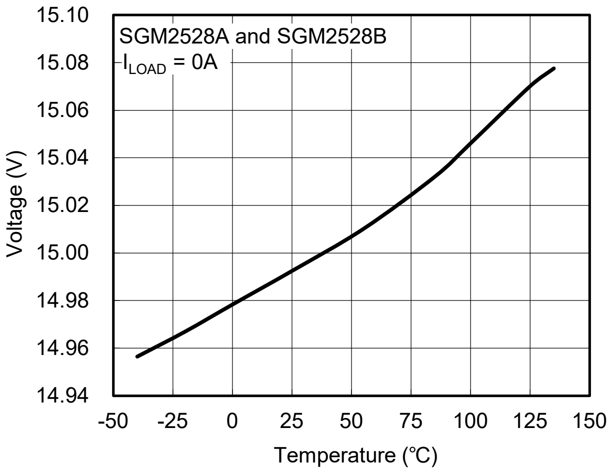
UVLO Turn-On Voltage vs. Temperature



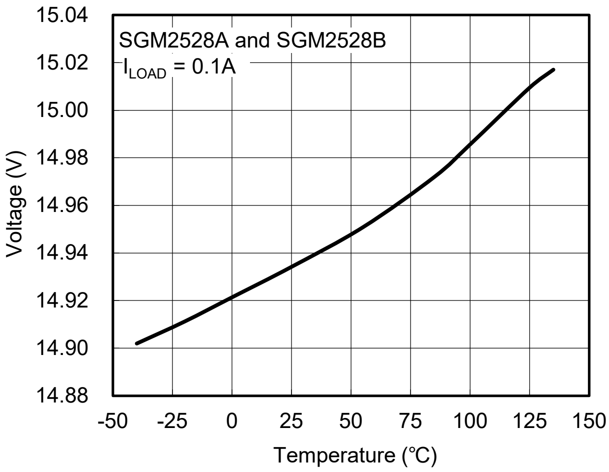
UVLO Hysteresis vs. Temperature



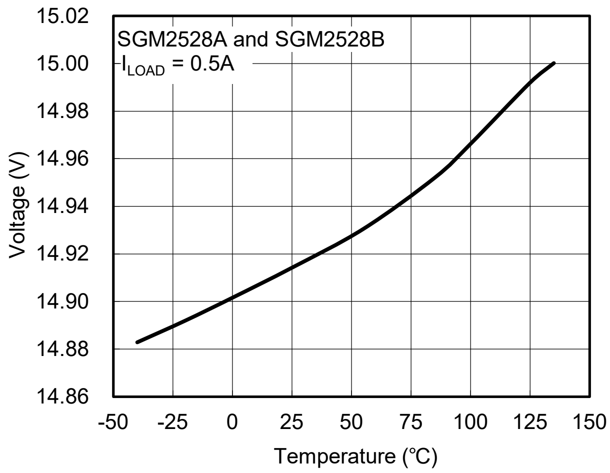
Output Clamping Voltage vs. Temperature



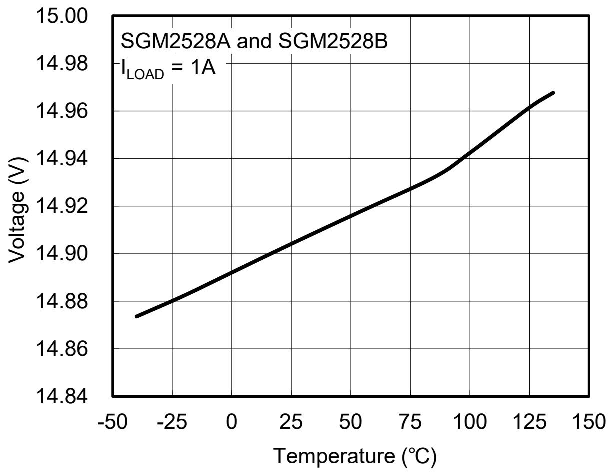
Output Clamping Voltage vs. Temperature



Output Clamping Voltage vs. Temperature

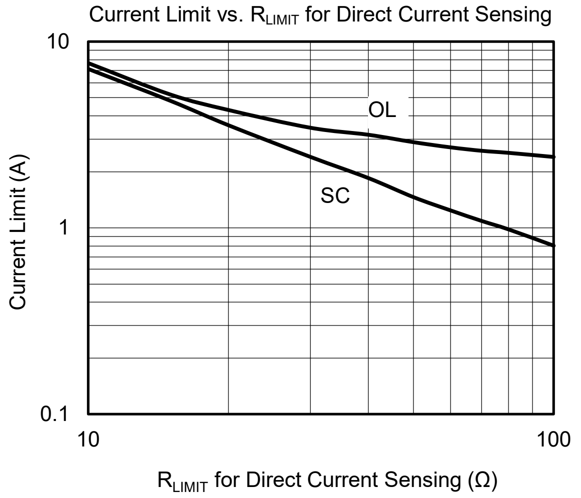


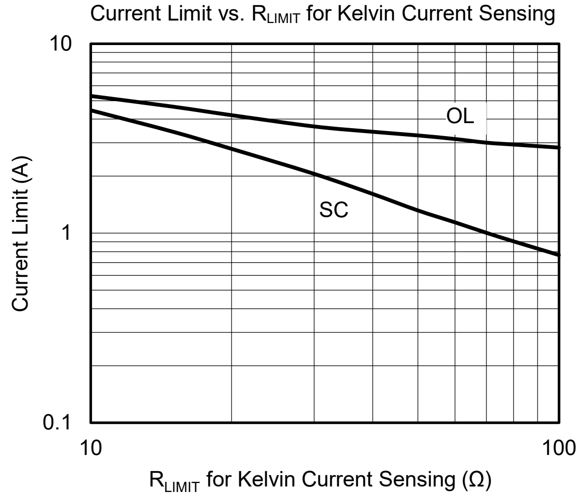
Output Clamping Voltage vs. Temperature

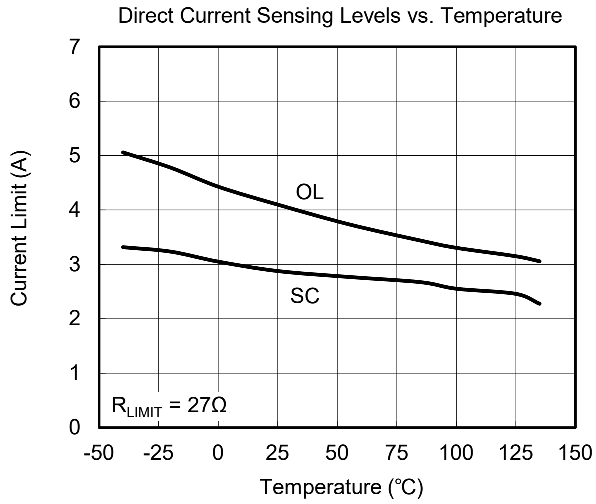


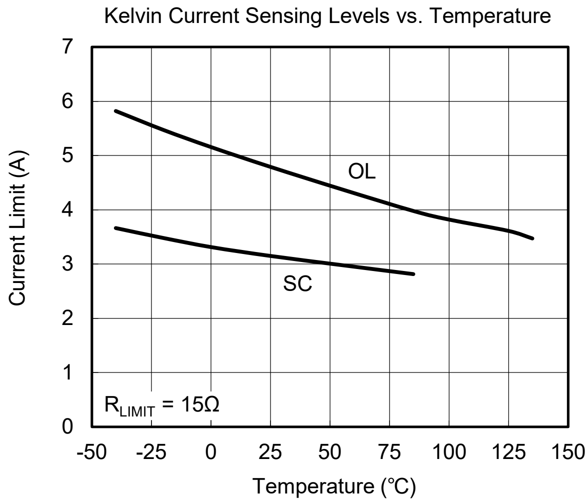
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

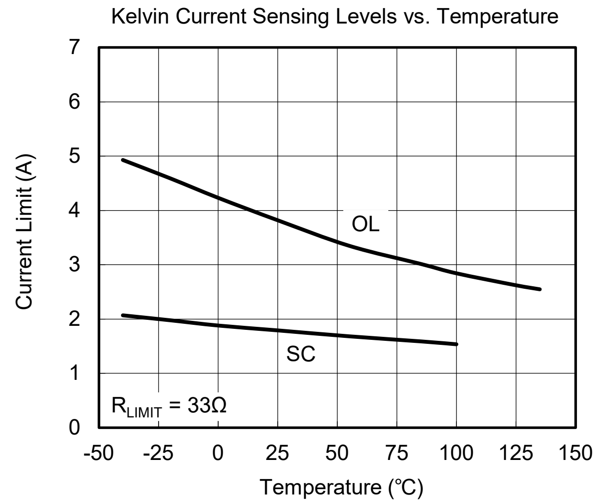
T_J = +25℃, unless otherwise noted.

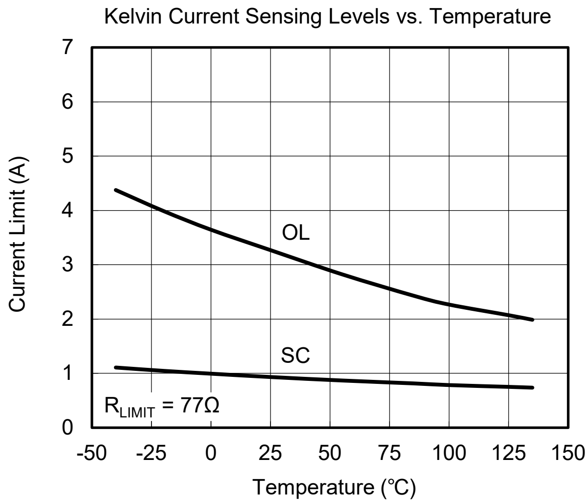






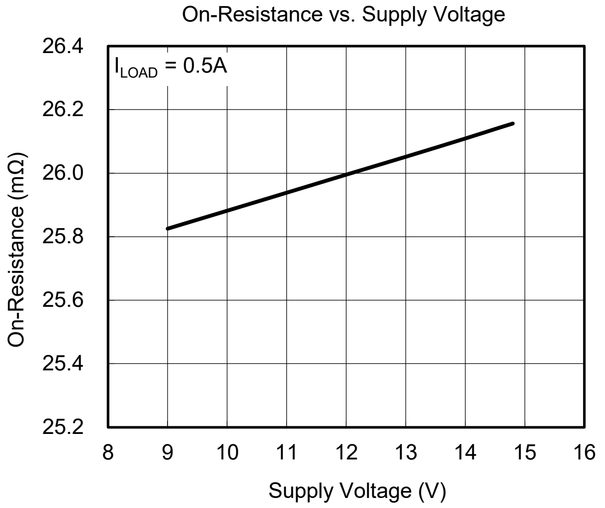


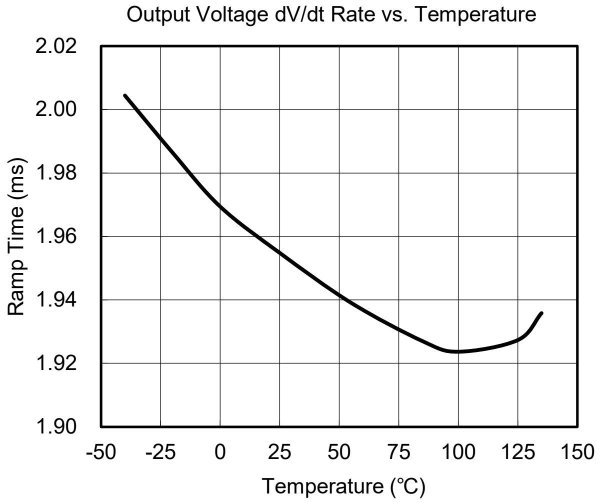


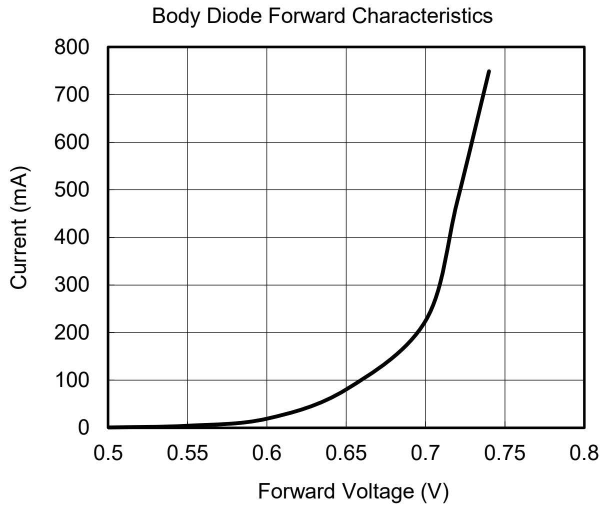


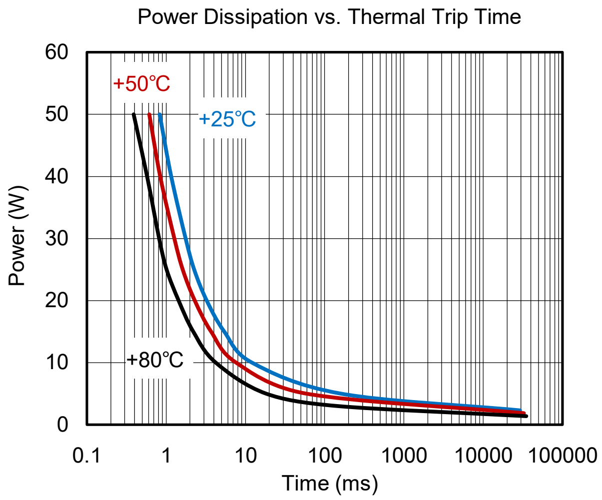
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.





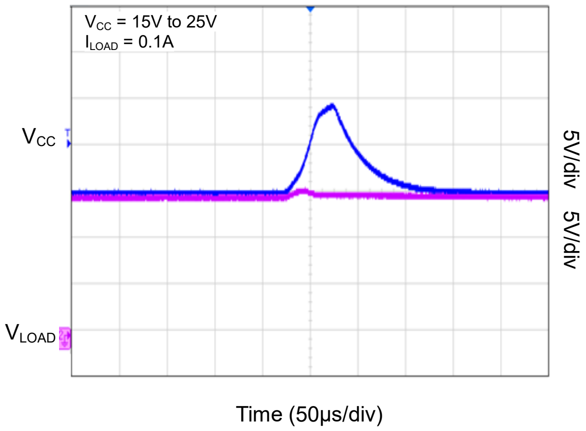




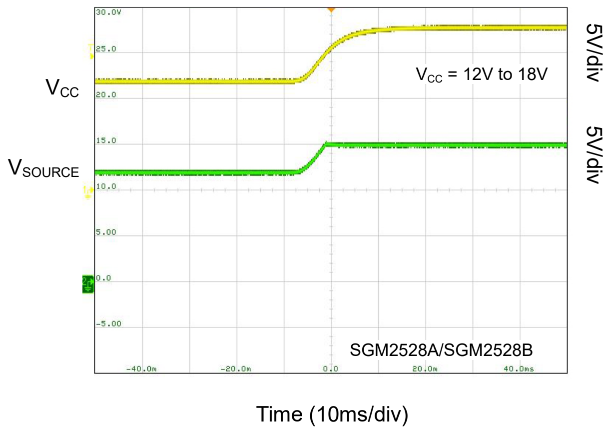
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

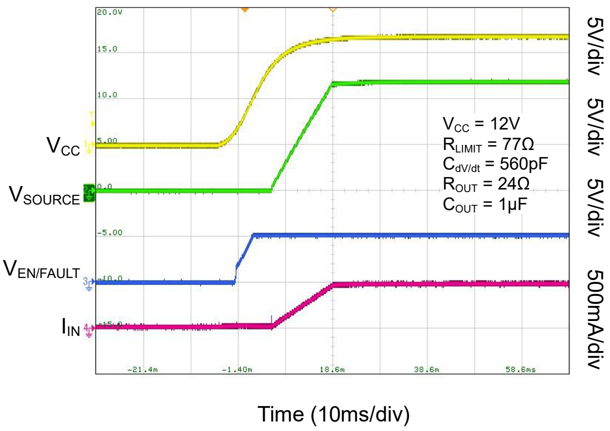
Input Transient Response



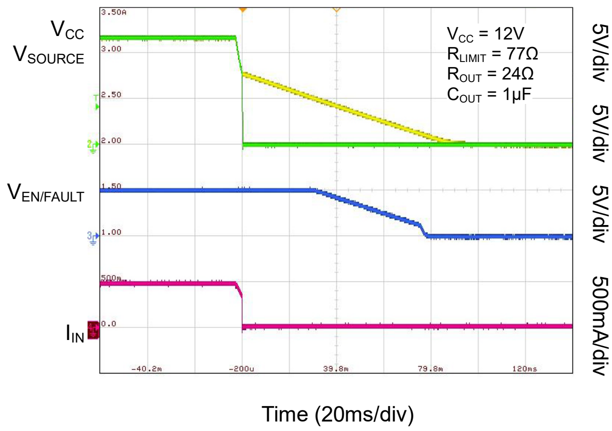
VCC Over-Voltage Clamping



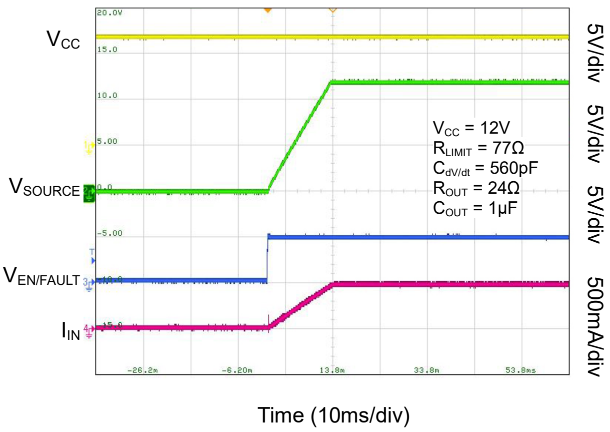
VCC Power-On



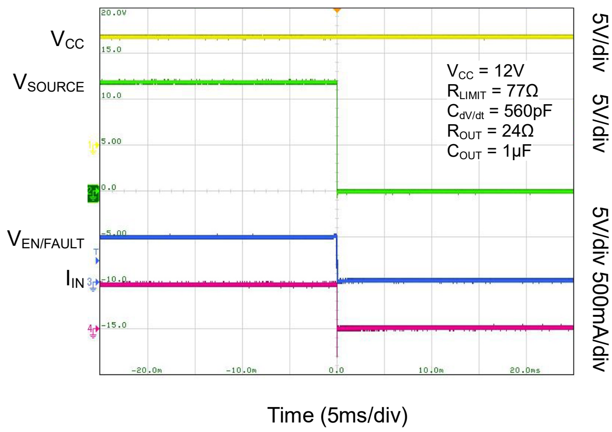
VCC Power-Off



EN/FAULT Power-On



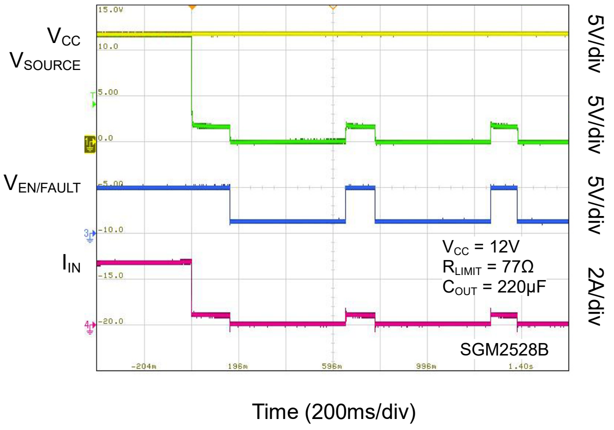
EN/FAULT Power-Off



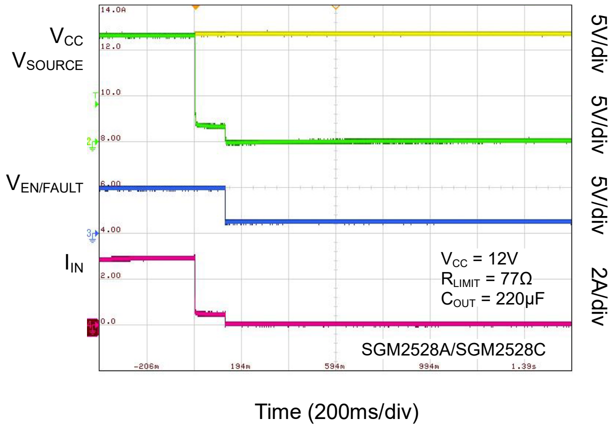
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25°C, unless otherwise noted.

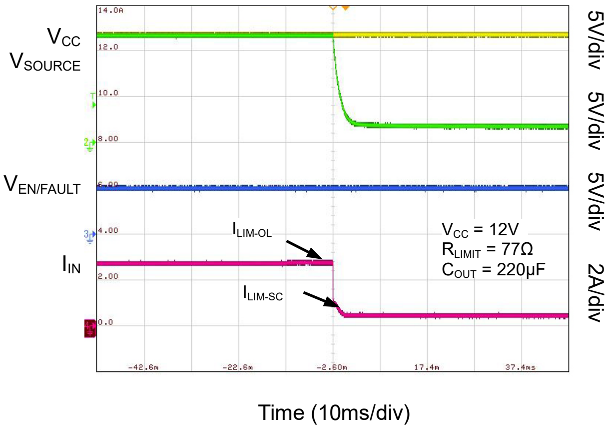
Over-Current Response



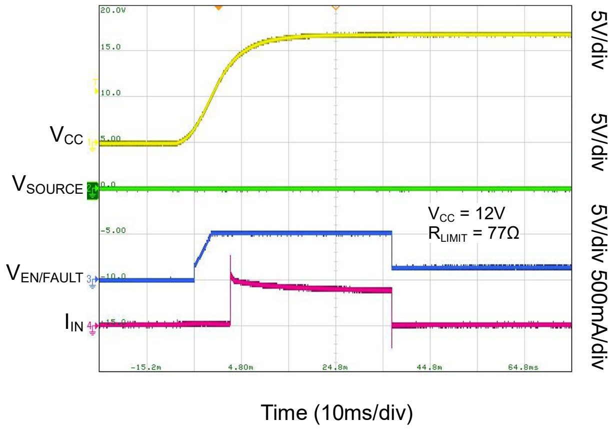
Over-Current Response



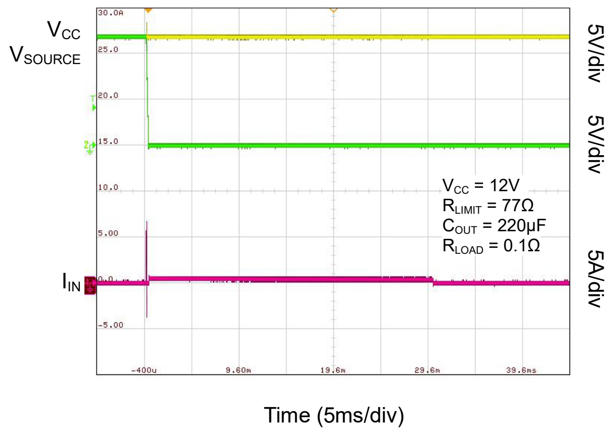
Overload Current Limit & Short-Circuit Current Limit



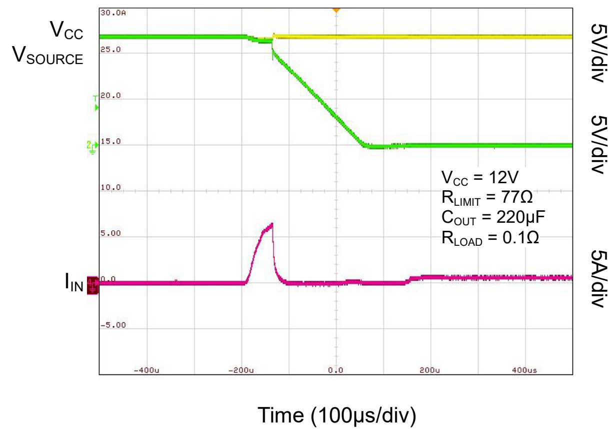
Wake-Up to Short-Circuit



Short-Circuit Response



Short-Circuit (Zoom-In)



TYPICAL APPLICATION CIRCUITS

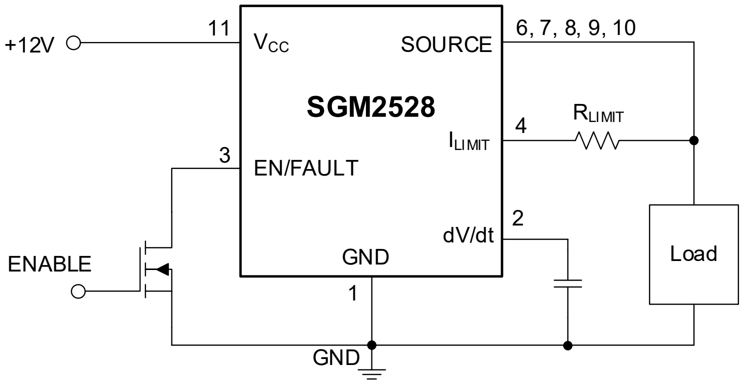


Figure 1. Application Circuit with Direct Current Sensing

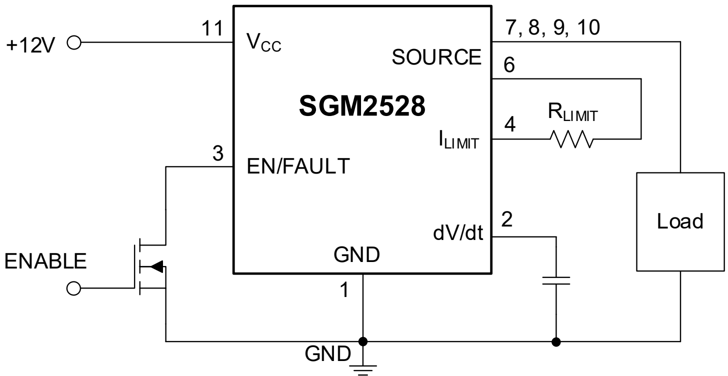


Figure 2. Application Circuit with Kelvin Current Sensing

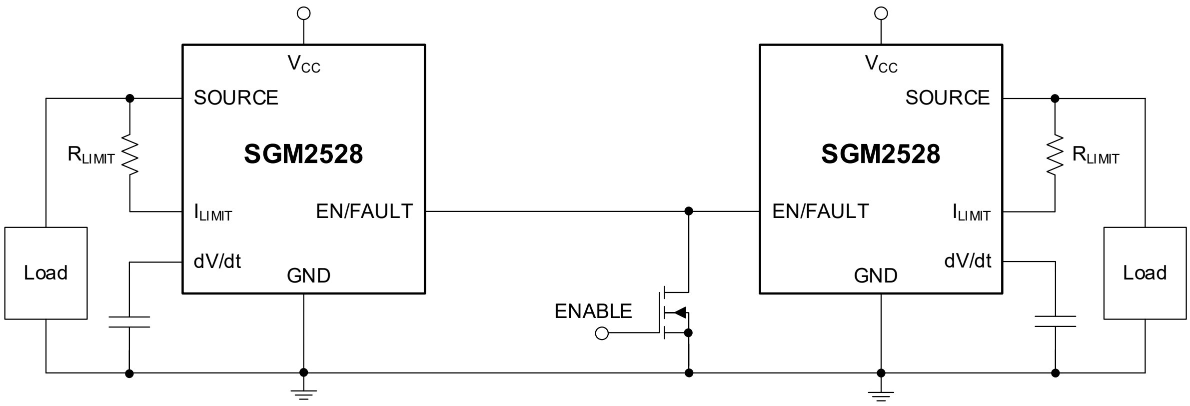
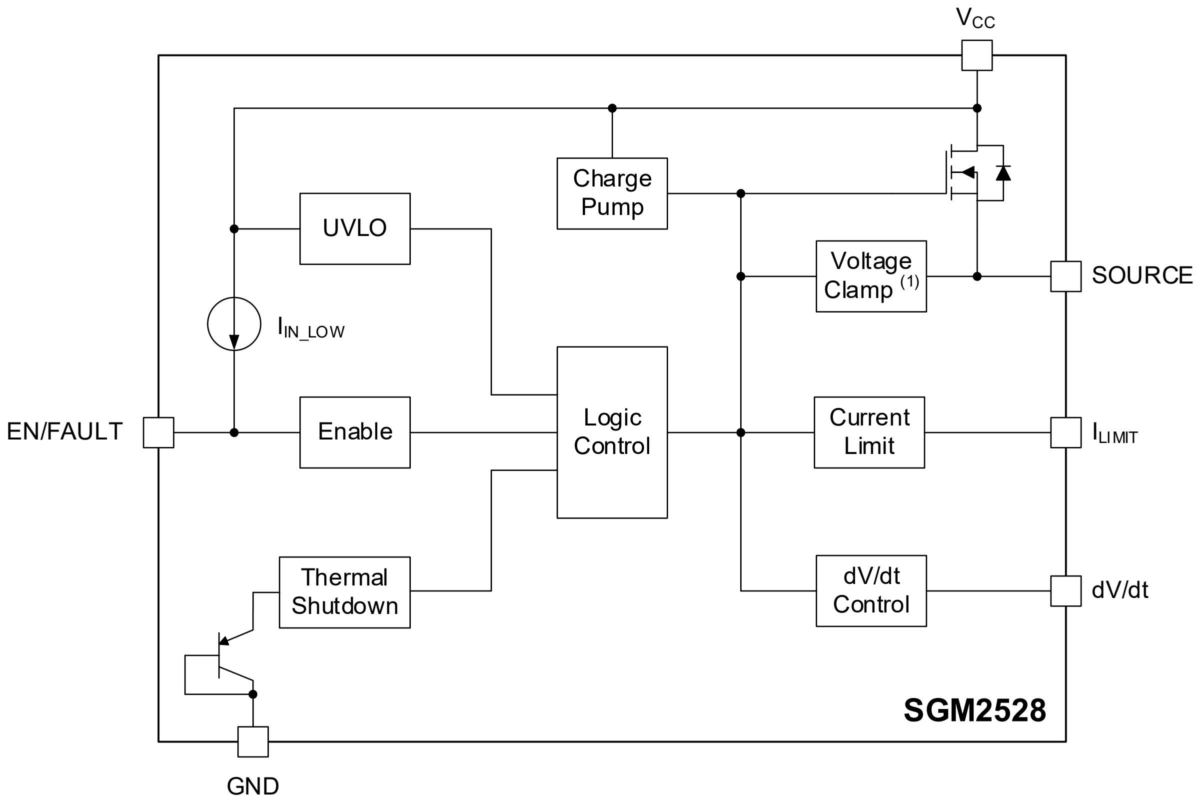


Figure 3. Common Thermal Shutdown

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. SGM2528A and SGM2528B versions.

Figure 4. Block Diagram

APPLICATION INFORMATION

Basic Operation

This device is a smart eFuse with enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 9V to 18V.

For hot plug boards, the device provides inrush current control and programmable output ramp rate. The SGM2528 integrates over-current and short-circuit protections. The precision over-current limit helps minimize over design of the input power supply. The short-circuit protection with fast response isolates the load from input immediately when the short-circuit is detected. The device provides precision monitoring of bus voltage for brown-out and over-voltage conditions, and asserts fault for downstream system. The SGM2528 is designed to protect systems such as hard disks, PCIE SSDs and motherboard systems.

The input voltage will be limited by the device's internal control circuitry and then applied to the load. The slew rate of the output voltage is controlled by the internal dV/dt circuit. The output voltage will ramp up in 2ms, unless additional capacitor is placed at the dV/dt pin to slow down the ramp-up rate.

The device will not shut down unless the temperature exceeds the factory-set shutdown threshold. When entering current limit mode, the device will not be shut down, but the FET current will be limited to the value set by the I_{LIMIT} pin. When entering input over-voltage clamp mode, the device will also not be shut down, but the output voltage will be limited to 15V even the input voltage is larger.

APPLICATION INFORMATION (continued)

Current Limit

The current mirror structure is applied to limit the peak current of the device, which measures a small fraction of the load current, so that the loss made by the sensing resistor is reduced. In addition, current mirror structure also reduces the cost of the sensing resistor.

The current limit circuit has two limit levels: a lower current limit level will be triggered by the excessive load where the gate voltage is high and the FET is fully on. A higher current limit level will be triggered by a short-circuit event, where the device is actively limiting the current and the gate voltage is at an intermediate level.

When overload occurs, the internal current limit amplifier of the device regulates the load current to the current limit threshold I_{LIM-OL}. The output voltage will drop under regulation, which leads to higher current limit level (see page 10 for Overload Current Limit & Short-Circuit Current Limit characteristic). If the fault persists, the device continues to operate in the current limit mode, causing the internal temperature of the device to rise until the thermal shutdown occurs. During thermal shutdown, the SGM2528A/SGM2528C remain latched-off, while the SGM2528B performs auto-retry when T_J falls below T_{SD} - 22℃. During auto-retry, the load current should be lower than short-circuit current limit (I_{LIM-SC}) to ensure normal soft-start.

When a serious over-current event similar to a short-circuit event occurs, the SGM2528 triggers a fast-trip response to prevent the system from being damaged by excessive current flowing through the device. A fast-trip comparator with scalable threshold ($I_{FAST-TRIP}$ = 1.8 × I_{LIM-OL}) is adopted inside the device, which allows users to program the fast-trip threshold.

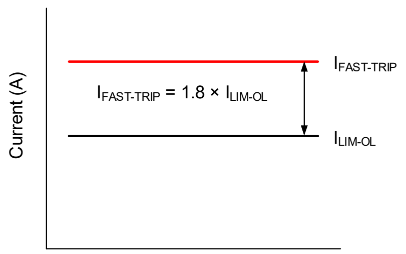


Figure 5. Fast-Trip Current

The device will be completely turned off if the current exceeds $I_{FAST-TRIP}$. Then the device will turn on again after a short of deglitch time in a current limit mode. In this way, the rapid recovery can be realized after a transient severe over-current event, and the drop of V_{SOURCE} voltage can be minimized. If the fault persists, the device continues to operate in the current limit mode, causing the internal temperature of the device to rise until the thermal shutdown occurs.

There are two methods to bias the I_{LIMIT} pin with a sensing resistor (R_{LIMIT}). They are shown in Figure 1 and Figure 2.

For the direct current sensing method, since the sensing resistor is placed between the I_{LIMIT} pin and the load, the bond wire resistance is inevitably included in the current limit circuit. This resistor not only affects the current limit accuracy, but may also vary slightly as the impedance between the sensing resistor and the SOURCE pin changes. Considering that the 5 SOURCE pins are connected in parallel, the on-resistance of the device will be slightly reduced, and the bond wire resistance of this pin is also one fifth of the other pins.

For the Kelvin current sensing method, the sensing resistor is placed between the I_{LIMIT} pin and one of the SOURCE pins. Since the current limit circuit senses the voltage on the die, any bond wire resistance as well as external impedance will not affect the current limit levels. Compared with direct current sensing, this method has only four SOURCE pins for power, which will make the on-resistance slightly larger.

Over-Voltage Clamp (SGM2528A/SGM2528B)

The over-voltage clamp circuit monitors the output voltage. If the input voltage is larger than 15V, the device will regulate the main integrated FET to make the output voltage limited to 15V. This can not only ensure the continuity of the device during transient operation, but also protect the load. If the over-voltage event lasts for a long time, the power consumption of the main FET may overheat the device, then trigger the thermal protection circuit which will turn off the device.

Under-Voltage Lockout

The under-voltage lockout circuit monitors the input voltage via a comparator with hysteresis. In its high state, the internal output switch is enabled. A low level on this pin will turn off the output switch.

dV/dt Circuit

The SGM2528 is designed to control the inrush current during hot plugging. This limits the voltage sag on the backplane power supply voltage and prevents unintended resets of the system power supply.

APPLICATION INFORMATION (continued)

A slew rate controlled startup (dV/dt) regardless of the load is realized by the internal circuit, which generates a fixed slope ramp signal. The rising slope of the output voltage is determined by this ramp and the scaling factor.

If the dV/dt pin is left open, the output voltage ramps up in approximately 2ms. By connecting an external capacitor from this pin to ground, the user can get a longer output ramp-up time. There is a constant current source of about 100nA inside the dV/dt pin. Considering the low current level of the current source, it is recommended to connect a ceramic capacitor or a low leakage capacitor to the dV/dt pin if necessary, and external electrolytic capacitors are not recommended for this pin.

The total ramp time (t_{0-12}) of output voltage for 0V to 12V can be calculated using the following equations:

$$t_{0-12} = 25.5e6\ (5pF + C_{EXT}) \quad (1)$$

$$C_{EXT} = \frac{t_{0-12}}{25.5e6} - 5pF \quad (2)$$

where:
C_{EXT} is in Farads.
t is in seconds.

If the device is turned off due to a fault, disable or input power recycling, the output voltage will ramp up from 0V via the timing capacitor being discharging when it is turned back on.

EN/FAULT

The EN/FAULT not only controls the on/off state of the internal FET, but also indicates whether the device is shut down due to thermal protection, so it is a multifunctional, bidirectional pin. The output of the device turns on when the EN/FAULT is high and vice versa.

Considering the 3-state operation of this pin, it should be connected to an open-drain or open collector circuit instead of a circuit with a pull-up structure.

As shown in Figure 6, if the device triggers thermal protection and shuts down, the EN/FAULT pin will be pulled down to logic medium level (1.45V, TYP). The voltage signal at this pin can be monitored by an external circuit to obtain information on whether thermal shutdown of the device has occurred. If this pin shares an external open-drain or open collector circuit with another device in the family like Figure 3 shows, a thermal shutdown failure of either device will cause both devices to shut down.

There are two ways to enable the output of latched thermal devices, either by pulling the EN/FAULT pin to ground through an external switch and then going high, or when the input power is recycled. For auto-retry devices, as long as the die temperature of the device in the shutdown state is below the temperature threshold, both devices will restart.

Thermal Shutdown

The SGM2528 integrates a temperature sensing circuit for sensing the die temperature on the power FET. If the temperature exceeds the temperature threshold (158℃), the device enters thermal shutdown mode and the load is powered down. For latched thermal devices, the output will be enabled in two ways: recycling the input or toggling the EN/FAULT pin. For auto-retry devices, as long as the die temperature drops by more than 22℃, the output will be enabled and the load will power up again.

To increase the device trip time during transient events at high power conditions, the thermal shutdown temperature threshold is set high. Therefore, it is not recommended to allow this device to work for a long time in a working condition above +125℃.

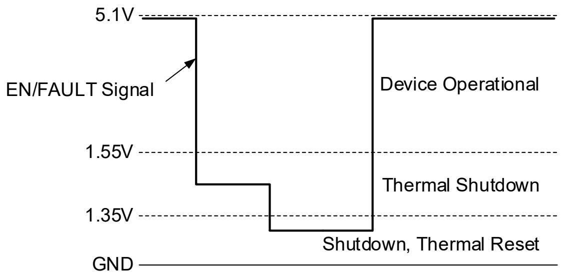


Figure 6. EN/FAULT Signal Levels

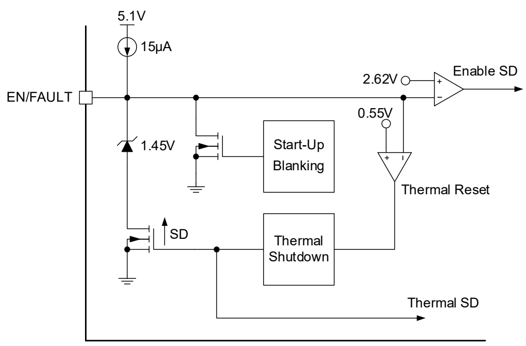


Figure 7. EN/FAULT Simplified Circuit

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2024 – REV.A.2 to REV.A.3	Page
Update Absolute Maximum Ratings and Recommended Operating Conditions	2
Added Typical Performance Characteristics	8, 9
Added Application Information	12

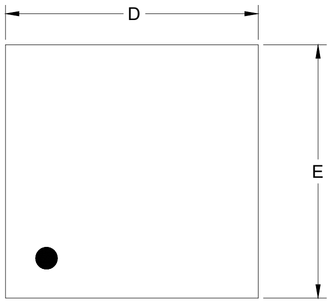
OCTOBER 2022 – REV.A.1 to REV.A.2	Page
Update Application Information section	9, 10, 11

AUGUST 2020 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	6

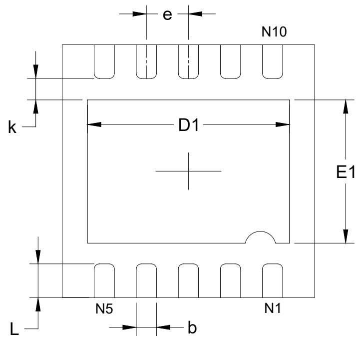
Changes from Original (JULY 2020) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

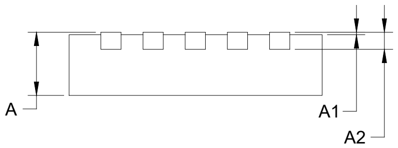
TDFN-3×3-10L



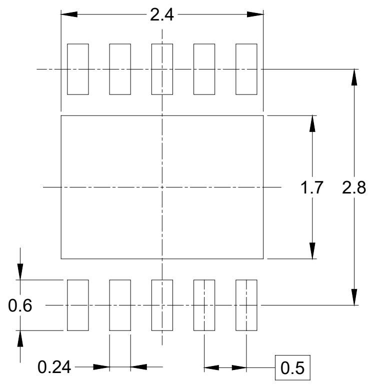
TOP VIEW



BOTTOM VIEW



SIDE VIEW



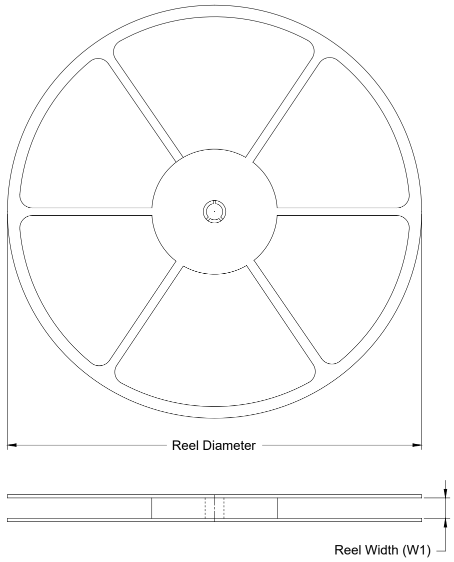
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

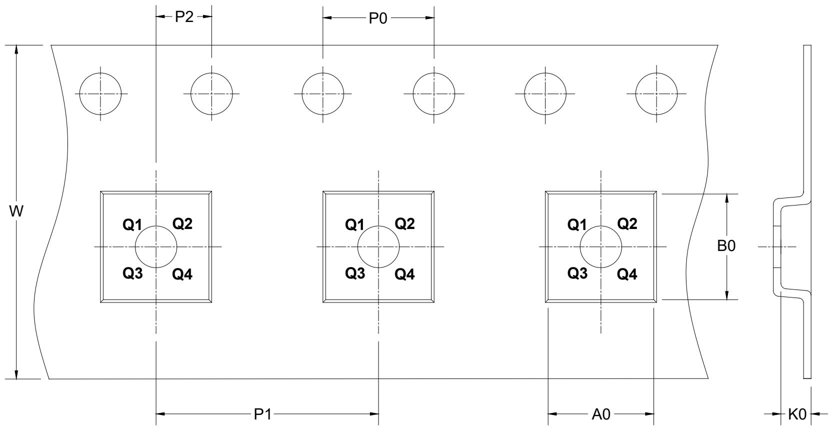
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

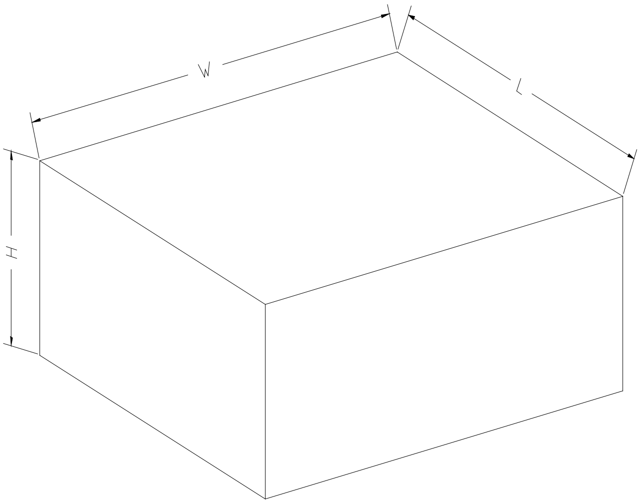
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002