SGM66075

Low-I_Q, High Efficiency 9A Valley Current Synchronous Boost Converter with Bypass Switch

GENERAL DESCRIPTION

The SGM66075 is a high power density synchronous Boost converter with integrated low R_{DSON} bypass switch from the input to output. The device operates with 2MHz (TYP) switching frequency in Boost mode. At light load, the device operates in I^2C programmable PFM mode to maximize efficiency.

The SGM66075 has a wide input range from 2.3V to 5.3V. After startup, the device is capable to operate down to 2.1V input before shutdown. Boost output voltage is programmable from 2.85V to 5.0V via I^2C interface with 50mV step.

During operation, when the input voltage is higher than the programmed output voltage, the SGM66075 operates in bypass mode via the integrated low R_{DSON} bypass switch to maximize the system efficiency. The current limit of bypass switch can be programmed to 9.4A (TYP) with 1μs (TYP) deglitch or 6.5A (TYP) with 1ms (TYP) deglitch.

When EN pin is pulled to logic high, the SGM66075 can be programmed in auto bypass mode, forced bypass mode or low power bypass mode. In auto bypass mode, when the input voltage falls below or rises above the programmed output voltage, the device automatically switches to either Boost or bypass mode to maintain the output voltage regulation. In low power bypass mode, the device will turn off more circuits to achieve lower quiescent current than forced bypass mode.

The maximum I^2C programmable Boost valley current limit of SGM66075 is 9A (TYP). For high pulsating load applications, the device is capable to support 5A peak current at 3.4V output when the input source voltage drops to 2.7V.

The SGM66075 is available in a Green WLCSP-1.73×1.73-16B package.

FEATURES

- **Up to 96.7% Efficiency at V_{IN} = 3.3V, V_{OUT} = 3.4V, I_{LOAD} = 1A**
- **Wide V_{IN} Range from 2.3V to 5.3V**
  - **2.1V after Startup**
- **Programmable Output Voltage from 2.85V to 5.0V**
  - **SGM66075: 3.4V Default V_{OUT}**
  - **SGM66075-3.6: 3.6V Default V_{OUT}**
- **I_{OUT} ≥ 5A (Peak) at V_{OUT} = 3.4V, V_{IN} ≥ 2.7V**
- **Integrated Bypass Mode with 9mΩ Bypass Switch**
- **Low Power Bypass Mode**
- **Programmable Valley Inductor Current Limit and Output Voltage**
- **True Load Disconnect**
- **Low-Ripple Light-Load PFM Mode**
- **I^2C Controlled Interface**
- **Protection Features:**
  - **Short-Circuit Protection**
  - **Over-Current Protection**
  - **Over-Temperature Protection**
- **Available in a Green WLCSP-1.73×1.73-16B Package**

APPLICATIONS

Single-Cell Ni-Rich, Si-Anode, Li-Ion, LiFePO4
Smart-Phones or Tablet PCs
2.5G, 3G, 4G Mini-Module Data Cards

TYPICAL APPLICATION

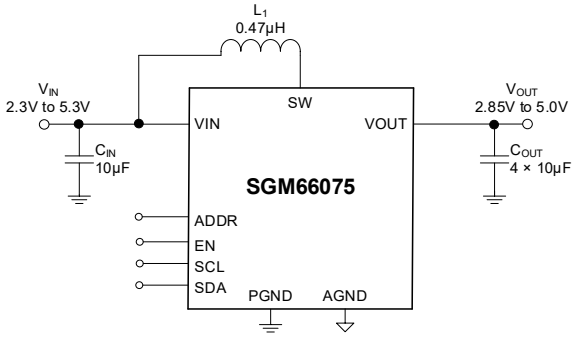


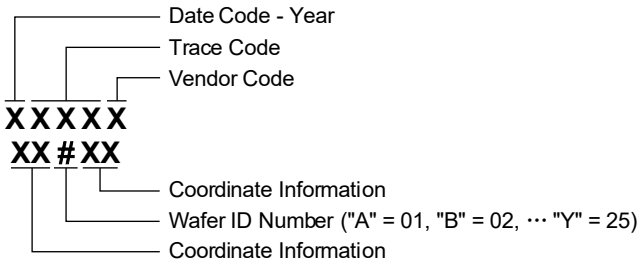
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM66075	WLCSP-1.73×1.73-16B	-40℃ to +125℃	SGM66075XG/TR	0YG XXXXX XX#XX	Tape and Reel, 3000
SGM66075-3.6	WLCSP-1.73×1.73-16B	-40℃ to +125℃	SGM66075-3.6XG/TR	1GU XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, EN, VOUT, ADDR Voltages ..... -0.3V to 6V
SCL, SDA Voltages ..... -0.3V to 6V
SW Voltage ..... -0.3V to 6V
SW Voltage (10ns Transient) ..... -1V to 8V
Valley Current into SW 9A
Package Thermal Resistance
WLCSP-1.73×1.73-16B, θ_{JA} ..... 46.9℃/W
WLCSP-1.73×1.73-16B, θ_{JB} ..... 11℃/W
WLCSP-1.73×1.73-16B, θ_{JC} ..... 29.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±500V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.3V to 5.3V
Inductance, L ..... 200nH to 470nH
Output Effective Capacitance, C_{OUT} .....
..... 9μF to 100μF, 14μF (TYP)
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

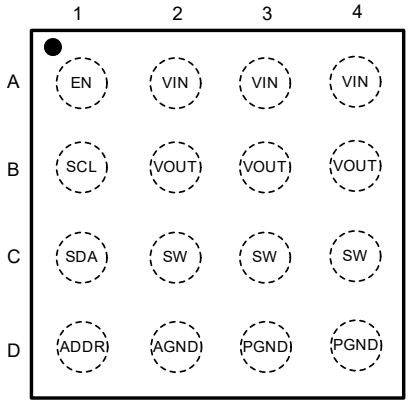
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.73×1.73-16B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1	EN	AI	Enable. When this pin is high, the device is enabled. When this pin is low, a pull-down resistor R_{PD} is connected to this pin.
B1	SCL	DI	Serial Interface Clock. SDA can be released when receiving 9 clock pulses on the SCL line if SDA is stuck low by the device.
C1	SDA	DIO	Serial Interface Data Line.
D1	ADDR	AI	I^2C Slave Address Pin. This pin can be pulled high, pulled low or floating. During POR, the pull-down resistor and pull-up resistor connected to this pin are both 100kΩ.
A2, A3, A4	VIN	P	Input Power Supply. Connect one 10μF or larger capacitors between this pin and PGND.
B2, B3, B4	VOUT	P	Output Voltage. Connect four 10μF or larger capacitors between this pin and PGND.
C2, C3, C4	SW	P	Switching Node. Connect to the inductor.
D2	AGND	P	Analog Ground.
D3, D4	PGND	P	Power Ground.

NOTE: AI = analog input, DI = digital input, DIO = digital input/output, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 3.2V and V_{EN} = 1.2V, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
Operating Quiescent Current into V_{IN}	I_Q	Boost mode in auto bypass mode, device not switching, I_{OUT} = 0mA, V_{IN} = 3.2V, V_{OUT} = 3.6V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011	T_J = -40℃ to +85℃		25	45	μA
		Bypass mode in auto bypass mode, V_{IN} = 3.6V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011			23	45	
		Forced bypass mode, V_{IN} = 3.6V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011			18	40	
		Low power bypass mode, V_{IN} = 3.6V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011			16	35	
Operating Quiescent Current into V_{OUT}		Boost mode in auto bypass mode, device not switching, I_{OUT} = 0mA, V_{IN} = 3.2V, V_{OUT} = 3.6V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011			8	25	μA
Shutdown Current	I_{SD}	V_{IN} = 3.6V, V_{EN} = 0V			0.4	5	μA
I^2C Under-Voltage Lockout Threshold	V_{UVLO_I2C}	V_{IN} Rising			1.60		V
		V_{IN} Falling			1.46		
		Hysteresis			0.14		
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising				2.3	V
		V_{IN} Falling				2.1	
		Hysteresis			0.12		
EN, SDA, SCL, ADDR							
Low-Level Input Voltage	V_{IL}					0.4	V
High-Level Input Voltage	V_{IH}			0.9			V
EN Pull-Down Resistance	R_{PD}	V_{IN} = 3.2V, V_{EN} = 0.3V			390		kΩ
Input Leakage Current	I_{lkg}	Input connected to GND	T_J = -40℃ to +85℃		0.01	0.6	μA
		Input connected V_{IN}			0.01	0.6	μA
Output							
Regulated DC Voltage Accuracy	V_{OUT}	V_{IN} = 3.2V, V_{EN} = 1.2V, VOUT_SET[5:0] = 001011		-2		2	%
		V_{IN} = 3.2V, V_{EN} = 1.2V, VOUT_SET[5:0] = 100001		-2		2	
Power Switch							
Low-side Switch MOSFET On-Resistance	R_{DSON}	V_{IN} = 3.2V, V_{OUT} = 3.4V, V_{EN} = 1.2V			17	45	mΩ
High-side Rectifier MOSFET On-Resistance					27	54	mΩ
High-side Bypass MOSFET On-Resistance		V_{IN} = 3.2V, V_{EN} = 1.2V			9	25	mΩ

ELECTRICAL CHARACTERISTICS (continued)

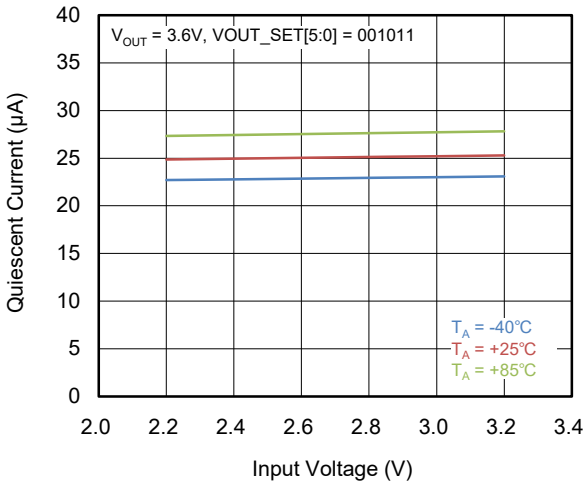
(T_J = -40℃ to +125℃, V_{IN} = 3.2V and V_{EN} = 1.2V, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Leakage Current into SW	I_{lkg}	EN = GND, V_{OUT} = V_{SW} = 3.4V, T_J = -40℃ to +85℃		0.01	1	μA
VOUT Sink Capability	V_{SINK}	EN = GND, V_{IN} = 3.2V, I_{OUT} = -10mA			0.3	V
Valley Inductor Current Limit		V_{IN} = 2.9V, V_{OUT} = 3.6V, V_{EN} = 1.2V, auto PFM/PWM, ILIM[3:0] = 1010, T_J = +25℃	7	9	11	A
Bypass Mode Current Limit		V_{IN} = 3.2V, V_{EN} = 1.2V, 1ms deglitch, T_J = +25℃	4.9	6.5	8.1	A
		V_{IN} = 3.2V, V_{EN} = 1.2V, 1μs deglitch, T_J = +25℃	8.1	9.4	10.8	
Soft-Start Input Current Limit		ILIM1		1000		mA
		ILIM2		2000		mA
Oscillator						
Switching Frequency	f_{SW}	V_{IN} = 3.2V, V_{OUT} = 4.5V, V_{EN} = 2.7V, VOUT_SET[5:0] = 100101		2		MHz
Thermal Shutdown						
Thermal Shutdown (1)	T_{SD}			160		℃
Thermal Shutdown Hysteresis(1)	T_{SD_HYS}			20		℃
Timing						
Startup Time		V_{IN} = 3.2V, V_{OUT} = 3.4V, R_{LOAD} = 50Ω, Time from active V_{IN} to V_{OUT} settled		500		μs

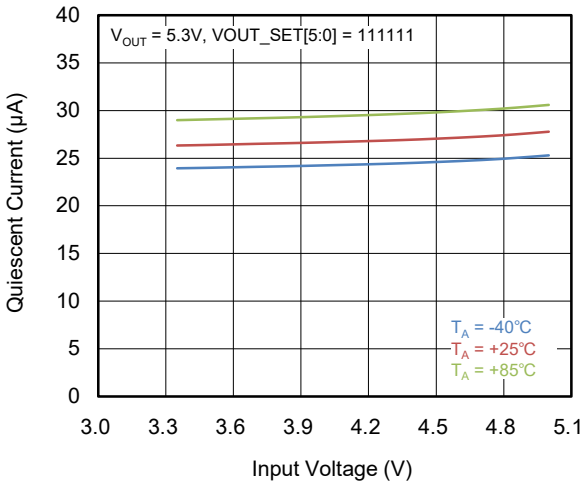
NOTE:
1. Specified by characterization. Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

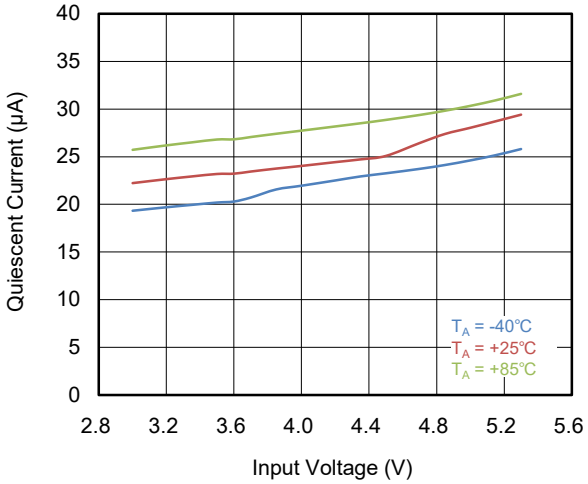
Quiescent Current in Boost Mode vs. Input Voltage



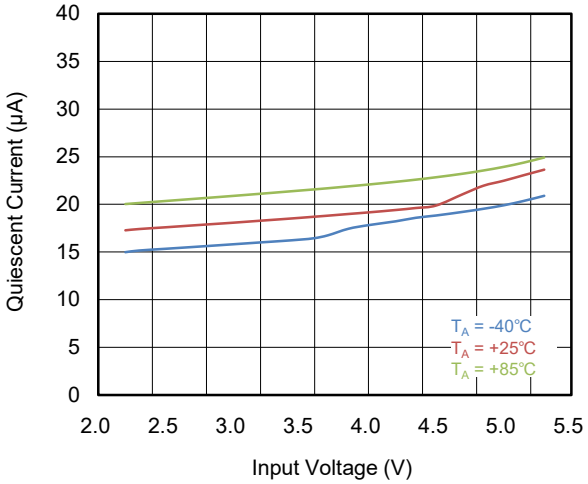
Quiescent Current in Boost Mode vs. Input Voltage



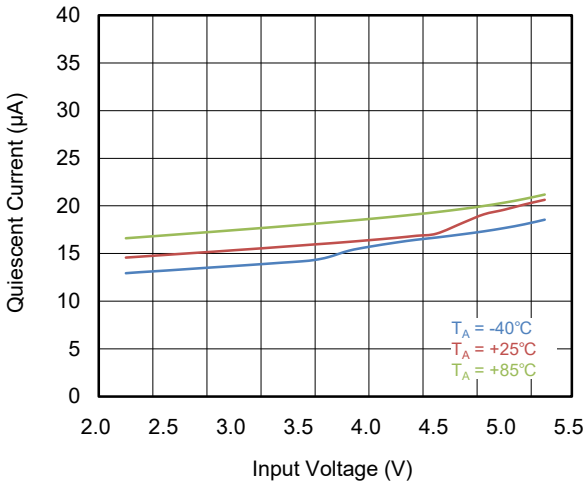
Quiescent Current in Bypass Mode vs. Input Voltage



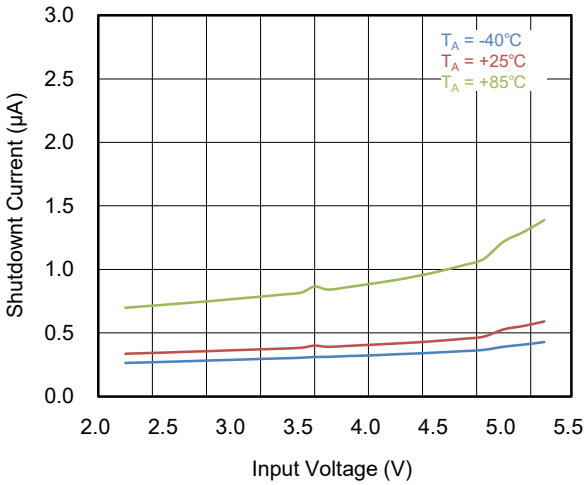
Quiescent Current in Forced Bypass Mode vs. Input Voltage



Quiescent Current in Low Power Bypass Mode vs. Input Voltage



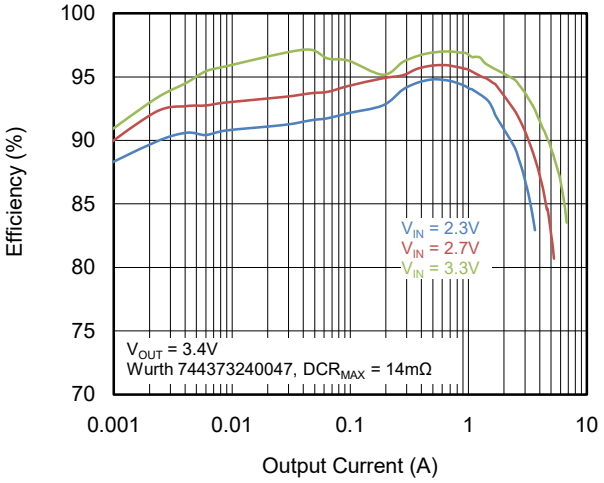
Shutdown Current vs. Input Voltage



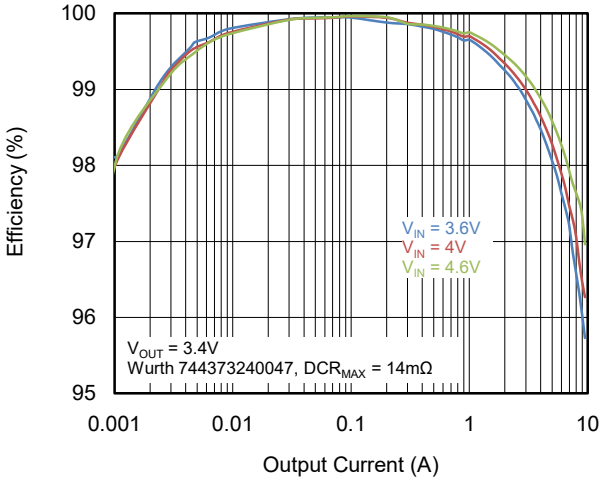
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, C_{OUT} = 14μF and L_1 = 0.47μH, unless otherwise noted.

Efficiency vs. Output Current in Boost Mode



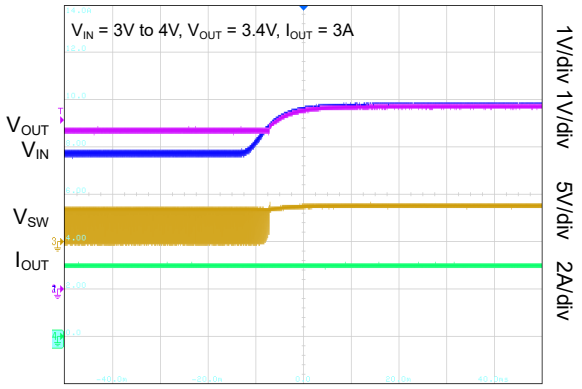
Efficiency vs. Output Current in Bypass Mode



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

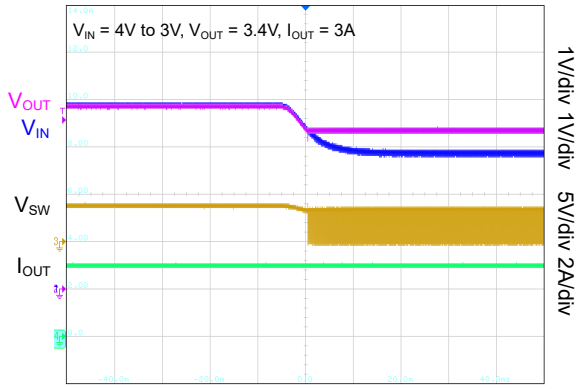
At T_A = +25℃, C_{OUT} = 14μF and L_1 = 0.47μH, unless otherwise noted.

Boost Mode to Bypass Mode by V_{IN} Rising



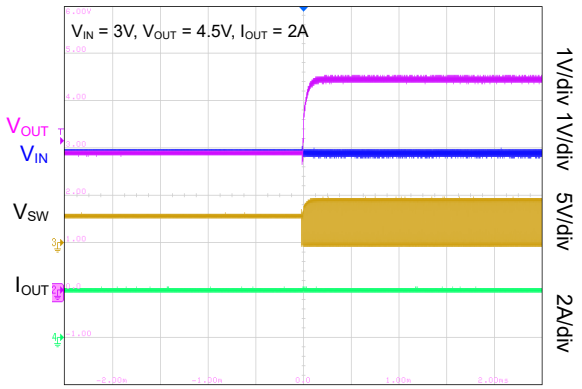
Time (10ms/div)

Bypass Mode to Boost Mode by V_{IN} Falling



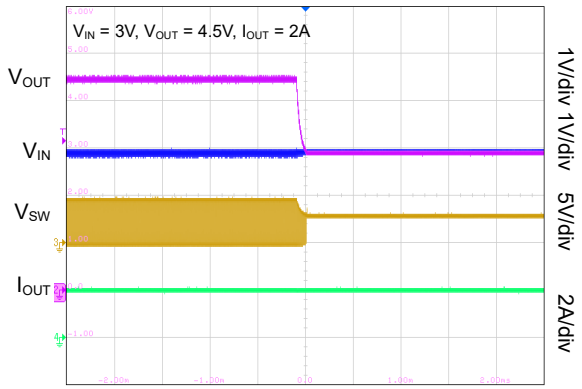
Time (10ms/div)

Bypass Mode to Boost Mode by Registers



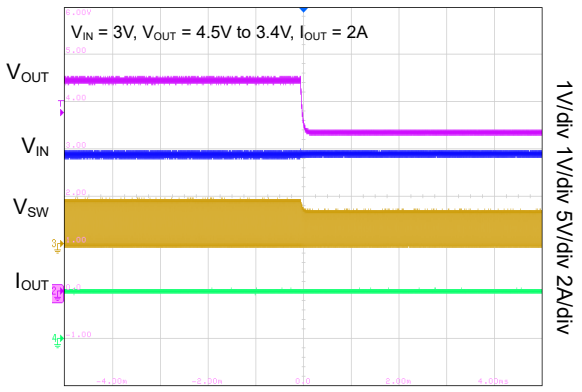
Time (500μs/div)

Boost Mode to Bypass Mode by Registers



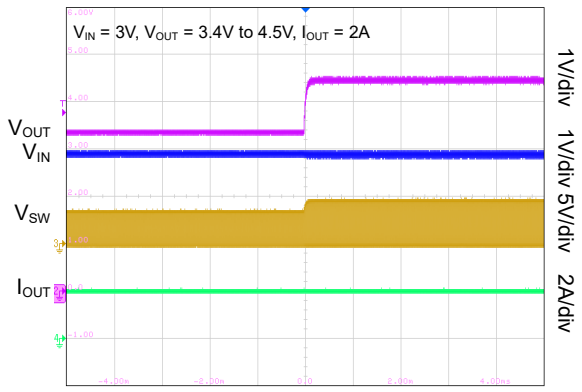
Time (500μs/div)

Dynamic Voltage Scaling



Time (1ms/div)

Dynamic Voltage Scaling

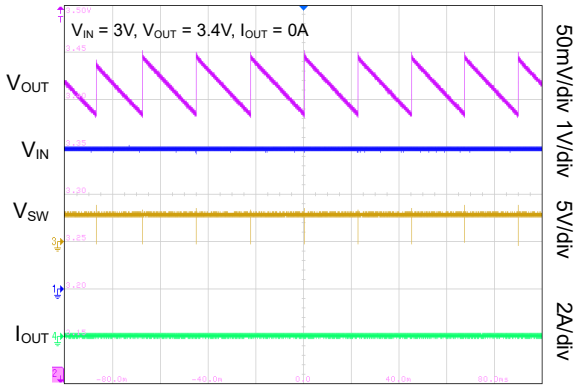


Time (1ms/div)

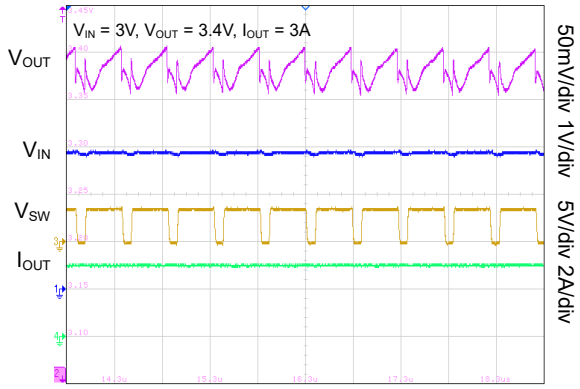
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, C_{OUT} = 14μF and L_1 = 0.47μH, unless otherwise noted.

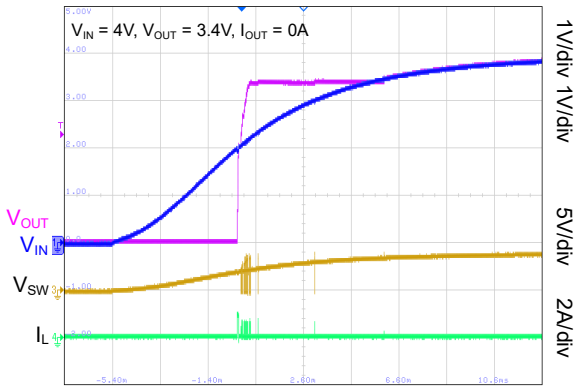
Boost Steady State



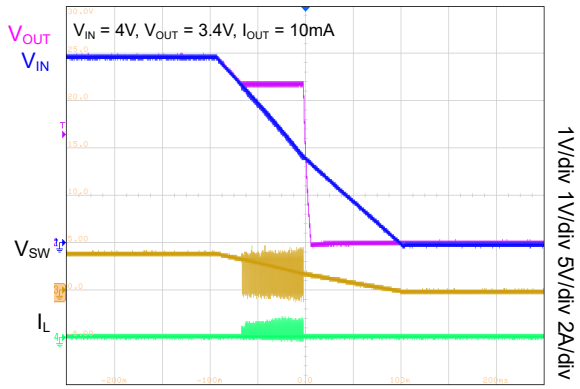
Boost Steady State



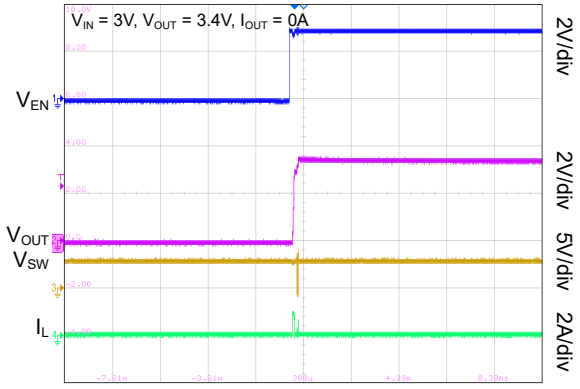
Bypass Power On



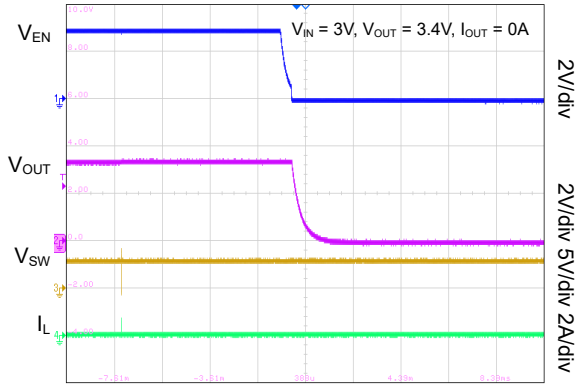
Bypass Power Off



Boost EN Startup



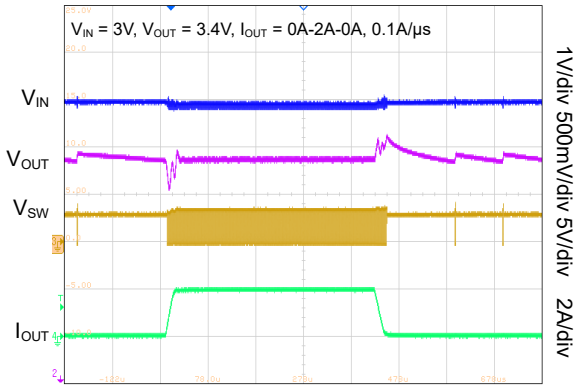
Boost EN Shutdown



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

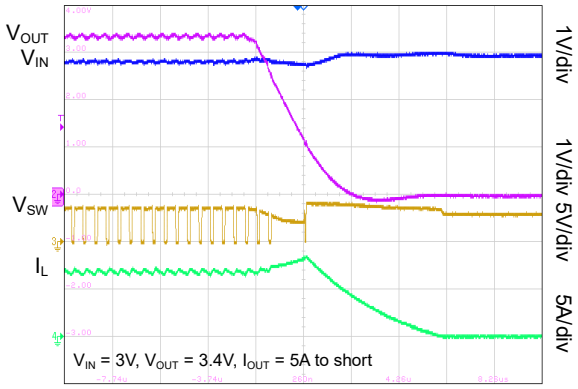
At T_A = +25℃, C_{OUT} = 14μF and L_1 = 0.47μH, unless otherwise noted.

Load Transient



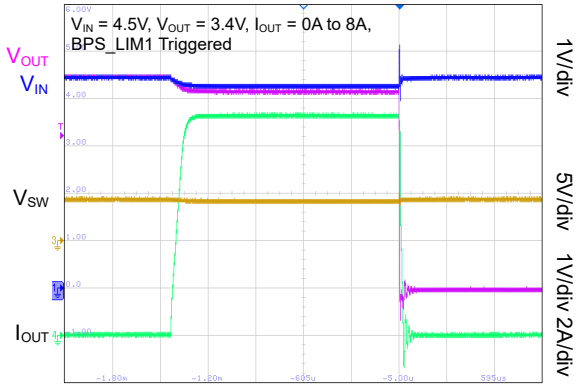
Time (100μs/div)

Boost Short-Circuit Protection



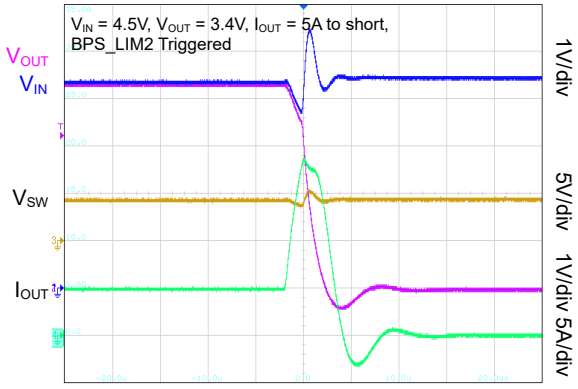
Time (2μs/div)

Bypass Short-Circuit Protection



Time (300μs/div)

Bypass Short-Circuit Protection



Time (5μs/div)

FUNCTIONAL BLOCK DIAGRAM

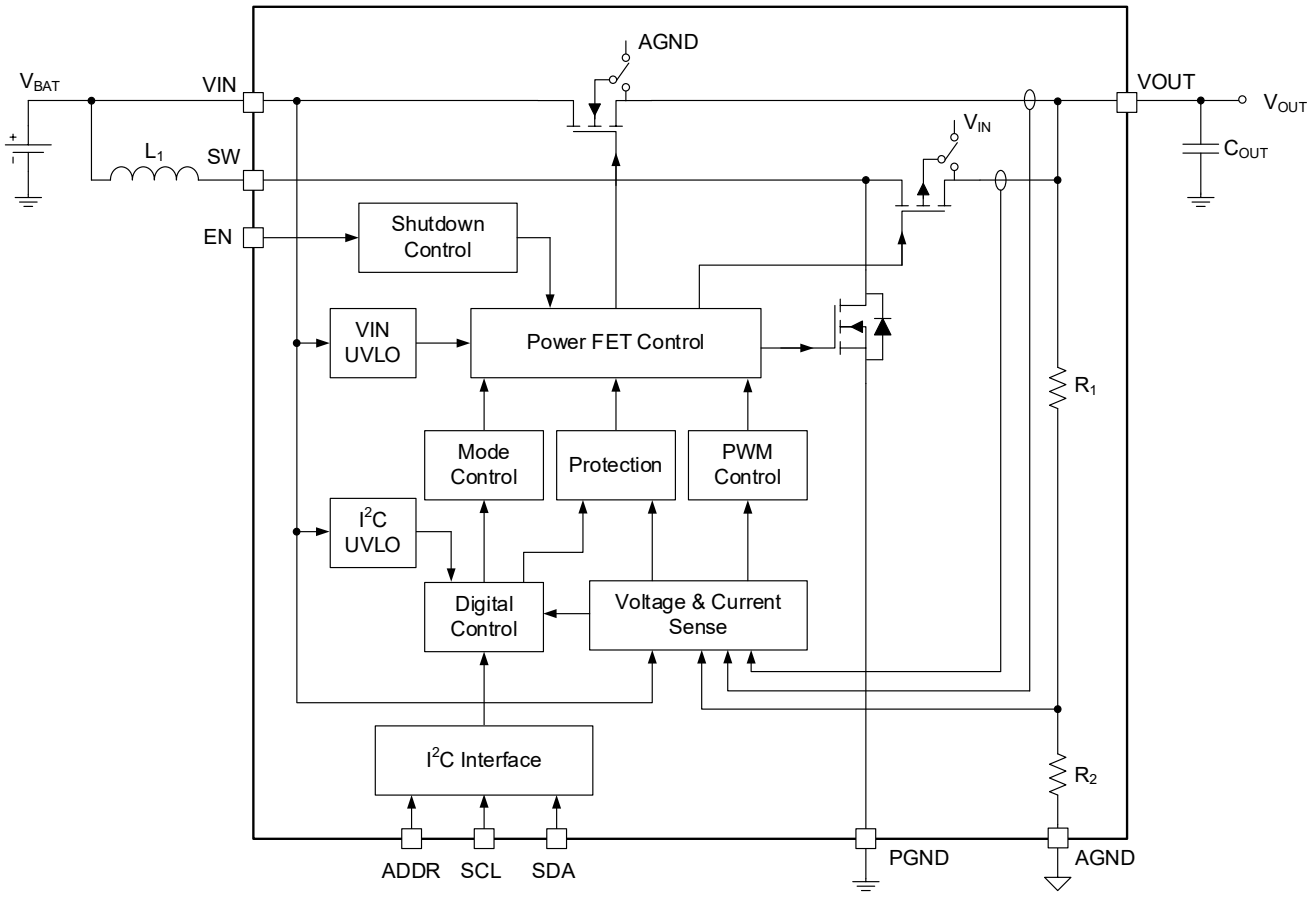


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM66075 is a high power density synchronous Boost converter with a 9mΩ R_{DSON} bypass switch. The device is capable to start up from 2.3V input, and operate down to 2.1V input after startup which is suitable for applications requiring further discharge the input source to achieve higher usage. The device implements standard I^2C communication bus to program the device operating conditions such as output voltage, current limit, operation mode and fault status.

The SGM66075 can be programmed to operate in auto bypass mode in which the device can transit between Boost mode and bypass mode automatically based on the difference of input voltage and programmed output voltage. Forced bypass mode is also programmable to bypass the input voltage via the 9mΩ bypass switch. The device has a dedicated slave address program pin to configure 3 different addresses.

Startup and Shutdown

When the input voltage is above the UVLO rising threshold of 2.3V, and EN pin is pulled to logic high, the SGM66075 starts to ramp the output voltage. During the initial startup phase, the device has a linear pre-charge phase to charge the output voltage. During pre-charge phase, the device sources a 1A (TYP) DC current to charge the output voltage for 1ms (TYP), if the output voltage is not able to reach the input voltage, the pre-charge current is increased to 2A (TYP) for 1.5ms (TYP). Once the output voltage reaches the input voltage during any pre-charge phase, the device enters soft-start phase to turn on Boost switching and ramp the output voltage towards the programmed output voltage. During soft-start, the current limit can be set to the programmed Boost valley limit or 2A (TYP) via Soft-Start bit in the ILIMSET register to limit the inrush current drawn from the source during startup. Refer to Figure 3 below for a typical startup sequence.

The device implements a software enable function via DEV_EN bit in the CONFIG register. EN pin needs to be pulled to logic high in order to use the software enable function. After EN pin pulled high or DEV_EN bit set to 1, a delay of at least 200μs is required before I^2C communication starts.

Pulling the EN pin to logic low, decreasing the input voltage below the input UVLO falling threshold or toggling DEV_EN bit to 0, the device stops switching immediately.

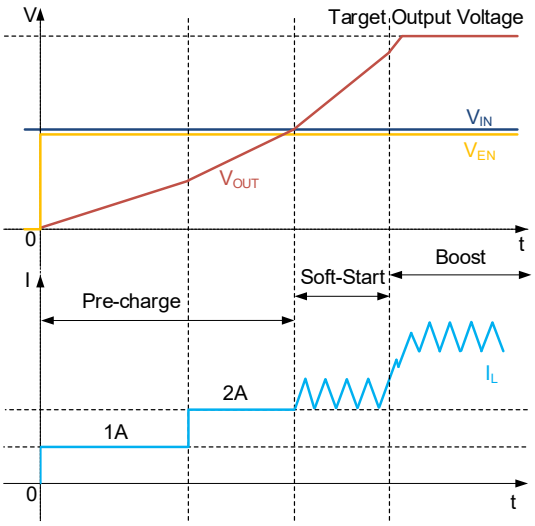


Figure 3. Startup Sequence

Power Good

The SGM66075 implements output voltage power good function via STATUS register (PGOOD_STAT bit). When the output voltage reaches above 90% of the programmed output voltage, the PGOOD_STAT bit is toggled to 1. When the output voltage drops 50mV (TYP) below the 90% of the programmed output voltage, PGOOD_STAT bit is toggled to 0. If the output voltage fails to reach the input voltage in the pre-charge phase or the output voltage fails to reach 90% of the programmed output voltage in the soft-start time, the FAULT_FLAG bit is toggled to 1 and PGOOD_STAT bit is not toggled.

Programmable Output Voltage

The output voltage of the SGM66075 is programmable via VOUT register, and the programmable range is from 2.85V to 5V with 50mV step. In Boost mode, if the output voltage reaches above 6V (TYP), the device stops switching.

Slave Address Selection

The SGM66075 implements an ADDR pin to configure up to 3 different I^2C slave addresses. Pulling the ADDR pin to logic low, 0x75 is configured, logic high configures 0x76, and leave the ADDR pin floating configures 0x77. The slave address cannot be changed when VIN is above the I^2C UVLO threshold.

Table 1. Slave Address Selection

ADDR	Slave Address
Low	0x75
High	0x76
Floating	0x77

DETAILED DESCRIPTION (continued)

Boost Control Architecture

The SGM66075 implements 2MHz (TYP) fixed frequency valley current mode control architecture to regulate the output voltage in Boost mode. The internal error amplifier compares the output voltage with an internal reference to generate an error signal and this error signal is compared with the current signal sensed from the high-side Boost power FET to determine the turning off of the high-side power FET. After a short period of dead time, the low-side power FET turns on to charge the inductor. When the clock signal arrives, the low-side power FET turns off.

The valley current mode control offers excellent load and line transient performance, in addition, the fixed frequency operation avoids variable frequency noise issues for noise sensitive applications.

Output Voltage Discharge

The device can be programmed to enable output discharge function when either EN pin or DEV_EN bit is toggled to low. When V_{OUT} is larger than 2V (TYP), V_{OUT} will be discharged by a 100mA (TYP) current source. When V_{OUT} is lower than 2V (TYP), V_{OUT} will be discharged by a 15Ω (TYP) resistor. Thermal shutdown will not enable output voltage discharge.

PFM/FPWM Operation and Spread Spectrum

The SGM66075 can be programmed to operate in auto PFM mode or FPWM mode via MODE_CTRL bit in the CONFIG register. Efficiency at light load can be improved in auto PFM mode and constant frequency for the entire operation load range can be achieved in the FPWM mode.

When the SGM66075 operates in CCM mode, the device can be programmed to have spread spectrum frequency modulation (SSFM) feature via SSFM bit = 1 in CONFIG register. The switching frequency varies from 1.8MHz to 2.4MHz when SSFM is enabled.

Auto Bypass, Forced Bypass and Low Power Bypass Modes

The SGM66075 implements a low R_{DSON} bypass switch between VIN and VOUT pins. When auto bypass mode is configured, as the input voltage rises above the target output voltage by 100mV (TYP), the device turns on the bypass switch and disables the Boost operation after 6μs. As the input voltage drops below the target output voltage in auto bypass mode, the Boost power FET starts switching immediately, and the bypass FET remains on for 7μs (TYP) before turning off. With the Boost power FETs and bypass FET on at the same time, sufficient energy is delivered to the output without causing significant voltage drop at the output. Refer to Figure 4 and Figure 5 below for a typical auto bypass operation.

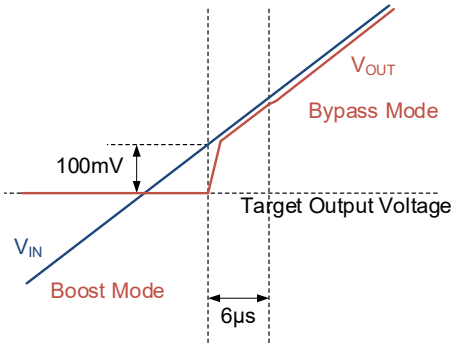


Figure 4. Typical Boost to Bypass in Auto Bypass Mode

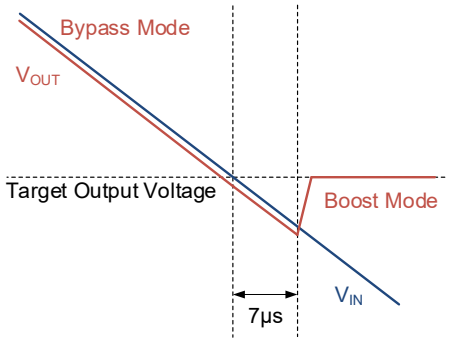


Figure 5. Typical Bypass to Boost in Auto Bypass Mode

Forced bypass mode can be programmed by CONFIG register AUTO_BYPASS[1:0] bits to be 0b01. In this mode, the Boost switch is disabled and the bypass FET is turned on to bypass the input voltage. Auto bypass and forced bypass mode can be changed on the fly and the device maintains the programmed output voltage regulation when mode changes.

Low power bypass mode can be programmed via CONFIG register AUTO_BYPASS[1:0] bits to be 0b00. Compared to forced bypass mode, the device consumes less power in low power bypass mode by turning off more internal circuits. Over-current protection, short-circuit protection and thermal shutdown are still in operation under low power bypass mode.

DETAILED DESCRIPTION (continued)

Fault

When any of thermal shutdown, PG fault in startup phase, output short-circuit occurs, FAULT_FLAG bit in the STATUS register is toggled to 1. The FAULT_FLAG is a host read clear signal.

Reset

REG_RST bit in the CONFIG register toggled to 1 resets all register values to the default settings and turns off the device. After 160ms (TYP), the device automatically resumes operation.

It should be noted that only toggling REG_RST bit to 1 or finishing digital logic POR can reset all the registers. Pulling down EN will not change the register values and the device can still communicate with the host when EN is low.

Current Limit

In Boost mode, the SGM66075 has a maximum valley switch current limit of 9A (TYP) to prevent the load from excessive current damage. When the Boost current limit is reached, the ILIM_BST_FLAG bit in the STATUS register is toggled to 1, and the ILIM_BST_FLAG is a host read clear signal. The Boost valley current limit is also programmable from 4A (TYP) to 9A (TYP) via ILIM[3:0] bits in the ILIMSET register and can be disabled via the ILIM_OFF bit in the ILIMSET register. In addition, the SGM66075 has a PLIM of 12A (TYP) to protect the device under extreme conditions. Once the inductor current reaches PLIM, the device will shut down and the FAULT_FLAG bit will be toggled to 1. The PLIM can be turned off by setting the PLIM_OFF bit to 1.

In bypass mode, the bypass switch of SGM66075 has two current limit levels of 6.5A (TYP) or 9.4A (TYP). The 6.5A (TYP) bypass current limit has a deglitch time of 1ms (TYP). The current will not be limited in the deglitch time and the bypass switch will turn off if the high bypass current lasts for more than 1ms (TYP). When the 9.4A (TYP) bypass current limit is reached for more than 1μs (TYP), the device stops operation immediately. The two current limit levels can be disabled independently via BYPASS_ILIM1_OFF and BYPASS_ILIM2_OFF in the ILIMSET register. When current limit is reached in the bypass mode, ILIM_BPS_FLAG bit in the STATUS register is toggled to 1. The ILIM_BPS_FLAG is a host read clear signal.

Short-Circuit Protection

The SGM66075 has short-circuit protection when the output voltage is shorted to ground. When V_{OUT} is lower than V_{IN} - 300mV, the PLIM will be changed to 7A (TYP) or 5A (TYP) according to the PLIM bit. Once the inductor current reaches PLIM in such condition, the device enters short-circuit protection, which is a quick response to the output short. When V_{OUT} is lower than V_{IN} - 1V, the device will turn off the switches and enter short-circuit protection. The hiccup mode is applied during the short-circuit protection. In hiccup mode, the device turns on with the pre-charge phase to attempt start up, if the output is still shorted, the device turns off for 160ms (TYP), then the hiccup cycle repeats. Refer to Figure 6 below for a typical short-circuit hiccup protection mode.

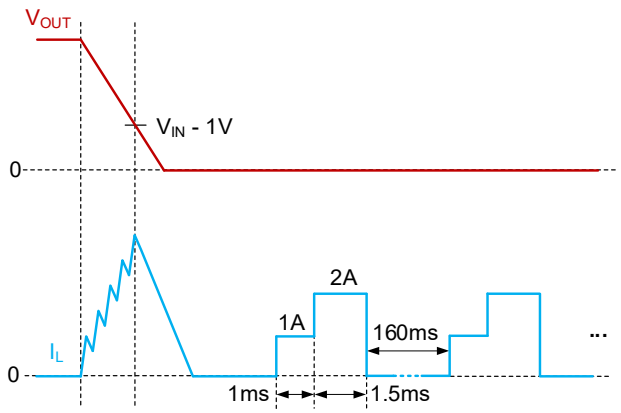


Figure 6. Typical Short-Circuit Protection

When the output short condition is removed, the device automatically enters the startup sequence to ramp the output voltage towards the programmed output. Hiccup protection mode effectively reduces the device power dissipation in short-circuit condition.

Thermal Shutdown

The SGM66075 implements thermal shutdown feature to prevent the device from excessive thermal dissipation. When the die temperature reaches above 160℃ (TYP), the device turns off, and the TSD_FLAG bit in the STATUS register is toggled to 1. After the die temperature drops 20 ℃ (TYP) below the TSD temperature, the device resumes operation with a normal startup sequence. The TSD_FLAG is a host read clear signal.

DETAILED DESCRIPTION (continued)

I^2C Serial Interface and Data Communication

Standard I^2C interface is used to program SGM66075 parameters and get status reports. I^2C is a well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM66075 operates as a slave device and its address can be set as 0x75, 0x76 or 0x77 by pulling ADDR pin low, high or floating. It has five 8-bit registers, numbered from REG0x00 to REG0x04. A register read beyond 0x04 returns 0xFF.

Physical Layer

The SGM66075 supports I^2C standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (up to 1000kbit/s) communication speeds. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

I^2C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 7. All transactions begin by the master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high-to-low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

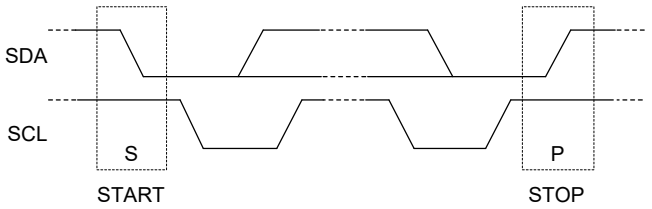


Figure 7. I^2C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by the master. Bit transfer in I^2C is shown in Figure 8.

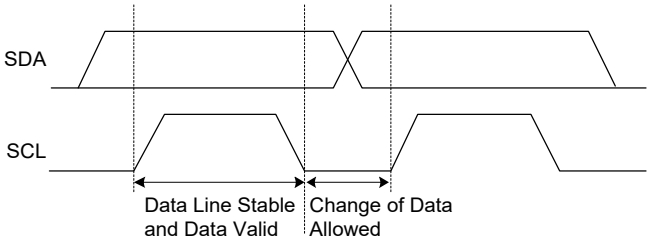


Figure 8. I^2C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 9 shows the byte transfer process with I^2C interface.

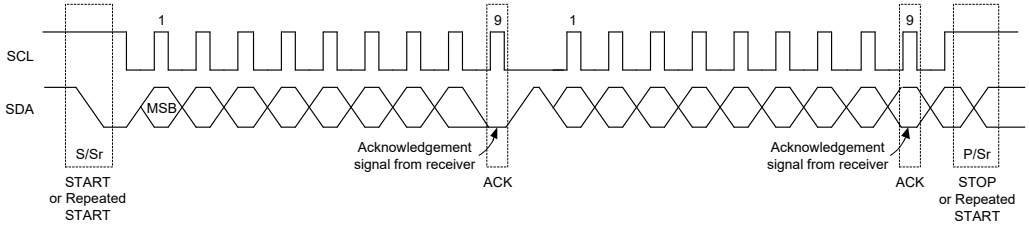


Figure 9. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 10.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 11 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register as shown in Figure 12, it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

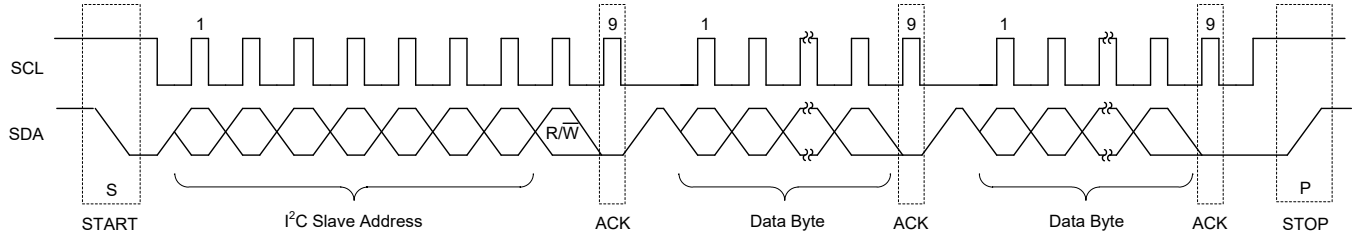


Figure 10. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

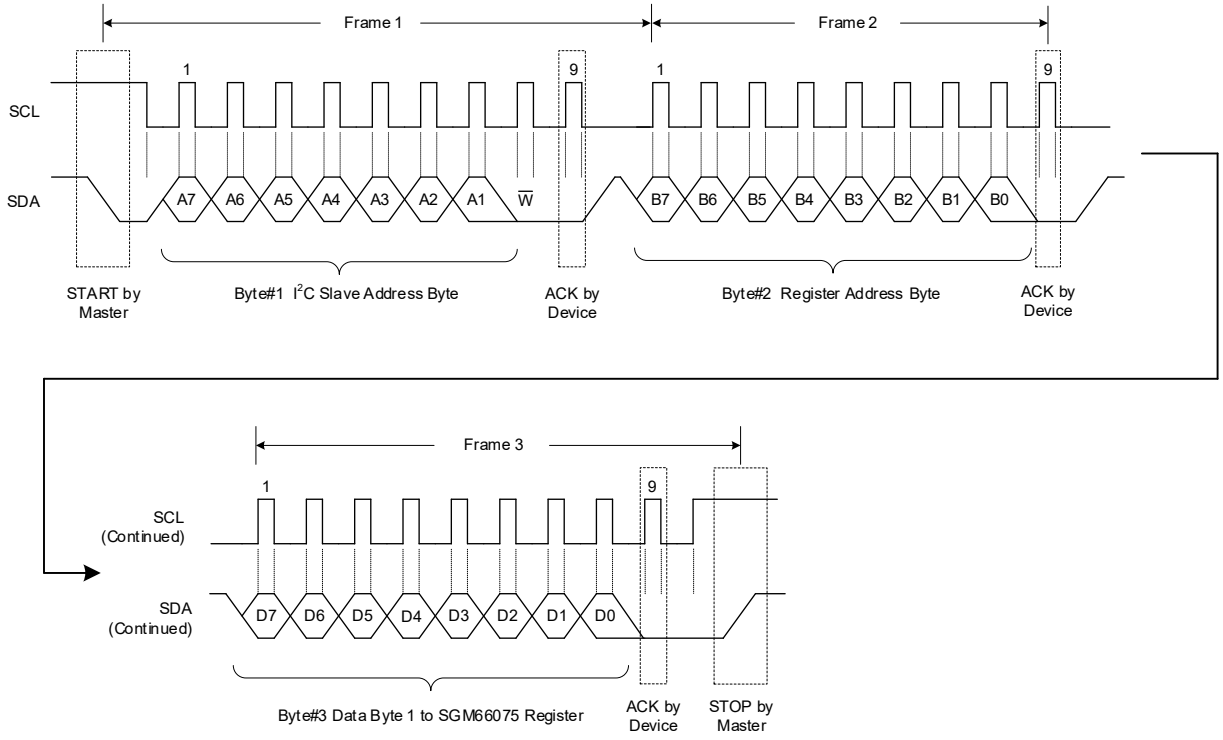


Figure 11. A Single Write Transaction

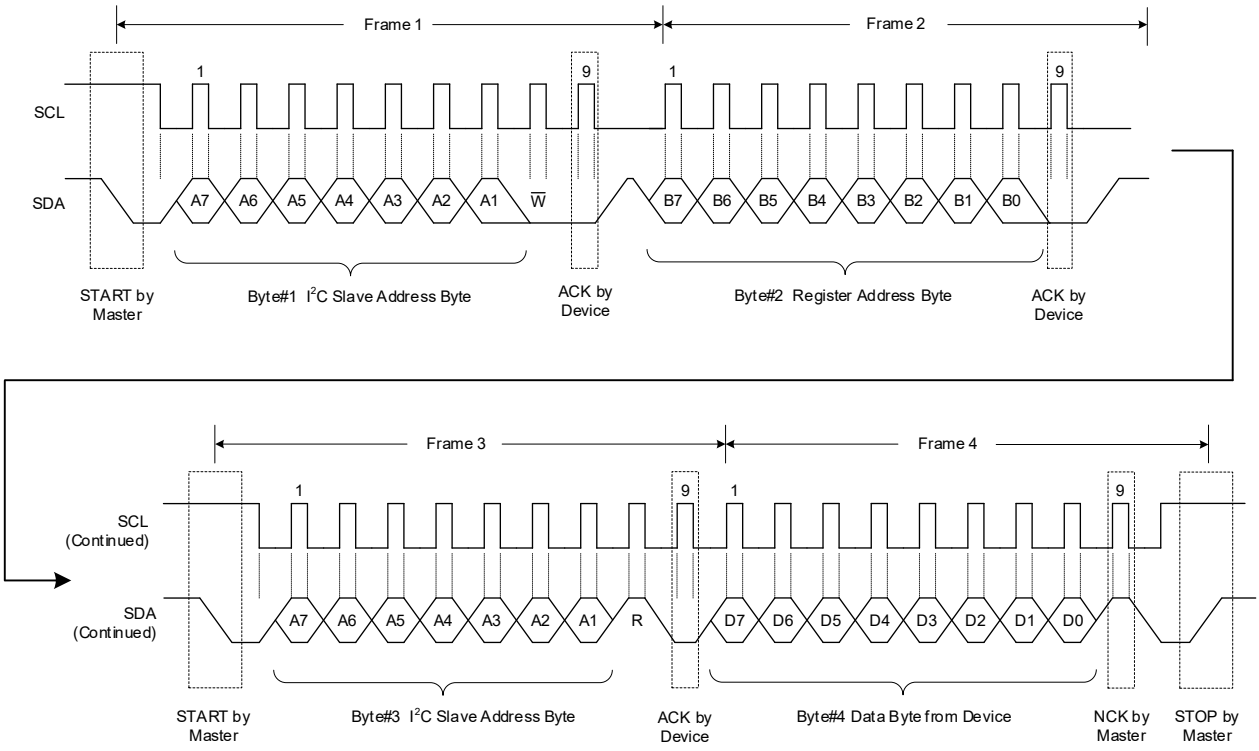


Figure 12. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM66075 for REG0x00 through REG0x04 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (its address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

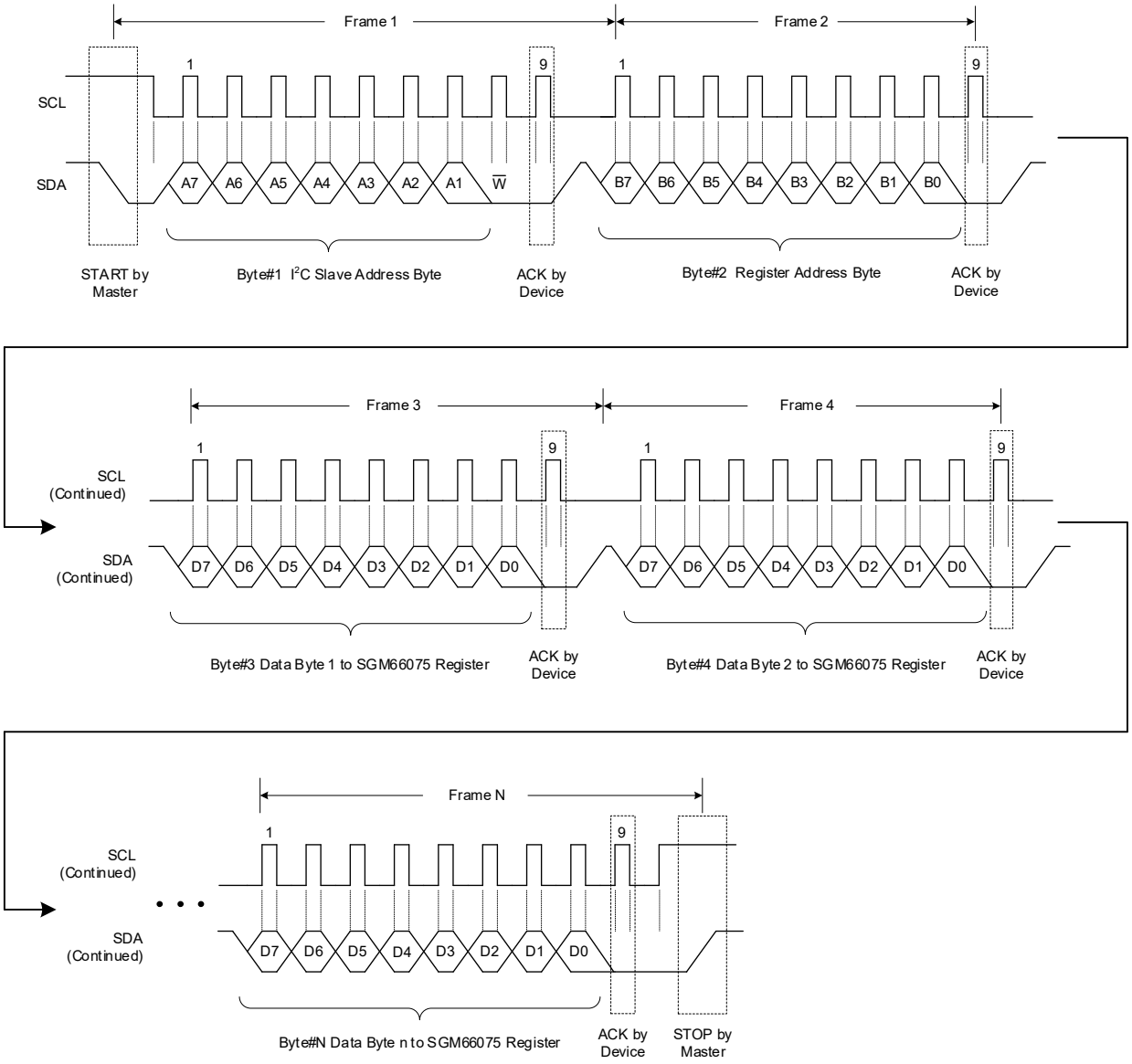


Figure 13. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

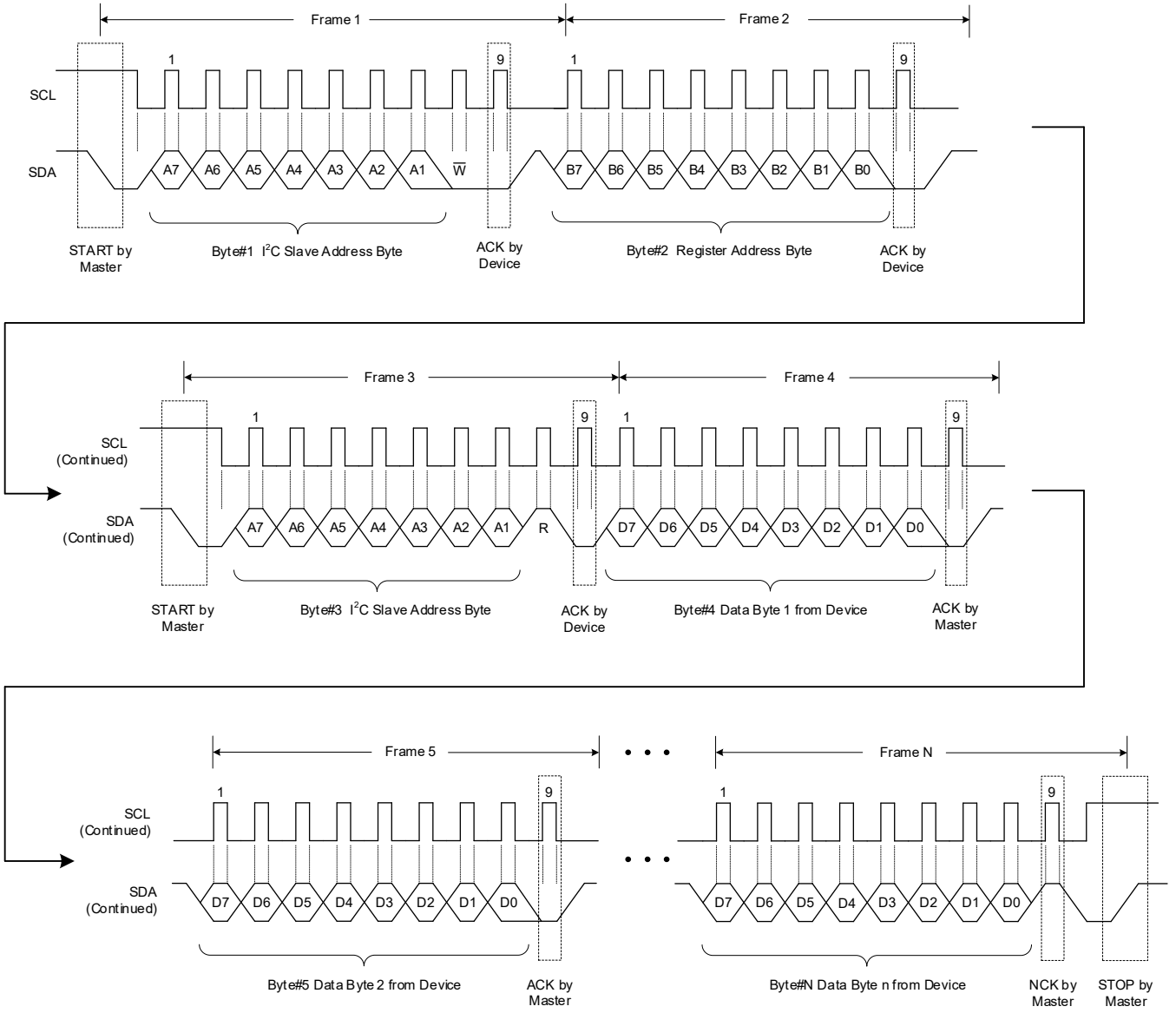


Figure 14. A Multi-Read Transaction

REGISTER MAPS

Bit Types:
R: Read only
R/W: Read/Write
RC: Bit(s) cleared to 0 by being read

7-bit I^2C Slave Device Address: 0b1110 1xx + W/R
The device I^2C address is determined by the state of ADDR pin in the POR sequence, as described in Slave Address Selection section.

I^2C Register Address Map

Register Name	Address	R/W	Description	Default
DEVICE ID	0x00	R	DEVICE ID	0x21
CONFIG	0x01	R/W	CONFIG	0x68
VOUT	0x02	R/W	VOUT SET	0x0B
ILIMSET	0x03	R/W	ILIM SET	0x16
STATUS	0x04	R	Status	0x10

REG0x00: DEVICE ID Register [Reset = 0x21]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Manufacturer[3:0]	0010	R	Device identity.
D[3:0]	DEV_VER[3:0]	0001	R	Device version.

REG0x01: CONFIG Register [Reset = 0x68]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/W	Device reset bit. 0: Keep current register setting. 1: Reset to default register value. This bit returns to 0 after register reset is completed.	REG_RST
D[6]	DEV_EN	1	R/W	Device enable bit. 0: Disable the device. 1: Device enable.	REG_RST
D[5:4]	AUTO_BYPASS[1:0]	10	R/W	Device auto bypass bit. 00: Device operates in low power bypass mode. 01: Device operates in forced bypass mode (Only bypass mode). 10 ~ 11: Device operates in auto bypass mode (Auto transition between DC/DC Boost and bypass).	REG_RST
D[3]	VOUT_DISCHG	1	R/W	0: When the regulator is disabled, VOUT is not discharged. 1: When the regulator is disabled, VOUT discharges through an internal pull-down resistor.	REG_RST
D[2]	PLIM	0	R/W	Changing PLIM when V_{OUT} < V_{IN} - 300mV. 0: Set PLIM = 7A. 1: Set PLIM = 5A.	REG_RST
D[1]	SSFM	0	R/W	Spread modulation control. 0: Spread spectrum modulation is disabled. 1: Spread spectrum modulation is enabled in PWM mode.	REG_RST
D[0]	MODE_CTRL	0	R/W	Device mode of operation bit. 0: PFM with automatic transition into PWM operation. 1: Forced PWM operation.	REG_RST

REGISTER MAPS (continued)

REG0x02: VOUT Register [Reset = 0x0B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PLIM_OFF	0	R/W	Enable/Disable PLIM in Boost mode. 0: PLIM enabled. 1: PLIM disabled.	REG_RST
D[6]	LOOP_MODECHANGE	0	R/W	Regulating the loop parameters when mode changing from bypass to Boost. 0: Error amplifier remains unchanged. 1: Error amplifier increases when mode changes.	REG_RST
D[5:0]	VOUT_SET[5:0]	001011	R/W	Output voltage setting, DC/DC Boost/bypass mode change. It has an offset of 2.85V and a range from 2.85V to 5.0V with 50mV voltage step for VOUT. It is set to 3.4V (SGM66075)/3.6V (SGM66075-3.6) as default. 000000: 2.850V 000001: 2.900V 000010: 2.950V 000011: 3.000V 000100: 3.050V 000101: 3.100V 000110: 3.150V 000111: 3.200V 001000: 3.250V 001001: 3.300V 001010: 3.350V 001011: 3.400V (SGM66075 Default) 001100: 3.450V 001101: 3.500V 001110: 3.550V 001111: 3.600V (SGM66075-3.6 Default) 010000: 3.650V 010001: 3.700V 010010: 3.750V 010011: 3.800V 010100: 3.850V 010101: 3.900V 010110: 3.950V 010111: 4.000V 011000: 4.050V 011001: 4.100V 011010: 4.150V 011011: 4.200V 011100: 4.250V 011101: 4.300V 011110: 4.350V 011111: 4.400V 100000: 4.450V 100001: 4.500V 100010: 4.550V 100011: 4.600V 100100: 4.650V 100101: 4.700V 100110: 4.750V 100111: 4.800V 101000: 4.850V 101001: 4.900V 101010: 4.950V 101011 ~ 111111: 5.000V	REG_RST

REGISTER MAPS (continued)

REG0x03: ILIMSET Register [Reset = 0x16]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BYPASS_ILIM2_OFF	0	R/W	Enable/Disable 9.4A Bypass Switch Current Limit in Bypass mode. 0: 9.4A bypass current limit enabled. 1: 9.4A bypass current limit disabled.	REG_RST
D[6]	BYPASS_ILIM1_OFF	0	R/W	Enable/Disable 6.5A Bypass Switch Current Limit in Bypass mode. 0: 6.5A bypass current limit enabled. 1: 6.5A bypass current limit disabled.	REG_RST
D[5]	ILIM_OFF	0	R/W	Enable/Disable Valley Inductor Current Limit in DC/DC Boost mode. 0: Current Limit Enabled. 1: Current Limit Disabled.	REG_RST
D[4]	Soft-Start	1	R/W	Soft-Start selection bit. 0: DC/DC Boost soft-start current is limited per ILIM bit settings. 1: DC/DC Boost soft-start current is limited to 2000mA (TYP) inductor valley current.	REG_RST
D[3:0]	ILIM[3:0]	0110	R/W	Inductor valley current limit in DC/DC Boost mode. 0000: 4000mA 0001: 4500mA 0010: 5000mA 0011: 5500mA 0100: 6000mA 0101: 6500mA 0110: 7000mA(Default) 0111: 7500mA 1000: 8000mA 1001: 8500mA 1010 ~ 1111: 9000mA	REG_RST

REG0x04: STATUS Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	TSD_FLAG	0	RC	Thermal shutdown flag bit. 0: Normal operation. 1: Thermal shutdown tripped. This flag is reset after readout.	REG_RST
D[6]	RESERVED	0	R	Reserved.	REG_RST
D[5]	DCDCMODE_STAT	0	R	DC/DC mode of operation status bit. 0: Device operates in PWM mode. 1: Device operates in PFM mode.	REG_RST
D[4]	OPMODE_STAT	1	R	Device mode of operation status bit. 0: Device operates in bypass mode. 1: Device operates in DC/DC mode.	REG_RST
D[3]	ILIM_BPS_FLAG	0	RC	Current limit flag bit (bypass mode). 0: Normal operation. 1: Indicate that the bypass FET current limit has triggered in bypass mode. This flag is reset after readout.	REG_RST
D[2]	ILIM_BST_FLAG	0	RC	Current limit flag bit (DC/DC Boost mode). 0: Normal operation. 1: Indicate that the valley inductor current limit has triggered in DC/DC Boost mode. This flag is reset after readout.	REG_RST
D[1]	FAULT_FLAG	0	RC	FAULT flag bit. 0: Normal operation. 1: Indicate that a fault condition has occurred. This flag is reset after readout.	REG_RST
D[0]	PGOOD_STAT	0	R	Power Good status bit. 0: Indicate the output voltage is out of regulation. 1: Indicate the output voltage is within its nominal range. This bit is set if the converter is forced in bypass mode.	REG_RST

APPLICATION INFORMATION

Typical Application

The SGM66075 can be used as a power solution for portable devices. For portable devices using single-cell Li-Ion battery application, the SGM66075 can output 4A at 2.5V input and 3.4V output.

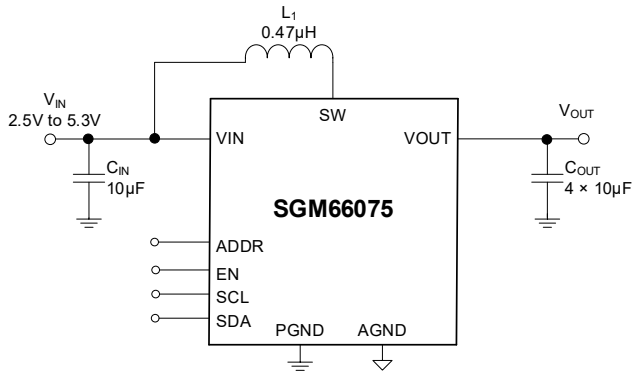


Figure 15. Typical Application Circuit

Application Design Requirement

The design parameters are listed in Table 1 and the external components are listed in Table 2.

Table 1. Design Parameters

Parameters	Values
Input Voltage	2.5V to 5.3V
Output Voltage	V_{OUT} = 3.4V (V_{IN} < 3.5V), V_{OUT} = V_{IN} (V_{IN} > 3.5V)
Output Load Current	4A

Table 2. External Components

Designator	Value	Part Number
Input Capacitor (C_{IN})	10μF	Murata GRM155R60J106ME05
Output Capacitor (C_{OUT})	4 × 10μF	Murata GRM155R60J106ME05
Inductor (L_1)	0.47μH	Wurth 744373240047

Inductor Selection

The inductor serves as an energy storage element for the SGM66075. The recommended inductance for the SGM66075 is 0.33μH or 0.47μH. The selected inductor should have sufficient saturation current at minimal input voltage. For this application requirement, the maximal inductor current can be calculated with the following equations.

The average inductor current can be calculated with Equation 1.

$$I_{IN} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} = \frac{I_{OUT}}{(1\text{-}D) \times \eta} \quad (1)$$

The peak-to-peak inductor ripple current can be calculated with Equation 2.

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (2)$$

Then the peak inductor current can be calculated by Equation 3.

$$I_{L(PEAK)} = I_{IN} + \frac{\Delta I_L}{2} = \frac{I_{OUT}}{(1\text{-}D) \times \eta} + \frac{V_{IN} \times D}{2 \times L \times f_{SW}} \quad (3)$$

Based on the peak inductor current, a 0.47μH 744373240047 from Wurth is selected.

When selecting the inductor, lower DCR inductor is recommended since it offers better conversion efficiency.

Input Capacitor Selection

Boost converter's input capacitor has continuous current throughout the entire switching cycle, a 0402 10μF ceramic capacitor should be placed as close as possible between the VIN pin and GND pin of the device. For applications where the SGM66075 is located far away from the input source, a 47μF or higher capacitance capacitor is recommended to damp the wiring harness inductance.

Output Capacitor Selection

The output capacitors used for this design requirement are 4 × 10μF capacitors from Murata. Ceramic capacitor's DC derating effect should be taken into consideration when selecting the output capacitor, the recommended minimal effective output capacitance for this application is 14μF.

Output capacitor serves as the energy storage element for the output load as well as suppressing output voltage ripple. More output capacitance helps to improve the output voltage ripple as well as improving load transient performance.

Equation 4 is used to estimate the necessary capacitance to achieve desired output voltage ripple, where ΔV is the maximum allowed ripple.

$$C_{MIN} = \frac{I_{OUT} \times (V_{OUT}\text{-}V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (4)$$

APPLICATION INFORMATION (continued)

Layout Considerations

In addition to component selection, layout is a critical step to ensure the performance of any switch mode power supplies. Poor layout could result in system instability, EMI failure, and device damage. Thus, place the inductor, input and output capacitors as close to the IC as possible, and use wide and short traces for current carrying traces to minimize PCB inductance.

For Boost converter, the current loop of the output capacitor from VOUT pin back to the PGND pin of the device should be as small as possible.

Layout Example

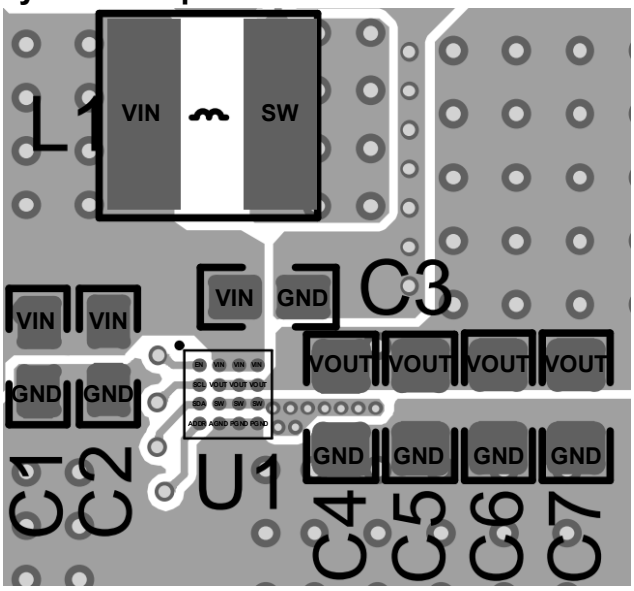


Figure 16. SGM66075 PCB Layout

REVISION HISTORY

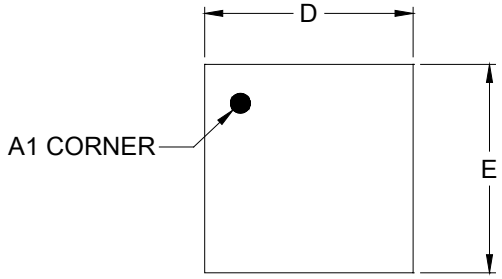
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

FEBRUARY 2025 – REV.A to REV.A.1	Page
Updated the Figure 1, Figure 16 and Electrical Characteristics	1, 24, 5
Updated the Register Maps	21-23
Updated the Pin Description	3
Deleted I^2C Interface Timing Characteristics and I^2C Interface Timing Diagram	6

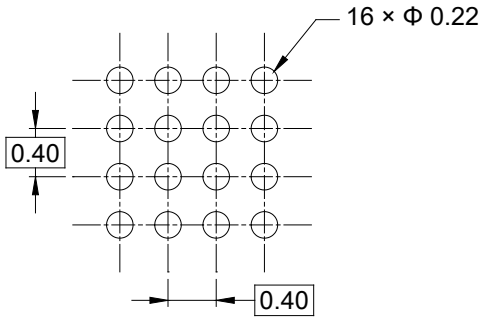
Changes from Original (SEPTEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

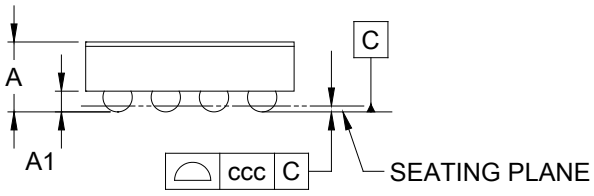
WLCSP-1.73×1.73-16B



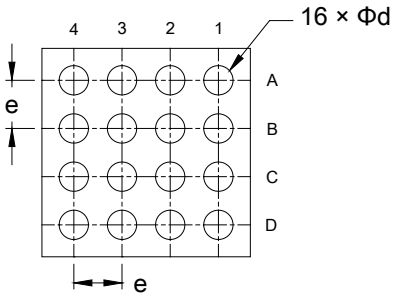
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



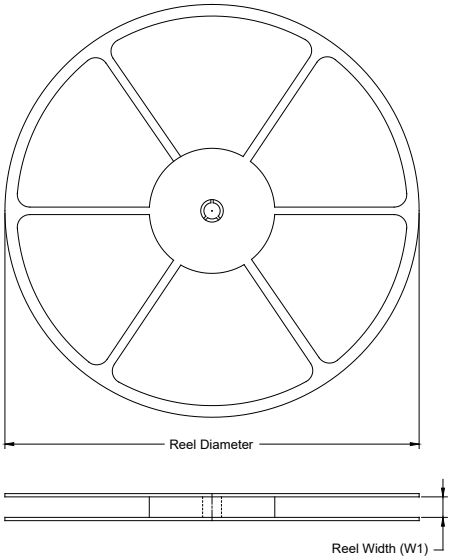
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.625
A1	0.152	-	0.192
D	1.700	-	1.760
E	1.700	-	1.760
d	0.213	-	0.273
e	0.400 BSC		
ccc	0.050		

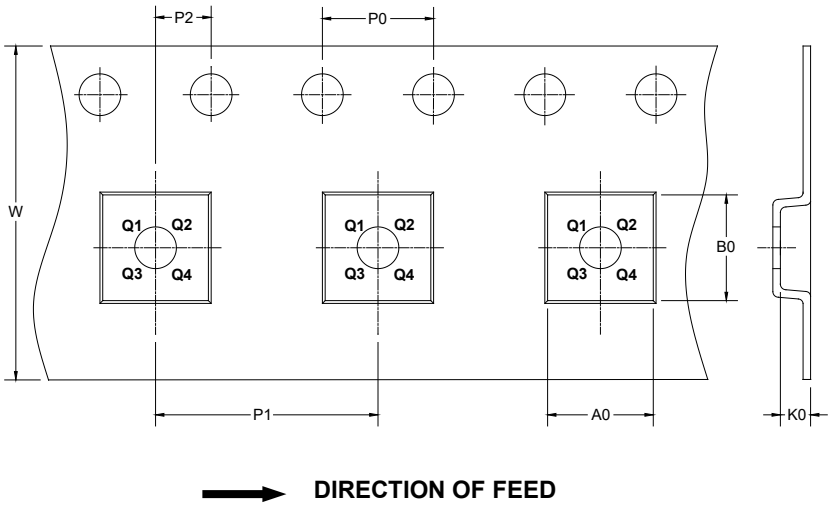
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



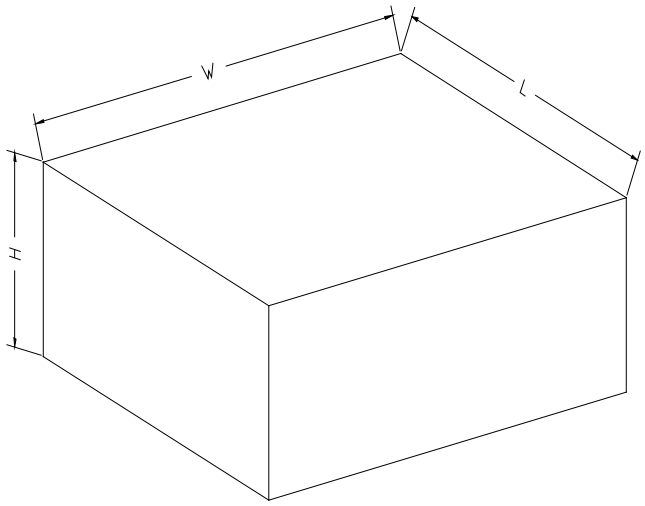
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.73×1.73-16B	7″	9.5	1.86	1.86	0.71	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002