SGM894B
Voltage Detector with Delay Time Adjustable

GENERAL DESCRIPTION

The SGM894B is a low power consumption voltage detector with high accuracy detection. The miniature device offers tremendous flexibility with an adjustable threshold that is available from 1V to 5.0V with 0.1V increments.

In addition, the C_D pin of SGM894B has an external capacitor connected to GND, which can adjust the release delay time. Consequently delay time can be set to more than 1s when the delay capacitor (C_D) is 1μF. The device is very suitable for applications in power sequencing, reset sequencing and power switching.

The SGM894B is available in Green XTDFN-0.9×1.2-4L and SC70-4 (R) packages. They are specified over the -40℃ to +125℃ operating temperature range.

APPLICATIONS

Power Sequencing and Reset Sequencing
Power Switching
Portable Equipment
Computers/Servers

FEATURES

- **High Accuracy Detection: ±1% (TYP)**
- **Low Power Consumption:0.4μA (TYP) at V_{IN} = 1V**
- **Detection Voltage Range: 1.0V to 5.0V (0.1V Increments)**
- **Operating Voltage Range: 1V to 6V**
- **Detection Voltage Temperature Coefficient: ±40ppm/℃ (TYP)**
- **N-Channel Open-Drain Output**
- **Built-in Delay Circuit: Adjustable Delay Time**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green XTDFN-0.9×1.2-4L and SC70-4 (R) Packages**

TYPICAL APPLICATION

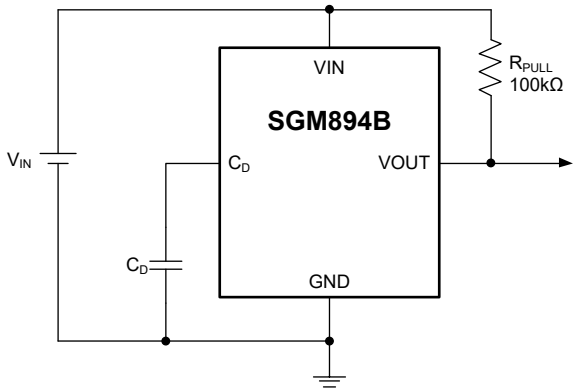


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	DETECTION VOLTAGE (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM894B-1.0	1.0	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.0XXEJ4G/TR	Q0XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.0XC4G/TR	OS0XX	Tape and Reel, 3000
SGM894B-1.1	1.1	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.1XXEJ4G/TR	Q6XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.1XC4G/TR	OS1XX	Tape and Reel, 3000
SGM894B-1.2	1.2	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.2XXEJ4G/TR	R9XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.2XC4G/TR	OS2XX	Tape and Reel, 3000
SGM894B-1.4	1.4	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.4XXEJ4G/TR	S1XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.4XC4G/TR	OS4XX	Tape and Reel, 3000
SGM894B-1.6	1.6	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.6XXEJ4G/TR	S3XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.6XC4G/TR	OS6XX	Tape and Reel, 3000
SGM894B-1.8	1.8	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-1.8XXEJ4G/TR	S4XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-1.8XC4G/TR	OS7XX	Tape and Reel, 3000
SGM894B-2.0	2.0	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.0XXEJ4G/TR	S6XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.0XC4G/TR	OS9XX	Tape and Reel, 3000
SGM894B-2.2	2.2	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.2XXEJ4G/TR	S8XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.2XC4G/TR	OSBXX	Tape and Reel, 3000
SGM894B-2.3	2.3	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.3XXEJ4G/TR	S9XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.3XC4G/TR	OSCXX	Tape and Reel, 3000
SGM894B-2.5	2.5	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.5XXEJ4G/TR	U0XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.5XC4G/TR	OSEXX	Tape and Reel, 3000
SGM894B-2.7	2.7	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.7XXEJ4G/TR	U2XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.7XC4G/TR	OT0XX	Tape and Reel, 3000
SGM894B-2.8	2.8	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.8XXEJ4G/TR	U3XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.8XC4G/TR	OT1XX	Tape and Reel, 3000

PACKAGE/ORDERING INFORMATION (continued)

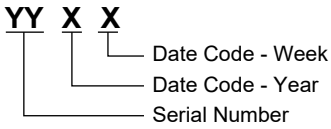
MODEL	DETECTION VOLTAGE (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM894B-2.9	2.9	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-2.9XXEJ4G/TR	U4XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-2.9XC4G/TR	OT2XX	Tape and Reel, 3000
SGM894B-3.0	3.0	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-3.0XXEJ4G/TR	Q3XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-3.0XC4G/TR	OT3XX	Tape and Reel, 3000
SGM894B-3.3	3.3	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-3.3XXEJ4G/TR	U7XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-3.3XC4G/TR	OT6XX	Tape and Reel, 3000
SGM894B-3.9	3.9	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-3.9XXEJ4G/TR	V3XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-3.9XC4G/TR	OTCXX	Tape and Reel, 3000
SGM894B-4.6	4.6	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-4.6XXEJ4G/TR	Q5XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-4.6XC4G/TR	OU3XX	Tape and Reel, 3000
SGM894B-5.0	5.0	XTDFN-0.9×1.2-4L	-40℃ to +125℃	SGM894B-5.0XXEJ4G/TR	L7XX	Tape and Reel, 3000
		SC70-4 (R)	-40℃ to +125℃	SGM894B-5.0XC4G/TR	OU7XX	Tape and Reel, 3000

NOTE: For more models not listed above, please contact your local SGMICRO sales representatives.

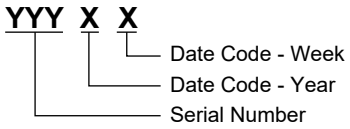
MARKING INFORMATION

NOTE: XX = Date Code.

XTDFN-0.9×1.2-4L



SC70-4 (R)



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN} ..... GND - 0.3V to 7V
Output Current, I_{OUT} 30mA
Output Voltage Range, V_{OUT} ..... GND - 0.3V to 7V
C_D Pin Voltage Range, V_{CD} ..... GND - 0.3V to V_{IN} + 0.3V
C_D Pin Current, I_{CD} 5mA
Package Thermal Resistance
XTDFN-0.9×1.2-4L, θ_{JA} ..... 243℃/W
SC70-4 (R), θ_{JA} ..... 680℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

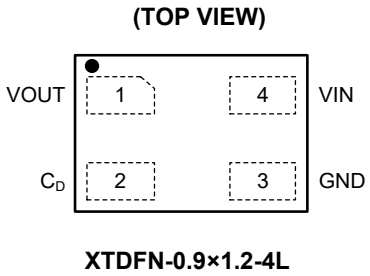
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

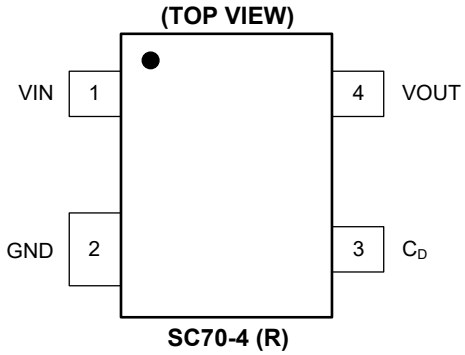
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



XTDFN-0.9×1.2-4L



SC70-4 (R)

PIN DESCRIPTION

PIN		NAME	FUNCTION
XTDFN-0.9×1.2-4L	SC70-4 (R)		
1	4	VOUT	Active-Low Output Pin.
2	3	C_D	Adjustable Delay Capacitor Pin.
3	2	GND	Ground Pin.
4	1	VIN	Supply Voltage Pin.

ELECTRICAL CHARACTERISTICS

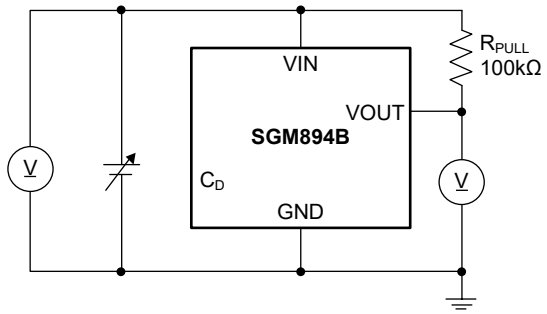
(T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_{IN}	V_{DET} = 1V to 5V, T_J = -40℃ to +125℃		1		6	V
Detection Voltage	V_{DET}	V_{IN} = 1V to 6V, Test Circuit 1	T_J = +25℃	E-1			V
			T_J = -40℃ to +125℃	E-2			
Hysteresis Voltage	V_{HYS}	V_{IN} = 1V to 6V, R_{PULL} = 100kΩ, Test Circuit 1		E-3			V
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/(\Delta T_J \times V_{DET})$	T_J = -40℃ to +125℃, Test Circuit 1			±40	±150	ppm/℃
Supply Current	I_{CC}	Test Circuit 2	V_{IN} = 1V		0.4	0.7	μA
			V_{IN} = 3V		0.6	1.1	
			V_{IN} = 6V		1.0	1.5	
Output Current	I_{OUT}	V_{DS_NCH} = 0.5V, Test Circuit 3	V_{IN} = 1V	0.2	0.8		mA
			V_{IN} = 2V	9.0	12.0		
			V_{IN} = 3V	13.0	17.5		
			V_{IN} = 4V	15.0	20.5		
			V_{IN} = 5V	16.0	22.0		
			V_{IN} = 6V	16.5	23.0		
Leakage Current	I_{LEAK}	V_{IN} = V_{OUT} = 6V, C_D: Open, Test Circuit 3			0.02	1.50	μA
Delay Resistance	R_{DELAY}	V_{IN} = 5V, V_{CD} = 0V, Test Circuit 4		1.7	2.2	2.6	MΩ
C_D Pin Sink Current	I_{CD}	V_{CD} = 0.5V, V_{IN} = 1V, Test Circuit 4		110	230	350	μA
C_D Pin Threshold Voltage	V_{TCD}	T_J = -40℃ to +125℃, Test Circuit 5	V_{IN} = 2V	0.9	1.0	1.2	V
			V_{IN} = 6V	2.9	3.0	3.2	
Detection Delay Time	t_{DET0}	V_{IN} = 0.9 × $V_{DET(T)}$ → 1.1 × $V_{DET(T)}$, C_D: Open, Test Circuit 6			40	80	μs
Release Delay Time	t_{DR0}	V_{IN} = 1.1 × $V_{DET(T)}$ → 0.9 × $V_{DET(T)}$, C_D: Open, Test Circuit 6			150	250	μs

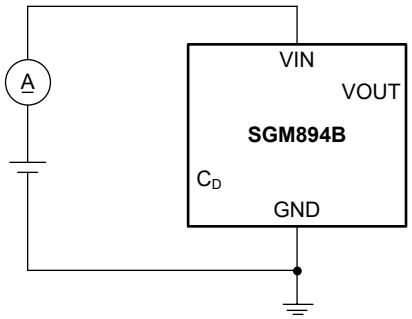
VOLTAGE CHART

Symbol	E-1		E-2		E-3		
Conditions	T_J = +25℃		T_J = -40℃ to +125℃		T_J = +25℃		
Nominal Voltage (V)	V_{DET} (V), 1% Accuracy		V_{DET} (V), 2% Accuracy		V_{HYS} (V)		
	MIN	MAX	MIN	MAX	MIN	TYP	MAX
1.0	0.990	1.010	0.980	1.020	0.030	0.050	0.070
1.1	1.089	1.111	1.078	1.122	0.033	0.055	0.077
1.2	1.188	1.212	1.176	1.224	0.036	0.060	0.084
1.4	1.386	1.414	1.372	1.428	0.042	0.070	0.098
1.6	1.584	1.616	1.568	1.632	0.048	0.080	0.112
1.8	1.782	1.818	1.764	1.836	0.054	0.090	0.126
2.0	1.980	2.020	1.960	2.040	0.060	0.100	0.140
2.2	2.178	2.222	2.156	2.244	0.067	0.110	0.153
2.3	2.277	2.323	2.254	2.346	0.070	0.115	0.160
2.5	2.475	2.525	2.450	2.550	0.076	0.125	0.174
2.7	2.673	2.727	2.646	2.754	0.082	0.135	0.188
2.8	2.772	2.828	2.744	2.856	0.085	0.140	0.195
2.9	2.871	2.929	2.842	2.958	0.088	0.145	0.202
3.0	2.970	3.030	2.940	3.060	0.091	0.150	0.209
3.3	3.267	3.333	3.234	3.366	0.100	0.165	0.230
3.9	3.861	3.939	3.822	3.978	0.118	0.195	0.272
4.6	4.554	4.646	4.508	4.692	0.139	0.230	0.321
5.0	4.950	5.050	4.900	5.100	0.151	0.250	0.349

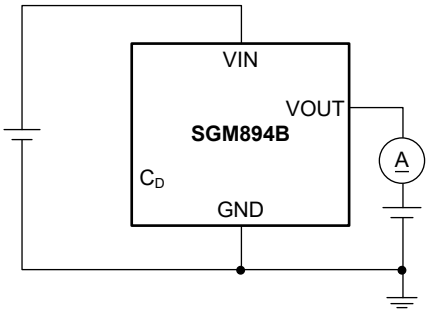
TEST CIRCUITS



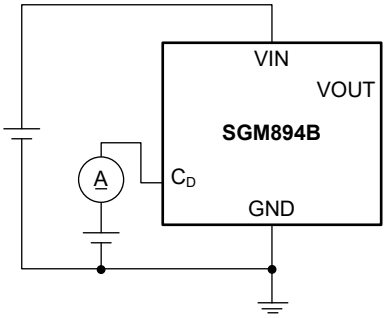
Test Circuit 1



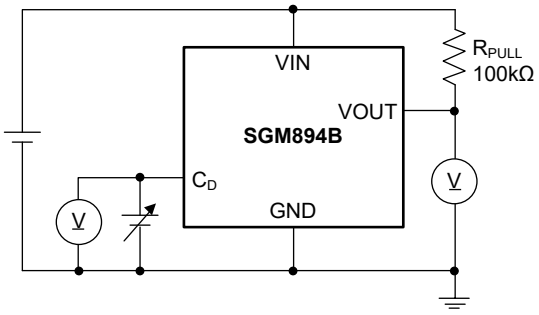
Test Circuit 2



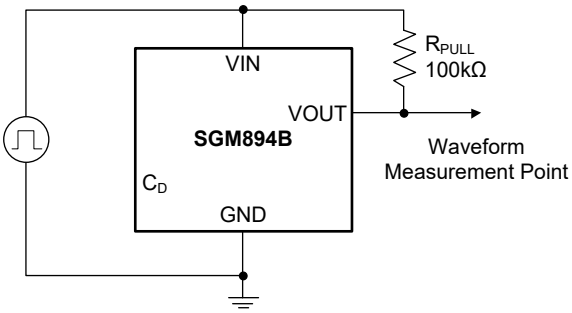
Test Circuit 3



Test Circuit 4



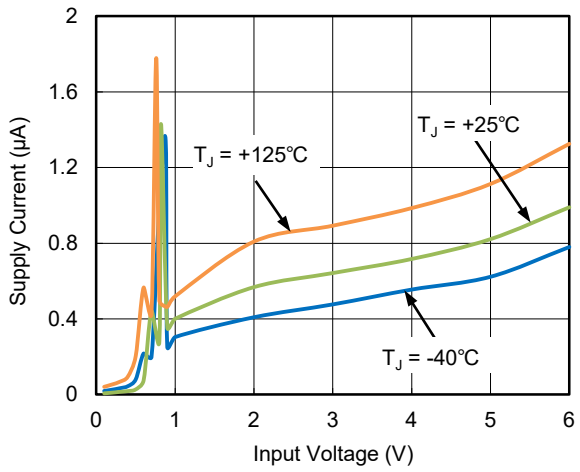
Test Circuit 5



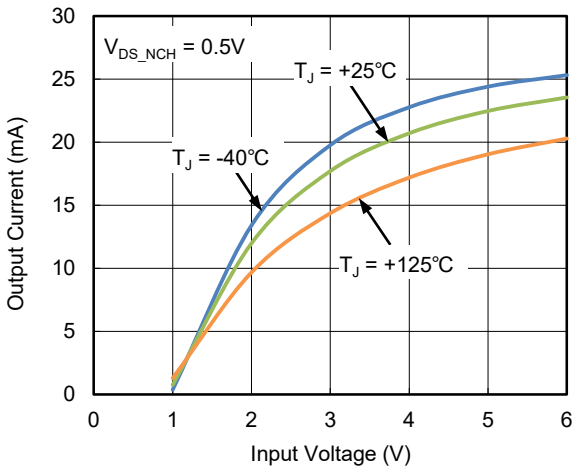
Test Circuit 6

TYPICAL PERFORMANCE CHARACTERISTICS

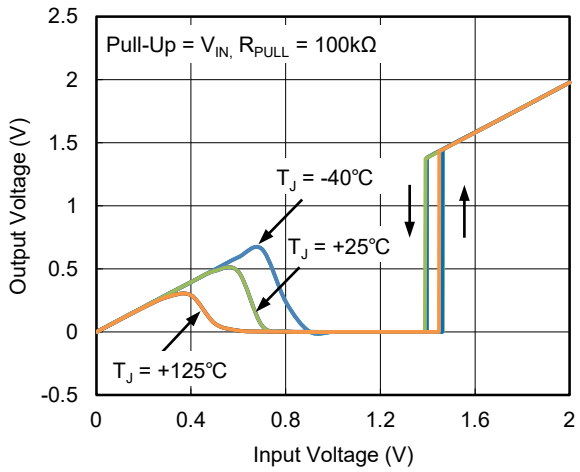
Supply Current vs. Input Voltage



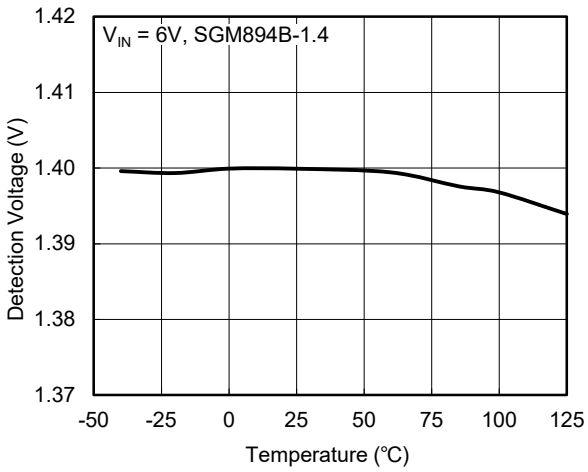
Output Current vs. Input Voltage



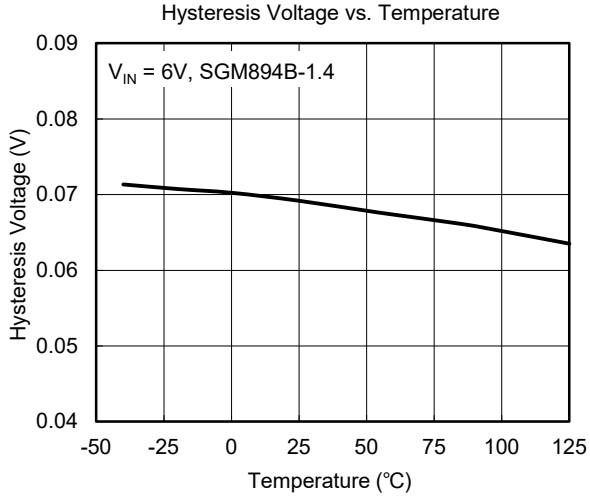
Output Voltage vs. Input Voltage



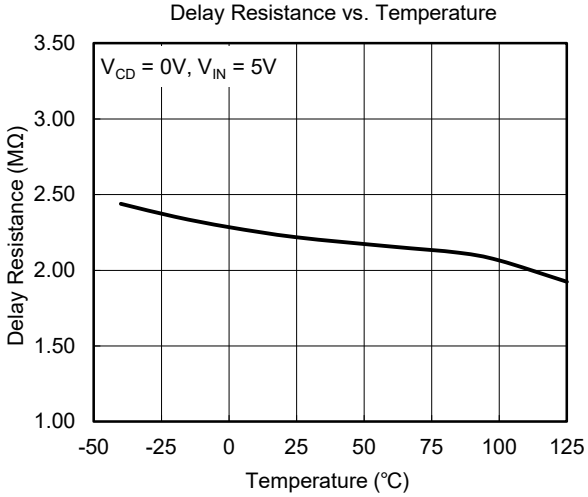
Detection Voltage vs. Temperature



Hysteresis Voltage vs. Temperature

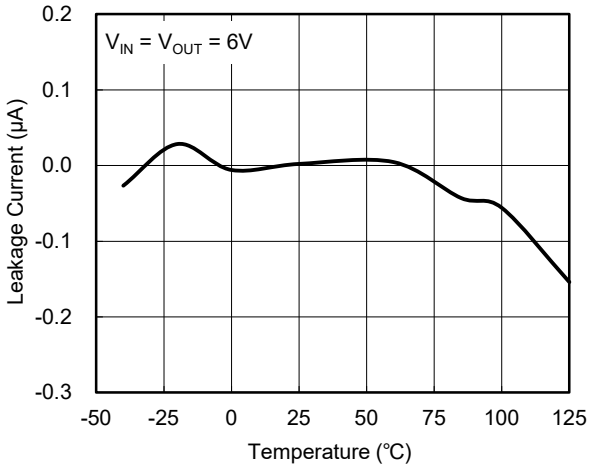


Delay Resistance vs. Temperature

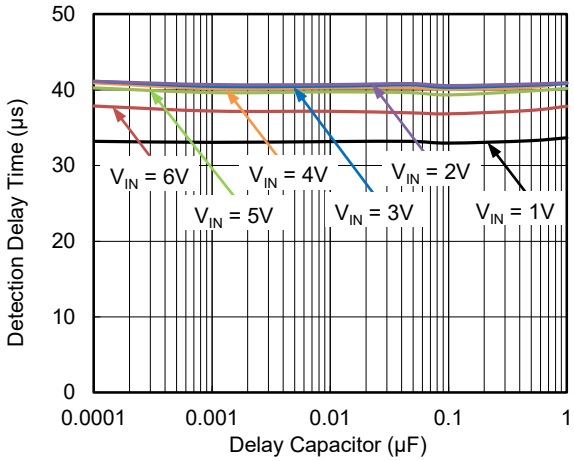


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

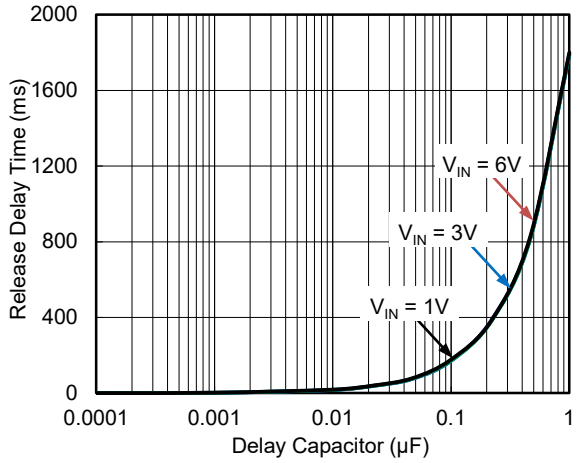
Leakage Current vs. Temperature



Detection Delay Time vs. Delay Capacitance



Release Delay Time vs. Delay Capacitance



FUNCTIONAL BLOCK DIAGRAM

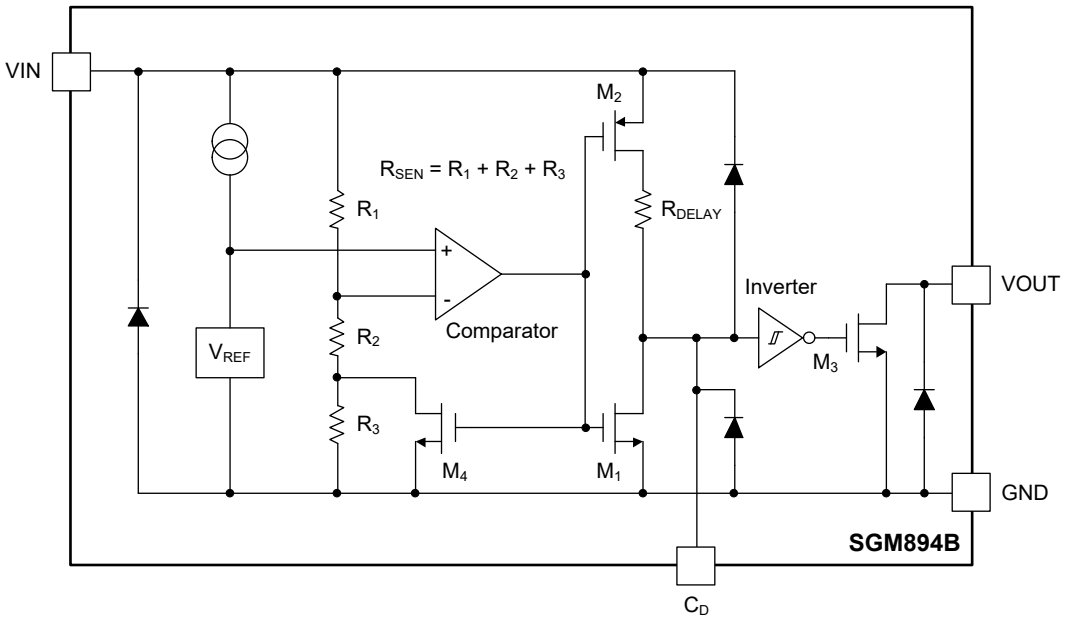


Figure 2. SGM894B Block Diagram

DETAILED DESCRIPTION

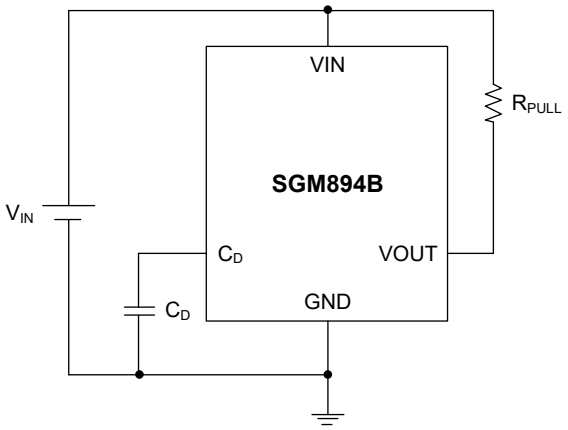


Figure 3. Typical Application Circuit Example

The output voltage (V_{OUT}) transition, the delay capacitance (C_D) charge and discharge are determined by the status of power supply and the input pin voltage (V_{IN}). Figure 4 is the timing chart of Figure 3. It may go through eight processes, and below words are shown as the description of the sequence.

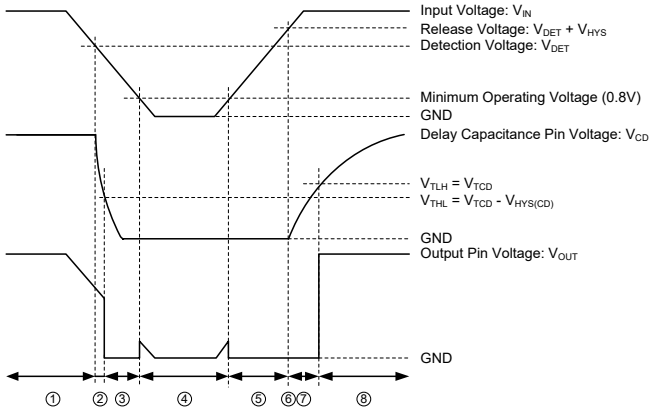


Figure 4. The Timing Chart of Figure 3

① Default Status before V_{IN} Falling

In original state, the delay capacitance voltage (V_{CD}) is charged to the input voltage (V_{IN}), which ranges from 1V to 6V.

In the beginning, V_{IN} is larger than the detection voltage (V_{DET}) plus the hysteresis (V_{HYS}). While V_{IN} starts dropping but still larger than V_{DET}, V_{OUT} keeps the high level (= V_{IN}).

NOTE: The high level voltage is determined by the power rail to which the pull-up resistor at V_{OUT} is connected.

② Triggered V_{DET} while V_{IN} Falling

When V_{IN} drops below V_{DET}, an N-ch transistor (M_1) is turned on to discharge the delay capacitor.

An internal inverter connected to the C_D pin is used as a comparator, where the high threshold $V_{TLH} = V_{TCD}$ and low-level threshold $V_{THL} = V_{TCD} - V_{HYS\_CD}$. Once V_{CD} drops to V_{THL}, the inverter state is toggled and V_{OUT} turns to logic low (= GND).

③ V_{OUT} Keeps Low until V_{IN} Rises

V_{CD} is fully discharged to GND and V_{IN} is below V_{DET}. Hence, V_{OUT} keeps logic low unless V_{IN} increases to $V_{DET} + V_{HYS}$ again.

④ V_{IN} Drops to GND

While the input pin voltage drops to less than 0.8V, and then increases to 0.8V or higher again, the output voltage may not be able to maintain the low level. Such an operation is called "Unspecified Operation".

⑤ V_{IN} Rising up to $V_{DET} + V_{HYS}$

The N-channel transistor (M_1) for the delay capacitance discharge will be turned off, and the delay capacitance will be charged via a delay resistor (R_{DELAY}), when V_{SEN} turns to be larger than $V_{DET} + V_{HYS}$.

⑥ C_D is Charged when V_{IN} Keeps High

Once V_{CD} is above V_{TCD}, when V_{IN} increases to $V_{DET} + V_{HYS}$ or higher, the C_D capacitor is charged with the time constant determined by R_{DELAY} and C_D. Thus, the release delay time (t_{DR}) can be given as:

$$t_{DR} = R_{DELAY} \times C_D \times 0.79 \quad (1)$$

where R_{DELAY} is 2.2MΩ (TYP).

Take C_D = 0.68μF as an example, t_{DR} is:

$$2.2 \times 10^6 \times 0.68 \times 10^{-6} \times 0.79 = 1182 \text{ (ms)}$$

NOTE: Because the time described in ③ is very short, t_{DR} may be relatively short when V_{CD} is not strictly discharged to GND.

⑦ V_{OUT} Goes High when C_D is Charged Full

When the C_D pin voltage reaches the C_D pin rising logic threshold voltage (= V_{TCD}), the inverter will be inverted. As a result, V_{OUT} changes into the high level (= V_{IN}). The release delay time without C_D (t_{DR0}) is defined as time which ranges from $V_{IN} = V_{DET} + V_{HYS}$ to the V_{OUT} of high level with unconnected C_D pin.

⑧ V_{OUT} Keeps High when $V_{IN} > V_{DET}$

The C_D pin is charged until the V_{CD} increases the input voltage level, when the input pin voltage is higher than the detection voltage ($V_{IN} > V_{DET}$). Therefore, V_{OUT} maintains the high level (= V_{IN}).

DETAILED DESCRIPTION (continued)

The V_{OUT} status is determined by the V_{IN} and V_{CD}. A summary table of transitions about V_{OUT} is shown below.

Table 1. Function Chart

V_{IN}	V_{CD}	Transition of V_{OUT} Condition (1)		
		①	⇒	②
L	L	L	⇒	L
	H			
	L	H		
	H			
H	L	L	⇒	L
	H		⇒	H
	L	H	⇒	
	H			

NOTE:
1. V_{OUT} transits from condition ① to ② because of the combination of V_{CD} and V_{IN}. V_{IN} should exceed the lowest operation voltage.

Examples:
(1). V_{OUT} ranges from 'L' to 'H' in the case of V_{IN} = 'H' ($V_{IN} \geq V_{DET} + V_{HYS}$), V_{CD} = 'H' ($V_{CD} \geq V_{TCD}$) while V_{OUT} is 'L'.

(2). V_{OUT} maintains 'H' when V_{CD} ranges from 'H' to 'L' ($V_{CD} \leq V_{TCD} - V_{HYS\_CD}$), V_{IN} = 'H' and V_{CD} = 'L' when V_{OUT} becomes 'H' in ex.1.

The release delay time is adjustable by the external capacitor C_D. The t_{DR} values for common ideal capacitors are shown below.

Table 2. Release Delay Time Chart (1) (2)

Delay Capacitance (C_D) (μF)	Release Delay Time (t_{DR}) (TYP) (ms)
0.010	17.4
0.022	38.2
0.047	81.7
0.100	174
0.220	382
0.470	817
1.000	1740

NOTE: The t_{DR} values above are calculated by the Equation 1.

APPLICATION INFORMATION

1. Do not exceed the absolute conditions, and use this IC within the stated maximum ratings. For temporary transitional voltage drop or voltage rising phenomenon, the IC may fail if the rated value is exceeded.

2. Note that a very noisy voltage implementing at the input voltage pin may cause a wrong operation. It is recommended to connect a decouple capacitor as close as possible to the input voltage pin to alleviate this phenomenon. Sometimes, users will mount a resistor between the power supply and the VIN pin. This resistor and the decouple capacitor build a low pass filter which filters the noise of the input voltage. In this case, the IC operation current generates a voltage drop through the series resistor. If the input pin voltage falls below the minimum operating voltage range, the operation may be wrong. Oscillation of the circuit may occur if the voltage drop exceeds the hysteresis voltage.

3. In case of fast VIN drop condition from 6V to 0V at release condition with a capacitor connected to the C_D pin, please place a Schottky barrier diode between the VIN pin and the C_D pin (see Figure 5).

4. The output pin of SGM894B is an open-drain NMOS. Consequently, the V_{OUT} voltage at detection and release condition is determined by resistance of a pull-up resistor and ON/OFF resistance of the NMOS. Choose suitable resistance of the pull-up resistor according to Figure 6.

During detection, the formula is given as:

$$V_{OUT} = V_{PULL}/(1 + R_{PULL}/R_{ON}) \quad (2)$$

where:
V_{PULL} is the pull-up voltage.
R_{ON} (1) is the on-resistance of N-channel driver M_3 that can be calculated as V_{DS_NCH}/I_{OUT} from electrical characteristics.

For example, when R_{ON} (2) = $0.5/(0.8 \times 10^{-3})$ = 625Ω (MIN) at V_{IN} = 1V, V_{PULL} = 3V and V_{OUT} ≤ 0.1V at detection, R_{PULL} can be calculated as follows:

$R_{PULL} = (V_{PULL}/V_{OUT} - 1) \times R_{ON} = (3/0.1 - 1) \times 625 \approx 18k\Omega$

In this case, R_{PULL} should be selected higher than or equal to 18kΩ in order to keep the output voltage less than 0.1V during detection.

NOTES:
1. R_{ON} is bigger when V_{IN} is smaller.

2. For calculation, choose the minimum V_{IN} value among the input voltage range.

During releasing, the formula is given as:

$$V_{OUT} = V_{PULL}/(1 + R_{PULL}/R_{OFF}) \quad (3)$$

where:
V_{PULL} is the pull-up voltage.
R_{OFF} is the off-resistance of N-channel driver M_3 that is 15MΩ (MIN) when the driver is off (as to V_{OUT}/I_{LEAK}).

For example, when V_{PULL} = 6V and $V_{OUT} \geq 5.99V$, R_{PULL} can be calculated as follows:

$R_{PULL} = (V_{PULL}/V_{OUT} - 1) \times R_{OFF} = (6/5.99 - 1) \times 15 \times 10^6 \approx 25k\Omega$

It is recommended to select the R_{PULL} smaller or equal to 25kΩ so that the output voltage can be higher than 5.99V during releasing.

6. SGMICRO is committed to product improvement and reliability. Users are required to incorporate fail-safe designs and post-aging protection treatment in their systems.

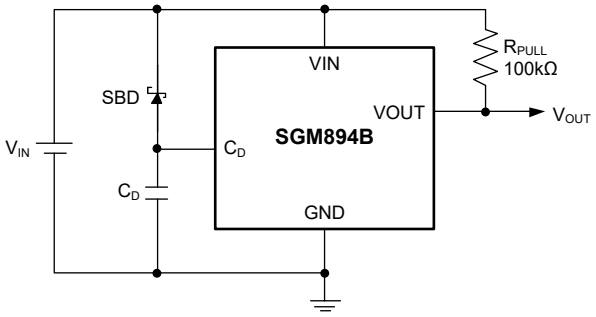
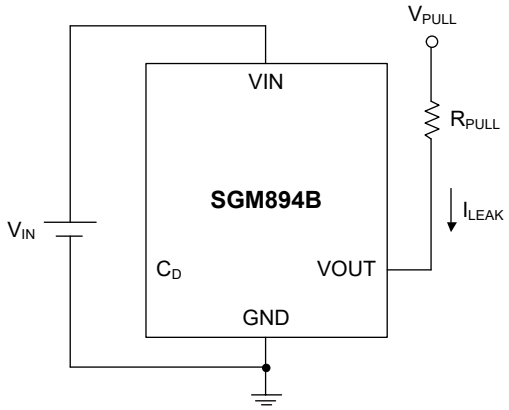


Figure 5. Circuit Example with the Delay Capacitor Pin (C_D) Connected to a Schottky Barrier Diode



NOTE: $R_{OFF} = V_{OUT}/I_{LEAK}$.

Figure 6. Circuit Example of the SGM894B

REVISION HISTORY

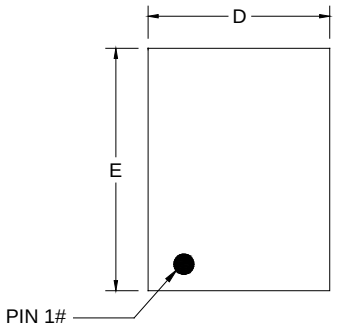
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

SEPTEMBER 2024 – REV.A to REV.A.1	Page
Updated Package/Ordering Information section	2, 3
Updated Voltage Chart section	6
Updated Detail Description section	11
Added Application Information section	13

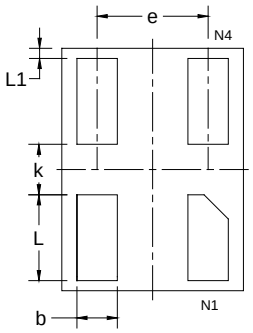
Changes from Original (JUNE 2021) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

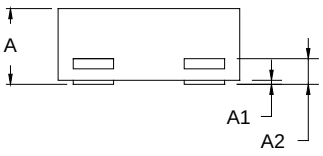
XTDFN-0.9×1.2-4L



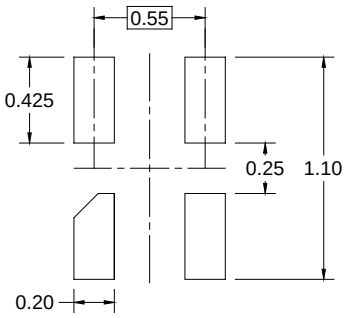
TOP VIEW



BOTTOM VIEW



SIDE VIEW



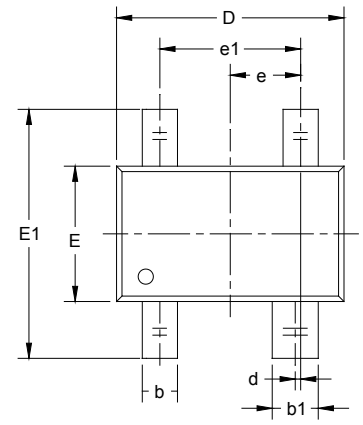
RECOMMENDED LAND PATTERN (Unit: mm)

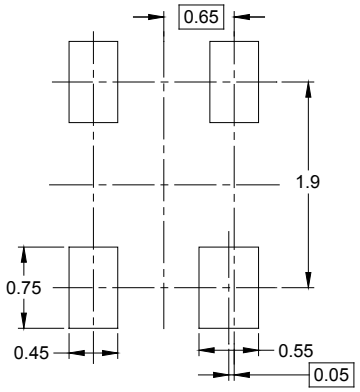
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.350	-	0.400
A1	0.000	-	0.050
A2	0.127 REF		
D	0.850	0.900	0.950
E	1.150	1.200	1.250
b	0.150	0.200	0.250
e	0.550 BSC		
L	0.375	0.425	0.475
L1	0.050 REF		
k	0.250 REF		

NOTE: This drawing is subject to change without notice.

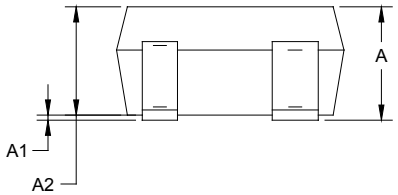
PACKAGE OUTLINE DIMENSIONS

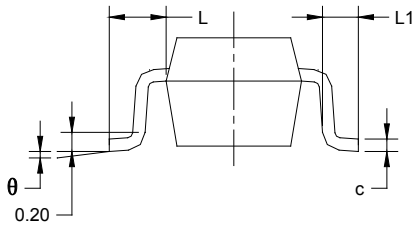
SC70-4 (R)





RECOMMENDED LAND PATTERN (Unit: mm)

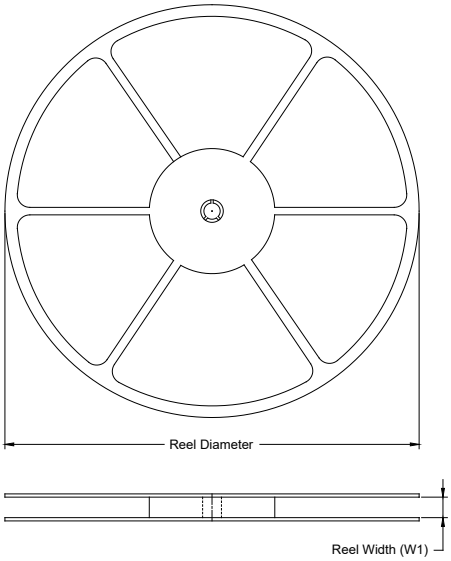




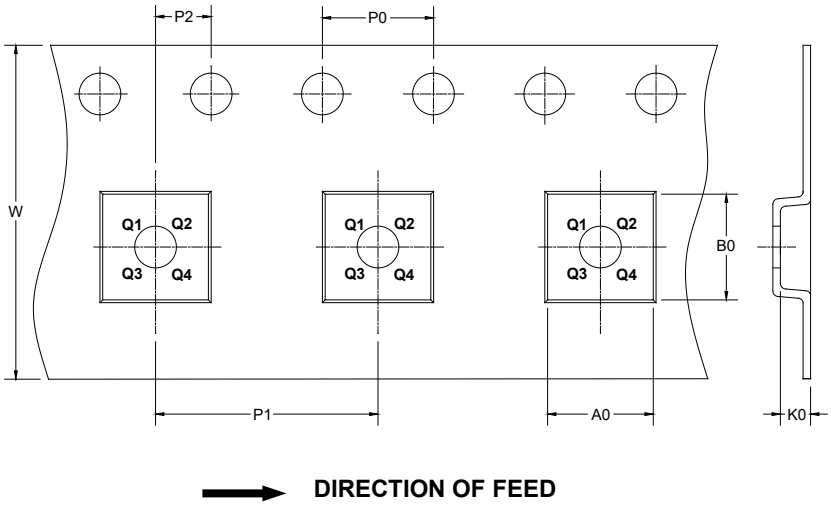
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.250	0.400	0.010	0.016
b1	0.350	0.500	0.014	0.020
c	0.080	0.150	0.003	0.006
d	0.050TYP		0.002TYP	
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.65 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



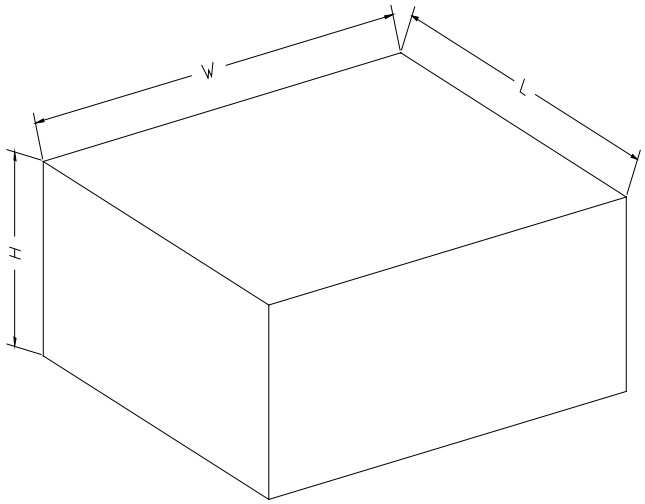
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
XTDFN-0.9×1.2-4L	7″	8.6	1.02	1.52	0.50	4.0	4.0	2.0	8.0	Q2
SC70-4 (R)	7″	9.5	3.20	2.80	1.30	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002