SGM61022C
2.5V to 5.5V, 2A High-Efficiency Buck Converter with AHP-COT Control

GENERAL DESCRIPTION

The SGM61022C is an efficient high-frequency synchronous Buck converter with an input voltage range of 2.5V to 5.5V and a wide output current range that is optimized for compact solutions.

SGM61022C operates in PWM mode at 2.2MHz (TYP) in the medium to heavy load range and automatically enters (reducing the loads) or exits (increasing the loads) the power-save mode (PSM) at light loads to maintain high efficiency.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

The SGM61022C is available in a Green TDFN-2×2-8AL package.

FEATURES

- **Input Voltage Range: 2.5V to 5.5V**
- **Output Current: 2A**
- **34μA (TYP) Quiescent Current**
- **AHP-COT Architecture**
- **Fast Load Transient Response**
- **100% Duty Cycle Capability**
- **High-Efficiency PSM under Light Load**
- **Output Discharge**
- **Short-Circuit Protection**
- **Power Good Output**
- **Thermal Shutdown**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

LPDDR5 Power Supplies
Smart Phone
General Purpose Point-of-Load Power Supplies
Battery-Powered Applications

TYPICAL APPLICATION

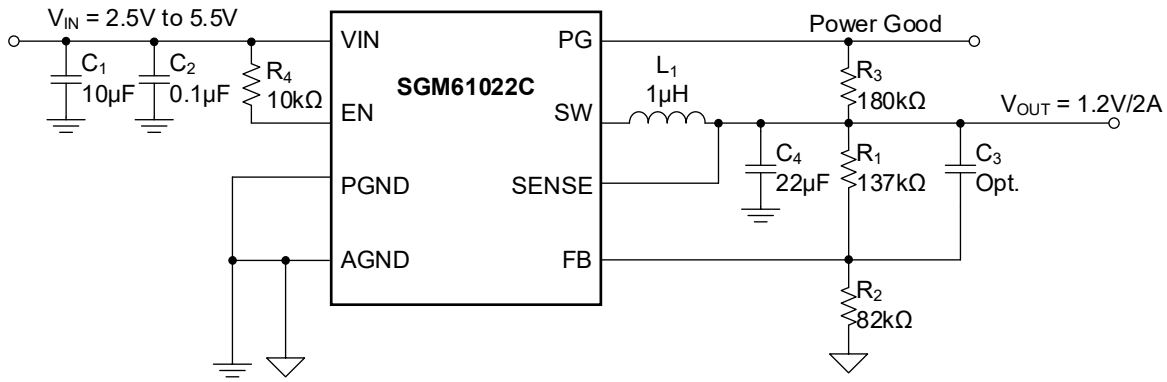


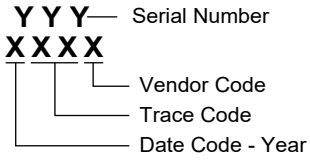
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61022C	TDFN-2×2-8AL	-40℃ to +125℃	SGM61022CXTDE8G/TR	1Q9 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, PG and SENSE Voltages ..... -0.3V to 6V
SW Voltage (DC) ..... -0.3V to V_{IN} + 0.3V
SW Voltage (AC, Less than 10ns) while Switching ..... -2V to 9V
FB Voltage ..... -0.3V to 3.6V
EN Voltage ..... -0.3V to V_{IN} + 0.3V
Sink Current at PG ..... 0mA to 0.5mA
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 59.7℃/W
TDFN-2×2-8AL, θ_{JB} ..... 24.2℃/W
TDFN-2×2-8AL, $\theta_{JC\ (TOP)}$ ..... 74.3℃/W
TDFN-2×2-8AL, $\theta_{JC\ (BOT)}$ ..... 10.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.5V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

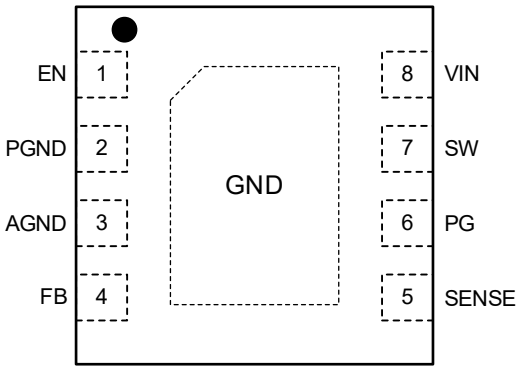
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	I/O (1)	FUNCTION
1	EN	I	Logic high sets the device active, logic low disables it and turns it into shutdown mode. It can connect a 10kΩ resistor to VIN pin if it is needed. Do not leave this pin floating.
2	PGND	G	Power Ground.
3	AGND	G	Analog Ground. Connect this pin to the bottom resistor of FB and the PGND pin through an independent path.
4	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
5	SENSE	I	Output Voltage Sense Pin. Must be connected to output voltage.
6	PG	O	Power Good Open-Drain Output. If the output voltage is less than the regulation limit, this pin is pulled low. Pull this pin up with a resistor to a voltage below 5.5V. Leave this pin floating when not in use.
7	SW	P	Switching Node. Connect it to one terminal of the output inductor.
8	VIN	P	Power Supply Voltage Input.
Exposed Pad	GND	-	Connect it to GND. The thermal pad must be soldered to improve heat dissipation.

NOTE: 1. I = input, O = output, P = power, G = ground.

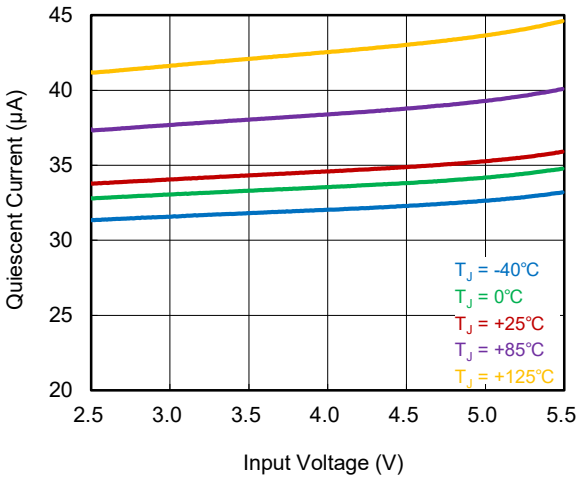
ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

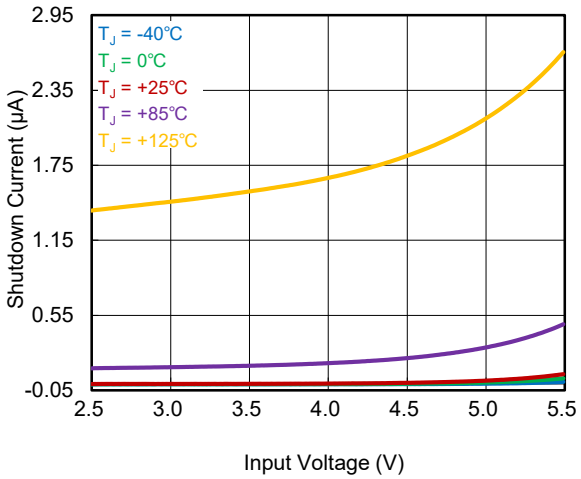
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Input Voltage Range	V_{IN}			2.5		5.5	V
Quiescent Current into VIN	I_Q	V_{IN} = 2.5V to 5.5V, I_{OUT} = 0mA, device no switching			34	60	μA
Shutdown Current into VIN	I_{SD}	V_{IN} = 2.5V to 5.5V, EN = low	T_J = +25℃		0.01	1.2	μA
			T_J = -40℃ to +125℃			5.6	
Under-Voltage Lockout	V_{UVLO}	Input voltage falling		2	2.1	2.2	V
Under-Voltage Lockout Hysteresis		Rising above V_{UVLO}			150		mV
Thermal Shutdown	T_{SD}	Temperature rising			155		℃
Thermal Shutdown Hysteresis	T_{HYS}	Temperature falling below T_{SD}			25		
Logic Interface (EN Mode)							
High Level Input Voltage	V_{IH}	V_{IN} = 2.5V to 5.5V		1.05			V
Low Level Input Voltage	V_{IL}	V_{IN} = 2.5V to 5.5V				0.35	V
Input Leakage Current	I_{LKG}				0.01	0.5	μA
Power Good							
Power Good Threshold	V_{PG}	V_{IN} = 2.5V to 5.5V, V_{FB} falling referenced to V_{FB} nominal		85	90	95	%
Power Good Hysteresis					5		
Low Level Voltage	V_{OL}	I_{SINK} = 500μA			0.065	0.12	V
PG Leakage Current	$I_{PG,LKG}$	V_{PG} = 3.6V			0.01	0.5	μA
Output							
Output Voltage Range	V_{OUT}			0.45		4	V
Feedback Regulation Voltage	V_{FB}	V_{IN} = 2.5V to 5.5V	T_J = +25℃	0.4455	0.45	0.4545	V
			T_J = -40℃ to +125℃	0.441	0.45	0.459	
Feedback Input Bias Current	I_{FB}	V_{FB} = 0.45V			1	50	nA
Output Discharge Resistor	R_{DIS}	EN = low, V_{OUT} = 1.8V			1.2		kΩ
Line Regulation		V_{IN} = 2.5V to 5.5V, V_{OUT} = 1.2V, I_{LOAD} = 1A			0.06		%/V
High-side MOSFET On-Resistance	R_{DSON}	I_{SW} = 500mA			120	175	mΩ
Low-side MOSFET On-Resistance					70	110	
High-side MOSFET Switch Current Limit	I_{LIM}				3.6		A

TYPICAL PERFORMANCE CHARACTERISTICS

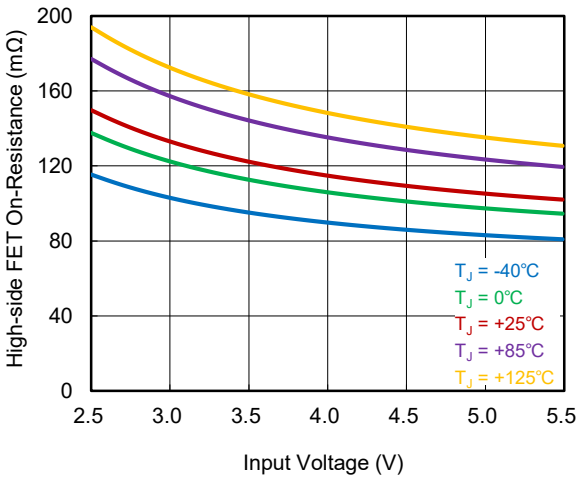
Quiescent Current vs. Input Voltage



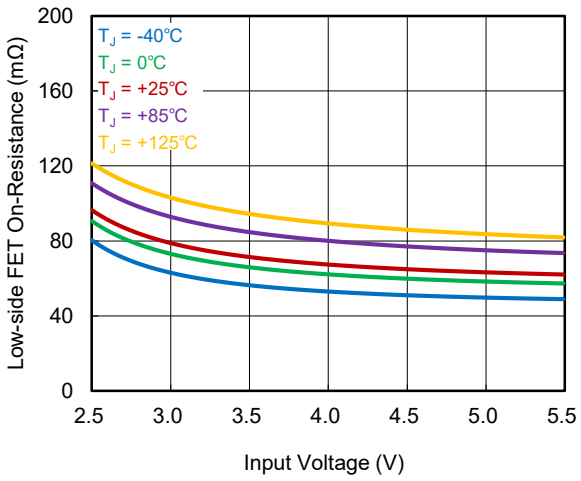
Shutdown Current vs. Input Voltage



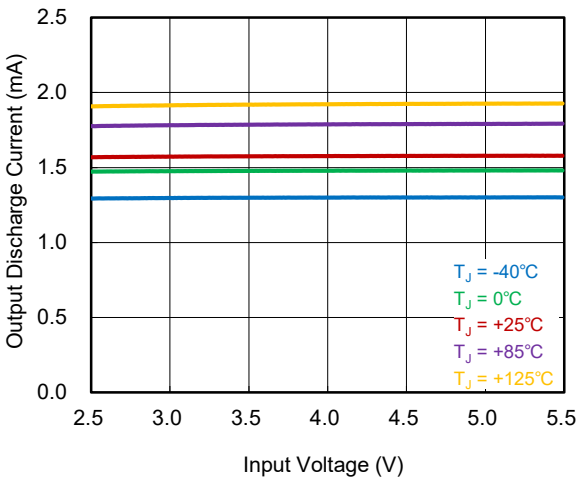
High-side FET On-Resistance vs. Input Voltage



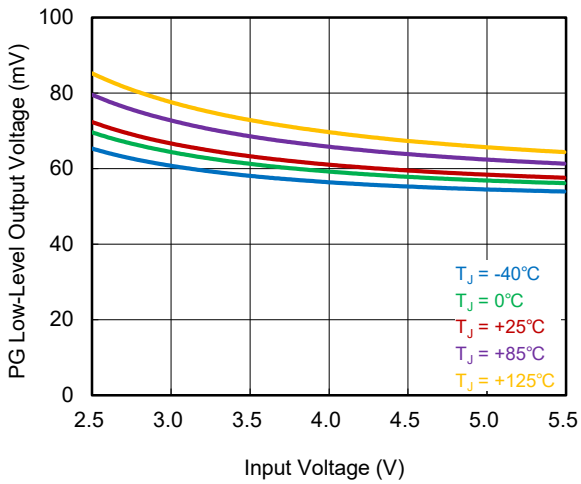
Low-side FET On-Resistance vs. Input Voltage



Output Discharge Current vs. Input Voltage



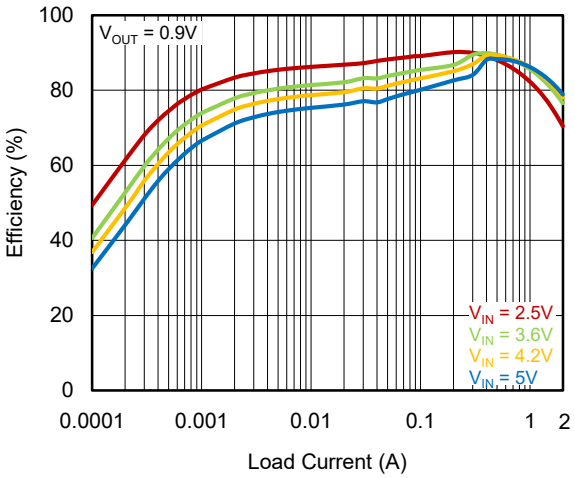
PG Low-Level Output Voltage vs. Input Voltage



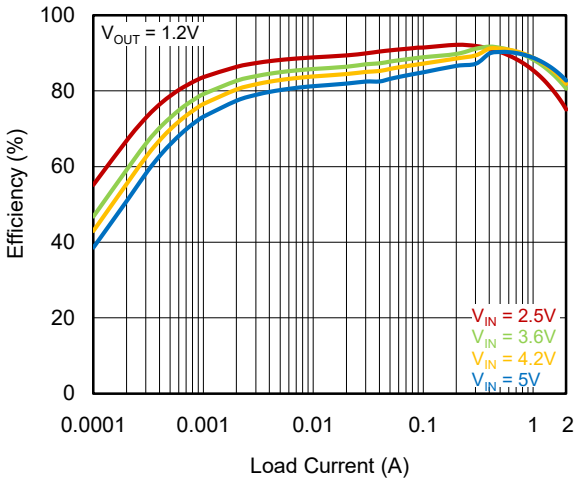
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 5.2mΩ), and C_{OUT} = 22μF, unless otherwise noted.

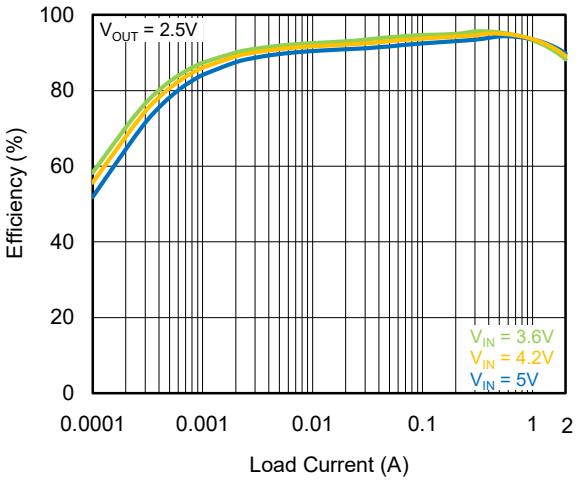
Efficiency vs. Load Current



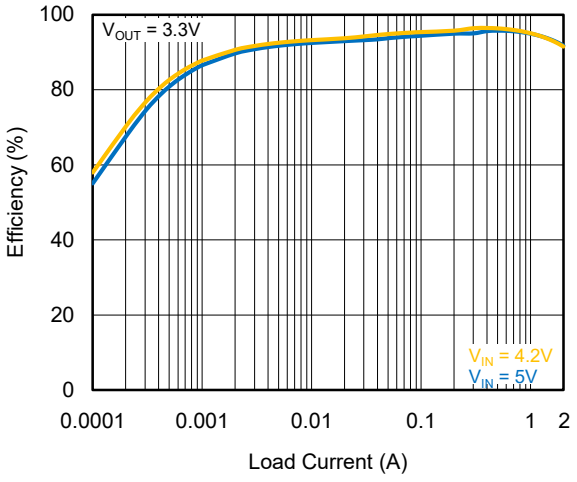
Efficiency vs. Load Current



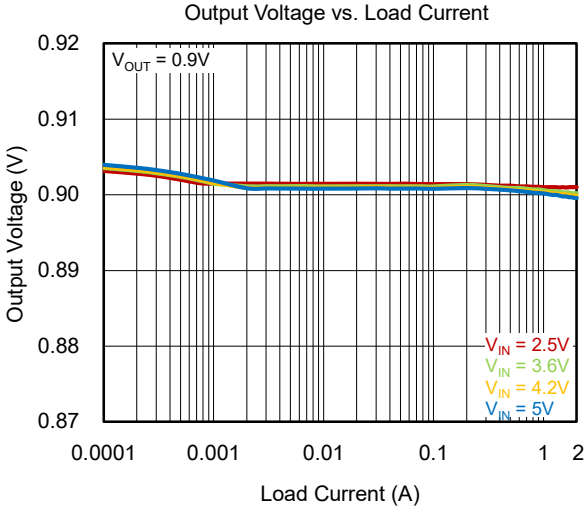
Efficiency vs. Load Current



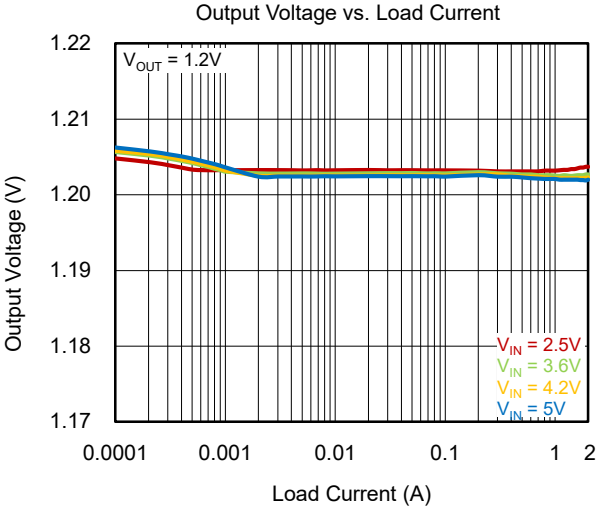
Efficiency vs. Load Current



Output Voltage vs. Load Current



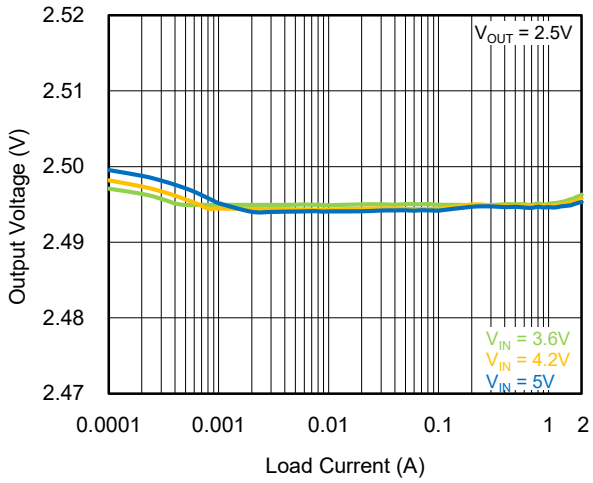
Output Voltage vs. Load Current



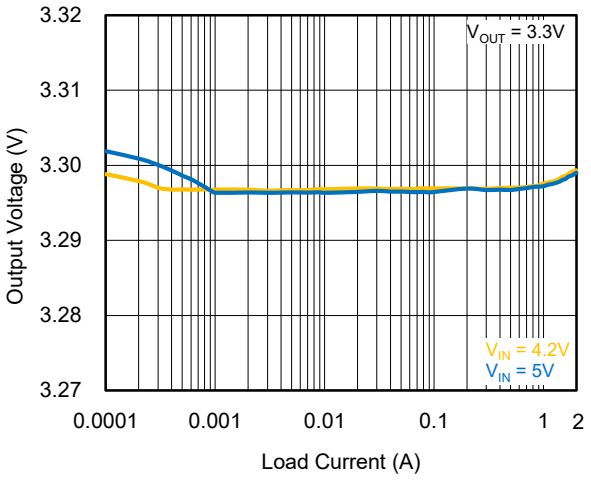
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 5.2mΩ), and C_{OUT} = 22μF, unless otherwise noted.

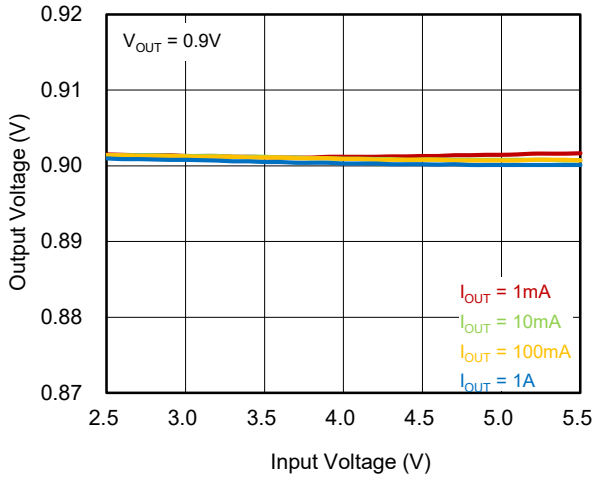
Output Voltage vs. Load Current



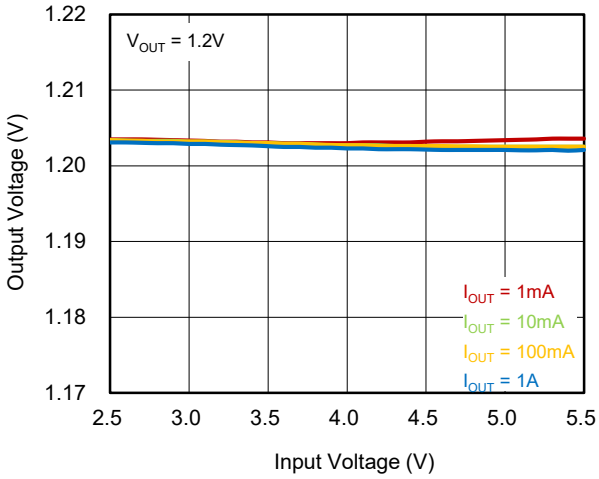
Output Voltage vs. Load Current



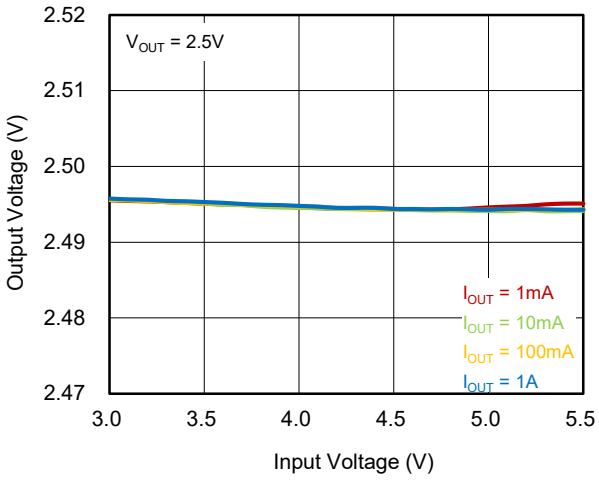
Output Voltage vs. Input Voltage



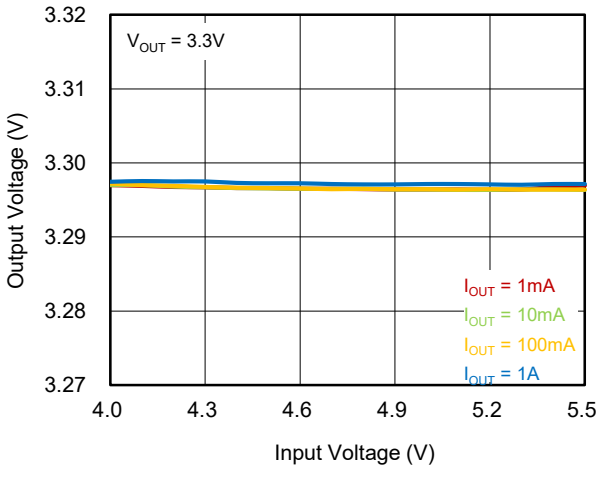
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage



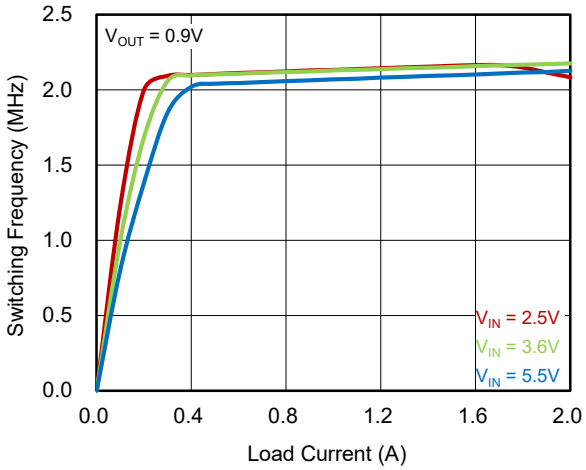
Output Voltage vs. Input Voltage



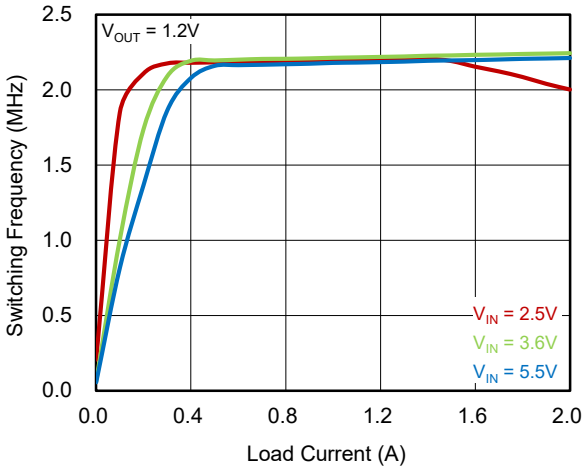
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 5.2mΩ), and C_{OUT} = 22μF, unless otherwise noted.

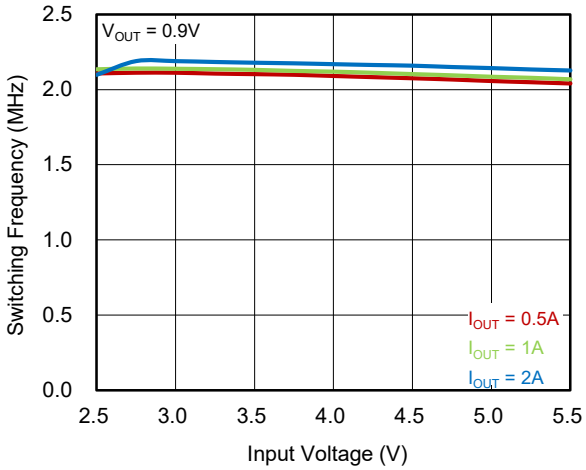
Switching Frequency vs. Load Current



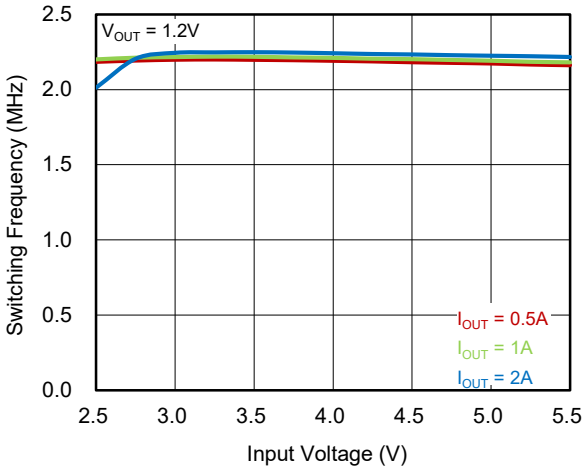
Switching Frequency vs. Load Current



Switching Frequency vs. Input Voltage



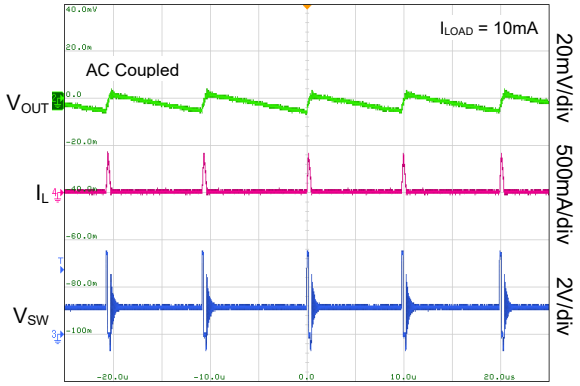
Switching Frequency vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

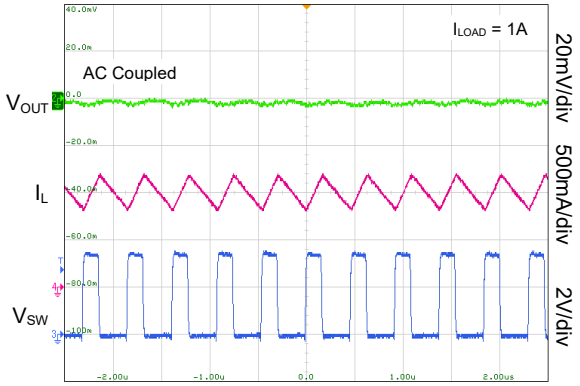
V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 5.2mΩ), and C_{OUT} = 22μF, unless otherwise noted.

Typical Operation In Power Save Mode



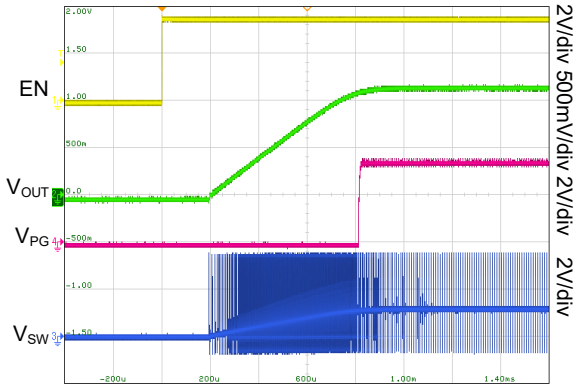
Time (5μs/div)

Typical Operation In PWM



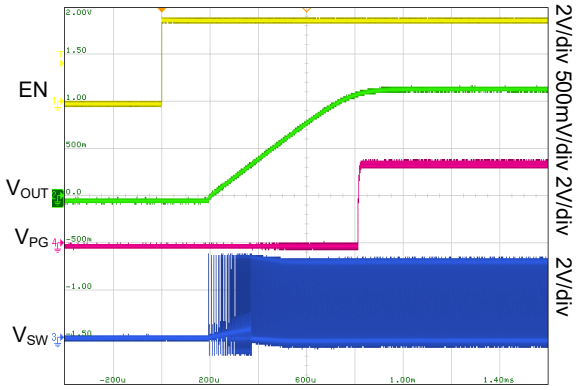
Time (500ns/div)

Startup with 10mA Load Current



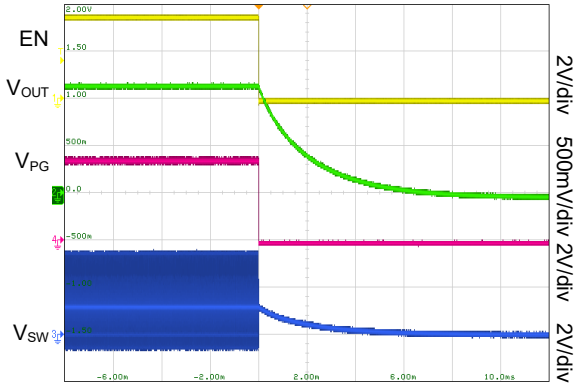
Time (200μs/div)

Startup with 2A Load Current



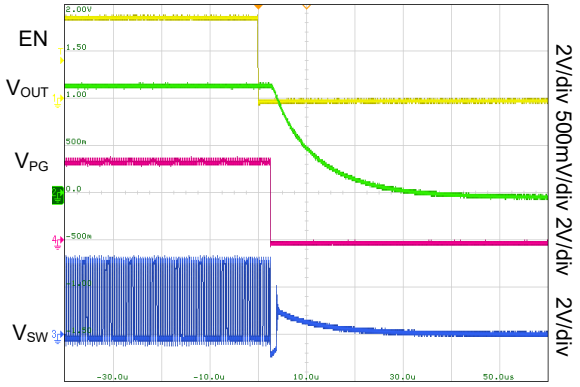
Time (200μs/div)

Shutdown with 10mA Load Current



Time (2ms/div)

Shutdown with 2A Load Current

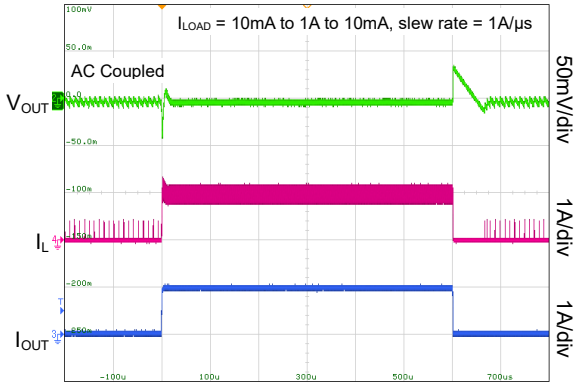


Time (10μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

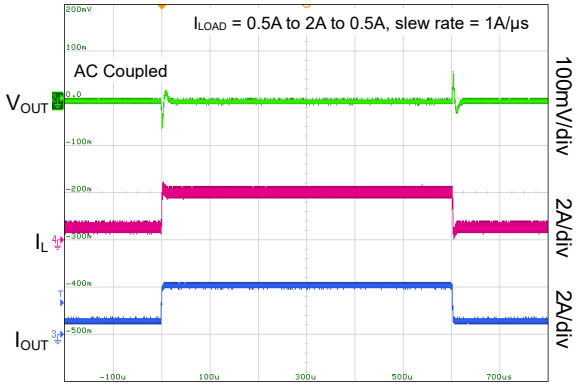
V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH (DCR = 5.2mΩ), and C_{OUT} = 22μF, unless otherwise noted.

Load Transient Response



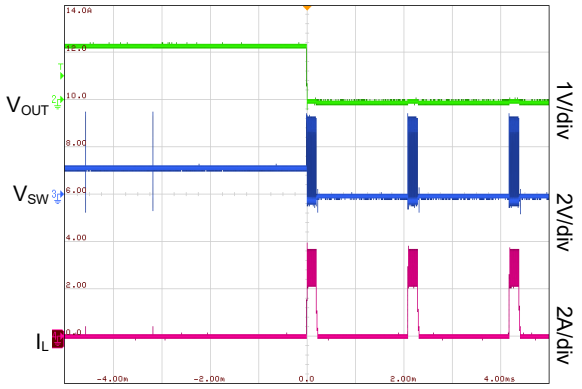
Time (100μs/div)

Load Transient Response



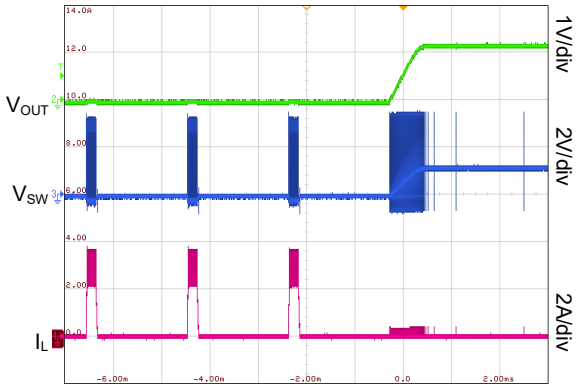
Time (100μs/div)

Current Limit with Output Short



Time (1ms/div)

Recover from Output Short



Time (1ms/div)

FUNCTIONAL BLOCK DIAGRAM

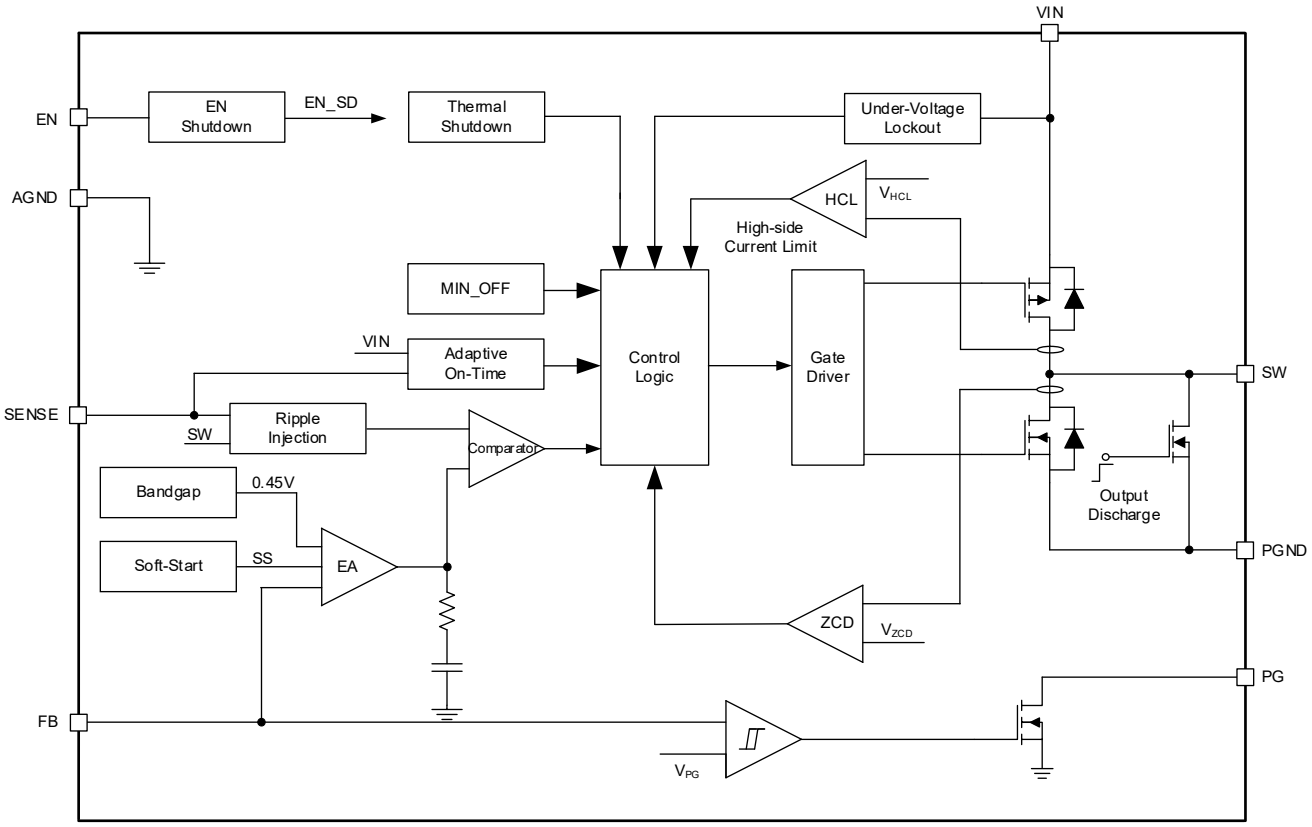


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61022C is a high-efficient Buck converter with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light load, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 2.2MHz (TYP). When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 150mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Enable and Disable

A logic high input to EN activates the device, and a logic low disables the device. A 10kΩ resistor is recommended to add between EN and VIN, and do not leave it floating.

Power Good (PG)

The power good output of SGM61022C will be low in the condition that the output voltage less than its nominal value. If the output exceeds 95% of the regulated voltage, the power good is in high impedance state. If the output voltage is less than 90% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum of 0.5mA sink current. A pull-up resistor connecting to power good output is required. When the device is disabled or under-voltage lockout, the PG pin is driven to low (see Table 1). The PG signal connected to the EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		Logic Status	
		High Z	Low
Enable (EN = High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} \leq V_{PG}$		√
Shutdown (EN = Low)			√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 1.4V$	Uncertain	

Soft-Start

When EN is set to logic high and after about 180μs delay, the device starts switching and V_{OUT} increases with 600μs (TYP) internal soft-start circuit.

Power-Save Mode (PSM)

Once the load current decreases, the SGM61022C will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous. Then a fixed on-time architecture is activated and the typical on-time is t_{ON} = 454ns × (V_{OUT}/V_{IN}).

100% Duty Cycle

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout, the output is discharged by the SW pin through a typical discharge resistor of R_{DIS}.

Inductor Current Limit

If there is an over-current or short-circuit, the device implements an inductor current limit cycle-by-cycle. When the high-side switch current limit is triggered, the high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current. If the high-side current limit event lasts for more than 32 cycles, both high-side and low-side are turned off. A new startup is initiated automatically (hiccup) after 2ms (TYP). The hiccup repeats until the overload or short-circuit fault is released. The actual current limit value maybe larger than the static current limit due to internal propagation delays.

DETAILED DESCRIPTION (continued)

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{SD} (+155℃ TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

In this section, power supply design with the SGM61022C synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

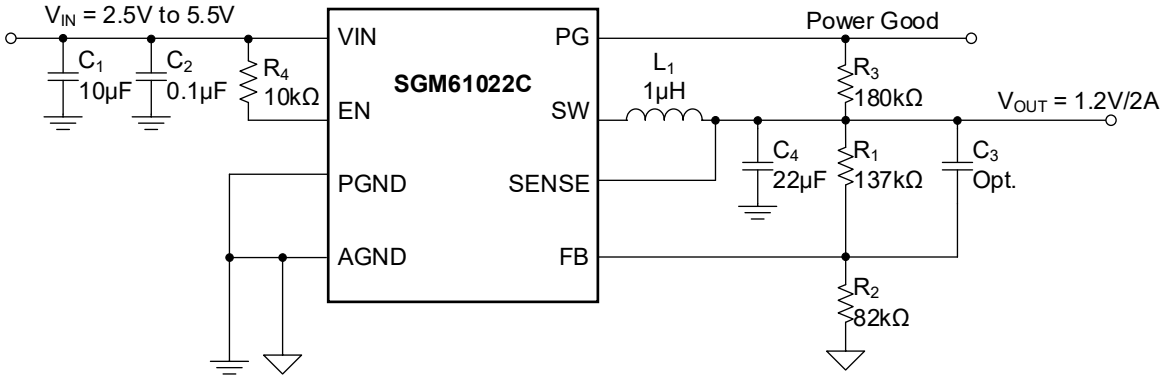


Figure 3. SGM61022C Typical Application Circuit

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.2V
Output Ripple Voltage	< 20mV
Output Current (MAX)	2A

Table 3. Components List

Reference	Description	Manufacturer
C_1	10μF, Ceramic Capacitor, 10V, X7R, Size 0603	Std
C_2	0.1μF, Ceramic Capacitor, 10V, X7R, Size 0603	Std
C_3	Optional	Std
C_4	22μF, Ceramic Capacitor, 6.3V, X5R, Size 0603	Std
L_1	1μH, Power Inductor, DCR(TYP) = 5.2mΩ, WCX0430C1R0MT	Sunlord
R_1	137kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_2	82kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_3	180kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_4	10kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std

Input and Output Capacitor Selection

The high frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X7R and 0603 size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

For output capacitor design, output ripple, transient response and loop stability should be considered. Choosing ceramic capacitor with X5R or better dielectric is very important for temperature characteristics.

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 2 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

where:

- I_{OUT_MAX} is the maximum output DC current.
- ΔI_L is the inductor current ripple (peak-to-peak).
- f_{SW} is switching frequency (MHz).
- L is the inductance value (μH).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 3 to set the desired output voltage. The value of R2 needs to be less than 100kΩ, and do not choose a very small value for R_2 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_2 \times \left(\frac{V_{OUT}}{0.45V} - 1 \right) \quad (3)$$

A feedforward capacitor improves transient response to the load steps and reduces the output ripple in PSM.

LC Filter

The inductor (L) and the output capacitor (C) form a low-pass filter for removing switching AC components and passing the DC voltage to the output. Note that variations are as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the C_{OUT}, due to tolerances and bias voltage derating, the effective capacitance can vary by +20% to -50%.

Thermal Considerations

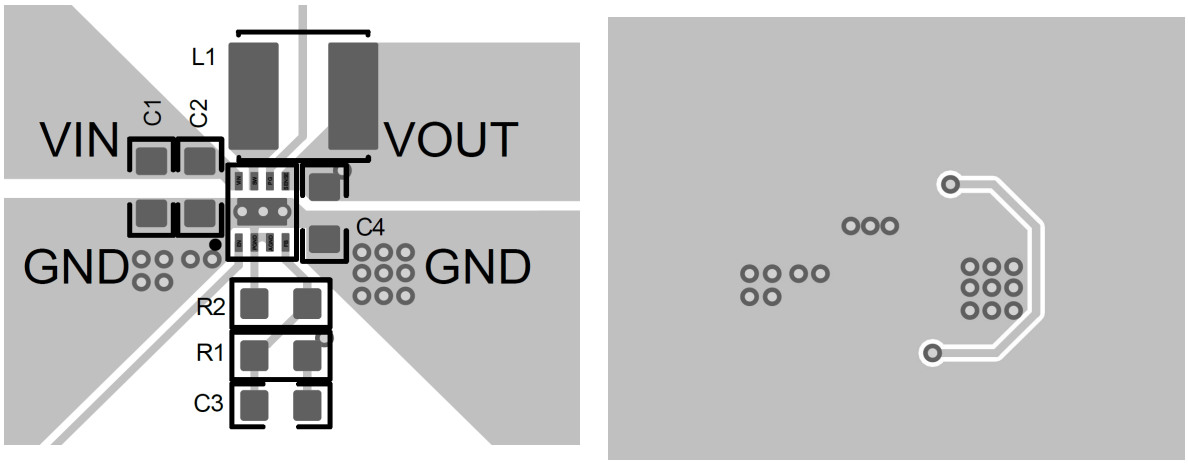
Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGM61022C is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself plays a significant role in helping to transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61022C.

- Place the input/output capacitors and the inductor as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.
- Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.



Top Layer Bottom Layer

Figure 4. PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

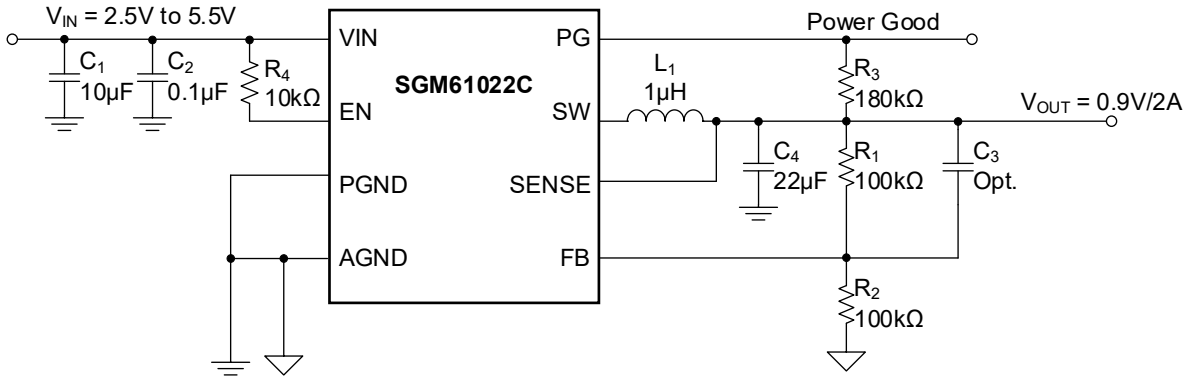


Figure 5. 0.9V Output Voltage Application

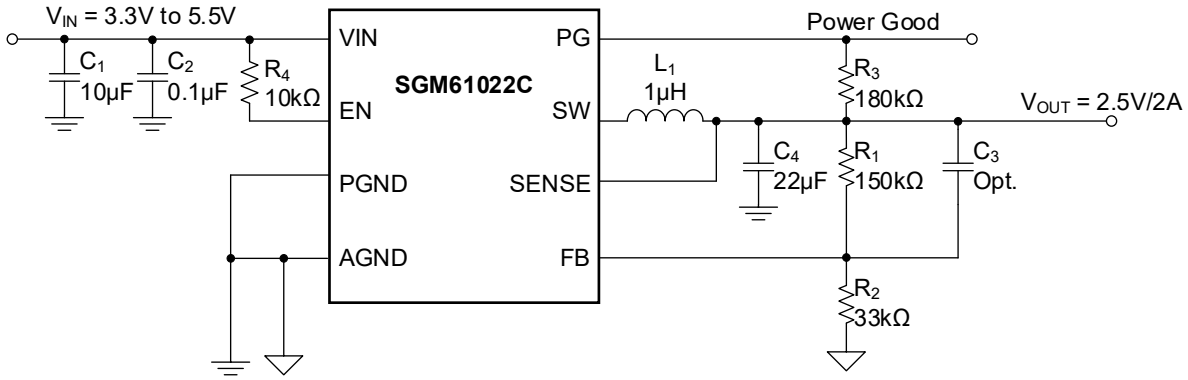


Figure 6. 2.5V Output Voltage Application

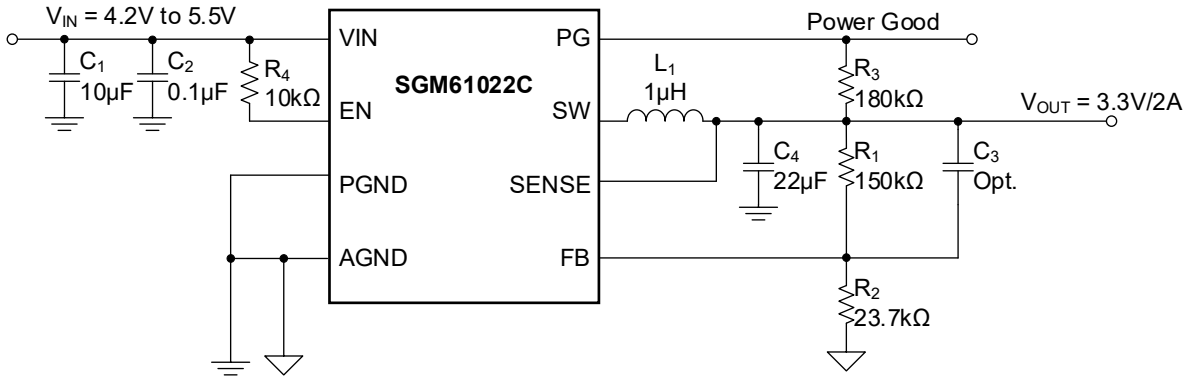


Figure 7. 3.3V Output Voltage Application

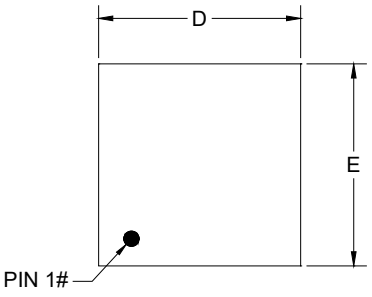
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

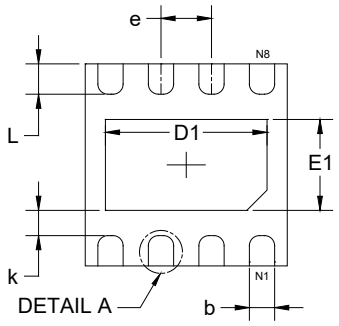
Changes from Original to REV.A (AUGUST 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

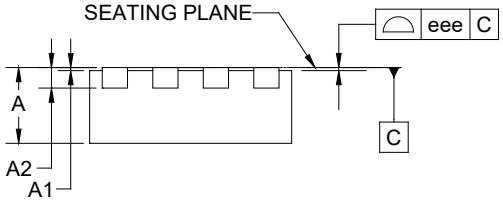
TDFN-2×2-8AL



TOP VIEW

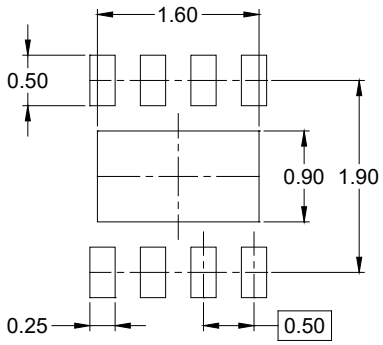


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



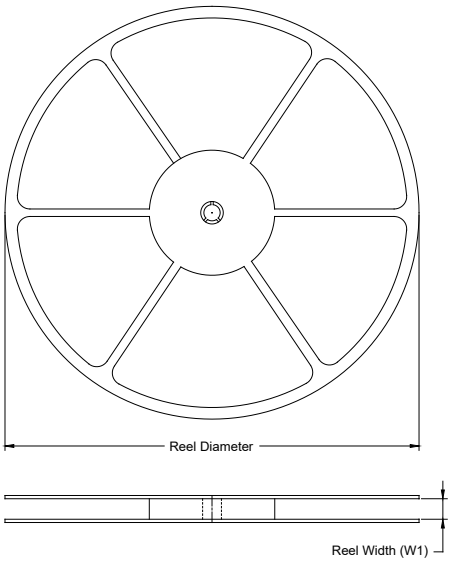
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
D1	1.450	-	1.700
E	1.900	-	2.100
E1	0.750	-	1.000
k	0.200	-	-
e	0.500 BSC		
L	0.200	-	0.400
eee	0.080		

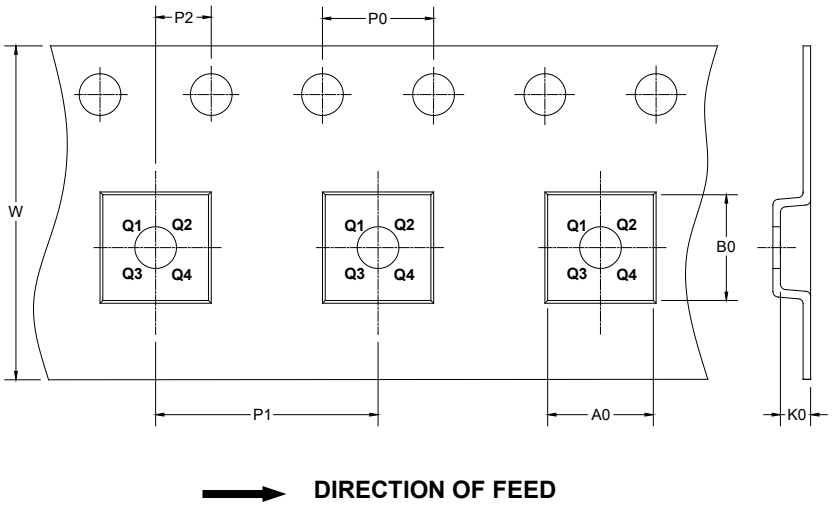
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



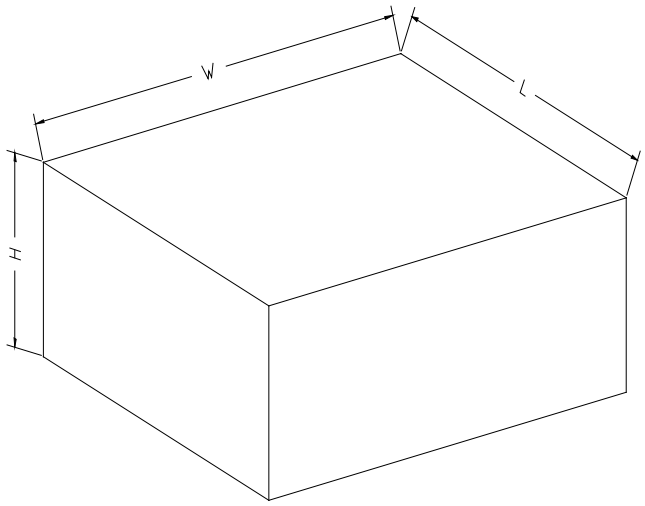
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002