SGM795
Programmable USB Type-C Port Controller

GENERAL DESCRIPTION

The SGM795 is a USB Type-C Port Controller (TCPC) designed in compliance with the latest USB Type-C and PD 3.2 standards. It encapsulates VBUS and VCONN power control, USB Type-C CC logic, the USB PD BMC physical layer, and a portion of the USB PD protocol layer. The SGM795 has programmable Rp and Rd settings for each CC line and performs USB Type-C detection, including attachment and orientation. The SGM795 incorporates a complete BMC encoding system, including a receiver and a transmitter. This enables the SGM795 to send and receive USB PD messages on the configuration channel (CC) connection, support a VBUS voltage level up to 20V, and execute role swaps as needed. BMC PD module fully accommodates alternative interfaces in Type-C specification. For communication with the USB Type-C Port Manager (TCPM), the SGM795 utilizes I^2C and employs an INT signal to request attention.

The SGM795 is available in a Green WLCSP-1.17×1.17-9B package.

FEATURES

- **Dual-Role PD Compatible**
- **Attach/Detach Detection as Host, Device or DRP**
- **Active Cable Recognition**
- **Current Capability Advertisement and Detection**
- **Integrated VBUS Bleed/Force Discharge**
- **VCONN Switch with Programmable OCP**
- **VCONN Over-Temperature Protection**
- **VCONN to CC Dual Side OVP**
- **Dead Battery Support**
- **Ultra-Low Power Mode for Attach Detection**
- **Support TCPCI over I^2C Communication at 1.2V and 1.8V Level**
- **BIST Mode Supported**
- **USB PD PHY Supports PD 3.2 Except Fast Role Swap Function**
- **Available in a Green WLCSP-1.17×1.17-9B Package**

APPLICATIONS

Smart Phones
Tablets and Laptops

TYPICAL APPLICATION

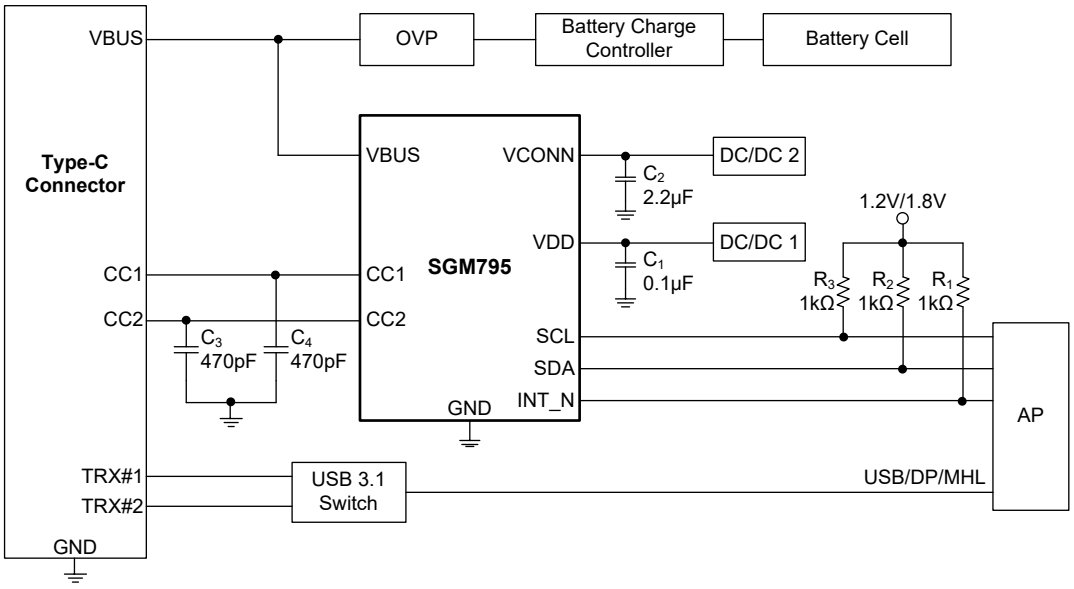


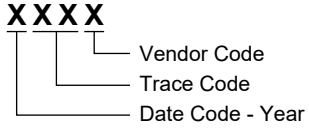
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM795	WLCSP-1.17×1.17-9B	-40℃ to +85℃	SGM795YG/TR	795 XXXX	Tape and Teel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD/VCONN Voltage ..... -0.3V to 6V
CC1/CC2 Voltage ..... -0.3V to 24V
VBUS Voltage ..... -0.3V to 28V
SDA, SCL, INT_N Voltage ..... -0.3V to 6V
Package Thermal Resistance
WLCSP-1.17×1.17-9B, θ_{JA} ..... 146.4℃/W
WLCSP-1.17×1.17-9B, θ_{JB} ..... 32.2℃/W
WLCSP-1.17×1.17-9B, θ_{JC} ..... 65.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±3000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

VDD Input Voltage ..... 3.0V to 5.5V
VCONN Input Voltage ..... 3.3V to 5.5V
VCONN Supply Current ..... 200mA to 600mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

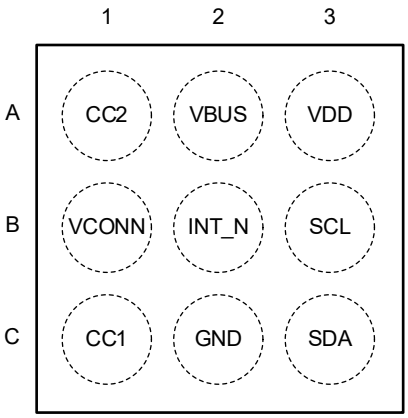
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-1.17×1.17-9B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	CC2	AI/AO	Configuration Channel Pins. It is used to detect when an attachment is connected and its orientation. Connect to CC1/CC2 of Type-C connector. For stable communication, place a minimum of 470pF ceramic capacitor between the CC2 and GND pins, as close to the device as possible.
A2	VBUS	AI	VBUS Input Pin. It is used to attach and detach detection. Connect to VBUS pin of Type-C Connector.
A3	VDD	P	Input Supply Voltage Pin. Use a 0.1μF or larger ceramic capacitor between VDD and GND pins close to the device.
B1	VCONN	P	VCONN Power Input Pin. It can be switched to the selected CC pin. Short VCONN to GND if not used. Use a 2.2μF or larger ceramic capacitor between VCONN and GND pins close to the device.
B2	INT_N	DO	Open-Drain Interrupt Output Pin. Low signal asserted to notify TCPM of alert register updates. Use a 1kΩ pull-up to the logic high rail.
B3	SCL	DI/DO	I^2C Clock Signal Pin. Connect it to the I^2C master. The device I^2C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
C1	CC1	AI/AO	Configuration Channel Pins. It is used to detect when an attachment is connected and its orientation. Connect to CC1/CC2 of Type-C connector. For stable communication, place a minimum of 470pF ceramic capacitor between the CC1 and GND pins, as close to the device as possible.
C2	GND	P	Ground.
C3	SDA	DI/DO	I^2C Data Signal Pin. Connect it to the I^2C master. The SDA line is forced to release when the 25ms I^2C timeout fault occurs.

NOTE: AI = analog input, AI/AO = analog input/output, DO = digital output, DI/DO = digital input/output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V to 5.5V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDD Supply						
VDD Voltage Range	V_{DD}		3		5.5	V
VCONN Voltage Range	V_{CONN}		3.3		5.5	V
UVLO Rising Voltage	V_{UVLO_H}		2.3	2.44	2.6	V
UVLO Falling Voltage	V_{UVLO_L}		2.0	2.20	2.3	V
UVLO Hysteresis	V_{UVLO_HYS}			240		mV
Common Normative Signaling Requirements						
Bit Rate	f_{BR}		270	300	330	Kbps
Common Normative Signaling Requirements for Transmitter						
Maximum Difference between the Bit-Rate during the Part of the Packet Following the Preamble and the Reference Bit-Rate	p_{BR}				0.25	%
Time from the End of Last Bit of a Frame until the Start of the First Bit of the Next Preamble	t_{IFG}		25			μs
Time before the Start of the First Bit of the Preamble when the Transmitter Shall Start Driving the Line	t_{SD}		-1		1	μs
BMC Common Normative Requirements						
Time to Cease Driving the Line after the End of the Last Bit of the Frame	t_{ED_BMC}				23	μs
Fall Time	t_F		300			ns
Time to Cease Driving the Line after the Final High-to-Low Transition	t_{HL_BMC}		1			μs
Rise Time	t_R		300			ns
Voltage Swing	V_{SWING}		1.05	1.125	1.2	V
Transmitter Output Impedance	z_{DRIVER}		33		75	Ω
BMC Receiver Normative Requirements						
Time Window for Detecting Non-Idle	t_{TW}		12		20	μs
Receiver Input Impedance	z_{BMC_RX}		1			MΩ
Power Consumption						
Stand-by Mode	I_{SB_SINK}	Sink current consumption in cable attached, V_{DD} = V_{DD_I2C} = 3.8V (TYP)	80	105	130	μA
Low Power Mode	I_{LP_DRP}	CC toggle at DRP mode when port is unconnected and waiting for connection, V_{DD} = V_{DD_I2C} = 3.8V (TYP)	12	18	25	μA
Stand-by BMC-TX Current	I_{SB_BMC}	Stand-by sink attached current when transmitting BIST carrier mode 2, V_{DD} = V_{DD_I2C} = 3.8V (TYP)	0.9	1.2	1.4	mA
Shutdown Mode	I_{SD}	The CC pin exposes RD and disables all functions except I^2C functions, V_{DD} = V_{DD_I2C} = 3.8V (TYP)	2	3	5	μA
Shutdown Mode When V_{DD} unequal V_{DDI2C}	I_{SD_I2C}	The CC pin exposes RD and disables all functions except I^2C functions, V_{DD} = 3.8V (TYP), V_{DD_I2C} = 1.2V to 5.5V			20	μA
VCONN Power	I_{VCONN}	VCONN current consumption when VCONN without supply to CC, V_{CONN} = 3V to 5.5V, V_{DD} = 5V (TYP)	0	1	2	μA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 5.5V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Port Control						
R_{ON} for VCONN Switch	R_{ON}	V_{CONN} = 3V to 5.5V		0.7	1	Ω
VCONN OCP Setting Range	I_{OCP}	V_{CONN} = 3.3V to 5.5V	200		600	mA
VCONN OCP Range	I_{OCP_RANGE}	V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 200mA	126	200	269	mA
		V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 300mA	228	300	365	
		V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 400mA	339	400	454	
		V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 500mA	437	500	557	
		V_{DD} = 3.3V, V_{CONN} = 5V, OCP setting = 600mA	548	600	651	
Time for VCONN Switch to Turn-On State	t_{SOFT_VCCON}	V_{DD} = 3.3V, V_{CONN} = 3.3V		320		μs
		V_{DD} = 3.3V, V_{CONN} = 5V		350		
SRC 80μA CC Current	$ICC_{80μ}$		64	80	96	μA
SRC 180μA CC Current	$ICC_{180μ}$		166	180	194	μA
SRC 330μA CC Current	$ICC_{330μ}$		304	330	356	μA
SNK Rd	Rd		4.59	5.10	5.61	kΩ
Ra	Ra			1.1		kΩ
UFP Pull-Down Voltage in Dead Battery under SRC 80μA	V_{DEAD_DEFF}	V_{DD} = 0V dead battery	0.25		1.5	V
UFP Pull-Down Voltage in Dead Battery under SRC 180μA	$V_{DEAD\_1.5A}$	V_{DD} = 0V dead battery	0.45		1.5	V
UFP Pull-Down Voltage in Dead Battery under SRC 330μA	V_{DEAD_3A}	V_{DD} = 0V dead battery	0.85		2.45	V
VBUS						
VBUS Voltage Detection Level	V_{BUSIN}				20	V
Source Bulk Capacitance when a Port is Powered from a Dedicated Supply	C_{SRC_BULK}		10		150	μF
Bulk Capacitance on VBUS a Sink is Allowed after a Successful Negotiation	$C_{SNK\_BULK\_PD}$		1		100	μF
VBUS Bleed Discharge	I_{VBUS_BLEED}	V_{BUS} = 5V	610	660	725	μA
VBUS Force Discharge	I_{VBUS_FORCE}	V_{BUS} = 5V, V_{DD} = 3.8V	84	100	115	mA
VBUS Present Rising Threshold				4		V
VBUS Present Falling Threshold				3.5		V
VBUS vsafe0V Threshold					0.8	V
VBUS vsafe5V Low Threshold					4.75	V
VBUS vsafe5V High Threshold			5.5			V
OTSD						
VCONN Thermal Protection Shutdown	T_{VCONN_OTSDH}			145		°C
VCONN Thermal Protection Release	T_{VCONN_OTSDL}			135		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V to 5.5V, T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
I²C Electrical Characteristics						
I²C Bus Supply Voltage	V_{DD_I2C}		1.2		2.0	V
Low-Level Input Voltage	V_{IL}				0.4	V
High-Level Input Voltage	V_{IH}		0.86			V
Low-Level Output Voltage	V_{OL}	Open-drain, I_{OL} = 20mA			0.4	V
Input Current Each I/O Pin	I_{IN}	V_{DD} = 3V to 5.5V, 0.1 × V_{DD} < V_{IN} < 0.9 × V_{DD_MAX}	-1		1	μA
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Pulse Width of Spikes that Must Be Suppressed by the Input Filter	t_{SP}				50	ns
Data Hold Time	t_{HDDAT}		0			ns
Data Set-Up Time	t_{SUDAT}		50			ns

Timing Diagram

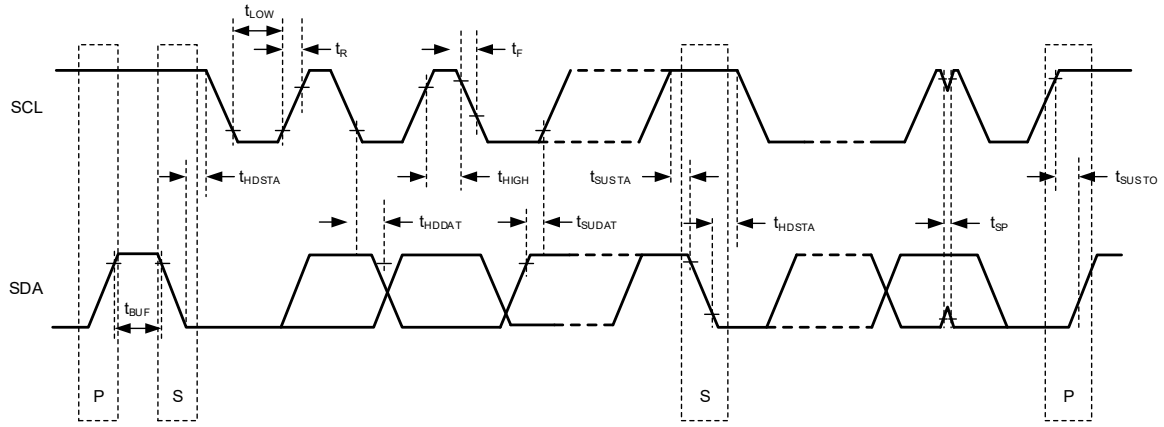


Figure 2. I²C Waveform Information

FUNCTIONAL BLOCK DIAGRAM

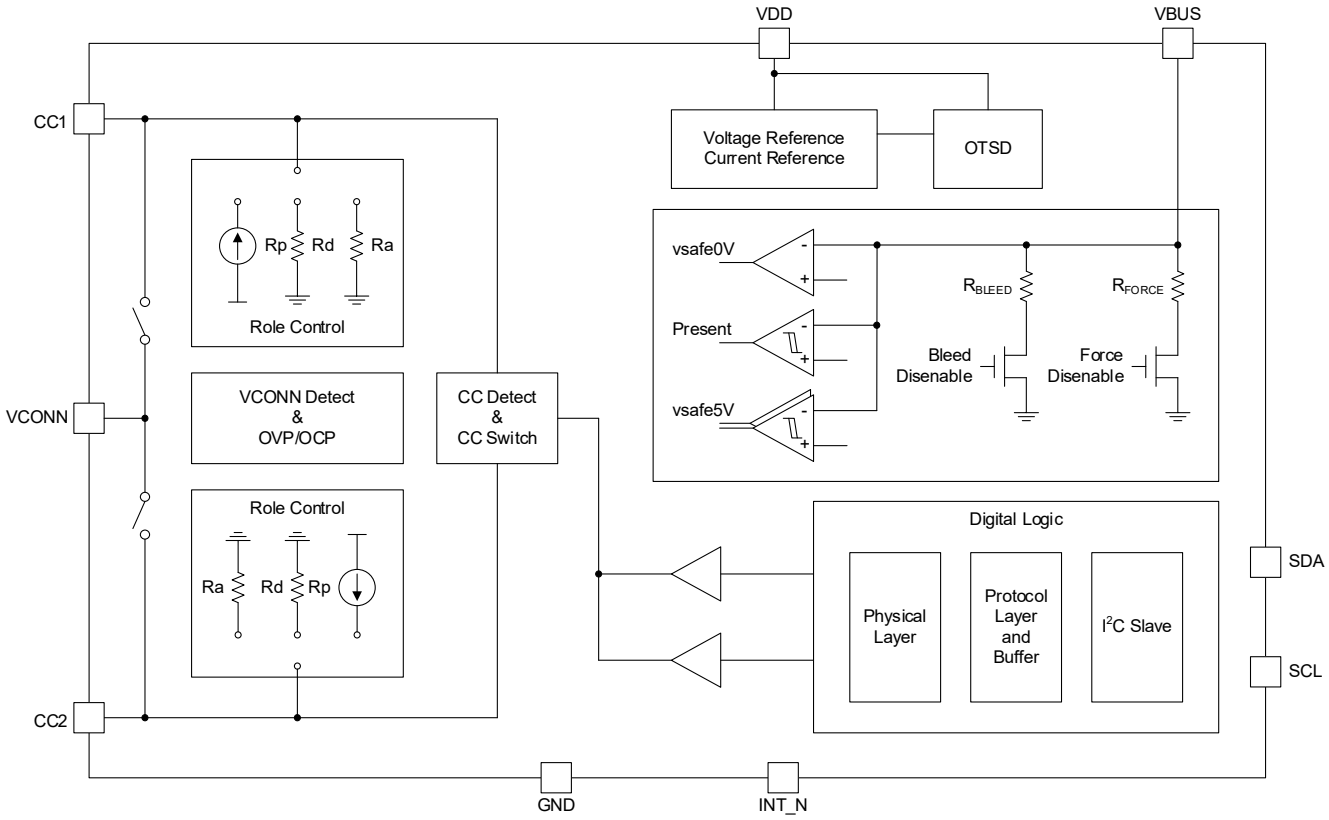


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM795 acts as a USB Type-C Port Controller (TCPC), operating at the PD PHY level to oversee USB Type-C connectivity and Power Delivery (PD). It fulfills three primary functions pivotal to USB Type-C port functionality: power control of VBUS and VCONN, CC logic and detection, and USB PD message delivery.

Featuring a USB Type-C Port Controller Interface (TCPCI), the SGM795 seamlessly interfaces with the USB Type-C Port Manager (TCPM) within an Application Processor (AP) via the I^2C interface. Utilizing the INT_N signal, the SGM795 requests attention when necessary.

Integrated with CC logic and programmable Rp and Rd settings for each CC line, the SGM795 facilitates USB port attachment and detachment detection, role identification, cable orientation determination, and Type-C current detection/advertisement.

Equipped with a USB PD BMC physical layer and a portion of the protocol layer, the SGM795 manages the transmission and reception of USB PD messages, enabling diverse functionalities such as power negotiations and data role negotiations over the Type-C port. Operationally, the SGM795 receives messages from the TCPM, performs a 32-bit CRC calculation, encodes the message, and transmits it over the CC wire. Conversely, it detects SOP* and validates packet integrity upon receiving data from the CC wire, automatically responds with a GoodCRC indication, and notifies the TCPM of received data by activating the interrupt signal (INT_N).

Furthermore, the SGM795 implements VBUS detection and internal VBUS discharge to comply with USB Type-C port standards. It integrates a VCONN power switch for active cable management, detecting VCONN over-voltage, over-current and over-temperature conditions. Additionally, it provides mechanisms for handling Built-In Self Test (BIST) mode in accordance with defined standards.

Configuration Channel (CC) Detection

In the USB Type-C solution, the CC1 and CC2 pins on the connector play a crucial role in establishing and managing the source-to-sink connection. These pins are utilized for a variety of functions including attachment and detachment detection, role identification, cable orientation determination, Type-C current detection/advertisement, and discovery of alternate and accessory modes.

The SGM795 incorporates multiple comparators designed to ascertain the voltage values present on the CC1 and CC2 pins corresponding to different source (SRC) or sink (SNK) roles. Upon detecting a change on the CC1 or CC2 wires, the SGM795 promptly updates the CC_STATUS register, signaling the connection result and the current CC state. To ensure accurate reporting of CC line states, the SGM795 employs debounce filtering for a duration of t_{TCPC} filter. Subsequently, the assertion of the interrupt signal INT_N indicates a state change to the TCPM.

This status information furnishes the TCPM with all necessary data to determine the attachment and detachment status of the cable, empowering seamless management of the USB Type-C connection.

DRP Toggle

The SGM795 offers the flexibility to perform autonomous or manual DRP toggles, catering to diverse operational requirements. In autonomous DRP toggles, the SGM795 seamlessly executes DRP toggling between SRC and SNK roles. This autonomous toggling involves dynamic switching between Rd and Rp configurations, with programmable DRP period and duty cycle settings.

To enable autonomous DRP toggling, the ROLE_CONTROL register must be programmed with either 0x4A or 0x45, indicating DRP autonomous toggling mode, and the starting value of DRP. Notably, the SGM795 initiates DRP toggling only upon receiving the Look4Connection command from the TCPM via the COMMAND register.

On the other hand, manual DRP control grants complete authority to the TCPM, enabling direct manipulation of the Rp/Rd configurations as per specific requirements. To exercise manual control, the TCPM toggles between writing 0x0A and 0x05 to the ROLE_CONTROL register, signaling changes in the CC1/CC2 values. This control mechanism is utilized when the SGM795 is operating solely as SRC or SNK, or when a connection has been detected via DRP toggling, but the TCPM intends to initiate Try.SRC or Try.SNK operations.

DETAILED DESCRIPTION (continued)

USB PD BMC PHY

The SGM795 sends and receives messages constructed in the TCPM and places them on the CC connections. It should be noted that the SGM795 incorporates the entire USB PD Physical Layer, utilizing BMC encoding, and also a portion of the protocol layer. Specifically, the USB PD Physical Layer comprises a pair of transmitters and receivers that communicate via a single signal wire (CC), operating exclusively in a half-duplex mode. This configuration ensures efficient and reliable data transmission across the channel. The SGM795 implements the following portions of the USB PD protocol layer:

- CRC Receive Timer.
- Retry Counter.
- Message ID is not checked in the SGM795 when a non-GoodCRC message is received. Retried messages that are received are passed to the TCPM via I^2C.
- A message transmission is considered successful after receiving a GoodCRC response with the matching Message ID and SOP type.
- Way of discard message when asynchronous message is received.
- BIST handing as follows: Each incoming BIST message is responded to with GoodCRC without passing to the policy engine. The SGM795 provides the mechanism to send BIST continuous carrier mode 2 message for $t_{BistContMode}$.

VBUS Detection

The SGM795 boasts the capability to monitor the VBUS voltage level for various states including VBUS present, vsafe5V, or vsafe0V. When VBUS rises above 4V, the SGM795 promptly reports VBUS present, whereas indicating VBUS absent when the voltage falls below 3.5V. Furthermore, when VBUS drops below 0.8V, the SGM795 reports that VBUS is at vsafe0V.

For precise vsafe5V detection, the SGM795 incorporates 4.75V and 5.5V detection thresholds in a vendor-defined register. This enables the TCPM to read the register and determine whether the VBUS voltage falls within the vsafe5V range as specified in the PD specification. In accordance with this detection, the SGM795 generates an interrupt when the VBUS voltage deviates from the vsafe5V threshold, whether lower or higher.

It's important to note that the VBUS detection circuit is enabled by default but can be disabled by the TCPM as needed, allowing for flexible management of VBUS monitoring functionalities.

VBUS Discharge

The SGM795 incorporates an internal force discharge circuit and a bleed discharge circuit, both controllable by the TCPM, to facilitate VBUS discharge, eliminating the need for external VBUS discharge if the PD standard requirements are met. The force discharge feature employs a higher current discharge to swiftly bring VBUS below vsafe0V upon detecting a disconnection event as signaled by the TCPM. If the TCPM requires confirmation of VBUS discharge completion, it can access the EXTENDED_STATUS register for this information.

In addition to force discharge, the SGM795 also integrates a bleed discharge mechanism, which utilizes a lower current discharge to efficiently deplete the bulk capacitance present on VBUS. This combination of force and bleed discharge circuits offers comprehensive VBUS discharge functionality, ensuring compliance with PD standard requirements while optimizing system performance.

VCONN Switch and Protections

VCONN is an essential requirement for active cables and e-markers in the USB Type-C ecosystem. To fulfill this requirement, the SGM795 integrates a 3W VCONN switch, which is under the control of the TCPM. This switch applies voltage to the VCONN pin connected to the selected CC pin, as indicated by the value of the PLUG_ORIENT bit in the TCPC_CONTROL register. By default, the switch is disabled and can be activated by setting the ENABLE_VCONN bit in the POWER_CONTROL register. Subsequently, the TCPM can verify the application of VCONN voltage on the CC line by querying the VCONN_PRESENT status.

DETAILED DESCRIPTION (continued)

Before enabling the VCONN switch, it is imperative that the TCPM verifies the voltage on the VCONN pin to ensure that it is within a valid range. Premature removal of voltage from the VCONN pin before disabling the VCONN switch can trigger a VCONN fault condition, resulting in the clearing of the ENABLE_VCONN bit.

To maintain safety standards, the SGM795 incorporates VCONN over-voltage protection and programmable over-current protection mechanisms to prevent false operation conditions. Furthermore, the SGM795 detects over-temperature conditions to prevent damage. In the event of any fault, the protection mechanisms promptly respond by setting the FAULT_STATUS bit and disabling the VCONN switch.

Interrupts

The INT_N pin of the SGM795 is utilized to communicate events to software running on the TCPM.

After an event occurs, the SGM795 sets the corresponding bit in the ALERT registers and activates the INT_N pin low to notify the TCPM that an unmasked status change has occurred. These bits remain asserted until the TCPM writes a logical 1 to clear them.

In the event that the FAULT flag is triggered in the ALERT register, the TCPM is required to initially access the FAULT_STATUS register to determine the reason for the fault. Following this determination, the TCPM clears the FAULT bit by writing a logical 1 to the respective FAULT bit position. Subsequently, the TCPM writes a logical 1 to the FAULT bit of ALERT register after clearing all bits in the FAULT_STATUS register.

Dead Battery Mode

The SGM795 provides support for dead battery mode, activated when conditions such as low battery power or the absence of VDD occurs, resulting in the inability to sustain communication over USB Type-C. In dead battery mode, the SGM795 applies Rd to both CC1 and CC2 pins and adheres to all sink rules.

When the SGM795 is connected to a source, it operates as a sink, facilitating the provision of vbus power from the source. This enables the recharging of the battery to restore it to an operational level, ensuring continuous functionality and operational continuity even in challenging power conditions.

Type-C Port Controller (TCPC) Interface uses I^2C Protocol

The TCPC Interface (TCPCI) is the interface between a Type-C port manager and a Type-C port controller. SGM795 communicates with TCPM via I^2C bus.

Read and Write Function

The I^2C interface bus provides TCPM access to both read and write operations on the SGM795 and necessitates an external pull-up resistor. Below are the I^2C timing diagrams.

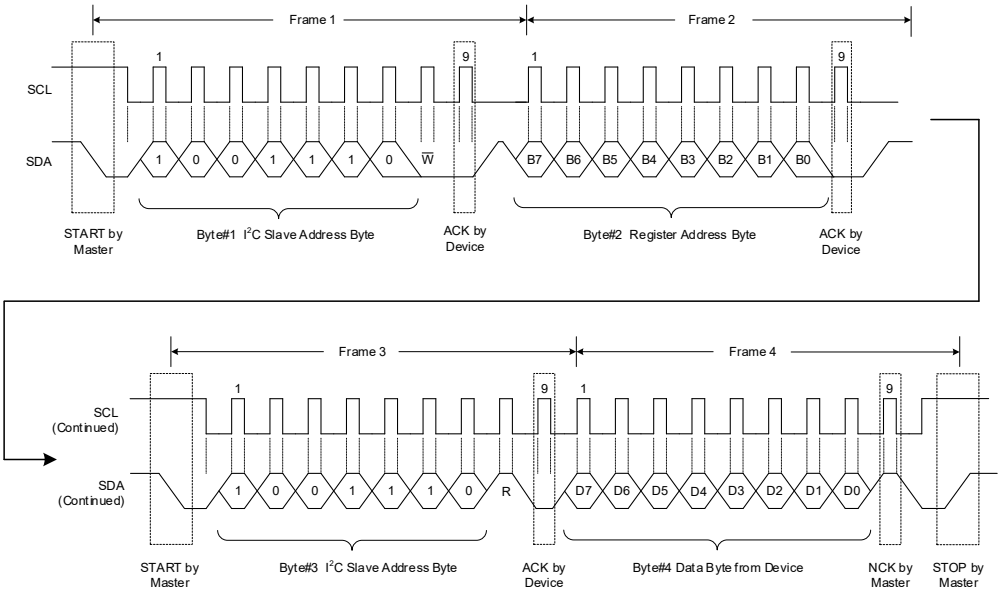


Figure 4. Read Single Byte of Data from Register

DETAILED DESCRIPTION (continued)

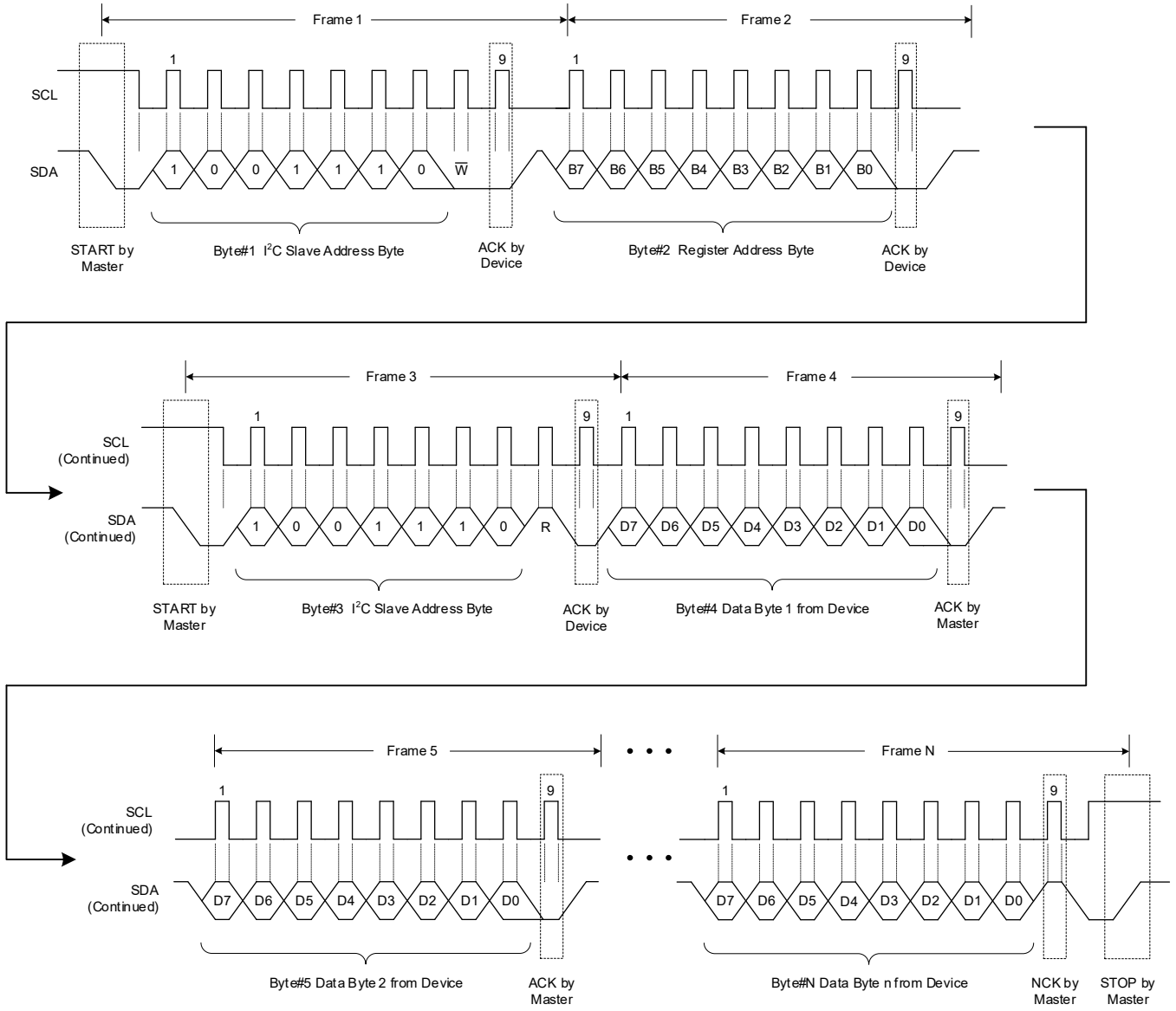


Figure 5. Read N Bytes of Data from Registers

DETAILED DESCRIPTION (continued)

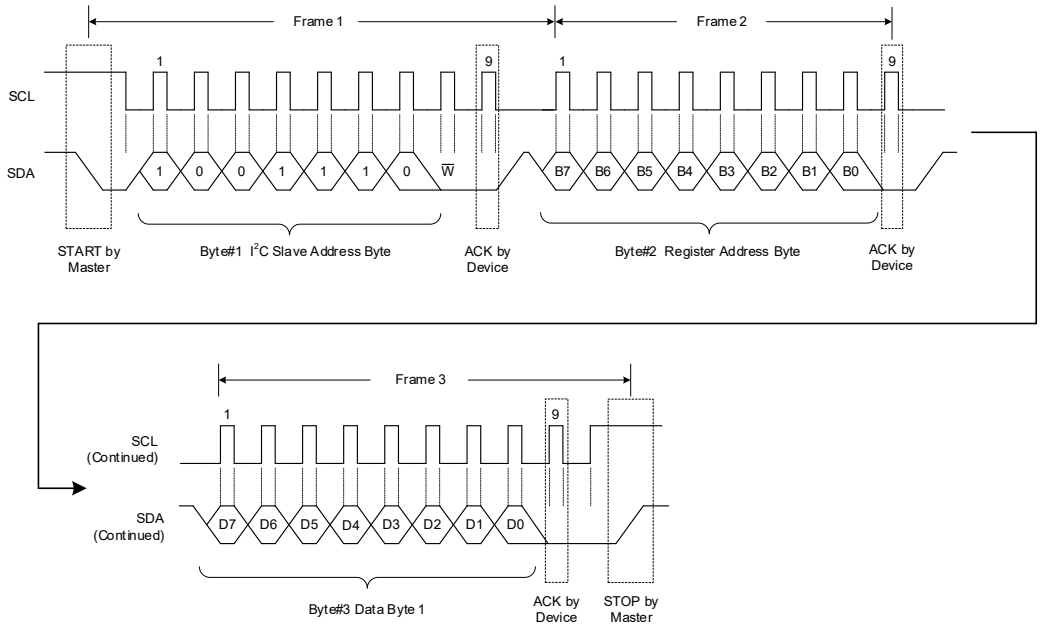


Figure 6. Write Single Byte of Data to Register

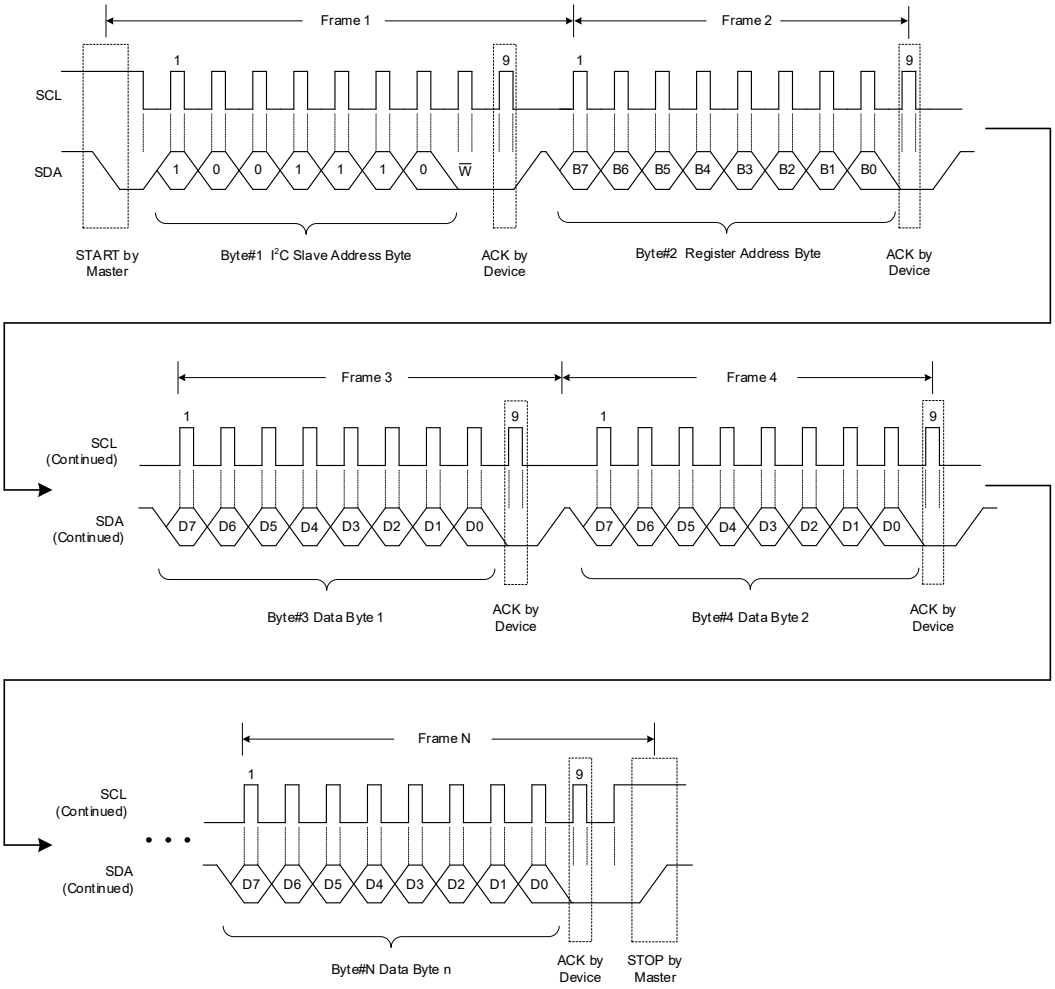


Figure 7. Write N Bytes of Data to Registers

REGISTER MAPS

Summary Register Map

Table 1 lists the SGM795 registers.

Table 1. SGM795 Registers

ADDRESS	REGISTER NAME	DEFAULT	TYPE
0x00h	VENDOR_ID Register	0x7E	R
0x01h	VENDOR_ID Register	0x37	R
0x02h	PRODUCT_ID Register	0x95	R
0x03h	PRODUCT_ID Register	0x07	R
0x04h	DEVICE_ID Register	0x20	R
0x05h	DEVICE_ID Register	0x10	R
0x06h	USBTYPEC_REV Register	0x23	R
0x08h	USBPD_VER Register	0x10	R
0x09h	USBPD_REV Register	0x32	R
0x0A	PDIF_VER Register	0x13	R
0x0B	PDIF_REV Register	0x20	R
0x10	ALERT_L Register	0x02	R, R/W1C
0x11	ALERT_H Register	0x02	R, R/W1C
0x12	ALERT_L_MASK Register	0x7F	R, R/W
0x13	ALERT_H_MASK Register	0x26	R, R/W
0x14	POWER_STATUS_MASK Register	0x4E	R, R/W
0x15	FAULT_STATUS_MASK Register	0xFF	R/W
0x16	EXTENDED_STATUS_MASK Register	0x01	R, R/W
0x19	TCPC_CONTROL Register	0x00	R, R/W
0x1A	ROLE_CONTROL Register	0x0A	R, R/W
0x1B	FAULT_CONTROL Register	0x00	R, R/W
0x1C	POWER_CONTROL Register	0x00	R, R/W
0x1D	CC_STATUS Register	0x00	R
0x1E	POWER_STATUS Register	0x00	R
0x1F	FAULT_STATUS Register	0x80	R, R/W1C
0x20	EXTENDED_STATUS Register	0x00	R, R/W
0x23	COMMAND Register	0x00	R/W
0x24	DEVICE_CAPABILITIES_1L Register	0xB8	R
0x25	DEVICE_CAPABILITIES_1H Register	0x1A	R
0x26	DEVICE_CAPABILITIES_2L Register	0x35	R
0x27	DEVICE_CAPABILITIES_2H Register	0x00	R
0x28	STANDARD_INPUT_CAPABILITIES Register	0x00	R
0x29	STANDARD_OUTPUT_CAPABILITIES Register	0x00	R
0x2E	MESSAGE_HEADER_INFO Register	0x02	R, R/W
0x2F	RECETVE_DETECT Register	0x00	R, R/W
0x30	RX_BYTE_COUNT Register	0x00	R
0x31	RX_BUF_FRAME_TYPE Register	0x00	R
0x32	RX_BUF_HEADER_BYTE_0 Register	0x00	R
0x33	RX_BUF_HEADER_BYTE_1 Register	0x00	R

REGISTER MAPS (continued)

ADDRESS	REGISTER NAME	DEFAULT	TYPE
0x34 ~ 0x4F	RX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register	0x00	R
0x50	TX_BUF_FRAME_TYPE Register	0x00	R, R/W
0x51	TX_BYTE_COUNT Register	0x00	R/W
0x52	TX_BUF_HEADER_BYTE_0 Register	0x00	R/W
0x53	TX_BUF_HEADER_BYTE_1 Register	0x00	R/W
0x54 ~ 0x6F	TX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register	0x00	R/W
0x90	SG_CTL Register	0x40	R, R/W
0x93	VCONOCP Register	0x80	R, R/W
0x97	SG_ST Register	0x00	R
0x98	SG_INT Register	0x00	R, R/W1C
0x99	SG_INT_MASK Register	0x00	R, R/W
0x9B	SG_SHUTDOWN Register	0x00	R, R/W
0x9F	WAKE_UP Register	0x80	R, R/W
0xA0	SOFT_RESET Register	0x00	R, W
0xA2	TDRP Register	0x03	R, R/W
0xA3	DRP_DUTY_CTRL0 Register	0x47	R/W
0xA4	DRP_DUTY_CTRL1 Register	0x01	R/W

Detailed Register Maps

Bit Types:
R: Read only
R/W: Read/Write
R/W1C: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.
7-bit I^2C Slave Device Address: 0b1001 110 + R/W

REG0x00: VENDOR_ID Register [Reset = 0x7E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID[7:0]	0111 1110	R	A unique 16-bit unsigned integer, representing the Vendor ID. Low byte.	N/A

REG0x01: VENDOR_ID Register [Reset = 0x37]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VID[15:8]	0011 0111	R	A unique 16-bit unsigned integer, representing the Vendor ID. High byte.	N/A

REG0x02: PRODUCT_ID Register [Reset = 0x95]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID[7:0]	1001 0101	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC. Low byte.	N/A

REG0x03: PRODUCT_ID Register [Reset = 0x07]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PID[15:8]	0000 0111	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC. High byte.	N/A

REG0x04: DEVICE_ID Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID[7:0]	0010 0000	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the SGM795. Low byte.	N/A

REGISTER MAPS (continued)

REG0x05: DEVICE_ID Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DID[15:8]	0001 0000	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the SGM795. High byte.	N/A

REG0x06: USBTYPEC_REV Register [Reset = 0x23]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBTYPEC_REV[7:0]	0010 0011	R	Byte 0 of a 16-bit USB Type-C Revision. Revision 2.3	N/A

REG0x08: USBPD_VER Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_VER[7:0]	0001 0000	R	Byte 0 of a 16-bit USB PD Version. Version 1.0.	N/A

REG0x09: USBPD_REV Register [Reset = 0x32]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	USBPD_REV[7:0]	0011 0010	R	Byte 1 of a 16-bit USB PD Revision. Revision 3.2.	N/A

REG0x0A: PDIF_VER Register [Reset = 0x13]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_VER[7:0]	0001 0011	R	Byte 0 of a 16-bit PD Interface (TCPC) Version. Version 1.3	N/A

REG0x0B: PDIF_REV Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	PDIF_REV[7:0]	0010 0000	R	Byte 1 of a 16-bit PD Interface (TCPC). Revision. Revision 2.0	N/A

REG0x10: ALERT_L Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ALARM_VBUS_VOLTAGE_H	0	R	Not support.	N/A
D[6]	TX_SUCCESS	0	R/W1C	0 = Cleared 1 = Reset or the SOP* message is successfully transmistted.	SOFT_RESET
D[5]	TX_DISCARD	0	R/W1C	0 = Cleared 1 = Reset or SOP* message transmission is not sent due to an incoming receive message.	SOFT_RESET
D[4]	TX_FAIL	0	R/W1C	0 = Cleared 1 = the SOP* message is successfully transmistted. No GoodCRC response is received on SOP* message transmission.	SOFT_RESET
D[3]	RX_HARD_RESET	0	R/W1C	0 = Cleared 1 = Received Hard Reset message	SOFT_RESET
D[2]	RX_SOP_MSG_STATUS	0	R/W1C	0 = Cleared 1 = Receive buffer register changed Note that RX_BYTE_COUNT being zero does not set this bit.	SOFT_RESET
D[1]	POWER_STATUS	1	R/W1C	0 = Cleared 1 = Port status changed The SGM795 will assert this bit after power-up due to a previous change of the TCPC_INITIAL bit in the POWER_STATUS register	SOFT_RESET
D[0]	CC_STATUS	0	R/W1C	0 = Cleared 1 = CC status changed SGM795 shall not assert this bit when the LOOKING4CONNECTION bit of CC_STATUS register changes state if EN_LOOKING4CON_ALERT bit of TCPC_CONTROL register is set to 0.	SOFT_RESET

REGISTER MAPS (continued)

REG0x11: ALERT_H Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VENDOR_DEFINED_ALERT	0	R/W1C	0 = Cleared 1 = A vendor defined alert that is unmasked has been detected. Defined in the SG_INT registers. TCPM SW should first clear the appropriate bit in SG_INT register before clearing this field.	SOFT_RESET
D[6]	ALERT_EXTENDED	0	R	Not support.	N/A
D[5]	EXTENDED_STATUS	0	R/W1C	0 = Cleared 1 = Extended status changed	SOFT_RESET
D[4]	BEGIN_SOP_MSG_STATUS	0	R	Not support.	N/A
D[3]	VBUS_SINK_DISCNT	0	R	Not support.	N/A
D[2]	RXBUF_OVFLOW	0	R/W1C	0 = SGM795 Rx buffer is functioning properly. 1 = SGM795 Rx buffer has overflowed.	SOFT_RESET
D[1]	FAULT	1	R/W1C	0 = No Fault. 1 = A Fault has occurred. Read the FAULT_STATUS register.	SOFT_RESET
D[0]	ALARM_VBUS_VOLTAGE_L	0	R	Not support.	N/A

REG0x12: ALERT_L_MASK Register [Reset = 0x7F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_ALARM_VBUS_VOLTAGE_H	0	R	Not support.	N/A
D[6]	M_TX_SUCCESS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[5]	M_TX_DISCARD	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[4]	M_TX_FAIL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[3]	M_RX_HARD_RESET	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[2]	M_RX_SOP_MSG_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[1]	M_POWER_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[0]	M_CC_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET

REG0x13: ALERT_H_MASK Register [Reset = 0x26]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_VENDOR_INT_STATUS	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[6]	ALERT_EXTENDED_MASK	0	R	Not support.	N/A
D[5]	M_EXTENDED_STATUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[4]	BEGIN_SOP_MSG_STATUS_MASK	0	R	Not support.	N/A
D[3]	M_VBUS_SINK_DISCNT	0	R	Not support.	N/A
D[2]	M_RXBUF_OVFLOW	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[1]	M_FAULT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[0]	M_ALARM_VBUS_VOLTAGE_L	0	R	Not support.	N/A

REGISTER MAPS (continued)

REG0x14: POWER_STATUS_MASK Register [Reset = 0x4E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DBG_ACC_CONNECT_MASK	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[6]	M_TCPC_INITIAL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[5]	M_SRC_HV	0	R	Not support.	N/A
D[4]	M_SRC_VBUS	0	R	Not support.	N/A
D[3]	M_VBUS_DET_EN	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[2]	M_VBUS_PRESENT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[1]	M_VCONN_PRESENT	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[0]	M_SINK_VBUS	0	R	Not support.	N/A

REG0x15: FAULT_STATUS_MASK Register [Reset = 0xFF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	M_ALL_REGISTERS_RESET	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[6]	M_FORCE_OFF_VBUS	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked This field has no meaning for SGM795.	SOFT_RESET
D[5]	M_AUTO_DISC_FAIL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked This field has no meaning for SGM795.	SOFT_RESET
D[4]	M_FORCE_DISC_FAIL	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[3]	M_VBUS_OC	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked This field has no meaning for SGM795.	SOFT_RESET
D[2]	M_VBUS_OV	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked This field has no meaning for SGM795.	SOFT_RESET
D[1]	M_VCON_OC	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[0]	M_I2C_ERROR	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET

REG0x16: EXTENDED_STATUS_MASK Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	RESERVED	0	R	Reserved	N/A
D[0]	M_VSAFE_0V	1	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET

REGISTER MAPS (continued)

REG0x19: TCPC_CONTROL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_SMBUS_PEC	0	R	Not support.	N/A
D[6]	EN_LOOKING4CON_ALERT	0	R/W	0 = Disable the CC_STATUS bit assertion of ALERT_L register when LOOKING4CONNECTION bit of CC_STATUS register changes. 1 = Enable the CC_STATUS bit assertion of ALERT_L register when LOOKING4CONNECTION bit of CC_STATUS register changes.	SOFT_RESET
D[5]	EN_WD_TIMER	0	R	Not support.	N/A
D[4]	DEBUG_ACC_CTRL	0	R	Not support.	N/A
D[3:2]	I2C_CK_STRETCH[1:0]	00	R	Not support.	N/A
D[1]	BIST_TEST_MODE	0	R/W	0 = Normal Operation. RECEIVE_DETECT-enabled messages passed to TCPM via alert. 1 = BIST Test Mode. RECEIVE_DETECT-triggered messages generate GoodCRC response but not reach TCPM via alert.	SOFT_RESET
D[0]	PLUG_ORIENT	0	R/W	0 = If VCONN is enabled, apply it to the CC2 pin. If PD messaging is enabled, monitor the CC1 pin for BMC communications. 1 = If VCONN is enabled, apply it to the CC1 pin. If PD messaging is enabled, monitor the CC2 pin for BMC communications	SOFT_RESET

REG0x1A: ROLE_CONTROL Register [Reset = 0x0A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	RESERVED	0	R	Reserved	N/A
D[6]	EN_DRP	0	R/W	0 = No DRP. Bits [3:0] determine the settings of Rp, Rd and Ra. 1 = DRP	SOFT_RESET
D[5:4]	RP_VALUE[1:0]	00	R/W	00 = Rp 01 = Rp 1.5A 10 = Rp 3.0A 11 = Reserved	SOFT_RESET
D[3:2]	CC2[1:0]	10	R/W	00 = Ra 01 = Rp (Use Rp definition in RP_VALUE[1:0]) 10 = Rd 11 = Open	SOFT_RESET
D[1:0]	CC1[1:0]	10	R/W	00 = Ra 01 = Rp (Use Rp definition in RP_VALUE[1:0]) 10 = Rd 11 = Open	SOFT_RESET

REGISTER MAPS (continued)

REG0x1B: FAULT_CONTROL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	RESERVED	000	R	Reserved	N/A
D[4]	DIS_FORCE_OFF_VBUS	0	R	Not support.	N/A
D[3]	DIS_VBUS_DISC_FAULT_TIMER	0	R/W	0 = VBUS discharge fault detection timer enabled 1 = VBUS discharge fault detection timer disabled This enables the timers for FORCE_DISC_FAIL bit of FAULT_STATUS register.	SOFT_RESET
D[2]	DIS_VBUS_OC	0	R	Not support.	N/A
D[1]	DIS_VBUS_OV	0	R	Not support.	N/A
D[0]	DIS_VCON_OC	0	R/W	0 = Fault detection circuit enabled 1 = Fault detection circuit disabled	SOFT_RESET

REG0x1C: POWER_CONTROL Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FR_SWAP_EN	0	R	Not support.	N/A
D[6]	VBUS_VOL_MONITOR	0	R	Not support.	N/A
D[5]	DIS_VOL_ALARM	0	R	Not support.	N/A
D[4]	AUTO_DISC_DISCNCT	0	R	Not support.	N/A
D[3]	BLEED_DISC	0	R/W	0 = Disable bleed discharge 1 = Enable bleed discharge of VBUS	SOFT_RESET
D[2]	FORCE_DISC	0	R/W	When FORCE_DISC is set, the SGM795 will initiate Force Discharge, which remains active until VBUS falls below Vsafe0V or until it times out. 0 = Disable forced discharge 1 = Enable forced discharge of VBUS.	SOFT_RESET
D[1]	VCONN_POWER_SPT	0	R/W	0 = SGM795 delivers at least 1W on VCONN 1 = SGM795 delivers at least the power indicated in VCONN_POWER[2:0] bit of the DEVICE_CAPABILITIES_2L register supported. Writing this bit has no function. Please use VCONN_OCP to set OCP values.	SOFT_RESET
D[0]	EN_VCONN	0	R/W	0 = Disable VCONN source 1 = Enable VCONN source to CC required	SOFT_RESET

REGISTER MAPS (continued)

REG0x1D: CC_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	RESERVED	00	R	Reserved	N/A
D[5]	LOOKING4CONNECTION	0	R	0 = SGM795 has stopped toggling or EN_DRP bit of ROLE_CONTROL register is 0 1 = SGM795 is toggling	SOFT_RESET
D[4]	CONNECT_RESULT	0	R	0 = SGM795 is presenting Rp 1 = SGM795 is presenting Rd	SOFT_RESET
D[3:2]	CC2_STATUS[1:0]	00	R	If CC2 bit of ROLE_CONTROL register is Rp or CONNECT_RESULT bit is 0: 00 = SRC.Open (Open, Rp) 01 = SRC.Ra (below maximum vRa) 10 = SRC.Rd (within the vRd range) 11 = reserved If CC2 bit of ROLE_CONTROL register is Rd or CONNECT_RESULT bit is 1: 00 = SNK.Open (Below maximum vRa) 01 = SNK.Default (Above minimum vRd-Connect) 10 = SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A 11 = SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A If CC2 bit of ROLE_CONTROLregister is Ra, this field is set to 00b. If CC2 bit of ROLE_CONTROLregister is Open, this field is set to 00b. This field always returns 00b if LOOKING4CONNECTION bit is 1 or EN_VCONN bit of POWER_CONTROL register is 1 and PLUG_ORIENT bit of TCPC_CONTROL register is 0. Alternatively, the returned value depends on CC2 bit of ROLE_CONTROL register.	SOFT_RESET
D[1:0]	CC1_STATUS[1:0]	00	R	If CC1 bit of ROLE_CONTROL register is Rp or CONNECT_RESULT bit is 0: 00 = SRC.Open (Open, Rp) 01 = SRC.Ra (below maximum vRa) 10 = SRC.Rd (within the vRd range) 11 = reserved If CC1 bit of ROLE_CONTROL register is Rd or CONNECT_RESULT bit is 1: 00 = SNK.Open (Below maximum vRa) 01 = SNK.Default (Above minimum vRd-Connect) 10 = SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A 11 = SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A If CC1 bit of ROLE_CONTROL register is Ra, this field is set to 00b. If CC1 bit of ROLE_CONTROL register is Open, this field is set to 00b. This field always returns 00b if LOOKING4CONNECTION bit is 1 or EN_VCONN bit of POWER_CONTROL register is 1 and PLUG_ORIENT bit of TCPC_CONTROL register is 0. Alternatively, the returned value depends on CC1 bit of ROLE_CONTROL register.	SOFT_RESET

REGISTER MAPS (continued)

REG0x1E: POWER_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DBG_ACC_CONNECT	0	R	0 = No Debug Accessory connected 1 = Debug Accessory connected	SOFT_RESET
D[6]	TCPC_INITIAL	0	R	0 = SGM795 initialization complete. All registers are valid 1 = SGM795 is still undergoing internal initialization. The only registers guaranteed to return the accurate values are 00h to 0Fh	SOFT_RESET
D[5]	SRC_HV	0	R	Not support.	N/A
D[4]	SRC_VBUS	0	R	Not support.	N/A
D[3]	VBUS_DET_EN	0	R	0 = VBUS present detection disabled 1 = VBUS present detection enabled The SGM795 will automatically assert this bit when the TCPM configures the chip to Non-Shutdown mode after power-up.	SOFT_RESET
D[2]	VBUS_PRESENT	0	R	0 = VBUS Disconnected 1 = VBUS Connected The SGM795 will report VBUS present if it detects VBUS is higher than 4V. The SGM795 will report VBUS is not present if it detects VBUS is lower than 3.5V. The SGM795 may report VBUS is not present if VBUS is between 3.5V and 4V.	SOFT_RESET
D[1]	VCONN_PRESENT	0	R	0 = VCONN is not present 1 = This bit will be asserted if VCONN presents CC1 or CC2. The fixed detection threshold is 2.4V.	SOFT_RESET
D[0]	SINK_VBUS	0	R	Not support.	N/A

REG0x1F: FAULT_STATUS Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ALL_REGISTERS_RESET	1	R/W1C	This bit is asserted when the SGM795 resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs. TCPM can execute the initialization procedure by reading this bit, and during the initialization, this bit needs to be cleared.	SOFT_RESET
D[6]	FORCE_OFF_VBUS	0	R	Not support.	N/A
D[5]	AUTO_DISC_FAIL	0	R	Not support.	N/A
D[4]	FORCE_DISC_FAIL	0	R/W1C	0 = No discharge failure 1 = Discharge commanded by the TCPM failed If FORCE_DISC bit of POWER_CONTROL register is set, the SGM795 will report a discharge fails if VBUS is not below vsafe0V within tSafe0v.	SOFT_RESET
D[3]	VBUS_OC	0	R	Not support.	N/A
D[2]	VBUS_OV	0	R	Not support.	N/A
D[1]	VCON_OC	0	R/W1C	0 = No fault detected 1 = Over-current VCONN fault latched	SOFT_RESET
D[0]	I2C_ERROR	0	R/W1C	0 = No Error 1 = I^2C error has occurred.	SOFT_RESET

REG0x20: EXTENDED_STATUS Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	RESERVED	000 0000	R	Reserved	N/A
D[0]	VSAFE_0V	0	R	0 = VBUS is not at vSafe0V 1 = VBUS is at vSafe0V The SGM795 reports that VBUS is at vSafe0V when SGM795 detects that VBUS is below 0.8V.	SOFT_RESET

REGISTER MAPS (continued)

REG0x23: COMMAND Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	COMMAND[7:0]	0000 0000	R/W	00100010 = DisableVbusDetect Disable Vbus present and vSafe0V detection. 00110011 = EnableVbusDetect Enable Vbus present and vSafe0V detection. 10011001 = Look4Connection Start DRP toggling if EN_DRP bits of ROLE_CONTROL register is 1b. If CC1/CC2 bit of ROLE_CONTROL register is 01b, start with Rp, if CC1/CC2 register of ROLE_CONTROL register is 10b, start with Rd. Reading this register always return 0x00 value.	SOFT_RESET

REG0x24: DEVICE_CAPABILITIES_1L Register [Reset = 0xB8]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	ROLES_SUPPORT[2:0]	101	R	000 = Type-C Port Manager can configure the port as source only or sink only (not DRP) 001 = Source only 010b = Sink only 011 = Sink with accessory support (optional) 100 = DRP only 101 = Source, Sink, DRP, Adapter/Cable all supported 110 = Source, Sink, DRP 111 = Not valid	N/A
D[4]	ALL_SOP_SUPPORT	1	R	0 = All SOP* except SOP'_DBG/SOP"_DBG 1 = All SOP* messages are supported Configured in RECEIVE_DETECT and TRANSMIT.	N/A
D[3]	SOURCE_VCONN	1	R	0 = SGM795 cannot switch VCONN 1 = SGM795 can switch VCONN	N/A
D[2]	CPB_SINK_VBUS	0	R	0 = SGM795 cannot control the sink path to the system load 1 = SGM795 can control the sink path to the system load	N/A
D[1]	SOURCE_HV_VBUS	0	R	0 = SGM795 cannot control the source high voltage path to VBUS 1 = SGM795 can control the source high voltage path to VBUS	N/A
D[0]	SOURCE_VBUS	0	R	0 = SGM795 cannot control the source path to VBUS 1 = SGM795 can control the source path to VBUS	N/A

REG0x25: DEVICE_CAPABILITIES_1H Register [Reset = 0x1A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_NONDEFAULT_TARGET	0	R	0 = VBUS_NONDEFAULT_TARGET register not implemented (default) 1 = VBUS_NONDEFAULT_TARGET register implemented	N/A
D[6]	CPB_VBUS_OC	0	R	0 = VBUS OCP is not reported by the SGM795 1 = VBUS OCP is reported by the SGM795	N/A
D[5]	CPB_VBUS_OV	0	R	0 = VBUS OVP is not reported by the SGM795 1 = VBUS OVP is reported by the SGM795	N/A
D[4]	CPB_BLEED_DISC	1	R	0 = No Bleed Discharge implemented in SGM795 1 = Bleed Discharge is implemented in the SGM795 Support for BLEED_DISC bit of POWER_CONTROL register implemented.	N/A
D[3]	CPB_FORCE_DISC	1	R	0 = No Force Discharge implemented in SGM795 1 = Force Discharge is implemented in the SGM795	N/A
D[2]	VBUS_MEASURE_ALARM	0	R	0 = No VBUS voltage measurement nor VBUS Alarms 1 = VBUS voltage measurement and VBUS Alarms Support for FORCE_DISC bit of POWER_CONTROL register implemented.	N/A
D[1:0]	SOURCE_RP_SUPPORT[1:0]	10	R	00 = Rp default only 01 = Rp 1.5A and default 10 = Rp 3.0A, 1.5A, and default 11 = Reserved Rp values which can be programmed by the TCPM through the ROLE_CONTROL register.	N/A

REGISTER MAPS (continued)

REG0x26: DEVICE_CAPABILITIES_2L Register [Reset = 0x35]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SINK_DISCONNECT_DET	0	R	0 = VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default = Use VBUS_PRESENT bit of POWER_STATUS register is 0b to indicate a sink disconnect) 1 = VBUS_SINK_DISCONNECT_THRESHOLD is implemented	N/A
D[6]	STOP_DISC_THD	0	R	0 = VBUS_STOP_DISCHARGE_THRESHOLD is not implemented 1 = VBUS_STOP_DISCHARGE_THRESHOLD is implemented	N/A
D[5:4]	VBUS_VOL_ALARM_LSB[1:0]	11	R	11 = Not support this function.	N/A
D[3:1]	VCONN_POWER[2:0]	010	R	000 = 1.0W 001 = 1.5W 010 = 2.0W 011 = 3W 100 = 4W 101 = 5W 110 = 6W 111 = External	N/A
D[0]	VCONN_OCF	1	R	0 = SGM795 is not capable of detecting a VCONN fault 1 = SGM795 is capable of detecting a VCONN fault	N/A

REG0x27: DEVICE_CAPABILITIES_2H Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DEVICE_CAPABILITIES_3 _SUPPORT	0	R	0 = TCPC does not support the DEVICE_CAPABILITIES_3 register 1 = TCPC supports the DEVICE_CAPABILITIES_3 register	N/A
D[6]	MSG DISABLE DISCONNECT	0	R	0 = Sink TCPC disables PD message delivery when ALERT_H. VBUS_SINK_DISCNT has been asserted 1 = Sink TCPC disables PD message delivery using the condition as defined in RECEIVE_DETECT. MSG_DISABLE_DISCNCT	N/A
D[5]	GENERIC_TIMER	0	R	0 = GENERIC_TIMER register is not supported 1 = GENERIC_TIMER register is supported	N/A
D[4]	LONG_MSG	0	R	0 = TCPC only supports 30 bytes content of the SOP* message. The value in RX_BYTE_COUNT shall be less than or equal to 31. The value in TX_BYTE_COUNT shall be less than or equal to 30 1 = TCPC is capable of supporting 264 bytes content of the SOP* message. The TX_BUF holds up to 264 bytes content of the SOP* message. The TCPM can write up to 132 bytes to the TX_BUF_BYTE_x in one burst. The value supported in TX_BYTE_COUNT COUNT shall be up to 132. RX_BUF holds up to 264 bytes content SOP* message plus a 30 bytes content SOP* message	N/A
D[3]	SMBUS_PEC	0	R	0 = TCPC_CONTROL.EN_SMBUS_PEC is not implemented 1 = TCPC_CONTROL.EN_SMBUS_PEC implemented	N/A
D[2]	SOURCE_FR_SWAP	0	R	0 = Not capable of sending Fast Role Swap signal as Source when Receiving SendFRSwapSignal COMMAND or receiving STANDARD INPUT Source Fast Role Swap low 1 = Capable of sending Fast Role Swap signal as Source TCPC when Receiving SendFRSwapSignal COMMAND. If STANDARD_INPUT_CAPABITILIES.SOURCE_FR_SWAP = 1, capable of sending Fast Role Swap signal as Source when STANDARD INPUT Source Fast Role Swap is set low	N/A
D[1]	SINK_FR_SWAP	0	R	0 = POWER_CONTROL.FR_SWAP_EN Enable not supported as Sink 1 = POWER_CONTROL.FR_SWAP_EN Enable supported as Sink	N/A
D[0]	WD_TIMER	0	R	0 = TCPC_CONTROL.EN_WD_TIMER not implemented 1 = TCPC_CONTROL.EN_WD_TIMER implemented	N/A

REGISTER MAPS (continued)

REG0x28: STANDARD_INPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	RESERVED	000	R	Reserved	N/A
D[4:3]	SOURCE_FR_SWAP[1:0]	00	R	00 = Not present in TCPC 01 = Present in TCPC as an input only pin 10 = Present in TCPC as a bidirectional pin, sharing with the STANDARD OUTPUT SIGNAL VBUS Sink Disconnect Detect Indicator. The “VBUS Sink Disconnect Detect Indicator” bit in STANDARD_OUTPUT_CAPABILIT IES register shall also be set to 1 11 = Reserved	N/A
D[2]	VBUS_EXT_OVP	0	R	VBUS External Over-Voltage Fault 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[1]	VBUS_EXT_OCP	0	R	VBUS External Over-Current Fault 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[0]	FORCE_OFF_VBUS	0	R	Force Off VBUS (Source or Sink) 0 = Not present in TCPC 1 = Present in TCPC	N/A

REG0x29: STANDARD_OUTPUT_CAPABILITIES Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	VBUS_SINK_DISCONNECT_ DET_IND	0	R	Sink Disconnect Detection Indicator 0 = Not present in TCPC 1 = Present in TCPC Shall present in TCPC if “Source Fast Role Swap” in STANDARD_INPUT_CAPABILITIES is set to 10b (present as a bidirectional pin).	N/A
D[6]	CPB_DBG_ACC_IND	0	R	Debug Accessory Indicator 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[5]	CPB_VBUS_PRESENT_MNT	0	R	VBUS Present Monitor 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[4]	CPB_AUDIO_ADT_ACC_IND	0	R	Audio Adapter Accessory Indicator 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[3]	CPB_ACTIVE_CABLE_IND	0	R	Active Cable Indicator 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[2]	CPB_MUX_CFG_CTRL	0	R	MUX Configuration Control 0 = Not present in TCPC 1 = Present in TCPC	N/A
D[1]	CPB_CONNECT_PRESENT	0	R	Connection Present 0 = No Connection 1 = Connection Controlled by the TCPM.	N/A
D[0]	CPB_CONNECT_ORIENT	0	R	Connector Orientation 0 = Not present in TCPC 1 = Present in TCPC	N/A

REGISTER MAPS (continued)

REG0x2E: MESSAGE_HEADER_INFO Register [Reset = 0x02]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	RESERVED	000	R	Reserved	N/A
D[4]	CABLE_PLUG	0	R/W	0 = Message originated from source, sink, or DRP 1 = Message originated from a Cable Plug	SOFT_RESET
D[3]	DATA_ROLE	0	R/W	0 = UFP 1 = DFP	SOFT_RESET
D[2:1]	USBPD_SPECREV[1:0]	01	R/W	00 = Revision 1.0 01 = Revision 2.0 10 = Revision 3.0 11 = Reserved	SOFT_RESET
D[0]	POWER_ROLE	0	R/W	0 = Sink 1 = Source	SOFT_RESET

REG0x2F: RECETVE_DETECT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	MSG_DISABLE_DISCNCT	0	R	Not support.	N/A
D[6]	EN_CABLE_RST	0	R/W	0 = SGM795 does not detect Cable Reset signaling 1 = SGM795 detects Cable Reset signaling	SOFT_RESET
D[5]	EN_HARD_RST	0	R/W	0 = SGM795 does not detect Hard Reset signaling 1 = SGM795 detects Hard Reset signaling	SOFT_RESET
D[4]	EN_SOP2DB	0	R/W	0 = SGM795 does not detect SOP_DBG'' message 1 = SGM795 detects SOP_DBG'' message	SOFT_RESET
D[3]	EN_SOP1DB	0	R/W	0 = SGM795 does not detect SOP_DBG' message 1 = SGM795 detects SOP_DBG' message	SOFT_RESET
D[2]	EN_SOP2	0	R/W	0 = SGM795 does not detect SOP'' message 1 = SGM795 detects SOP'' message	SOFT_RESET
D[1]	EN_SOP1	0	R/W	0 = SGM795 does not detect SOP' message 1 = SGM795 detects SOP' message	SOFT_RESET
D[0]	EN_SOP	0	R/W	0 = SGM795 does not detect SOP message 1 = SGM795 detects SOP message	SOFT_RESET

REG0x30: RX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_BYTE_COUNT[7:0]	0000 0000	R	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register. This is the number counts form RX_BUF_FRAME_TYPE to the RX_BUF register stored the last date byte.	SOFT_RESET

REG0x31: RX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	RESERVED	0000	R	Reserved	N/A
D[2:0]	RX_FRAME_TYPE[2:0]	000	R	Type of received frame 000 = Received SOP 001 = Received SOP' 010 = Received SOP" 011 = Received SOP_DBG' 100 = Received SOP_DBG'' 110 = Received Cable Reset All others are reserved.	SOFT_RESET

REGISTER MAPS (continued)

REG0x32: RX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_0[7:0]	0000 0000	R	Byte 0 (bits [7:0]) of message header	SOFT_RESET

REG0x33: RX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_HEAD_1[7:0]	0000 0000	R	Byte 1 (bits [15:8]) of message header	SOFT_RESET

REG0x34~REG0x4F: RX_BUF_OBJx(1~7)_BYTE_x(0~3) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_OBJx_BYTE_x[7:0]	0000 0000	R	Byte x(0~3) of data object x(1~7) of Receive Buffer.	SOFT_RESET

REG0x50: TX_BUF_FRAME_TYPE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	RESERVED	00	R	Reserved	N/A
D[5:4]	TX_RETRY_CNT[1:0]	00	R/W	00 = No message retry is required 01 = Automatically retry message transmission once 10 = Automatically retry message transmission twice 11 = Automatically retry message transmission three times	SOFT_RESET
D[3]	RESERVED	0	R	Reserved	N/A
D[2:0]	TX_FRAME_TYPE[2:0]	000	R/W	000 = Transmit SOP 001 : Transmit SOP' 010 = Transmit SOP" 011 = Transmit SOP_DBG' 100 = Transmit SOP_DBG'' 101 = Transmit Hard Reset 110 = Transmit Cable Reset 111 = Transmit BIST Carrier Mode 2 (SGM795 shall exit the BIST mode no later than $t_{BISTContMode}$ max)	SOFT_RESET

REG0x51: TX_BYTE_COUNT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_BYTE_COUNT[7:0]	0000 0000	RW	The number of bytes the TCPM will write	SOFT_RESET

REG0x52: TX_BUF_HEADER_BYTE_0 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_0[7:0]	0000 0000	R/W	Byte 0 (bits [7:0]) of message header	SOFT_RESET

REG0x53: TX_BUF_HEADER_BYTE_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_HEAD_1[7:0]	0000 0000	R/W	Byte 1 (bits [15:8]) of message header	SOFT_RESET

REG0x54 ~ REG0x6F: TX_BUF_OBJx(1 ~ 7)_BYTE_x(0 ~ 3) Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_OBJx_BYTE_x	0000 0000	R/W	Byte x(0~3) of data object x(1~7) of Transmit Buffer.	SOFT_RESET

REGISTER MAPS (continued)

REG0x90: SG_CTL Register [Reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DIS_VCONN_OV	0	R/W	0 = Fault detection circuit enabled 1 = Fault detection circuit disabled	SOFT_RESET
D[6]	VCONN_OTP_EN	1	R/W	VCONN OTP enable 0 = Disable OTP 1 = Enable OTP	SOFT_RESET
D[5]	RESERVED	0	R	Reserved	N/A
D[4]	LPRPRD	0	R/W	Low power mode Rp Rd 0 = Low power mode RD 1 = Low power mode RP	SOFT_RESET
D[3]	LPEN	0	R/W	Low power mode enable 0 = Standby mode 1 = Low power	SOFT_RESET
D[2]	RESERVED	0	R	Reserved	N/A
D[1]	VBUS_DETEN	0	R/W	VBUS detection enable 0 = Measure off 1 = Operation The SGM795 will automatically assert this bit when the TCPM configures the chip to Non-Shutdown mode after power-up.	SOFT_RESET
D[0]	RESERVED	0	R	Reserved	N/A

REG0x93: VCONOCP Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VCONOCP[2:0]	100	R/W	VCONN over-current control selection 000 = Current level = 200mA 001 = Current level = 300mA 010 = Current level = 400mA 011 = Current level = 500mA 100 = Current level = 600mA 101 to 111 = Reserved If VCONNOCP is triggered, the switch will turn off timing under 55μs.	SOFT_RESET
D[4:0]	RESERVED	0 0000	R	Reserved	N/A

REG0x97: SG_ST Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	RESERVED	00	R	Reserved	N/A
D[5]	OTP_STATUS	0	R	0 = default 1 = OTP triggered	SOFT_RESET
D[4]	VBUS_5_5	0	R	0 = VBUS is under 5.5V 1 = VBUS is over 5.5V	SOFT_RESET
D[3]	VBUS_4_75	0	R	0 = VBUS is under 4.75V 1 = VBUS is over 4.75V	SOFT_RESET
D[2]	RESERVED	0	R	Reserved	N/A
D[1]	VSAFE0V_STATUS	0	R	0 = VBUS is not at vSafe0V (default) 1 = VBUS is at vSafe0V	SOFT_RESET
D[0]	RESERVED	0	R	Reserved	N/A

REGISTER MAPS (continued)

REG0x98: SG_INT Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	RESERVED	0	R	Reserved	N/A
D[6]	INT_VCON_OTP	0	R/W1C	0 = Cleared 1 = VCONN over-temperature protection	SOFT_RESET
D[5]	INT_RA_DETACH	0	R/W1C	0 = Cleared (default) 1 = Ra detach	SOFT_RESET
D[4]	INT_VBUS_5_5	0	R/W1C	0 = VBUS under 5.5V 1 = VBUS without under 5.5V	SOFT_RESET
D[3]	INT_VBUS_4_75	0	R/W1C	0 = VBUS under 4.75V 1 = VBUS without under 4.75V	SOFT_RESET
D[2]	INT_VCON_OV	0	R/W1C	0 = Not in an over-voltage protection state 1 = Over-voltage fault latched.	SOFT_RESET
D[1]	INT_VSAFE0V_STATUS	0	R/W1C	0 = VBUS is not at vSafe0V (default) 1 = VBUS is at vSafe0V	SOFT_RESET
D[0]	INT_WAKEUP	0	R/W1C	0 = Cleared 1 = Low power mode exited	SOFT_RESET

REG0x99: SG_INT_MASK Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	RESERVED	0	R	Reserved	N/A
D[6]	M_VCON_OTP	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[5]	M_RA_DETACH	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[4]	M_VBUS_5_5	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[3]	M_VBUS_4_75	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[2]	M_VCON_OV	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[1]	M_VSAFE0V_STATUS	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET
D[0]	M_WAKEUP	0	R/W	0 = Interrupt masked 1 = Interrupt unmasked	SOFT_RESET

REG0x9B: SG_SHUTDOWN Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	RESERVED	00	R	Reserved	N/A
D[5]	Shutdown_OFF	0	R/W	0 = Shutdown mode 1 = Non-Shutdown mode	SOFT_RESET
D[4:0]	RESERVED	00000	R	Reserved	N/A

REG0x9F: WAKE_UP Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WAKEUP_EN	1	R/W	0 = Wakeup function disable 1 = Wakeup function enable	SOFT_RESET
D[6:0]	RESERVED	000 0000	R	Reserved	N/A

REGISTER MAPS (continued)

REG0xA0: SOFT_RESET Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:1]	RESERVED	0000 000	R	Reserved	N/A
D[0]	SOFT_RESET	0	W	Write 1 to trigger software reset.	SOFT_RESET

REG0xA2: TDRP Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	RESERVED	0000	R	Reserved	N/A
D[3:0]	TDRP[3:0]	0011	R/W	The period of DRP advertisement. (Period = TDRP[3:0] × 6.4 + 51.2ms) 0000 = 51.2ms 0001 = 57.6ms 0010 = 64ms 0011 = 70.4ms … 1110 = 140.8ms 1111 = 147.2ms	SOFT_RESET

REG0xA3: DRP_DUTY_CTRL0 Register [Reset = 0x47]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DUTY_SRC[7:0]	0100 0111	R/W	The duty of time when DRP advertises Source. (DUTY = (DUTY_SRC[9:0] + 1)/1024) 0000000000 = 1/1024 0000000001 = 2/1024 … 0101000111 = 328/1024 … 1111111110 = 1023/1024 1111111111 = 1024/1024 Note : Setting with 0xA4[9:8]	SOFT_RESET

REG0xA4: DRP_DUTY_CTRL1 Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:2]	RESERVED	0000 00	R	Reserved	N/A
D[1:0]	DUTY_SRC[9:8]	01	R/W	The duty of time when DRP advertises Source. (DUTY = (DUTY_SRC[9:0] + 1)/1024) 0000000000 = 1/1024 0000000001 = 2/1024 … 0101000111 = 328/1024 … 1111111110 = 1023/1024 1111111111 = 1024/1024 Note : Setting with 0xA3[7:0]	SOFT_RESET

APPLICATION INFORMATION

Typical Application

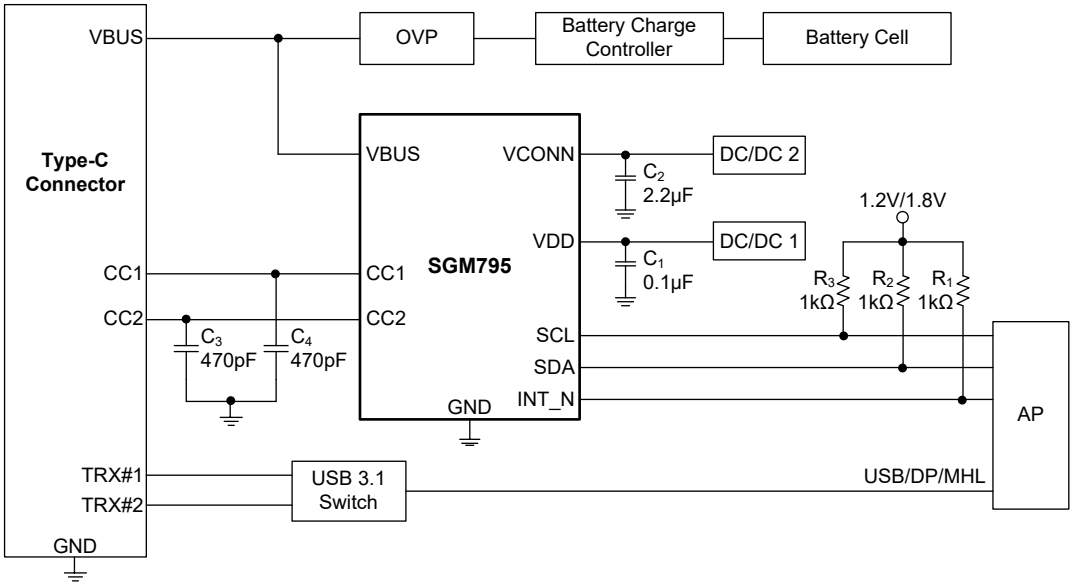


Figure 8. Typical Application Circuit

Table 2. Design Parameters

Reference	Description
R_1, R_2, R_3	1kΩ, 1%, 0402
C_1	100nF/50V/X7R, 0402
C_2	2.2uF/25V/X7R, 0402
C_3, C_4	470pF/25V/X7R, 0402

Design Procedure

The SGM795 is designed to accommodate power from an external battery with a wide range of VDD support. Its I^2C slave interface supports clock frequencies up to 1MHz at signal levels of both 1.2V and 1.8V. The pull-up resistor values for the SDA and SCL pins are chosen based on the maximum value of I^2C bus capacitance and frequency, depending on the signaling level of the I^2C master.

VCONN is employed to power Type-C active cables and other accessories with a minimum mandated power of 1W. Place a minimum 2.2μF capacitor with effective capacitance > 1μF between VCONN and GND pins close to the device. The SGM795 features an internal switch to direct power from the VCONN pin to either CC1 or CC2 pin. Equation 1 is utilized to determine the allowable VCONN power through the SGM795, considering its maximum $R_{DS(ON)}$ and the minimum I_{VCONN} current.

$$(V_{VCONN} - V_{CABLE})/R_{DS(ON)\_MAX} < I_{VCONOCP} \quad (1)$$

where:

V_{VCONN} represents voltage on the VCONN pin.

V_{CABLE} represents voltage required by cable.

$R_{DS(ON)\_MAX}$ denotes the maximum on-resistance of the VCONN switch.

$I_{VCONOCP}$ is the programmed VCONN over-current protection threshold.

LAYOUT

Layout Guidelines

1. A 0.1μF decoupling capacitor must be placed as close as possible to the VDD pin of the SGM795.

2. The trace width and thickness for CC1, CC2, and VCONN must be designed to support at least 1 Watt of power.

3. A minimum 470pF ceramic capacitor should be placed between each of the CC1/CC2 pins and GND, located as close to the device as possible.

The reference layout in Figure 9 utilizes a via-in-pad for the inner pad B2. This is necessitated by the tight spacing between the two pads. If PCB manufacturing capabilities permit the use of very fine traces (e.g., 2mils), the via-in-pad is not required.

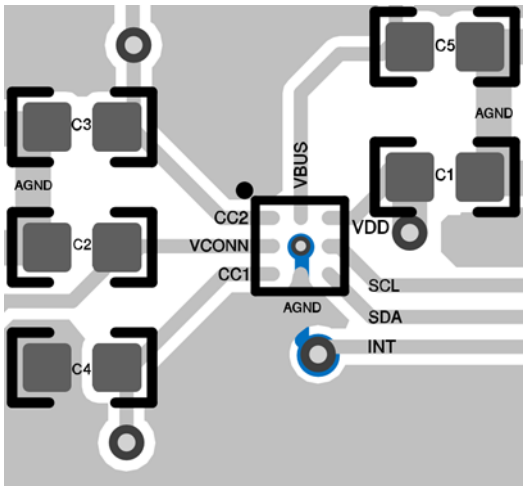


Figure 9. Referenced PCB layout

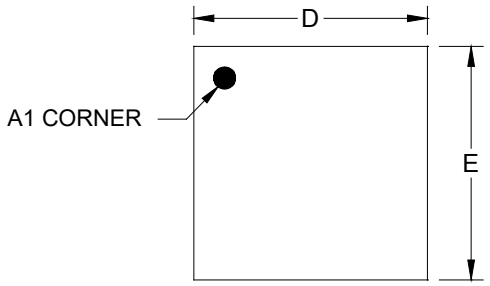
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

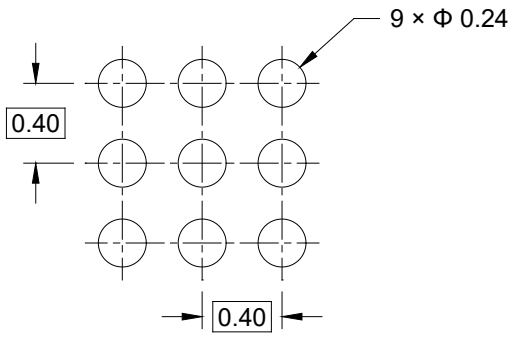
Changes from Original to REV.A (NOVEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

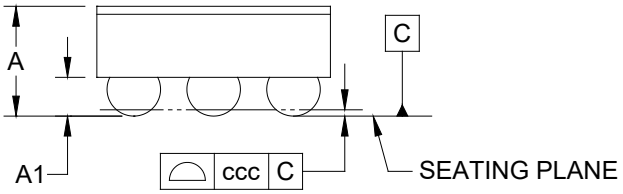
WLCSP-1.17×1.17-9B



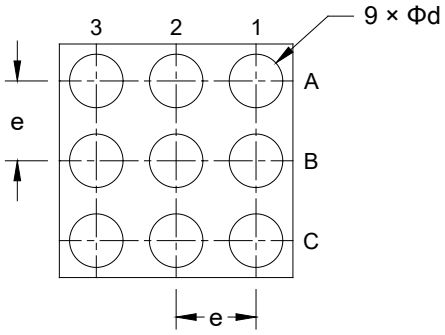
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



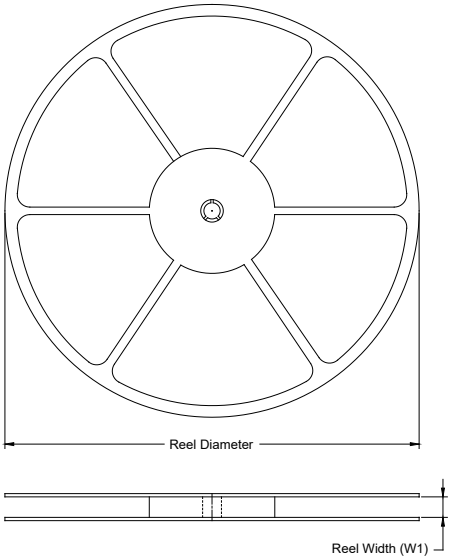
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.588
A1	0.174	-	0.214
D	1.140	-	1.200
E	1.140	-	1.200
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

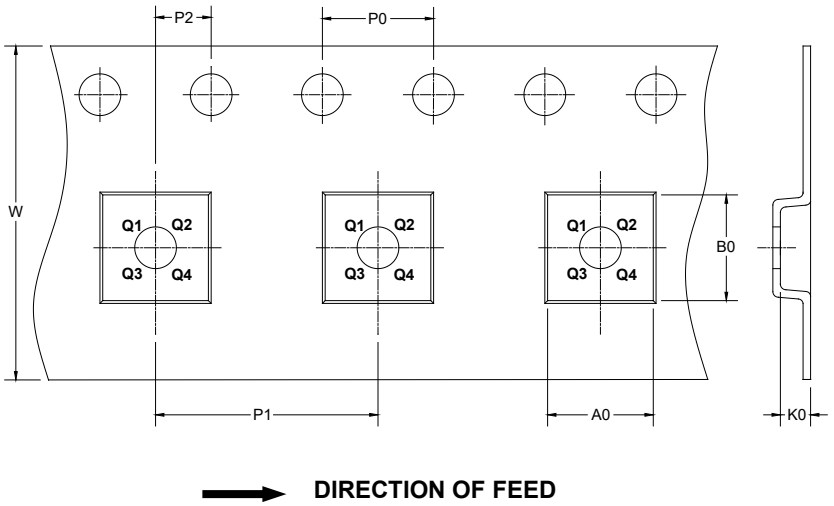
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

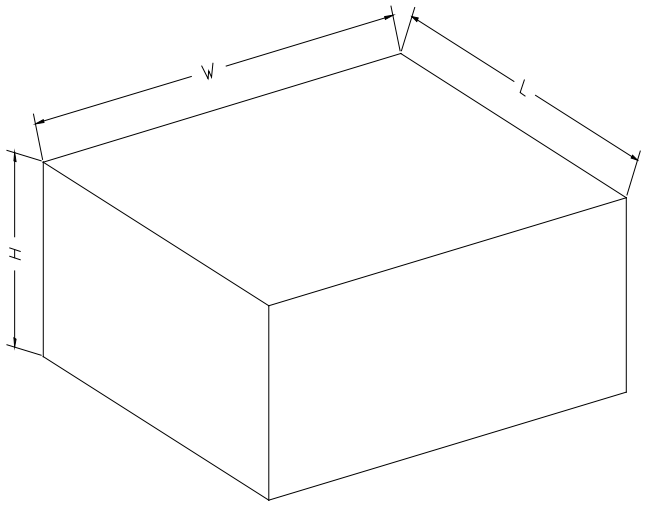
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.17×1.17-9B	7"	9.5	1.26	1.26	0.69	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002