SGM3807

Power PMIC with a Synchronous Buck and a Single Inductor Dual-Output DC/DC

GENERAL DESCRIPTION

The SGM3807 is a power PMIC which integrates a synchronous Buck converter and a single inductor dual-output (SIDO) DC/DC converter. The device is capable to operate in the input voltage range from 2.5V to 5.5V, and after start-up, the device is capable to operate down to 2.1V.

The output voltage of the Buck converter (BUCK) is programmable from 0.75V to 1.3V with 12.5mV per step, and the output current capability is up to 1.2A.

The SIDO converter of SGM3807 generates one positive power source and one negative power source, and each rail integrates a dedicated LDO to reduce the output ripple. The positive output (LDOP) is programmable from 6.0V to 11.3V with 100mV per step and up to 100mA load capability, while the negative output (LDON) is programmable from -26V to -16V with 25mV per step and up to 5mA load capability.

The SGM3807 is available in a Green WLCSP -2.05×2.35-20B package. The device operates over an ambient temperature range of -40℃ to +85℃.

APPLICATIONS

d-TOF Module
Wearable Micro LED Products

FEATURES

- 2.5V to 5.5V Input Voltage Range
- Input Low to 2.1V after Start-up
- Buck Converter (BUCK)
  - 1.4MHz Switching Frequency
  - 0.75V to 1.3V Output Voltage with 12.5mV Steps, ±1.1% Accuracy at PWM MODE
  - Up to 1.2A Output Current Capability
- SIDO Converter
  - LDOP: 6.0V to 11.3V Output Voltage with 100mV Steps, ±1.1% Accuracy, 10.3V V_{OUT} (Default)
  - LDOP: Up to 100mA Output Current Capability
  - LDON: -26V to -16V Output Voltage with 25mV Steps, ±1.1% Accuracy, -17V V_{OUT} (Default)
  - LDON: Up to 5mA Output Current Capability
  - 1.2MHz PWM Mode Switching Frequency
- Pulse-Skip Operation in Light Load Condition
- Programmability with I^2C Interface
  - Dynamic Voltage Scaling
  - Active Discharge
  - Internal Soft-Start Time to Limit Inrush Current
  - Turn-on/off Delay
- Dedicated Power Good
- Over-Temperature Protection (OTP)
- Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Available in a Green WLCSP-2.05×2.35-20B Package

TYPICAL APPLICATION

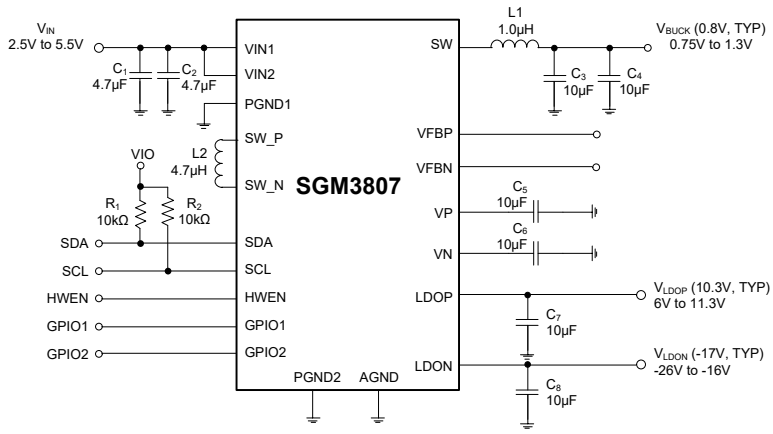


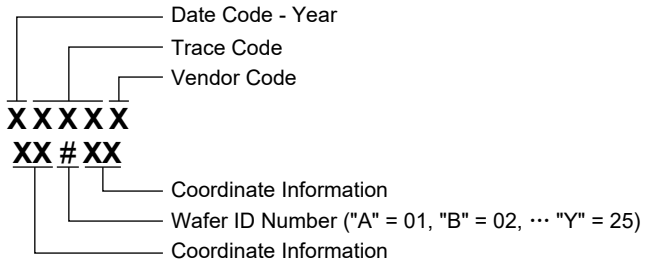
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3807	WLCSP-2.05×2.35-20B	-40℃ to +85℃	SGM3807YG/TR	3807 XXXXX XX#XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN1, VIN2, SCL, SDA, GPIO1, GPIO2 ..... -0.3V to 6V
SW, VFBP, VFBN, HWEN ..... -0.3V to 6V
SW (Transient: 10ns) ..... -1V to 8V
SW_P, VP, LDOP ..... -0.3V to 13.2V
SW_P (Transient: 10ns) ..... -2V to 15.2V
VN, LDON ..... -27V to 0.3V
SW_N ..... -27V to 6V
SW_N (Transient: 10ns) ..... -28V to 7V
Package Thermal Resistance
WLCSP-2.05×2.35-20B, θ_{JA} ..... 61.0℃/W
WLCSP-2.05×2.35-20B, θ_{JB} ..... 17.2℃/W
WLCSP-2.05×2.35-20B, θ_{JC} ..... 21.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{IN} ..... 2.5V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Extend to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

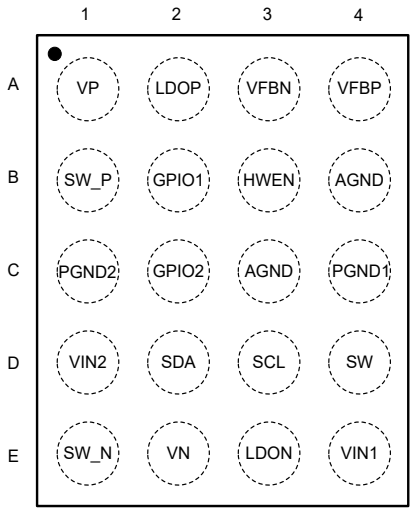
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

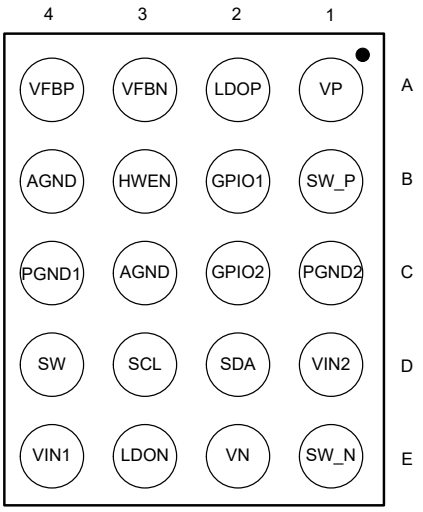
PIN CONFIGURATIONS

SGM3807 (TOP VIEW)



WLCSP-2.05×2.35-20B

SGM3807 (BOTTOM VIEW)



WLCSP-2.05×2.35-20B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	VP	P	SIDO Positive Output.
A2	LDOP	P	SIDO Positive LDO Output.
A3	VFBN	I	Buck DC/DC Output Voltage Negative Sense.
A4	VFBP	I	Buck DC/DC Output Voltage Positive Sense.
B1	SW_P	P	Switch Node of the SIDO DC/DC.
B2	GPIO1	O	Interrupt signal from the IC to the host, open-drain with active low.
B3	HWEN	I	Hardware Enable.
B4	AGND	G	Analog Ground.
C1	PGND2	G	Power Ground. Connect ground of input and output capacitors to this pin.
C2	GPIO2	I	Interrupt signal from external system to the IC.
C3	AGND	G	Analog Ground.
C4	PGND1	G	Power Ground. Connect ground of input and output capacitors to this pin.
D1	VIN2	I	Power Supply.
D2	SDA	I/O	I^2C Bus Data Line.
D3	SCL	I/O	I^2C Clock Data Line.
D4	SW	P	Switch Node of the Buck DC/DC.
E1	SW_N	P	Switch Node of the SIDO DC/DC.
E2	VN	P	SIDO Negative Output.
E3	LDON	P	SIDO Negative LDO Output.
E4	VIN1	I	Power Supply.

NOTE: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, all typical values are measured at T_J = +25℃, V_{IN} = 3.8V, V_{BUCK} = 0.8V, V_{LDOP} = 10.3V, V_{LDON} = -17V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General Features						
Input Voltage Range	V_{IN}		2.5		5.5	V
Under-Voltage Lockout Threshold	V_{UVLO_RISING}	V_{IN} rising	2.0	2.1	2.2	V
	$V_{UVLO\_FALLING}$	V_{IN} falling	1.9	2.0	2.1	V
Input Over-Voltage Lockout Threshold	V_{OVLO}		5.66	5.77	5.9	V
Input Over-Voltage Lockout Hysteresis	V_{OVLO_HYS}			95		mV
Power On Reset Threshold	V_{POR}		1.28	1.60	1.92	V
Power On Reset Threshold Hysteresis	V_{POR_HYS}			80		mV
VIN Supply Current	I_{Q_VIN}	HWEN = H or I2C_BIAS_EN = H and REGs_EN = H and no switching		63	110	μA
VP Supply Current	I_{Q_VP}			15	23	μA
VN Supply Current	I_{Q_VN}			10	13	μA
Chip Active but Rails are Off	$I_{Q\_STANDBY}$	HWEN = 0 and I2C_BIAS_EN = 1, OVLO, OT active		9	15	μA
Off Current	I_{Q_OFF}	V_{IN} < V_{POR}		0.7	2.0	μA
Shutdown Current	I_{Q_SHDN}	HWEN = 0, I^2C interface active		0.5	2.0	μA
Buck Converter (BUCK)						
Switching Frequency	f_{SW}			1400		kHz
Output Voltage Range	V_{BUCK}	12.5mV/step	0.75	0.8	1.3	V
Output Voltage Accuracy	V_{BUCK_ACC}	T_J = +25℃	-0.7		0.7	%
		T_J = -40℃ to +85℃	-1.1		1.1	%
Inductor Peak Current Limit	I_{PEAK1}	T_J = +25℃	1.9	2.3	2.7	A
SW MOSFET On-Resistance	R_{DSON1}	T_J = +25℃		90	120	mΩ
Rectifier On-Resistance	R_{DSON2}	T_J = +25℃		35	50	mΩ
Discharge Resistor of BUCK	R_{DIS1}			55		Ω
Over-Voltage Protection	$V_{BUCK\_OVP\_RISING}$	Above programmed output		145		mV
Power Good	$V_{BUCK\_PG\_RISING}$	Below programmed output		70		mV
	$V_{BUCK\_PG\_FALLING}$	Below programmed output		110		mV
Short-Circuit Detection Threshold	$V_{BUCK\_SCP\_FALLING}$			200		mV
Output Voltage Ripple	$BUCK_{RIPPLE}$	PWM Mode		10		mV
		Skip Mode		25		mV
Line Transient	$BUCK_{LINETRA}$	ΔV_{IN} = 0.5V, t_R/t_F = 10μs, I_{BUCK} = 300mA		25		mV
Line Regulation	$BUCK_{LINEREG}$	I_{BUCK} = 500mA, V_{IN} = 2.5V to 5.5V		1.2		mV
Load Transient	$BUCK_{LOADTRA\_OVERSHOOT}$	I_{BUCK} = 0mA to 300mA, t_R/t_F = 10μs		15		mV
	$BUCK_{LOADTRA\_UNDERSHOOT}$			70		mV
Load Regulation	$BUCK_{LOADREG}$	0mA ≤ I_{BUCK} ≤ 1200mA		8		mV
SIDO Converter (LDOP & LDON)						
Switching Frequency	f_{SW}			1200		kHz
Inductor Peak Current Limit	I_{PEAK}	T_J = +25℃	1.7	1.9	2.1	A

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, all typical values are measured at T_J = +25℃, V_{VIN} = 3.8V, V_{BUCK} = 0.8V, V_{LDOP} = 10.3V, V_{LDON} = -17V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Output Voltage Range (LDOP)	V_{LDOP}	100mV/step	6.0	10.3	11.3	V
Positive Output Voltage Accuracy (LDOP)	V_{LDOP_ACC}	T_J = +25℃	-0.9		0.9	%
		T_J = -40℃ to +85℃	-1.1		1.1	%
LDOP Maximum Current	I_{LDOP_MAX}		100			mA
Discharge Resistor of LDOP	R_{DIS2}			300		Ω
Over-Voltage Protection (1)	$V_{LDOP\_OVP\_RISING}$	Above programmed output		0.98		V
	$V_{LDOP\_OVP\_FALLING}$	Above programmed output		0.52		V
Power Good	$V_{LDOP\_PG\_RISING}$			90		%
	$V_{LDOP\_PG\_FALLING}$			85		%
Short-Circuit Detection Threshold	$V_{LDOP\_SCP\_FALLING}$			4.3		V
Output Voltage Ripple	$LDOP_{RIPPLE}$	PWM mode		6		mV
		Skip mode		35		mV
Line Transient	$LDOP_{LINETRA\_OVERSHOOT}$	ΔV_{IN} = 1V, t_R/t_F = 10μs, I_{LDOP} = 100mA		22		mV
	$LDOP_{LINETRA\_UNDERSHOOT}$			25		mV
Line Regulation	$LDOP_{LINEREG}$	I_{LDOP} = 100mA, I_{LDON} = 5mA, V_{IN} = 2.8V to 5.5V		7		mV
Load Transient	$LDOP_{LOADTRA\_OVERSHOOT}$	ΔI_{LDOP} = 0mA to 100mA, t_R/t_F = 10μs		55		mV
	$LDOP_{LOADTRA\_UNDERSHOOT}$			55		mV
Load Regulation	$LDOP_{LOADREG}$	0mA ≤ I_{LDOP} ≤ 100mA		10		mV
Negative Output Voltage Range (LDON)	V_{LDON}	25mV/step	-16	-17	-26	V
Negative Output Voltage Accuracy (LDON)	V_{LDON_ACC}	T_J = +25℃	-0.9		0.9	%
		T_J = -40℃ to +85℃	-1.1		1.1	%
LDON Maximum Current	I_{LDON_MAX}		5			mA
Discharge Resistor of LDON	R_{DIS3}			700		Ω
Over-Voltage Protection (1)	$V_{LDON\_OVP\_RISING}$	Below programmed output		-1.87		V
	$V_{LDON\_OVP\_FALLING}$	Below programmed output		-2.3		V
Power Good	$V_{LDON\_PG\_RISING}$			85		%
	$V_{LDON\_PG\_FALLING}$			90		%
Short Circuit Detection Threshold	$V_{LDON\_SCP\_RISING}$			-9.7		V
Output Voltage Ripple	$LDON_{RIPPLE}$	No load		35		mV
		Typical load		10		mV
Line Transient	$LDON_{LINETRA\_OVERSHOOT}$	ΔV_{IN} = 1V, t_R/t_F = 10μs, I_{LDON} = 5mA, I_{LDOP} = 100mA		30		mV
	$LDON_{LINETRA\_UNDERSHOOT}$			80		mV
Line Regulation	$LDON_{LINEREG}$	I_{LDON} = 5mA, V_{IN} = 2.8V to 5.5V		5		mV
Load Transient	$LDON_{LOADTRA\_OVERSHOOT}$	ΔI_{LDON} = 5mA, t_R/t_F = 10μs, V_{IN} = 2.5V to 5.5V		28		mV
	$LDON_{LOADTRA\_UNDERSHOOT}$			131		mV
Load Regulation	$LDON_{LOADREG}$	0mA ≤ I_{LDON} ≤ 5mA		25		mV

ELECTRICAL CHARACTERISTICS (continued)

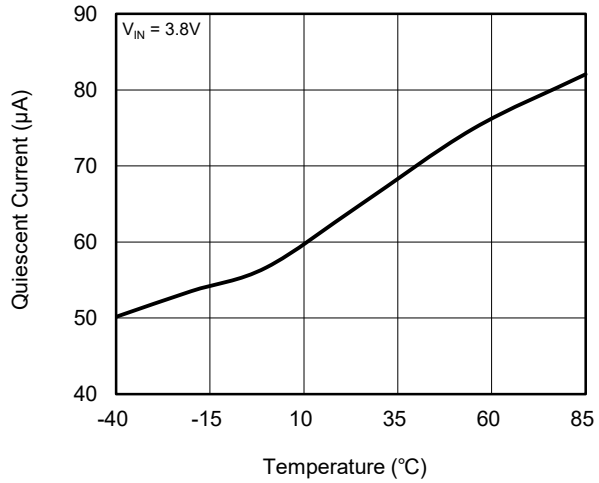
(T_J = -40℃ to +85℃, all typical values are measured at T_J = +25℃, V_{VIN} = 3.8V, V_{BUCK} = 0.8V, V_{LDOP} = 10.3V, V_{LDON} = -17V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Signals (SCL, SDA, HWEN, GPIO2, GPIO1)						
SCL Clock Frequency	f_{SCL}		100	400	1000	kHz
Low Level Input Voltage	V_{IL}				0.33	V
High Level Input Voltage	V_{IH}		0.80			V
SDA/GPIO1 Logic Output Low Level Voltage	V_{OL}	3mA sink			0.4	V
HWEN Pull-Down Resistance				0.9		MΩ
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}			140		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃
Short-Circuit Timer						
BUCK, LDOP Short-Circuit Detection Time in Start-up	t_{SCP}			2		ms
LDON Short-Circuit Detection Time in Start-up				4		ms
BUCK, LDOP, and LDON Short-Circuit Detection Time in Operation				0.85		ms
Efficiency						
Efficiency		I_{OUT_BST} = 50mA, I_{OUT_IBB} = -1mA, I_{OUT_BU} = 0.5A		85		%
RDSON_SIDO						
MN On-Resistance	R_{DSON_MN}	T_J = +25℃		110	150	mΩ
MP On-Resistance	R_{DSON_MP}	T_J = +25℃		500	560	mΩ
SP On-Resistance	R_{DSON_SP}	T_J = +25℃		260	300	mΩ

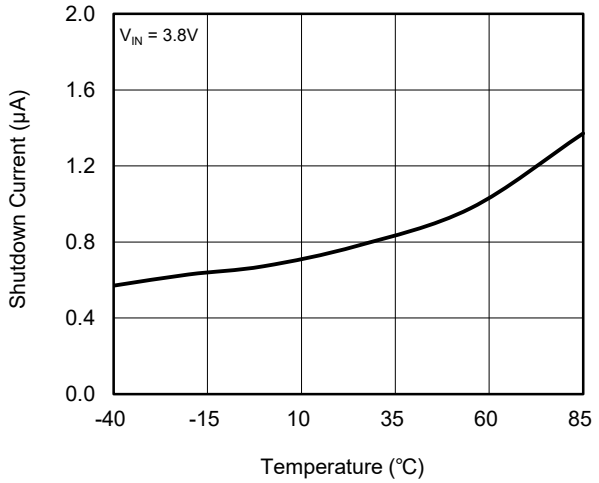
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

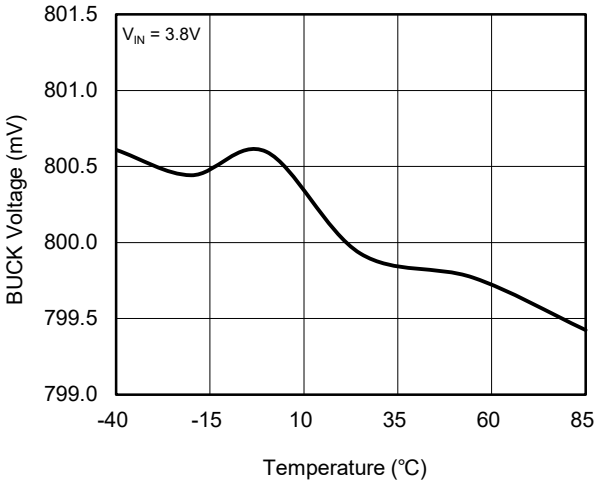
Quiescent Current vs. Temperature



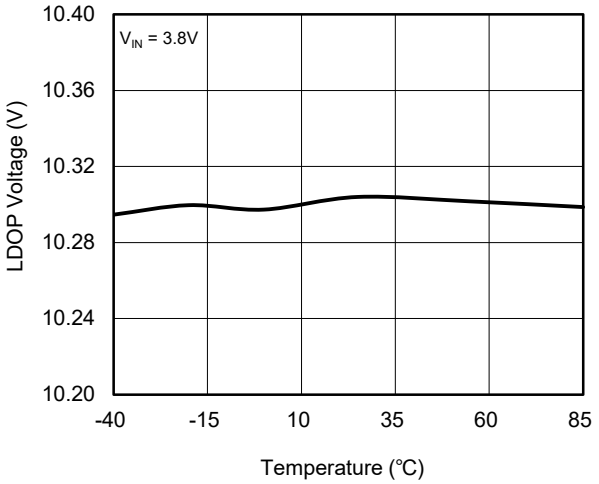
Shutdown Current vs. Temperature



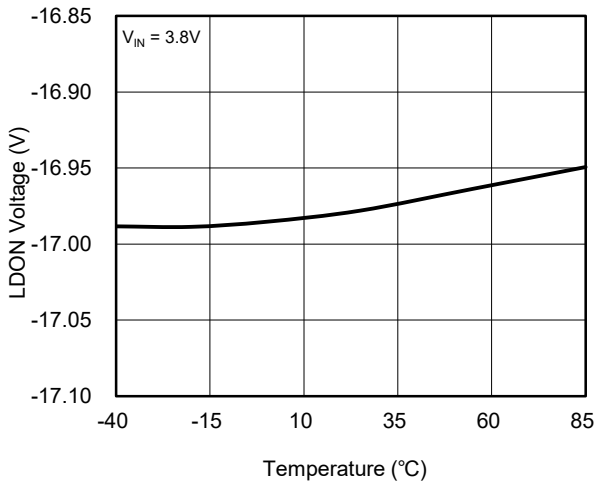
BUCK Voltage vs. Temperature



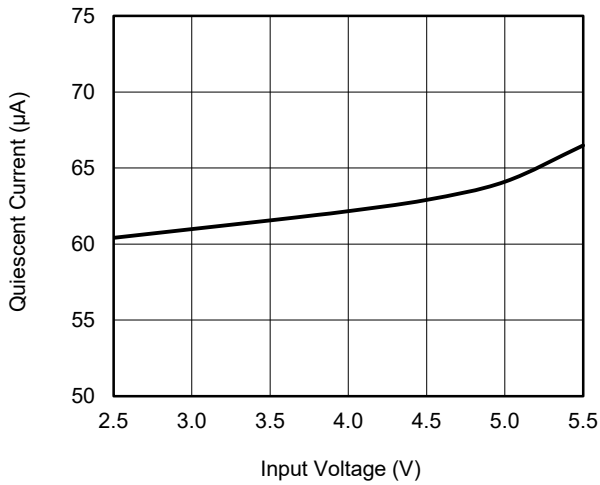
LDOP Voltage vs. Temperature



LDON Voltage vs. Temperature



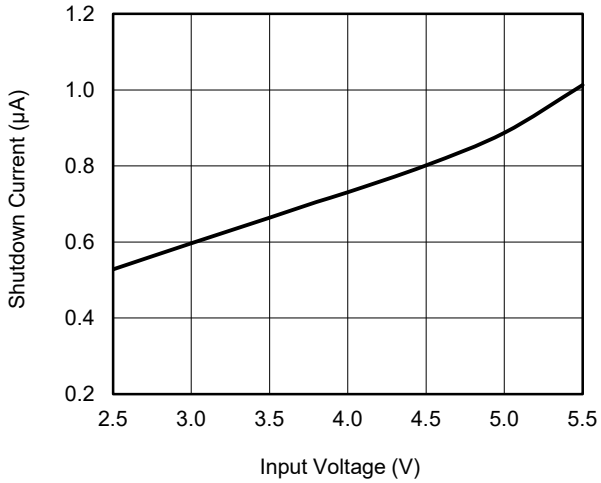
Quiescent Current vs. Input Voltage



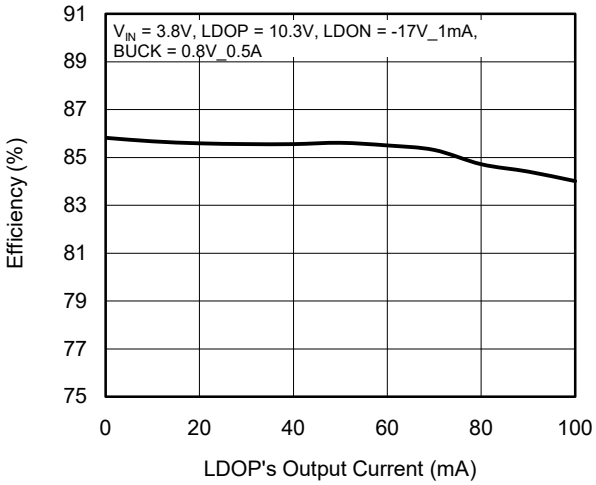
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

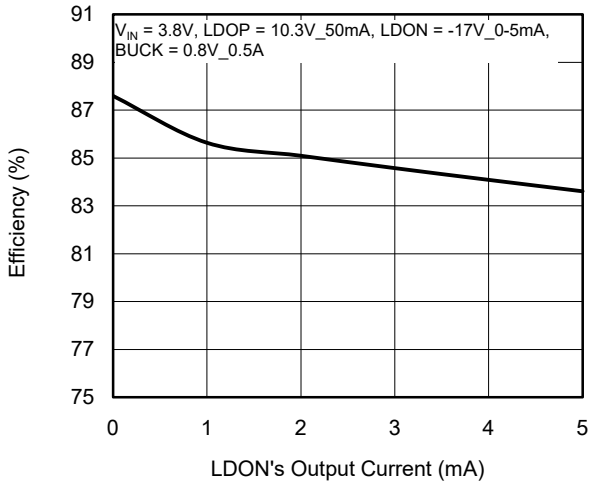
Shutdown Current vs. Input Voltage



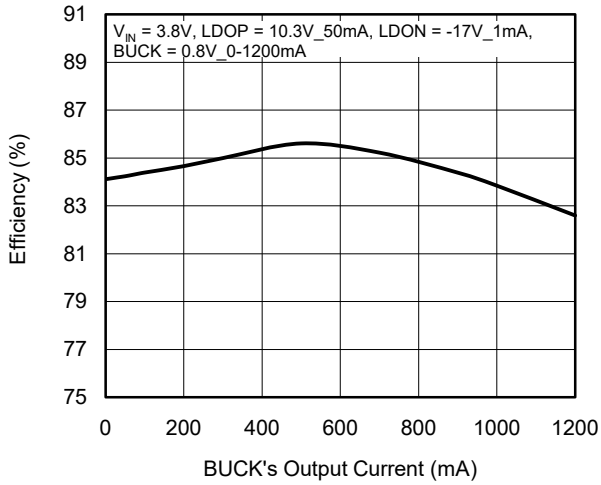
Efficiency vs. LDOP's Output Current



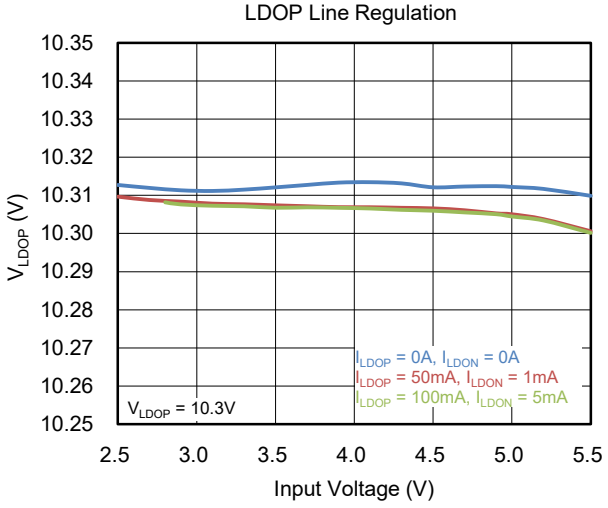
Efficiency vs. LDON's Output Current



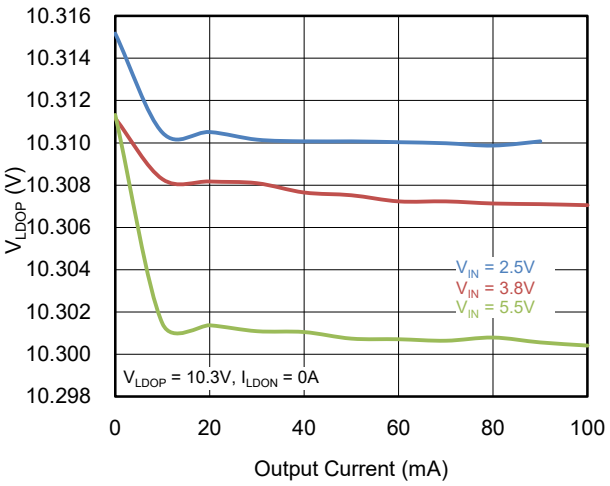
Efficiency vs. BUCK's Output Current



LDOP Line Regulation



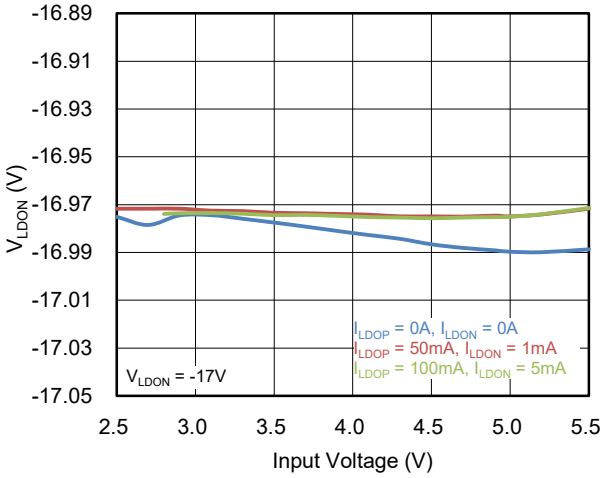
LDOP Load Regulation



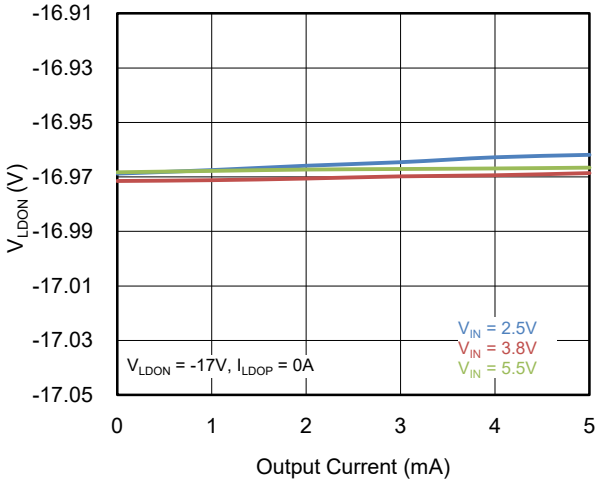
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

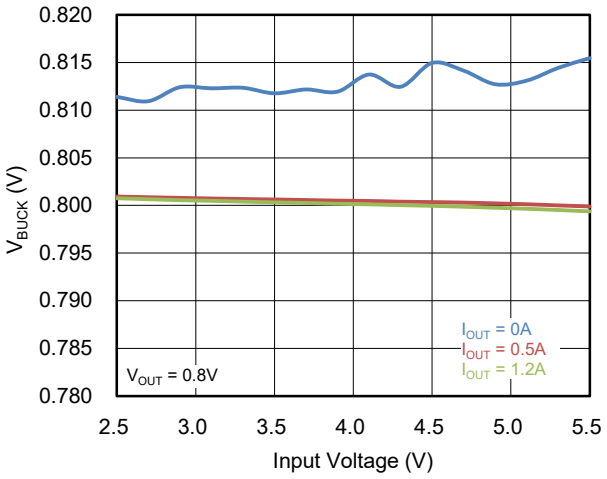
LDON Line Regulation



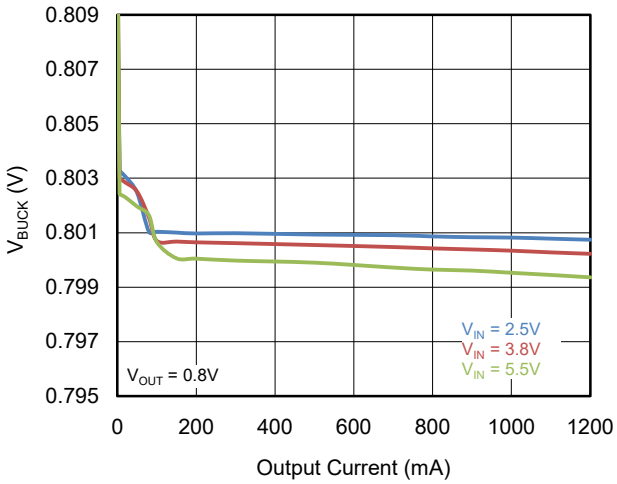
LDON Load Regulation



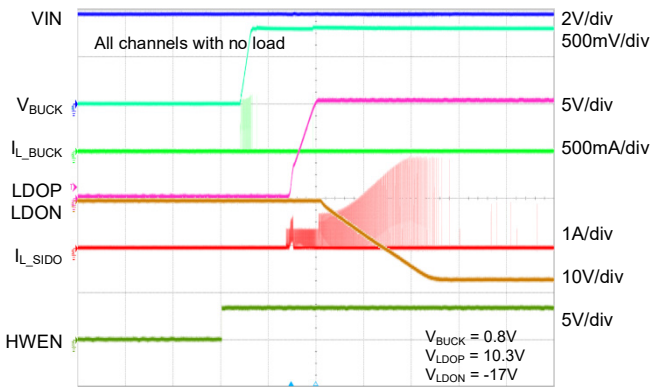
BUCK Line Regulation



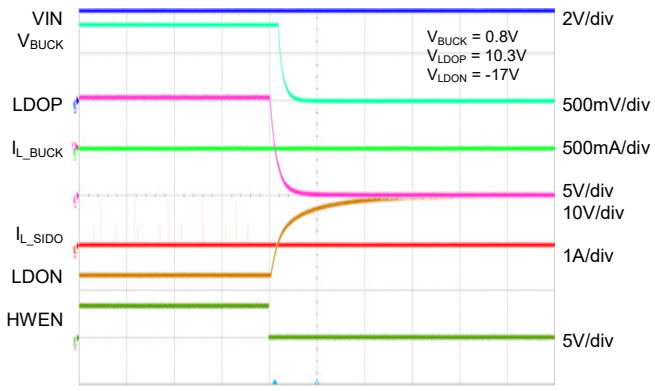
BUCK Load Regulation



Start-up Sequence with Hardware Enable (HWEN On)



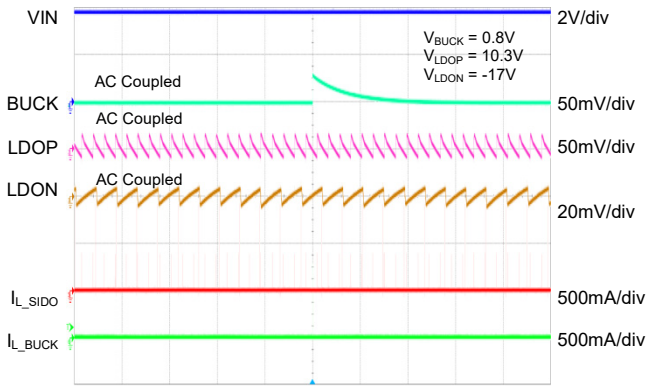
Start-up Sequence with Hardware Enable (HWEN Off)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

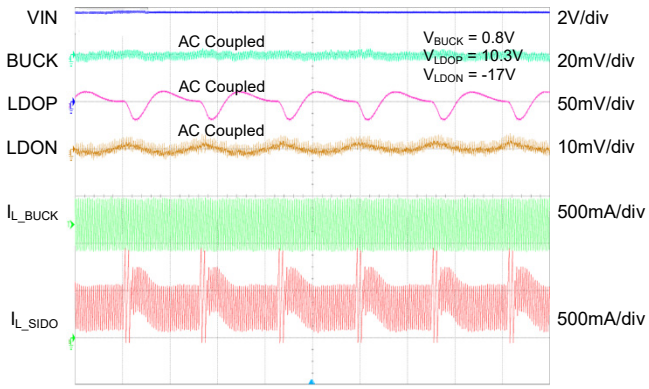
V_{IN} = 3.8V, unless otherwise noted.

Output Ripple at No Load



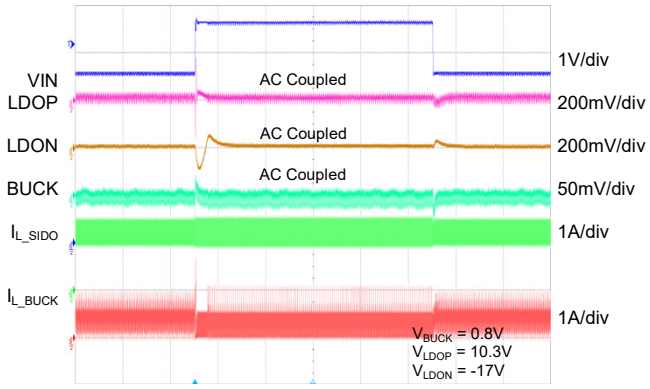
Time (20ms /div)

Output Ripple at Full Load



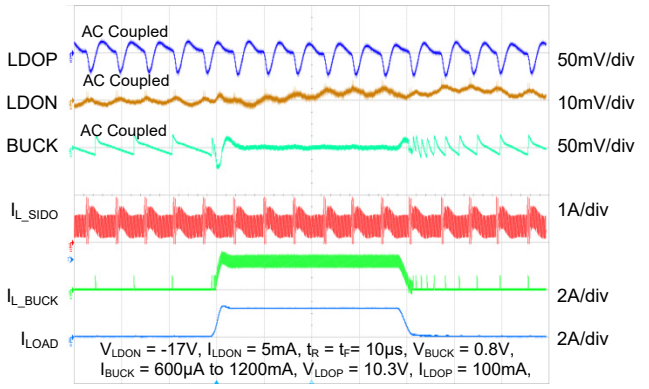
Time (20μs/div)

Line Transient



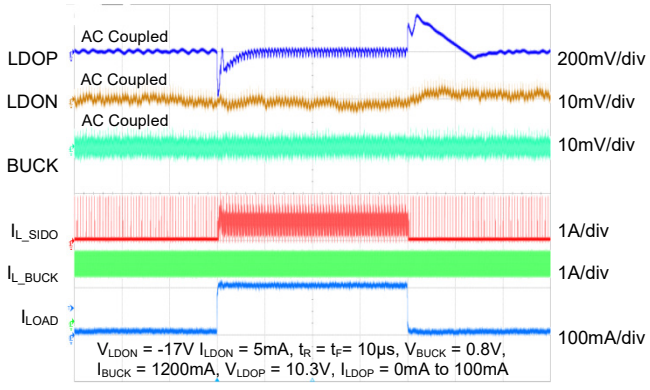
Time (1ms /div)

BUCK Load Transient



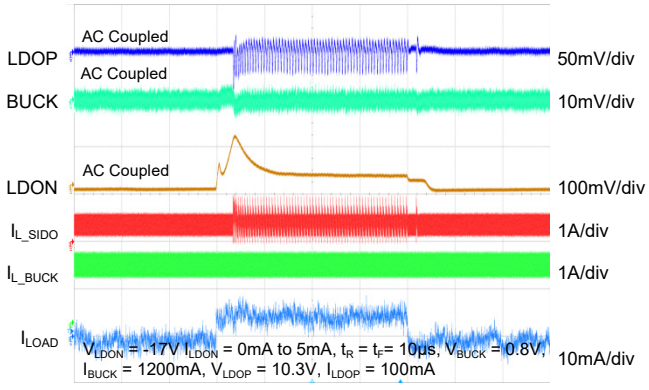
Time (50μs /div)

LDOP Load Transient



Time (500μs /div)

LDON Load Transient

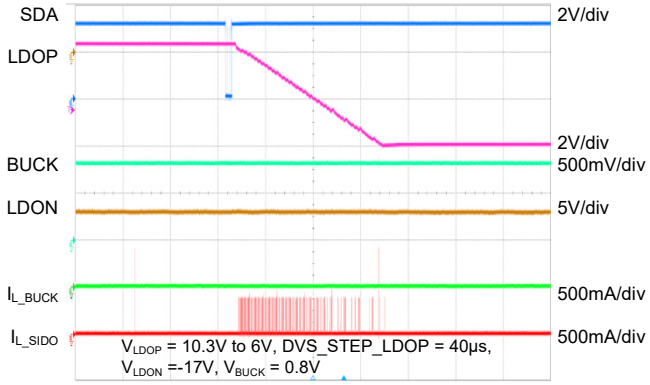


Time (500μs /div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

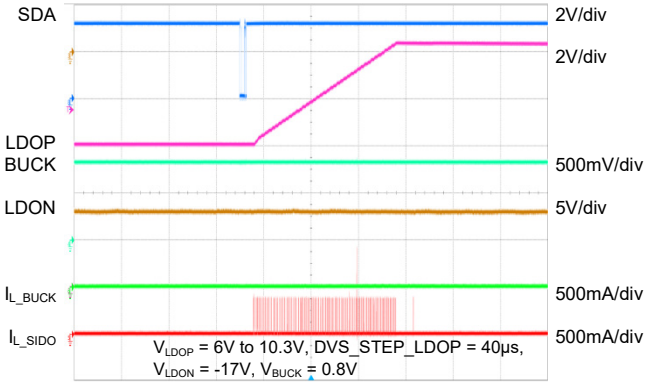
V_{IN} = 3.8V, unless otherwise noted.

LDOP DVS



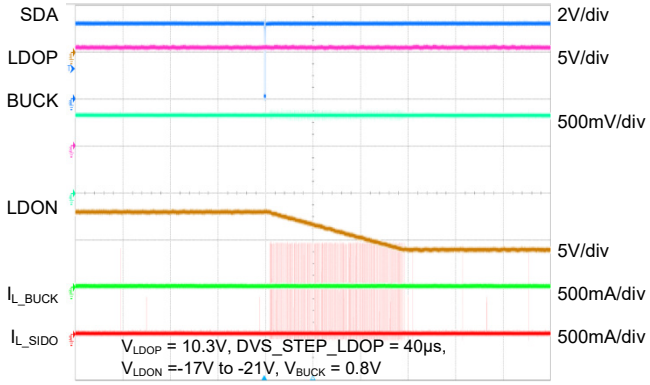
Time (500μs/div)

LDOP DVS



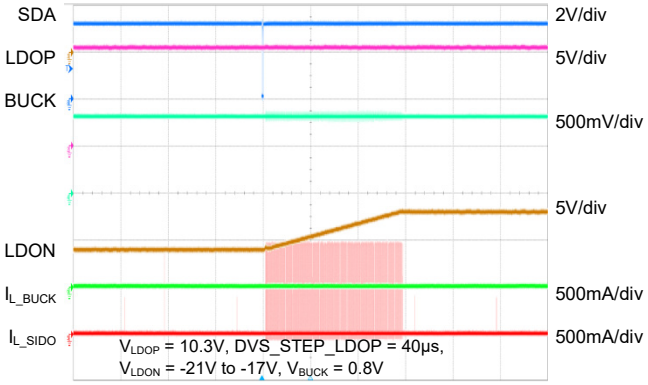
Time (500μs/div)

LDON DVS



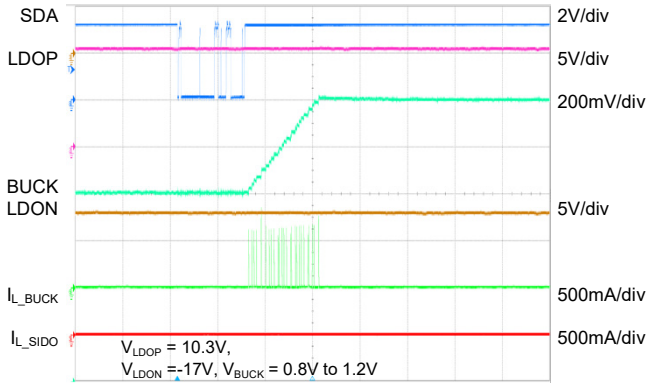
Time (2ms/div)

LDON DVS



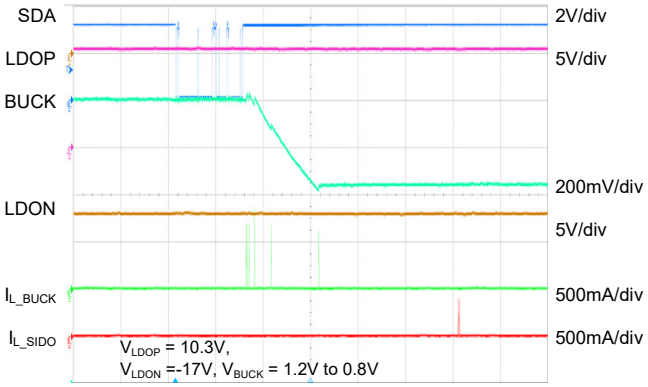
Time (2ms/div)

BUCK DVS



Time (50μs/div)

BUCK DVS

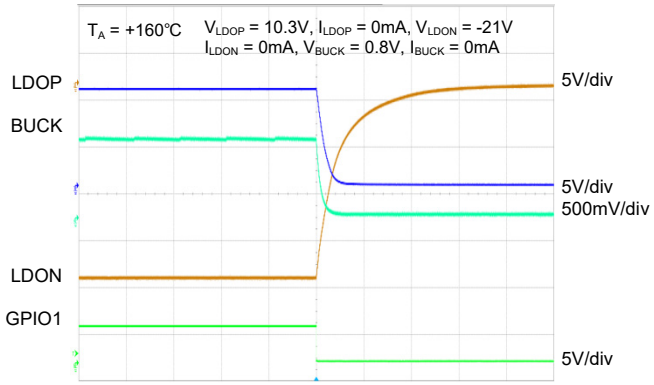


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

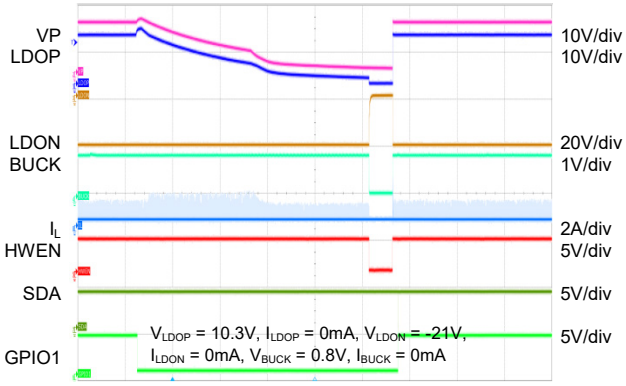
V_{IN} = 3.8V, unless otherwise noted.

OTP Sequence



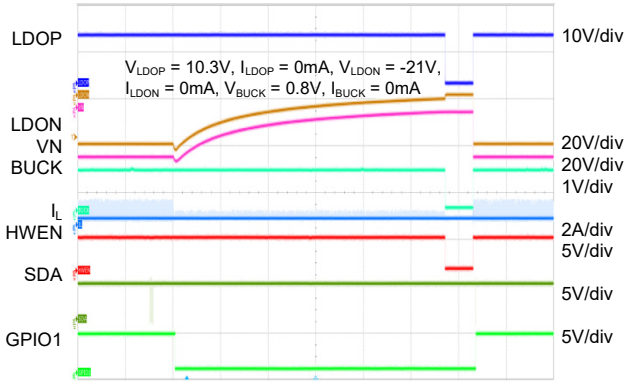
Time (10ms/div)

LDOP OVP with Shutdown Mode



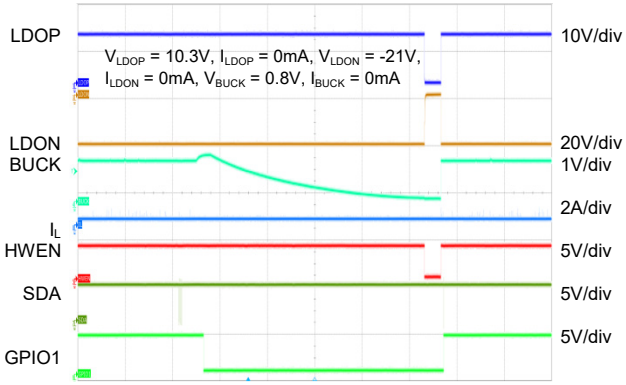
Time (1s/div)

LDON OVP with Shutdown Mode



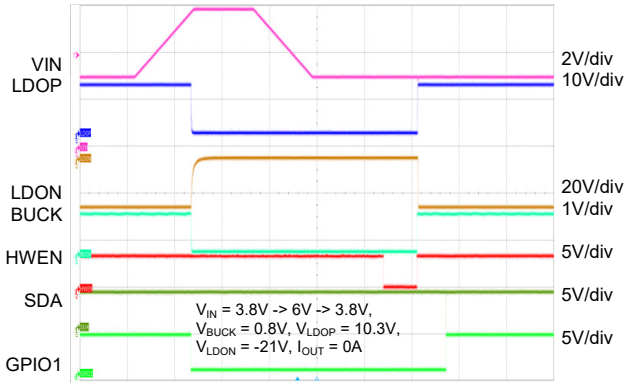
Time (2s/div)

BUCK OVP with Shutdown Mode



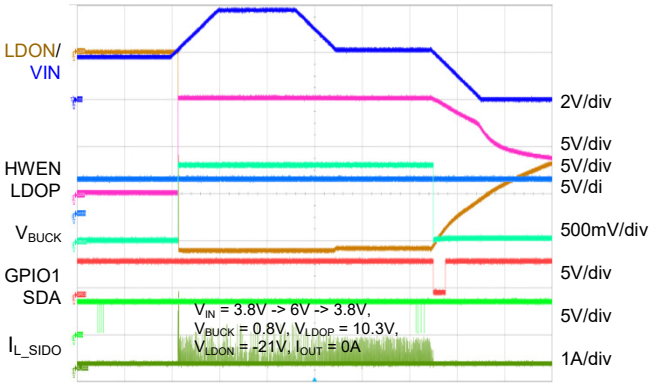
Time (2s/div)

OVLO Sequence



Time (200ms/div)

UVLO Sequence

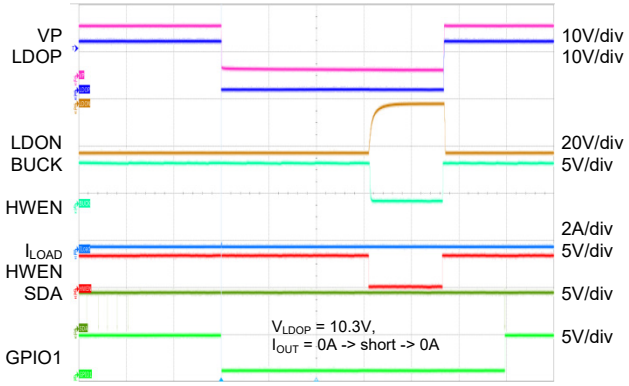


Time (200ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

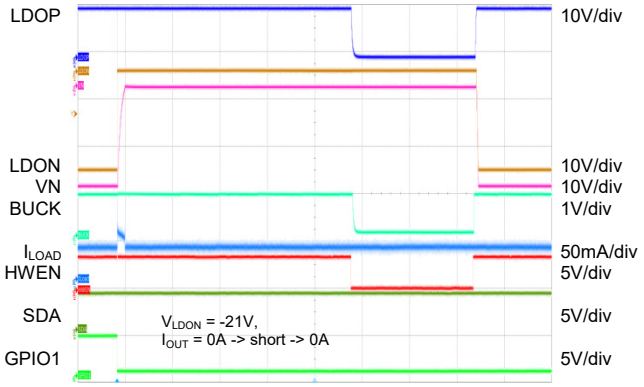
V_{IN} = 3.8V, unless otherwise noted.

LDOP SCP with Shutdown Mode



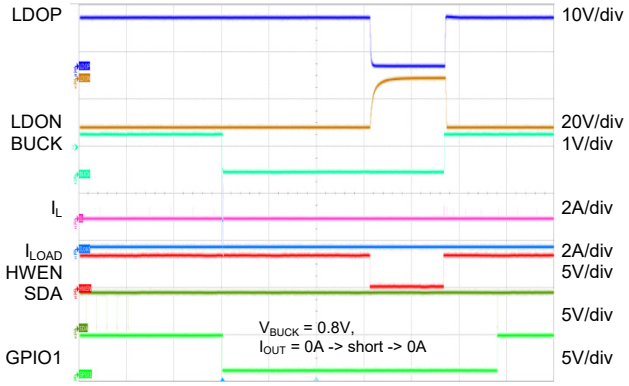
Time (100ms/div)

LDON SCP with Shutdown Mode



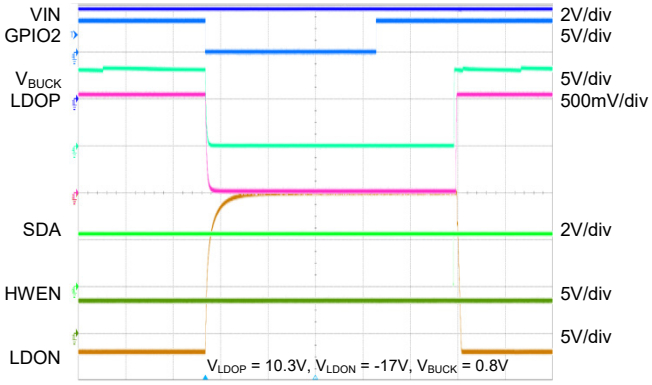
Time (60ms/div)

BUCK SCP with Shutdown Mode



Time (100ms/div)

GPIO2 Event Sequence



Time (50ms/div)

FUNCTIONAL BLOCK DIAGRAM

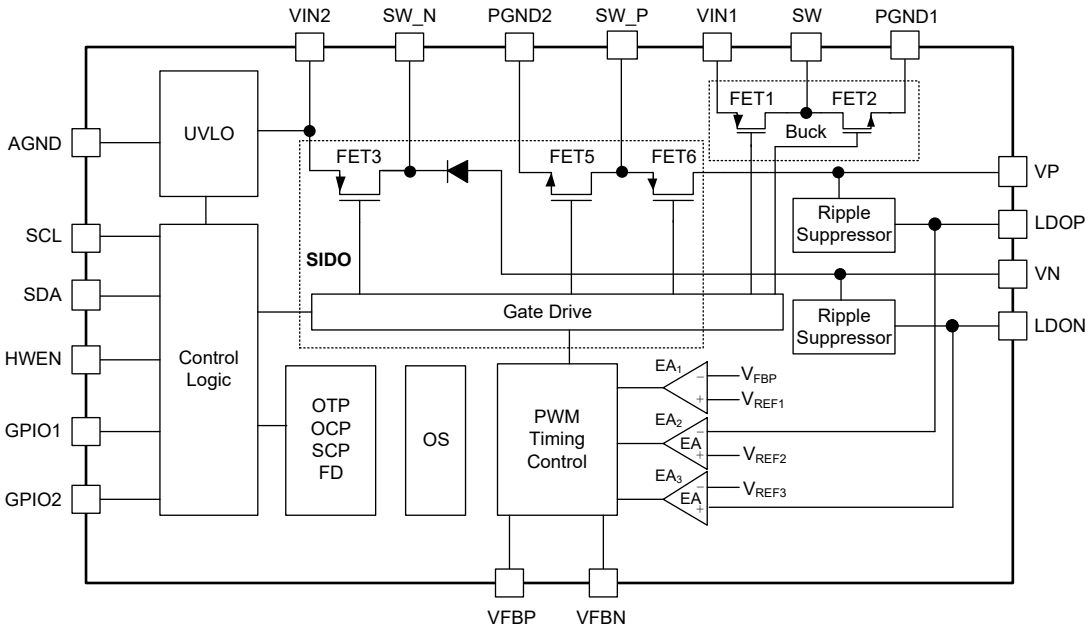


Figure 2. Functional Block Diagram

RECOMMENDED COMPONENTS OF TEST CIRCUITS

Table 1. Recommended BOM for Typical Applications

Reference	Quantity	Description	Part Number	Package	Supplier
L_1	1	4.7μH	DFE252012F-4R7M=P2	2520	Murata
L_2	1	1μH	DFE201610E-IR0M=P2	0806	Murata
C_{VP}	1	10μF	GRM21BR6YA106KE43L	0805	Murata
C_{VN}	1	10μF	CL31B106KBHNNNE	1206	Samsung
C_{LDOP}	1	10μF	GRM21BR6YA106KE43L	0805	Murata
C_{LDON}	1	10μF	CL31B106KBHNNNE	1206	Samsung
C_{BUCK}	2	10μF	GRM155R60J106ME15	0402	Murata
C_{IN1}	1	4.7μF	GRM155R60J475ME47	0402	Murata
C_{IN2}	1	4.7μF	GRM155R60J475ME47	0402	Murata

DETAILED DESCRIPTION

The SGM3807 is a high-performance, dedicated compact power PMIC that provides all the necessary power rails for single dToF module. A proprietary architecture is developed to achieve excellent regulation between two rails, which is considered as a common drawback when using single inductor to generate the two rails. The circuit maintains regulation on all rails without compromising performance in either Boost or inverter operation with any loading condition. In addition to the SIDO power stage, the device integrates a high efficiency COT synchronous Buck converter and operates with a nominal 1.4MHz switching frequency.

Buck Regulation

The integrated high-performance synchronous Buck converter operates with 1.4MHz (TYP) switching frequency and supports up to 1.2A load current. COT control architecture is implemented to provide excellent load and line transient performance.

The device supports output voltage DVS function via I^2C, where the output voltage is programmable from 0.75V to 1.3V with 12.5mV increment.

Buck Output Remote Sense

The Buck DC/DC also supports remote sense function, where the actual load is far away from the SGM3807.

VFBP and VFBN pins are connected to the Buck's internal error amplifier to provide feedback of the output voltage for regulation. The VFBP and VFBN pins are connected to the actual load's positive and negative terminals respectively.

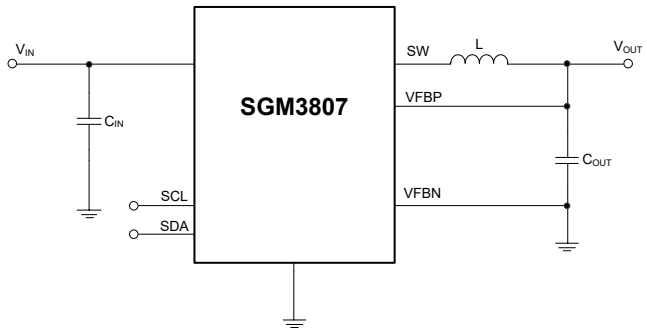


Figure 3. Buck Remote Sense

To ensure the Buck DC/DC stability, the minimal of 4μF effective output capacitance is recommended. For better load transient and output ripple performance, 16μF or higher effective output capacitance is recommended.

SIDO Regulation

The device integrates a single inductor dual-output (SIDO) DC/DC converter to provide a positive output voltage from 6.3V to 11.6V with 100mV adjustment step via I^2C, and a negative output voltage from -26.3V to -16.3V. Both rails support DVS function via I^2C. Each of the SIDO output rail integrates a LDO to reduce the output voltage ripple.

The proprietary architecture ensures excellent output voltage regulation, load and line transient performance of both positive and negative with a single inductor.

SIDO LDO

Each SIDO rail integrates a dedicated LDO to achieve excellent output voltage ripple and transient performance. Each LDO has dedicated current limit to support individual SIDO rail's short protection while not affecting the operation of the non-shorted rail.

Dynamic Voltage Scaling (DVS)

The SGM3807 implements dynamic voltage scaling on all three rails. The LDOP supports 100mV per step adjustment via REG0x00. The LDON supports 25mV per step adjustment via REG0x01 and REG0x02. The BUCK supports 12.5mV per step adjustment via REG0x03.

The SGM3807 also supports DVS slew rate adjustment of LDOP and LDON via REG0x11. The slew rate register configures both the voltage up and voltage down simultaneously.

DETAILED DESCRIPTION (continued)

Soft-Start, Start-up and Shutdown

The soft-start time of each rail is programmable via REG0x05. The SGM3807 supports 2 start-up control types, one is to start-up with toggling HWEN pin, and the other is controlling the individual rail's start-up via I^2C register settings. I^2C_BIAS_EN bit serves as the global I^2C start-up/shutdown control, and each rail has an individual enable bit in REG0x0F. Below is a start-up and shutdown truth table that summarizes the 2 control types:

Table 2. Start-up Control

HWEN	I^2C_BIAS_EN	I^2C_Regs_EN	On/Off DLY	Start Rail	Turn-off Rail
0-1	X	0	YES	YES	NO
0-1	X	1	NO	YES	NO
1-0	X	0	YES	NO	YES
1-0	1	1	NO	NO	NO
1-0	0	1	NO	NO	YES
0	0-1	0	NO	NO	NO
0	0	1	NO	NO	NO
0	1	1	NO	YES	NO
0	1	1-0	NO	NO	YES
0	1-0	1	NO	NO	YES

NOTE: I^2C_REGS_EN represents the enable signal for each rail.

In above truth table, the I^2C register programmed turn-on and turn-off delays is only enabled by toggling HWEN, and is independent of I^2C_BIAS_EN signal. If HWEN is pulled to logic low, I^2C_BIAS_EN and I^2C_REGS_EN will control the turn-on/off of individual rail, and I^2C programmable turn-on/off is not engaged.

The device implements I^2C programmable soft-start time via REG0x05. Regardless of HWEN or I^2C control, the individual rail will follow the programmed soft-start time to ramp the voltage towards programmed output voltage target.

For HWEN start-up, the device has a 700μs (TYP) delay time before performing the register programmed individual rail start-up delay.

Under-Voltage Lockout (UVLO)

The device is capable to operate from 2.5V to 5.5V input range, and after start-up, the device can work down to 2.1V with 1ms.

Input Over-Voltage Lockout (OVLO)

The SGM3807 implements input over-voltage protection. When the input voltage exceeds 5.77V (TYP), the device's all 3 rails stop switching immediately. The input OVP function has a 95mV (TYP) hysteresis, the OVLO_STATUS bit will toggle to logic low.

OVLO is a global fault condition, the host needs to restart the device via either HWEN or I^2C_EN based on the OVLO_STATUS signal.

Over-Current Protection (OCP)

The SGM3807 implements over-current protection on all three rails. The SIDO has an overall 1.9A (TYP) switch current limit. The BUCK rail implements a 2.3A (TYP) peak current limit, and the current limit is programmable via REG0x04. When OCP is triggered, corresponding rail's OCP_Status and OCP_Interrupt will toggle high.

Over-Temperature Protection (OTP)

The SGM3807 includes an OTP feature to prevent excessive power dissipation from overheating these devices. The OTP will shut down switching operation when the junction temperature exceeds +140℃. Once the junction temperature cools down by approximately 15℃, the OT_STATUS bit will toggle to logic low.

OTP is a global fault condition. The host needs to restart the device via either HWEN or I2C_EN based on the OTP_STATUS signal.

DETAILED DESCRIPTION (continued)

Short-Circuit Protection (SCP)

When the output voltage on LDOP drops below 4.3V or LDON rises above -9.7V, or BUCK rail's output voltage drops below 200mV, the SGM3807 enters short-circuit protection mode. During start-up, when the LDOP output voltage is unable to reach above 4.3V of the programmed voltage or LDON output voltage is unable to drops below -9.7V of the programmed voltage or BUCK output voltage is unable to reach above 200mV, after 2ms (TYP), the corresponding voltage rail is determined as short.

If any rail is shorted, the voltage rail will stop switching, and corresponding fault flag will be updated in the register.

The device needs to wait for the host to restart the device via either HWEN or I^2C_BIAS_EN. SCP_STATUS bit will toggle low when either HWEN or I^2C_BIAS_EN is toggled to logic low.

Output Over-Voltage Protection (OVP)

The device implements output over-voltage protection on all 3 rails. The BUCK rail implements a fixed 145mV (TYP) above programmed output voltage as the OVP threshold, and the OVP hysteresis is 46mV (TYP). Once OVP is triggered on any voltage rail, the corresponding voltage rail will stop switching, and corresponding register bit will flag this event.

LDON has a fixed 2.1V below the programmed output voltage as the OVP threshold. LDOP has a fixed 1V above the programmed output voltage as the OVP threshold.

Output Discharge

The device implements I^2C programmable output voltage discharge via REG0x0F. When either HWEN or I^2C_BIAS_EN/ I^2C_REGS_EN toggles low, it will enable the output voltage discharge. The LDOP and LDON implement the 300Ω and 700Ω discharge resistors respectively and the BUCK rail implements a 55Ω discharge resistor.

In addition, the SGM3807 turns on the output discharge when SCP or OVP occurs.

GPIO1

The SGM3807 offers an active low GPIO1 pin as an interrupt signal to notice the host if any interrupt bit is toggled high. When all the interrupts are cleared by the host, the GPIO1 will automatically toggles to logic high. And the GPIO1 will be automatically pulled high after reading REG0x0B and REG0x0C.

GPIO2

The SGM3807 offers an active low GPIO2 pin as an input to receive signal from external host. GPIO2 triggers logic low will also create an interrupt signal on GPIO1. The events below will occur when GPIO2 pin goes from logic high to low:

- GPIO2 interrupt/status event is created and a forced disabled register is set to high.
- SGM3807 is forced disabled. To re-enable the device, GPIO2 needs to be pulled to logic high first and forced disabled register has to be written with "0" from the I^2C interface.

GPIO2 has the highest priority over other commanding signals. GPIO2 toggle will clear the latch signal of SCP and OVP. If the device is in SCP hiccup mode, GPIO2 will also terminate the hiccup.

DETAILED DESCRIPTION (continued)

I²C Slave Address

The SGM3807 offers 3 bits OTP option for the device slave address. The default slave address is REG0x40, the first 3 bits of MSB is programmable and the remaining bit is 0. The default slave address is REG0x40.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3807 parameters and get status reports. I²C is well known for 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named as serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is the master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3807 operates as a slave device with address REG0x40. It has eighteen 8-bit registers, numbered from REG0x00 to REG0x11. A register read beyond REG0x11 returns REG0xFF.

Physical Layer

The SGM3807 supports I²C standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (up to 1000kbit/s) communication speeds. Bus lines are pulled high by weak current source or pull-up resistors and in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 4. All transactions are started by the master that applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

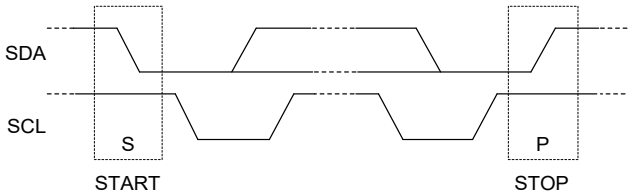


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the high period of the clock. The state of the SDA can only change when the clock (SCL) is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

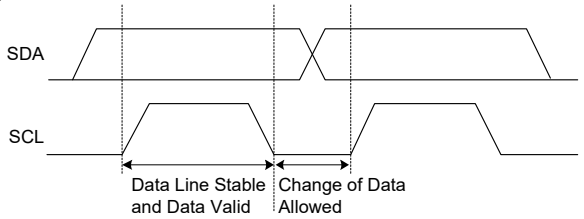


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the most significant bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

DETAILED DESCRIPTION (continued)

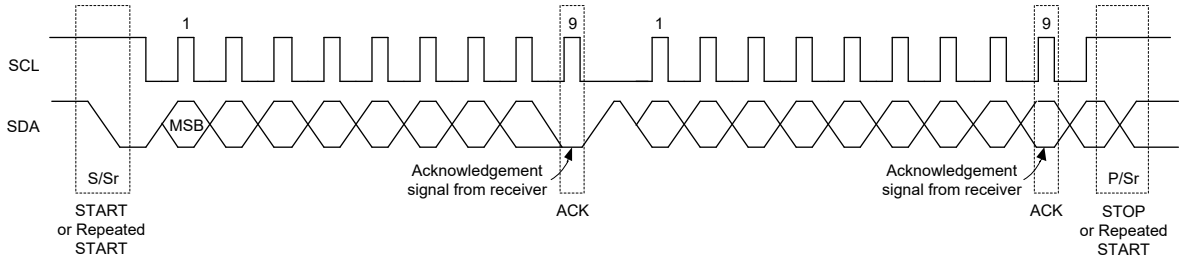


Figure 6. Byte Transfer Process

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte was received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including the acknowledge clock pulse. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address and then without a stop condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

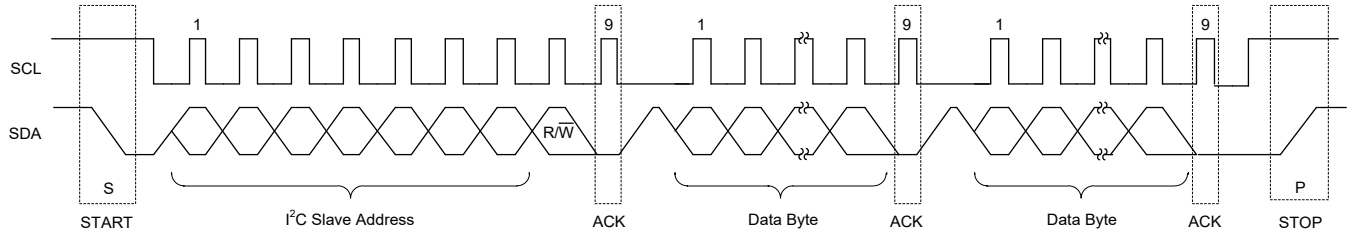


Figure 7. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

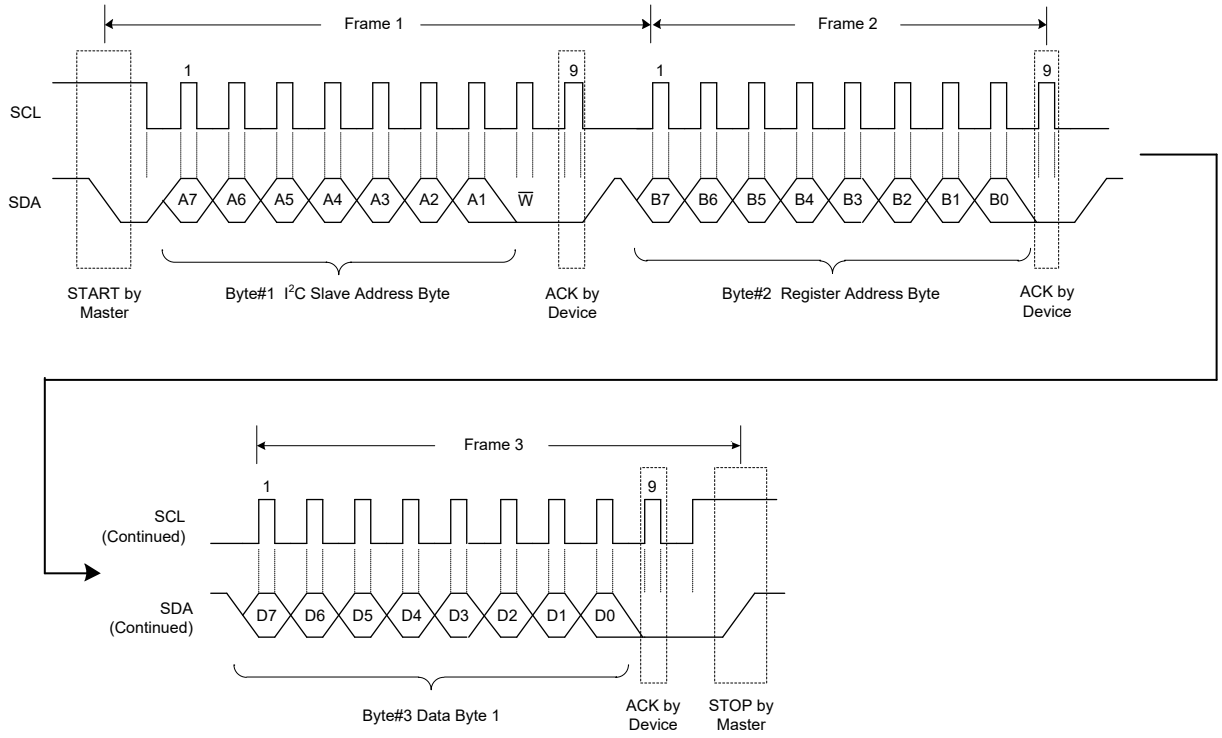


Figure 8. A Single Write Transaction

DETAILED DESCRIPTION (continued)

READ: If the master wants to read a single register (Figure 9), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

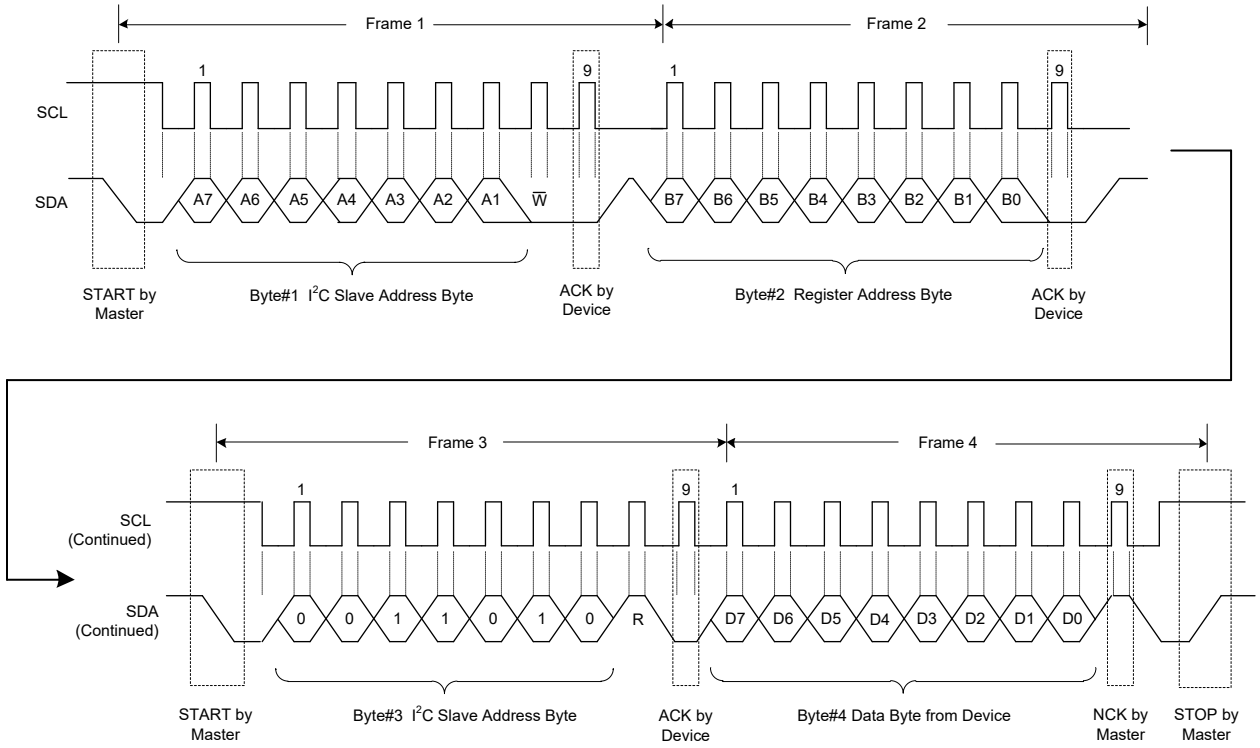


Figure 9. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3807 for REG0x00 through REG0x11 registers. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave to send the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

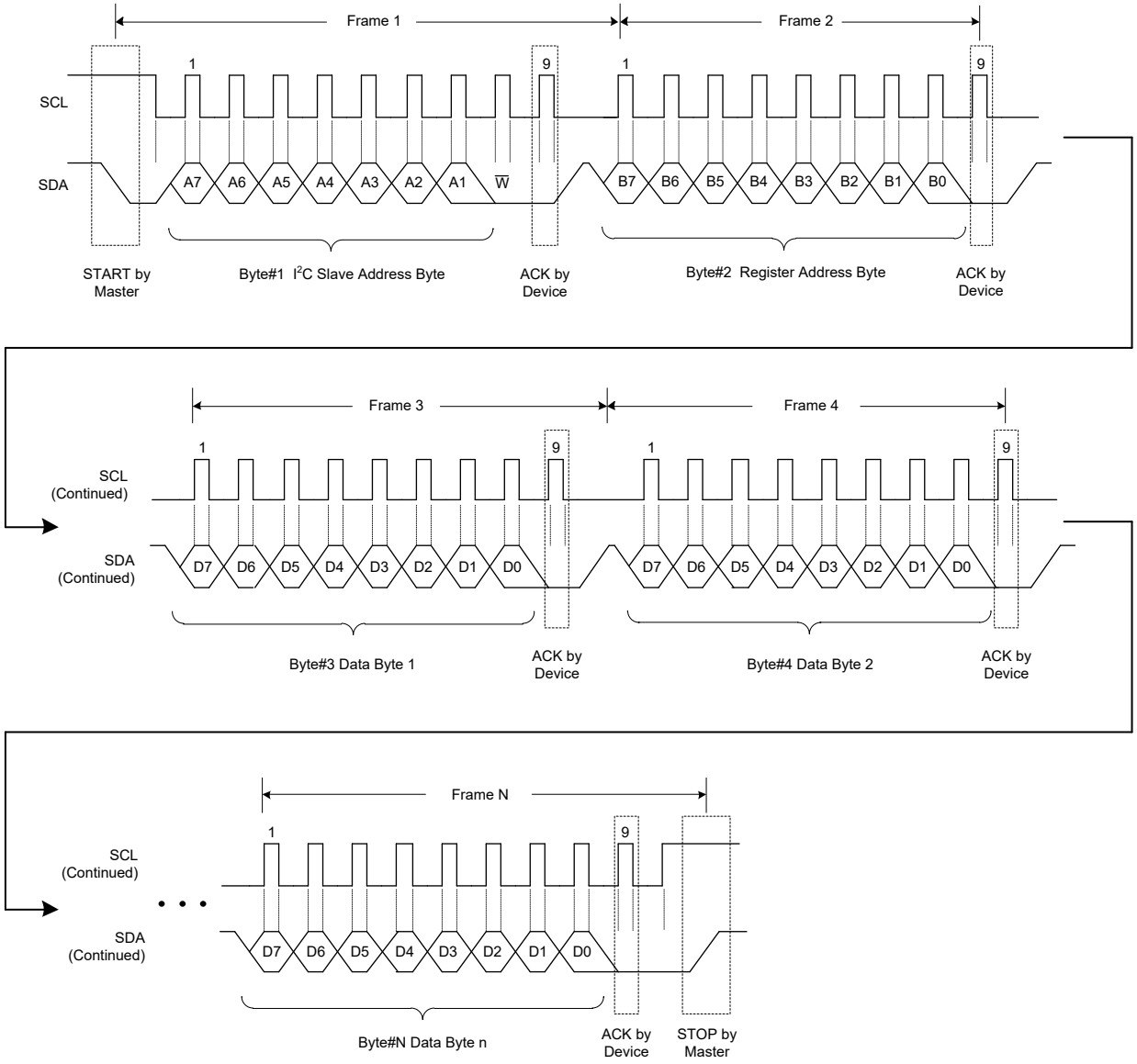


Figure 10. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

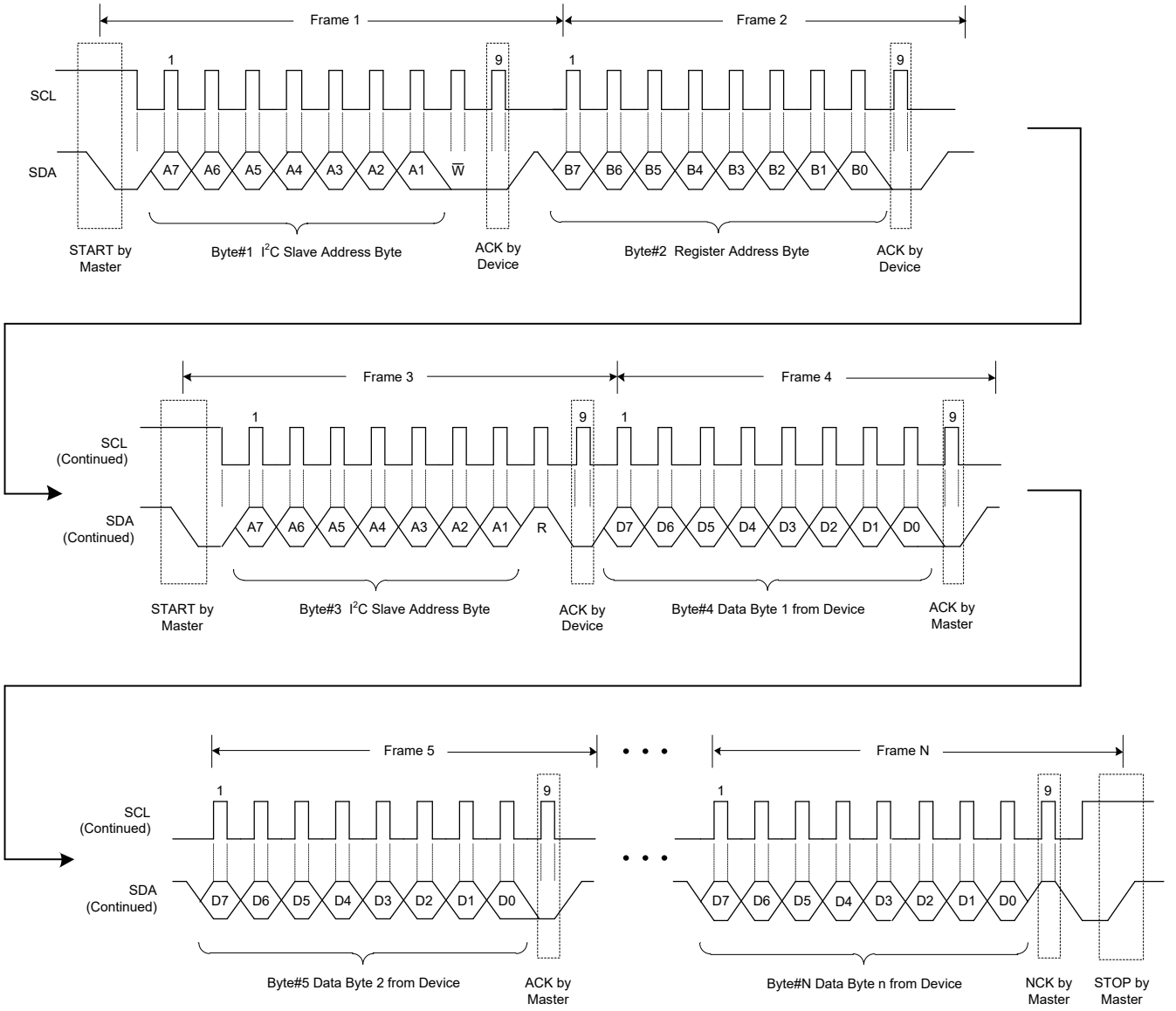


Figure 11. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I^2C Slave Address of SGM3807: 0x40

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	LDOP_VOUT	Reserved		LDOP [5:0]					
0x01	LDON1_VOUT	LDON1 [7:0]							
0x02	LDON2_VOUT	LDON2	Reserved						
0x03	BUCK_VOUT	Reserved		BUCK VOUT [5:0]					
0x04	BUCK_ILIM	Reserved				BUCK_ILIM [3:0]			
0x05	Soft-Start_Timing	Reserved	LOCK	LDOP_SS [5:4]		LDON_SS [3:2]		BUCK_SS [1:0]	
0x06	LDOP ON/OFF Delay	LDOP_ON_DLY [7:4]				LDOP_OFF_DLY [3:0]			
0x07	LDON ON/OFF Delay	LDON_ON_DLY [7:4]				LDON_OFF_DLY [3:0]			
0x08	BUCK ON/OFF Delay	BUCK_ON_DLY [7:4]				BUCK_OFF_DLY [3:0]			
0x09	Status 1	LDOP_OCP	LDON_OCP	BUCK_OCP	LDOP_OVP	LDON_OVP	BUCK_OVP	LDOP_SHORT	LDON_SHORT
0x0A	Status 2	BUCK_SHORT	LDOP_PG	LDON_PG	BUCK_PG	VIN_OVLO	VIN_UVLO_B	TSD	GPIO2
0x0B	Interrupt 1	LDOP_OCP_INT	LDON_OCP_INT	BUCK_OCP_INT	LDOP_OVP_INT	LDON_OVP_INT	BUCK_OVP_INT	LDOP_SHORT_INT	LDON_SHORT_INT
0x0C	Interrupt 2	BUCK_SHORT_INT	LDOP_PG_B_INT	LDON_PG_B_INT	BUCK_PG_B_INT	VIN_OVLO_INT	VIN_UVLO_INT	TSD_INT	GPIO2_B_INT
0x0D	Interrupt 1 Mask	LDOP_OCP_MASK	LDON_OCP_MASK	BUCK_OCP_MASK	LDOP_OVP_MASK	LDON_OVP_MASK	BUCK_OVP_MASK	LDOP_SHORT_MASK	LDON_SHORT_MASK
0x0E	Interrupt 2 Mask	BUCK_SHORT_MASK	LDOP_PG_B_MASK	LDON_PG_B_MASK	BUCK_PG_B_MASK	VIN_OVLO_MASK	VIN_UVLO_MASK	TSD_MASK	GPIO2_B_MASK
0x0F	MODE1	GPIO2_EN	LDOP_DISCHG	LDON_DISCHG	BUCK_DISCHG	I2C_BIAS_EN	LDOP_EN	LDON_EN	BUCK_EN
0x10	MODE2	SOFT-RST	Reserved						FORCED_DIS
0x11	DVS_SLEW_RATE	Reserved	Reserved	DVS_SLEW_RATE_LDON [5:3]			DVS_SLEW_RATE_LDOP [2:0]		

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit.

W/C: Writing a ‘0’ clears the bit. Writing a ‘1’ has no effect.

REGISTER MAPS (continued)

REG0x00: LDOP Register [Reset = 0x2C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R/W	Reserved	Soft-rst
D[5:0]	LDOP [5:0]	101100	R/W	LDOP Adjustment 000001 = 6.0V 000010 = 6.1V 000011 = 6.2V 000100 = 6.3V ……=…… 101100 = 10.3V (default) ……=…… 110011=11V	Soft-rst

REG0x01: LDON Register 1 [Reset = 0xBF]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	LDON1 [8:0]	110111111	R/W	LDON Adjustment. LDON2 of Register 0x02 is the highest bit here. 111100111 = -16V 111100110 = -16.025V 111100101 = -16.05V ……=…… 110111111 = -17V (default) ……=…… 100000000 = -21.775V 011111111 = -21.8V 011111110 = -21.825V ……=…… 001010111 = -26V	Soft-rst

NOTE: Register 0x01 and register 0x02 require a burst write, starting with register 0x01 and then register 0x02.

REG0x02: LDON Register 2 [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	LDON2	1	R/W	LDON Adjustment Refer to REG0x01.	Soft-rst
D[6:0]	Reserved	0000000	R/W	Reserved	Soft-rst

REG0x03: BUCK VOUT Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R/W	Reserved	Soft-rst
D[5:0]	BUCK_VOUT [5:0]	010000	R/W	BUCK V_{OUT} Adjustment 001100 = 0.75V 001101 = 0.7625V 001110 = 0.775V 001111 = 0.7875V 010000 = 0.8V(default) ……=…… 110110 = 1.275V 110111 = 1.2875V 111000 = 1.3V	Soft-rst

REGISTER MAPS (continued)

REG0x04: BUCK Current Limit Adjustment Register [Reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R/W	Reserved	Soft-rst
D[3:0]	BUCK_ILIM [3:0]	1111	R/W	BUCK OCP 0100 = 1262mA 1000 = 1694mA 1100 = 2126mA 1101 = 2234mA 1110 = 2342mA 1111 = 2450mA (default)	Soft-rst

REG0x05: Soft-Start Timing Register [Reset = 0x19]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved	Soft-rst
D[6]	LOCK	0	R/W	Lock needs set H to unlock. Registers 0x00, 0x01, 0x02, 0x03, 0x0F and 0x11 can be written when this bit is set high.	Soft-rst
D[5:4]	LDOP_SS [5:4]	01	R/W	Boost Soft-start Timing 00 = 0.5ms 01 = 1ms (default)	Soft-rst
D[3:2]	LDON_SS [3:2]	10	R/W	Buck-Boost Soft-start Timing 01 = 2ms (I_{OUT} = 0A) 10 = 4.5ms (default) 11 = 9ms	Soft-rst
D[1:0]	BUCK_SS [1:0]	01	R/W	BUCK Soft-start Timing 00 = 0.25ms 01 = 0.5ms (default) 10 = 1.5ms	Soft-rst

REGISTER MAPS (continued)

REG0x06: LDOP Turn-on/off Delay Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	LDOP_ON_DLY [7:4]	1000	R/W	LDOP Turn-on Delay 0001 = 0.5ms 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms (default) 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms	Soft-rst
D[3:0]	LDOP_OFF_DLY [3:0]	0000	R/W	LDOP Turn-off Delay 0000 = 0.25ms (default) 0001 = 0.5ms 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms	Soft-rst

REGISTER MAPS (continued)

REG0x07: LDON Turn-on/off Delay Register [Reset = 0xF1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	LDON_ON_DLY [7:4]	1111	R/W	LDON Turn-on Delay 0000 = 0.25ms 0001 = 0.5ms 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms (default)	Soft-rst
D[3:0]	LDON_OFF_DLY [3:0]	0001	R/W	LDON Turn-off Delay 0000 = 0.25ms 0001 = 0.5ms (default) 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms	Soft-rst

NOTE: For 0000 to 0110 in LDON turn-on delay, when the LDOP and LDON start at the same time, set DELAY as inaccurate.

REGISTER MAPS (continued)

REG0x08: BUCK Turn-on/off Delay Register [Reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	BUCK_ON_DLY [7:4]	0000	R/W	BUCK Turn-on Delay 0000 = 0.25ms (default) 0001 = 0.5ms 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms	Soft-rst
D[3:0]	BUCK_OFF_DLY [3:0]	1000	R/W	BUCK Turn-off Delay 0000 = 0.25ms 0001 = 0.5ms 0010 = 0.75ms 0011 = 1ms 0100 = 1.25ms 0101 = 1.5ms 0110 = 1.75ms 0111 = 2ms 1000 = 2.25ms (default) 1001 = 2.5ms 1010 = 2.75ms 1011 = 3ms 1100 = 3.25ms 1101 = 3.5ms 1110 = 3.75ms 1111 = 4ms	Soft-rst

REG0x09: Status 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	LDOP_OCP	0	R	LDOP OCP 0 = No OCP (default) 1 = LDOP OCP	Soft-rst
D[6]	LDON_OCP	0	R	LDON OCP 0 = No OCP (default) 1 = LDON OCP	Soft-rst
D[5]	BUCK_OCP	0	R	BUCK OCP 0 = No OCP (default) 1 = BUCK OCP	Soft-rst
D[4]	LDOP_OVP	0	R	LDOP OVP 0 = No OVP (default) 1 = LDOP OVP	Soft-rst
D[3]	LDON_OVP	0	R	LDON OVP 0 = No OVP (default) 1 = LDON OVP	Soft-rst
D[2]	BUCK_OVP	0	R	BUCK OVP 0 = NO OVP (default) 1 = BUCK OVP	Soft-rst
D[1]	LDOP_SHORT	0	R	LDOP SCP 0 = No SCP (default) 1 = LDOP SCP	Soft-rst
D[0]	LDON_SHORT	0	R	LDON SCP 0 = No SCP (default) 1 = LDON SCP	Soft-rst

REGISTER MAPS (continued)

REG0x0A: Status 2 Register [Reset = 0x75]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUCK_SHORT	0	R	BUCK SCP 0 = No SCP (default) 1 = BUCK SCP	Soft-rst
D[6]	LDOP_PG	1	R	LDOP Power Good 0 = No PG 1 = LDOP PG (default)	Soft-rst
D[5]	LDON_PG	1	R	LDON Power Good 0 = No PG 1 = LDON PG (default)	Soft-rst
D[4]	BUCK_PG	1	R	BUCK Power Good 0 = No PG (default) 1 = BUCK PG (default)	Soft-rst
D[3]	VIN_OVLO	0	R	VIN OVLO 0 = No OVLO (default) 1 = VIN OVLO Occurred	Soft-rst
D[2]	VIN_UVLO_B	1	R	VIN UVLO Backward 0 = VIN UVLO Occurred 1 = No VIN UVLO (default)	Soft-rst
D[1]	TSD	0	R	Device Thermal Shutdown 0 = No TSD (default) 1 = Device TSD	Soft-rst
D[0]	GPIO2	1	R	GPIO2 Status 0 = Low 1 = High (default)	Soft-rst

REG0x0B: Interrupt 1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	LDOP_OCP_INT	0	R/RC	LDOP OCP Interrupt 0 = Clear (default) 1 = LDOP OCP Interrupt	Soft-rst
D[6]	LDON_OCP_INT	0	R/RC	LDON OCP Interrupt 0 = Clear (default) 1 = LDON OCP Interrupt	Soft-rst
D[5]	BUCK_OCP_INT	0	R/RC	BUCK OCP Interrupt 0 = Clear (default) 1 = BUCK OCP Interrupt	Soft-rst
D[4]	LDOP_OVP_INT	0	R/RC	LDOP OVP Interrupt 0 = Clear (default) 1 = LDOP OVP	Soft-rst
D[3]	LDON_OVP_INT	0	R/RC	LDON OVP Interrupt 0 = Clear (default) 1 = LDON OVP Interrupt	Soft-rst
D[2]	BUCK_OVP_INT	0	R/RC	BUCK OVP Interrupt 0 = Clear (default) 1 = BUCK OVP Interrupt	Soft-rst
D[1]	LDOP_SHORT_INT	0	R/RC	SIDO SCP Interrupt 0 = Clear (default) 1 = LDOP SCP Interrupt	Soft-rst
D[0]	LDON_SHORT_INT	0	R/RC	LDON SCP Interrupt 0 = Clear (default) 1 = LDON SCP Interrupt	Soft-rst

REGISTER MAPS (continued)

REG0x0C: Interrupt 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUCK_SHORT_INT	0	R/RC	BUCK SCP Interrupt 0 = Clear (default) 1 = BUCK SCP Interrupt	Soft-rst
D[6]	LDOP_PG_B_INT	0	R/RC	LDOP Power Good Backward Interrupt 0 = Clear (default) 1 = LDOP PG Backward Interrupt	Soft-rst
D[5]	LDON_PG_B_INT	0	R/RC	LDON Power Good Backward Interrupt 0 = Clear (default) 1 = LDON PG Backward Interrupt	Soft-rst
D[4]	BUCK_PG_B_INT	0	R/RC	BUCK Power Good Backward Interrupt 0 = Clear (default) 1 = BUCK PG Backward Interrupt	Soft-rst
D[3]	VIN_OVLO_INT	0	R/RC	VIN OVLO Interrupt 0 = Clear (default) 1 = VIN OVLO Interrupt	Soft-rst
D[2]	VIN_UVLO_INT	0	R/RC	VIN UVLO Interrupt 0 = Clear (default) 1 = VIN UVLO Occurred Interrupt	Soft-rst
D[1]	TSD_INT	0	R/RC	Device Thermal Shutdown Interrupt 0 = Clear (default) 1 = Device TSD Interrupt	Soft-rst
D[0]	GPIO2_B_INT	0	R/RC	GPIO2 Backward Interrupt 0 = Clear (default) 1 = GPIO2 Backward Interrupt	Soft-rst

REG0x0D: Interrupt 1 Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	LDOP_OCP_MASK	0	R/W	LDOP OCP Mask 0 = No masking of interrupt (default) 1 = Interrupt will not change state when OCP occurs.	Soft-rst
D[6]	LDON_OCP_MASK	0	R/W	LDON OCP Mask 0 = No masking of interrupt (default) 1 = Interrupt will not change state when OCP occurs.	Soft-rst
D[5]	BUCK_OCP_MASK	0	R/W	BUCK OCP Mask 0 = Clear (default) 1 = Interrupt will not change state when OCP occurs.	Soft-rst
D[4]	LDOP_OVP_MASK	0	R/W	LDOP OVP Mask 0 = Clear (default) 1 = Interrupt will not change state when OVP occurs.	Soft-rst
D[3]	LDON_OVP_MASK	0	R/W	LDON OVP Mask 0 = Clear (default) 1 = Interrupt will not change state when OVP occurs.	Soft-rst
D[2]	BUCK_OVP_MASK	0	R/W	BUCK OVP Mask 0 = Clear (default) 1 = Interrupt will not change state when OVP occurs.	Soft-rst
D[1]	LDOP_SHORT_MASK	0	R/W	LDOP SCP Mask 0 = Clear (default) 1 = Interrupt will not change state when SCP occurs.	Soft-rst
D[0]	LDON_SHORT_MASK	0	R/W	LDON SCP Mask 0 = No SCP (default) 1 = Interrupt will not change state when SCP occurs.	Soft-rst

REGISTER MAPS (continued)

REG0x0E: Interrupt 2 Mask Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUCK_SHORT_MASK	0	R/W	BUCK SCP Mask 0 = No SCP (default) 1 = Interrupt will not change state when SCP occurs.	Soft-rst
D[6]	LDOP_PG_B_MASK	0	R/W	LDOP Power Good Backward Mask 0 = No PG (default) 1 = Interrupt will not change state when PG_B occurs.	Soft-rst
D[5]	LDON_PG_B_MASK	0	R/W	LDON Power Good Backward Mask 0 = No PG (default) 1 = Interrupt will not change state when PG_B occurs.	Soft-rst
D[4]	BUCK_PG_B_MASK	0	R/W	BUCK Power Good Backward Mask 0 = No PG (default) 1 = Interrupt will not change state when PG_B occurs.	Soft-rst
D[3]	VIN_OVLO_MASK	0	R/W	VIN OVLO Mask 0 = No SCP (default) 1 = Interrupt will not change state when VIN OVLO occurs.	Soft-rst
D[2]	VIN_UVLO_MASK	0	R/W	VIN UVLO Mask 0 = Clear (default) 1 = Interrupt will not change state when VIN UVLO occurs.	Soft-rst
D[1]	TSD_MASK	0	R/W	Device Thermal Shutdown Mask 0 = Clear (default) 1 = Interrupt will not change state when TSD occurs.	Soft-rst
D[0]	GPIO2_B_MASK	0	R/W	GPIO2 Backward Mask 0 = Clear (default) 1 = Interrupt will not change state when GPIO2 backward occurs.	Soft-rst

REG0x0F: Mode Control 1 Register [Reset = 0x80]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	GPIO2_EN	1	R/W	GPIO2 Enable 0 = Disable 1 = Enable (default)	Soft-rst
D[6]	LDOP_DISCHG	0	R/W	Output Discharge Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[5]	LDON_DISCHG	0	R/W	Output Discharge Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[4]	BUCK_DISCHG	0	R/W	Output Discharge Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[3]	I2C_BIAS_EN	0	R/W	Bias Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[2]	LDOP_EN	0	R/W	LDOP Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[1]	LDON_EN	0	R/W	LDON Enable 0 = Disable (default) 1 = Enable	Soft-rst
D[0]	BUCK_EN	0	R/W	BUCK Enable 0 = Disable (default) 1 = Enable	Soft-rst

REGISTER MAPS (continued)

REG0x10: Mode Control 2 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	SOFT_RST	0	R/W	Soft Rest 0 = Disable (default) 1 = Enable Reset all registers.	Soft-rst
D[6:1]	Reserved	000000	R/W	Reserved	Soft-rst
D[0]	FORCED_DIS	0	W/C	Forced Disable 0 = Disable (default) 1 = Enable When GPIO2 is triggered, this bit is automatically set to 1. This bit can only be written when GPIO2 is at high power level.	Soft-rst

REG0x11: DVS_SLEW_RATE Register [Reset = 0x1B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R/W	Reserved	Soft-rst
D[5:3]	DVS_SLEW_RATE_LDON [5:3]	011	R/W	010 = 30μs/step 011 = 40μs/step (default) 111 = 80μs/step	Soft-rst
D[2:0]	DVS_SLEW_RATE_LDOP [2:0]	011	R/W	011 = 40μs/step (default) 111 = 80μs/step	Soft-rst

NOTE: For DVS_SLEW_RATE_LDON, I_{LOAD_LDON} = 1mA, I_{LOAD_LDOP} = 0mA, I_{LOAD_BUCK} = 500mA.

APPLICATION INFORMATION

Typical Application

The SGM3807 is a DC/DC PMIC designed for dToF module applications. The device is capable to operate down to 2.1V after start-up. When the input voltage is above 3V, the typical LDOP output is 10.3V with 100mA load capability, the typical LDON output is -17V with 5mA load capability, and the typical Buck output is 0.8V with 1.2A load capability.

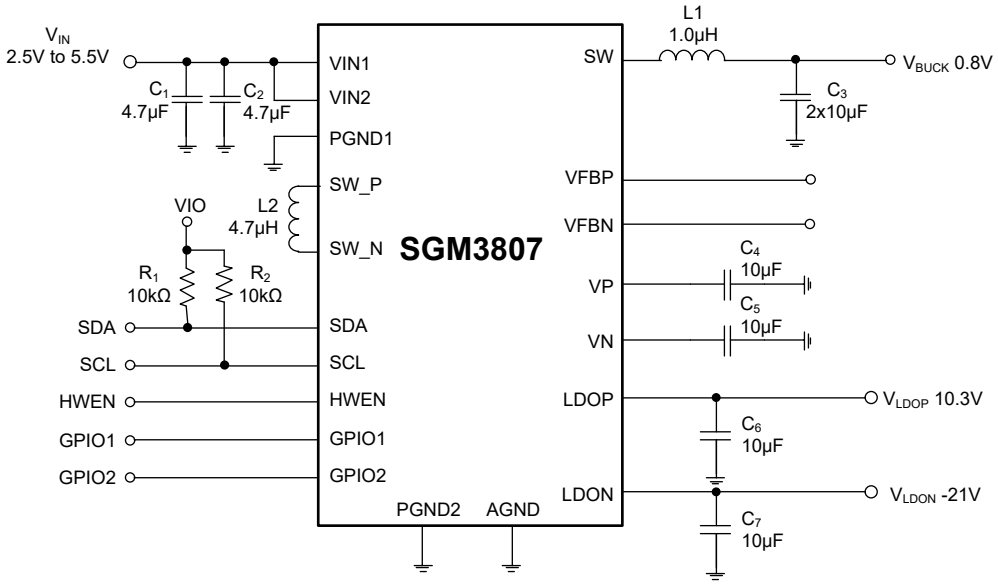


Figure 12. Typical Application Circuit

Application Design Requirement

The design parameters are listed in Table 3 for recommended external components selection.

Table 3. Design Parameters

Parameters	Values
Input Voltage	2.5V to 5.5V
Input Voltage after Start-up	2.1V
SIDO LDOP Output	10.3V
SIDO LDOP Load Current	100mA above 3.0V V_{IN}
SIDO LDON Output	-17V
SIDO LDON Load Current	5mA

SIDO Inductor Selection

The recommended inductor for the SIDO is 4.7μH. The selected inductor should have a saturation current rating higher than 2.15A, which is the SIDO's peak switch current limit. DFE252012F-4R7M from Murata is recommended. Lower DCR inductor is recommended to improve the device's operation efficiency.

Buck Inductor Selection

The SGM3807's Buck converter is designed to work with 1μH inductor. DFE201610E-1R0M from Murata is recommended. Lower DCR inductor is recommended to improve the device's operation efficiency.

Input Capacitor Selection

The input capacitor of SGM3807 serves as the decoupling capacitor for internal circuit as well as damping the input line's parasitic inductance. Two 4.7μF low ESR ceramic capacitors are recommended.

SIDO Output Capacitor Selection

The output capacitors for the positive and negative outputs of the SIDO is a critical components for SIDO's stability, as well as load transient, output voltage ripple. One 10μF low ESR ceramic capacitor is recommended for VP, VN, LDOP and LDON outputs. The selected capacitor should have enough voltage rating, and DC derating should be considered. The selected capacitor should have minimal of 2.5μF effective capacitance at 10.3V LDOP output and -21V LDON output.

Buck Output Capacitor Selection

Two 10μF low ESR ceramic capacitors are recommended for the Buck output. The selected capacitor should have minimal of 16μF effective capacitance at 0.8V.

APPLICATION INFORMATION (continued)

Layout Considerations

The PCB layout is quite important in the power supply design. An incorrect layout could cause many problems, such as instability, load and line transient regulation problems, output voltage noise, and EMI issues. Good grounding becomes important especially with heavy load current.

The following PCB layout guide should be applied:

• In order to avoid any inductive or capacitive coupling of the switching power supply noise to the sensitive analog control circuits, there are 3 separated grounds (AGND, PGND1 and PGND2) in the SGM3807. The signal ground (AGND) and noisy power ground (PGND1, PGND2) should be well separated on the PCB, and connected only at one point.

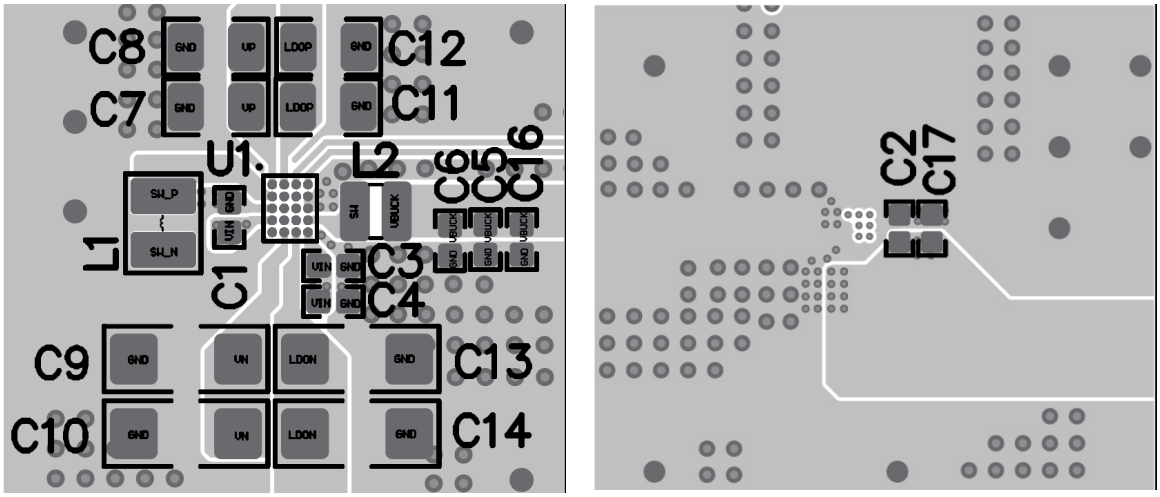
• Traces of switching nodes (SW, SW_P and SW_N) should be short and wide.

• Place input capacitors on VIN (VIN1, VIN2) as close as possible to the device.

• Place output capacitors on BUCK, LDOP, LDON, VP and VN as close as possible to the device.

• Use short and wide traces to connect the input capacitors on PVIN and the output capacitor.

• Differential routing for the VFBP and VFBN signals to the remote terminals is recommended when utilizing the remote sensing function of the Buck converter.



PCB Top Layer PCB Bottom Layer

Figure 13. PCB Layout Example

REVISION HISTORY

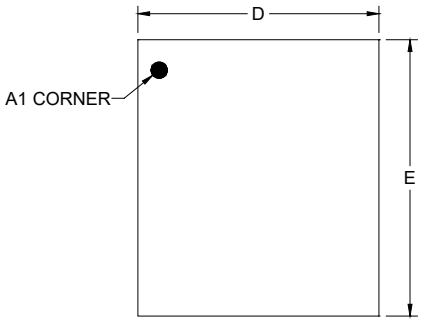
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MAY 2025 – REV.A to REV.A.1	Page
Added GPIO1 and GPIO2 pins in ABSOLUTE MAXIMUM RATINGS section	2

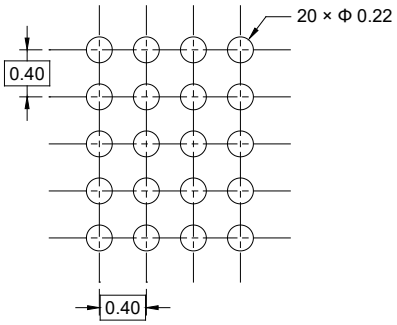
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

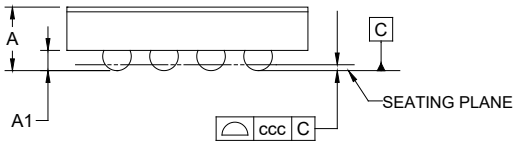
WLCSP-2.05×2.35-20B



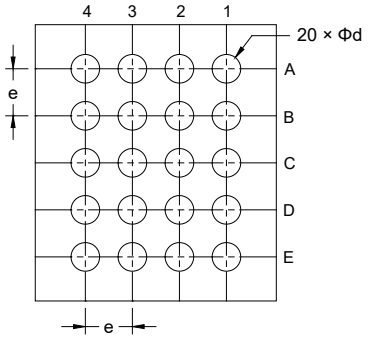
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



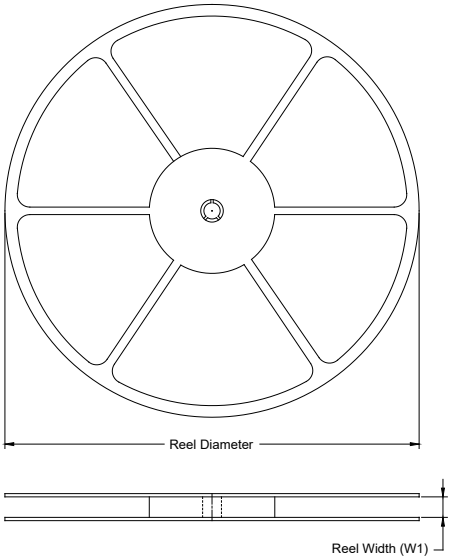
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.618
A1	0.152	-	0.192
D	2.020	-	2.080
E	2.320	-	2.380
d	0.213	-	0.273
e	0.400 BSC		
ccc	0.050		

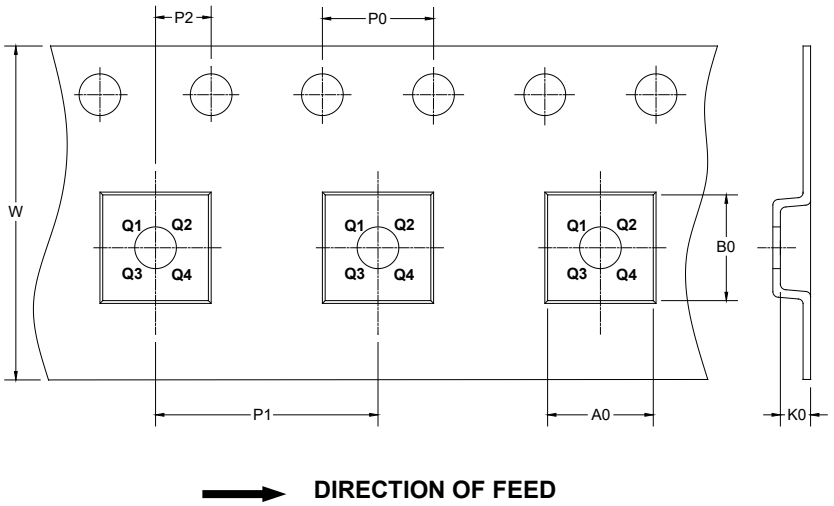
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

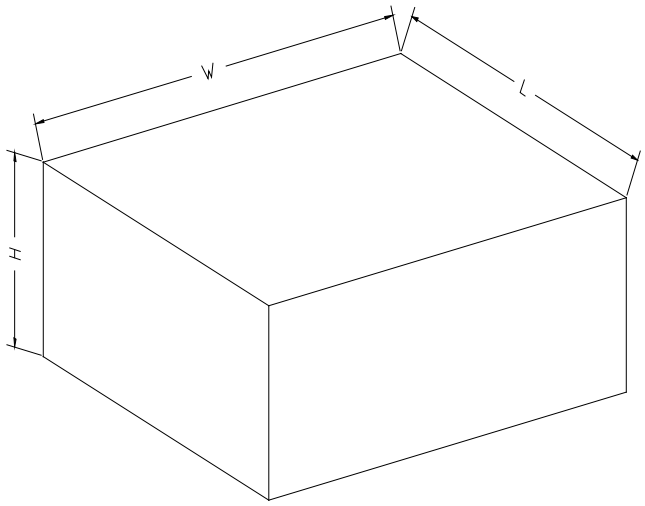
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.05×2.35-20B	7"	9.5	2.25	2.65	0.85	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002