SGM41544/SGM41544D
High Input Voltage, 5A Single-Cell Battery Charger with NVDC Power Path Management

FEATURES

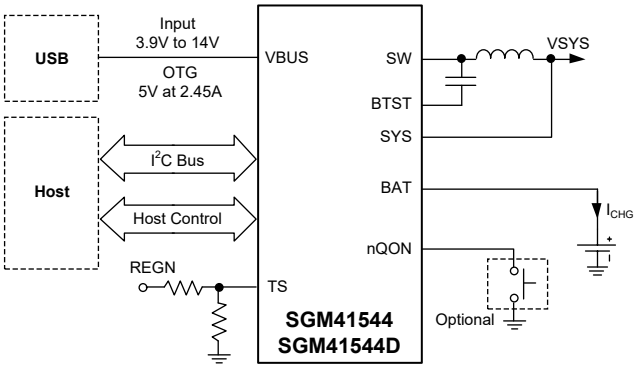
- 3.9V to 14V Operating Input Voltage Range
- Up to 22V Sustainable Voltage
- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 95.4% Charge Efficiency at 1A from 5V Input
  - 92.6% Charge Efficiency at 1.5A from 9V Input
  - Optimized for USB Voltage Input (9V/12V)
  - Selectable PFM Mode for Light Load Efficiency
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 2.45A Output
  - Boost Efficiency of 94.8% at 0.5A and 94.5% at 1A
  - Accurate Hiccup Mode Over-Current Protection
  - Output Short-Circuit Protection
  - Selectable PFM Mode for Light Load Operations
- Programmable Input Current Limit and Dynamic Power Management (IINDPM, 100mA to 3.25A with 50mA Resolution) to Support USB 2.0 and USB 3.0 Standards and High Voltage Adaptors
- Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM) with Selectable Offset
- VINDPM Tracking of Battery Voltage
- Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- High Battery Discharge Efficiency with 17mΩ Switch, Battery Discharge MOSFET up to 12A
- Input Current Optimizer (ICO) to Maximize Adaptor Output Current without Overloading
- Integrated ADC for System Monitor
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
- Flexible Autonomous and I^2C Operation Modes for Optimal System Performance
- Fully Integrated Switches, Current Sense and IR Compensation
- 4μA Ship Mode Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation
  - ±3% Charge Current Regulation at 1.792A
  - ±5% Input Current Regulation at 0.9A
- Safety
  - Battery Temperature Sensing (Charge/Boost Modes)
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

APPLICATIONS

Smart Phones, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41544/SGM41544D are battery chargers and system power path management devices with integrated converter and power switches for using with single-cell Li-Ion or Li-polymer batteries. This highly integrated 5A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. I^2C programming makes it a very flexible powering and charger design solution.

The devices include four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for Buck or Boost mode (HSFET, Q2), low-side switching FET for Buck or Boost mode (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

A wide range of input sources are supported, including standard USB hosts, charging ports and USB compliant high voltage adaptors. The default input current limit is automatically selected based on the built-in USB interface. This limit is determined by the detection circuit in the system (e.g. USB PHY). The SGM41544/SGM41544D are USB 2.0 and USB 3.0 power specifications compliant with input current and voltage regulation. It also meets USB On-The-Go (OTG) power rating specification and is capable of boosting the battery voltage to supply 5V on VBUS with 2.45A (MAX) current limit.

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.5V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the three phases of charging cycle: pre-conditioning, constant current or constant voltage. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger begins another charging cycle.

Several safety features are provided in the SGM41544/ SGM41544D such as over-voltage and over-current protections, battery temperature monitoring, charging safety timing, thermal shutdown and input UVLO. TS pin is connected to an NTC thermistor for battery temperature monitoring and protection in both charge and Boost modes according to JEITA profile. This device also features thermal regulation in which the charge current is reduced, if the junction temperature exceeds +120℃.

Charging status is reported by the STAT output and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

The SGM41544/SGM41544D provide a 7-bit analog-to-digital converter (ADC) for monitoring input current and charge current and input/battery/system/TS voltages.

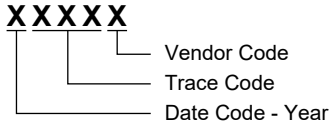
The SGM41544/SGM41544D are available in a Green TQFN-4×4-24L package.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41544	TQFN-4×4-24L	-40℃ to +85℃	SGM41544YTQF24G/TR	SGM41544 YTQF24 XXXXX	Tape and Reel, 3000
SGM41544D	TQFN-4×4-24L	-40℃ to +85℃	SGM41544DYTQF24G/TR	SGM0IT YTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to PGND)
- VBUS (Converter Not Switching) ..... -2V to 22V
- PMID (Converter Not Switching) ..... -0.3V to 22V
- STAT ..... -0.3V to 6V
- DSEL ..... -0.3V to 6V
- BTST ..... -0.3V to 22V
- SW ..... -2V to 16V
- SW (Peak for 10ns Duration) ..... -3V to 16V
- BAT, SYS (Converter Not Switching) ..... -0.3V to 6V
- SDA, SCL, nINT, OTG, REGN, TS, nCE, nQON ... -0.3V to 6V
- PSEL, nPG, D+, D- ..... -0.3V to 6V
- BTST to SW ..... -0.3V to 6V
- ILIM ..... -0.3V to 5V

Output Sink Current
- nINT, STAT ..... 6mA (MAX)
- DSEL ..... 2mA (MAX)

Package Thermal Resistance
- TQFN-4×4-24L, θ_{JA} ..... 30℃/W
- TQFN-4×4-24L, θ_{JB} ..... 7.7℃/W
- TQFN-4×4-24L, $\theta_{JC\ (TOP)}$ ..... 22.3℃/W
- TQFN-4×4-24L, $\theta_{JC\ (BOT)}$ ..... 1.9℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 3.9V to 14V (3)
Input Current (VBUS), I_{IN} ..... 3.25A (MAX)
Output Current (SW), I_{SYS} ..... 5A (MAX)
Battery Voltage, V_{BAT} ..... 4.624V (MAX)
Fast Charging Current, I_{BAT} ..... 5A (MAX)
Discharging Current with Internal MOSFET, I_{BAT}
- Continuous ..... Up to 6A
- Peak ..... 12A (TYP)

Operating Ambient Temperature Range ..... -40℃ to +85℃

NOTE:

3. The voltage spikes on either the BTST or SW pins should be less than the absolute maximum rating. Following the layout guidelines is helpful to minimize the switching noise.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

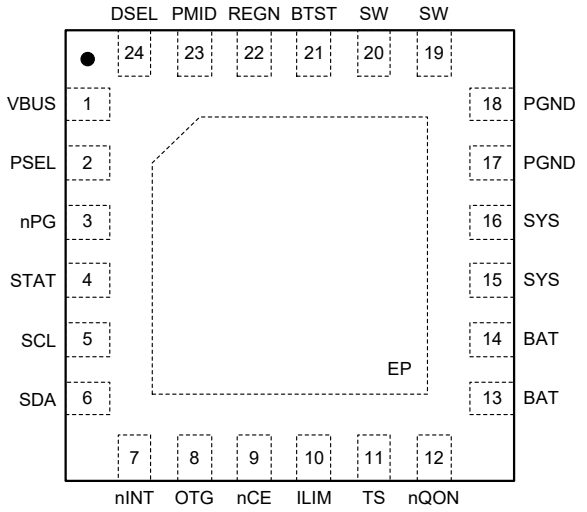
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

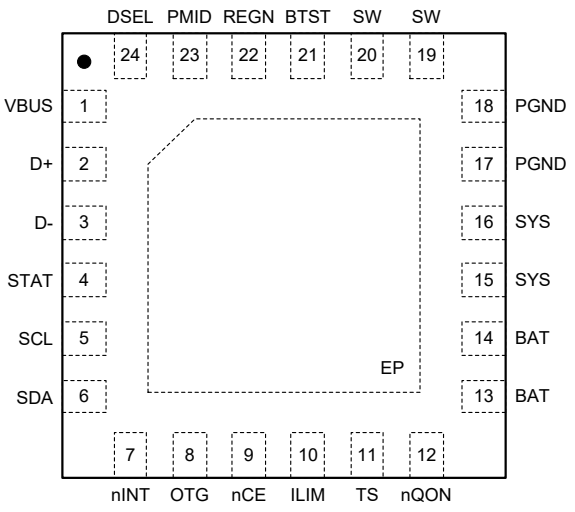
PIN CONFIGURATIONS

SGM41544 (TOP VIEW)



TQFN-4×4-24L

SGM41544D (TOP VIEW)



TQFN-4×4-24L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
SGM 41544	SGM 41544D			
1	1	VBUS	P	Charger Input (V_{IN}). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to PGND close to the device.
2	—	PSEL	DI	Power Source Selection Input. If PSEL is pulled high, the input current limit is set to 500mA (USB 2.0) and if it is pulled low, the limit is set to 2.4A (adaptor). When the I^2C link to the host is established, the host can program a different input current limit value by writing to the IINDPM[5:0] register. (SGM41544 only)
—	2	D+	AIO	Positive USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DP_DAC[2:0] register. (SGM41544D only)
3	—	nPG	DO	Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input (V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV}, V_{VBUS} is above sleep mode threshold, and V_{VBUS} > $V_{VBUSMIN}$ when I_{BAD_SRC} = 30mA). (SGM41544 only)
—	3	D-	AIO	Negative USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DM_DAC[2:0] register. (SGM41544D only)
4	4	STAT	DO	Open-Drain Charge Status Output. Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charger in sleep mode: high (LED OFF). Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS). The function can be disabled via EN_ICHG_MON[1:0] register.
5	5	SCL	DI	I^2C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
6	6	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail.
7	7	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
8	8	OTG	DI	Boost Mode Enable Input Pin (Active High). Boost mode is enabled when OTG_CONFIG bit is 1 and OTG pin is pulled high.
9	9	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low.

PIN DESCRIPTION (continued)

PIN		NAME	TYPE	FUNCTION
SGM 41544	SGM 41544D			
10	10	ILIM	AI	Input Current Limit. A resistor between ILIM and PGND pins can clamp the input current limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. When EN_ILIM = 1, the lower limit between IINDPM[5:0] registers and ILIM pin resistor setting set the actual input current limit. The ILIM pin can supply higher than 500mA current limit only. If the current limit is not triggered, the ILIM pin voltage indicates the actual input current limit by $I_{IN} = (K_{ILIM} \times V_{ILIM})/(R_{ILIM} \times 0.8V)$. Change EN_ILIM = 0 can disable both input current limit clamping and input current monitor function from ILIM pin.
11	11	TS	AI	Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and PGND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor. If NTC or TS pin function is not needed, use a 10kΩ/10kΩ pair for the resistor divider.
12	12	nQON	DI	BATFET On/Off Control Input. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn BATFET on, a logic low pulse with a duration of $t_{SHIPMODE}$ (1s TYP) can be applied to nQON. When VBUS source is not connected, a logic low pulse with a duration of t_{QON_RST} (10s TYP) resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (340ms TYP) and then goes back to provide a full power reset for system.
13, 14	13, 14	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and PGND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
15, 16	15, 16	SYS	P	Connection Point to Converter Output. SYS is connected to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect a 2×10μF capacitor between SYS pin and PGND close to the device.
17, 18	17, 18	PGND	P	Ground Pin of the Device
19, 20	19, 20	SW	P	Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
21	21	BTST	P	High-side Driver Positive Supply. It is internally connected to the boost-strap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
22	22	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Place a 4.7μF (10V rating) ceramic capacitor between REGN pin and PGND. It is recommended to place the capacitor close to the REGN pin.
23	23	PMID	P	PMID Pin. PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 10μF ceramic capacitor from PMID pin to PGND. It is the proper point for decoupling of high frequency switching currents.
24	24	DSEL	DO	D+/D- Multiplexer Selection Control (Active High). Place a 47nF (6V rating) ceramic capacitor between DSEL and PGND. The pin is normally kept low. For SGM41544D, the pin driven high indicates that the D+/D- detection of the device is in progress, and the D+, D- signals need to be controlled. After the detection is completed, the pin keeps high if DCP or HVDCP is detected, otherwise the pin returns to low.
EP	EP	Exposed Pad	P	Thermal Pad and Ground Reference. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie externally to the PCB ground plane (PGND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE: AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output, P = power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Currents							
Battery Discharge Current (BATP, BAT, SYS) in Buck Mode	I_{BAT}	V_{BAT} = 4.2V, V_{VBUS} < V_{VBUS_UVLOZ}, leakage between BAT and VBUS			0.1	1	μA
		HIZ mode, no VBUS, battery monitor disabled, T_J < 85℃	BATFET disabled (BATFET_DIS = 1)		4	6.5	
			BATFET enabled (BATFET_DIS = 0)		13	20	
Input Supply Current (VBUS) in Buck Mode when HIZ Mode is Enabled	I_{VBUS_HIZ}	HIZ mode, no battery, battery monitor disabled	V_{VBUS} = 5V		25	35	μA
			V_{VBUS} = 12V		50	67	
Input Supply Current (VBUS) in Buck Mode	I_{VBUS}	V_{VBUS} > V_{VBUS_UVLOZ}, V_{VBUS} > V_{BAT}, converter not switching			2.8	4	mA
		V_{VBUS} > V_{VBUS_UVLOZ}, V_{VBUS} > V_{BAT}, converter switching	V_{BAT} = 3.2V, I_{SYS} = 0A		3		
			V_{BAT} = 3.8V, I_{SYS} = 0A		3		
Battery Discharge Current in Boost Mode	I_{BOOST}	V_{BAT} = 4.2V, Boost mode, I_{VBUS} = 0A, converter switching	PFM_OTG_DIS = 0		3		mA
			PFM_OTG_DIS = 1		15		
BAT Pin and VBUS Pin Power-Up							
VBUS Operating Range	V_{VBUS_OP}			3.9		14	V
VBUS UVLO to Have Active I²C (with No Battery)	V_{VBUS_UVLOZ}	V_{VBUS} rising			3.4	3.7	V
V_{VBUS} Minimum (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT}$	V_{VBUS} rising			3.67	4.1	V
V_{VBUS} Hysteresis (as One of the Conditions) to Turn on REGN	$V_{VBUS\_PRESENT\_HYS}$	V_{VBUS} falling from above $V_{VBUS\_PRESENT}$			400		mV
Sleep Mode Falling Threshold	V_{SLEEP}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VBUS} falling, V_{BAT} = 4V, T_J = +25℃		15	60	115	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{VBUS} - V_{BAT}, $V_{VBUSMIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{VBUS} rising, V_{BAT} = 4V, T_J = +25℃		190	240	305	mV
VBUS Over-Voltage Rising Threshold – 6.5V Setting	$V_{VBUS\_OV\_RISE}$	V_{VBUS} rising	OVP[1:0] = 01	6.38	6.5	6.61	V
VBUS Over-Voltage Rising Threshold – 10.5V Setting			OVP[1:0] = 10	10.3	10.5	10.63	
VBUS Over-Voltage Rising Threshold – 14V Setting			OVP[1:0] = 11	14.1	14.3	14.5	
VBUS Over-Voltage Hysteresis – 6.5V Setting	$V_{VBUS\_OV\_HYS}$				100		V
VBUS Over-Voltage Hysteresis – 10.5V Setting					250		
VBUS Over-Voltage Hysteresis – 14V Setting					420		
BAT Voltage to Have Active I²C (No Source on VBUS)	V_{BAT_UVLOZ}	V_{BAT} rising		2.8			V
Battery Depletion Falling Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling		2.25	2.375	2.5	V
Battery Depletion Rising Threshold	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising		2.43	2.53	2.63	V
Bad Adaptor Detection Threshold	V_{VBUS_MIN}	V_{VBUS} falling			3.8		V
Bad Adaptor Detection Current Source	I_{BAD_SRC}	V_{VBUS} = 5V, sink current from VBUS to PGND			30		mA
Power Path Management							
Typical System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, BATFET disabled (BATFET_DIS = 1)	V_{BAT} > V_{SYS_MIN}		V_{BAT} + 60mV		V
			V_{BAT} < V_{SYS_MIN}		V_{SYS_MIN} + 160mV		

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Path Management							
Minimum DC System Voltage Output	V_{SYS_MIN}	V_{BAT} < V_{SYS_MIN}, I_{SYS} = 0A, SYS_MIN[2:0] = 101 (3.5V)		3.6	3.65		V
Maximum DC System Voltage Output	V_{SYS_MAX}	V_{BAT} = 4.4V, I_{SYS} = 0A, SYS_MIN[2:0] = 101 (3.5V)		4.41	4.46	4.51	V
Top Reverse Blocking MOSFET (RBFET) On-Resistance between VBUS and PMID	R_{ON_RBFET}				21		mΩ
Top Switching MOSFET (HSFET) On-Resistance between PMID and SW	R_{ON_HSFET}				24		mΩ
Bottom Switching MOSFET (LSFET) On-Resistance between SW and PGND	R_{ON_LSFET}				25		mΩ
BATFET Forward Voltage in Supplement Mode	V_{FWD}	BAT discharge current 10mA			25		mV
Battery Charger							
Typical Charge Voltage Range	$V_{BAT\_REG\_RANGE}$	VREG_SET = 0		3.856		4.624	V
		VREG_SET = 1		3.504		4.272	
Typical Charge Voltage Step	V_{BATREG_STEP}				16		mV
Charge Voltage Setting	V_{BAT_REG}	V_{BAT} = 4.208V (VREG[5:0] = 01 0110)	T_J = +25℃	4.192	4.208	4.224	V
			T_J = 0℃ to +65℃	4.187		4.229	
		V_{BAT} = 4.352V (VREG[5:0] = 01 1111)	T_J = +25℃	4.333	4.35	4.367	
			T_J = 0℃ to +65℃	4.329		4.371	
Charge Voltage Resolution Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.208V or V_{BAT_REG} = 4.352V	T_J = +25℃	-0.4		0.4	%
			T_J = 0℃ to +65℃	-0.5		0.5	
Typical Fast Charge Current Regulation Range	$I_{CHG\_REG\_RANGE}$			0		5056	mA
Typical Fast Charge Current Regulation Step	$I_{CHG\_REG\_STEP}$				64		mA
Fast Charge Current Regulation Accuracy	$I_{CHG\_REG\_ACC}$	V_{BAT} = 3.1V, T_J = +25℃	I_{CHG} = 128mA	90	115	140	mA
			I_{CHG} = 256mA	205	250	295	
			I_{CHG} = 1792mA	1740	1790	1840	
			I_{CHG} = 2048mA	2000	2048	2096	
		V_{BAT} = 3.8V, T_J = +25℃	I_{CHG} = 128mA	122	136	150	
			I_{CHG} = 256mA	250	265	280	
			I_{CHG} = 1792mA	1745	1790	1835	
			I_{CHG} = 2048mA	2005	2048	2090	
Battery LOWV Falling Threshold	V_{BAT_LOWV}	Fast charge to pre-charge, BATLOWV = 1		2.63	2.76	2.89	V
Battery LOWV Rising Threshold		Pre-charge to fast charge, BATLOWV = 1		2.9	2.99	3.08	V
Pre-Charge Current Range	I_{PRECHG_RANGE}			64		1024	mA
Typical Pre-Charge Current Step	I_{PRECHG_STEP}				64		mA
Pre-Charge Current Accuracy	I_{PRECHG_ACC}	V_{BAT} = 2.6V, I_{PRECHG} = 256mA, T_J = +25℃		-14		14	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
Termination Current Range	I_{TERM_RANGE}			64		1024	mA
Typical Termination Current Step	I_{TERM_STEP}				64		mA
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM} = 256mA, T_J = +25℃	I_{CHG} ≤ 1344mA	-8		8	%
			I_{CHG} > 1344mA	-8		8	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling		1.88	1.98	2.08	V
Battery Short Voltage Hysteresis	V_{SHORT_HYS}				200		mV
Battery Short Current	I_{SHORT}	V_{BAT} < 2.2V			90		mA
Recharge Threshold Below V_{BATREG}	V_{RECHG}	V_{BAT} falling	VRECHG = 0	85	100	120	mV
			VRECHG = 1	185	200	220	
System Discharge Load Current	I_{SYS_LOAD}				26		mA
SYS-BAT MOSFET (BATFET) On-Resistance	R_{ON_BATFET}	T_J = +25℃			17	21	mΩ
		T_J = -40℃ to +85℃			17	25	
Input Voltage and Current Regulation (DPM: Dynamic Power Management)							
Typical Input Voltage Regulation Range	V_{INDPM_RANGE}			3.9		15.3	V
Typical Input Voltage Regulation Step	V_{INDPM_STEP}				100		mV
Input Voltage Regulation Accuracy	V_{INDPM_ACC}	V_{INDPM} = 4.4V, 9V, T_J = -40℃ to +85℃		-1.2		1.2	%
Input Voltage Regulation Limit Tracking VBAT	V_{DPM_VBAT}	V_{BAT} = 4V, V_{INDPM} = 3.9V, VDPM_BAT_TRACK[1:0] = 11 (300mV)		4.2	4.3	4.4	V
Input Voltage Regulation Accuracy Tracking VBAT	$V_{DPM\_VBAT\_ACC}$			-2.4		2.4	%
Typical Input Current Regulation Range	I_{INDPM_RANGE}			100		3250	mA
Typical Input Current Regulation Step	I_{INDPM_STEP}				50		mA
Input Voltage Regulation Accuracy	$I_{INDPM100\_ACC}$	V_{VBUS} = 5V, current pulled from SW, I_{INDPM} (IINDPM[5:0]) =100mA		75	95	115	mA
Input Voltage Regulation Accuracy	I_{INDPM_ACC}	V_{VBUS} = 5V, current pulled from SW	USB150, I_{INDPM} (IINDPM[5:0]) = 150mA	125	142.5	160	mA
			USB500, I_{INDPM} (IINDPM[5:0]) = 500mA	450	475	500	
			USB900, I_{INDPM} (IINDPM[5:0]) = 900mA	820	855	890	
			Adaptor 1.5A, I_{INDPM} (IINDPM[5:0]) = 1500mA	1370	1425	1480	
			Adaptor 2A, I_{INDPM} (IINDPM[5:0]) = 2000mA	1840	1900	1960	
Input Current Regulation during System Start-Up Sequence	I_{IN_START}	V_{SYS} = 2.2V, I_{INDPM} (IINDPM[5:0]) ≥ 200mA			190		mA
Charge Current Setting Ratio	K_{ILIM}	I_{INMAX} = K_{ILIM}/R_{ILIM}, input current regulation by ILIM pin = 1.5A		310	340	370	A × Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D+/D- Detection						
D+/D- Voltage Source (0V)	V_{0P0_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 001 or DM_DAC[2:0] = 001	-0.15	0	0.15	V
D+/D- Voltage Source (0.6V)	V_{0P6_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 010 or I_{DM} < 1mA, DM_DAC[2:0] = 010	0.5	0.6	0.7	V
D+/D- Voltage Source (1.2V)	V_{1P2_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 011 or I_{DM} < 1mA, DM_DAC[2:0] = 011	1.075	1.2	1.325	V
D+/D- Voltage Source (2.0V)	V_{2P0_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 100 or I_{DM} < 1mA, DM_DAC[2:0] = 100	1.875	2	2.125	V
D+/D- Voltage Source (2.7V)	V_{2P7_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 101 or I_{DM} < 1mA, DM_DAC[2:0] = 101	2.575	2.7	2.825	V
D+/D- Voltage Source (3.3V)	V_{3P3_VSRC}	I_{DP} < 1mA, DP_DAC[2:0] = 110 or I_{DM} < 1mA, DM_DAC[2:0] = 110	3.15	3.3	3.45	V
D+ Connection Check Current Source	I_{10UA_ISRC}		7	10	13	μA
D+/D- Current Sink (100μA)	I_{100UA_ISINK}		50	100	150	μA
D+/D- Leakage Current	I_{DPDM_LKG}	D-, switch open	-0.5		0.5	μA
		D+, switch open	-0.5		0.5	
D+/D- Low Comparator Threshold	V_{0P4_VTH}		250	300	350	mV
D+ Low Comparator Threshold	V_{0P8_VTH}		0.85		0.93	V
D+/D- Comparator Threshold for Non-Standard Adaptor Detection (Divider 1, 3, or 4)	V_{2P7_VTH}		2.53		2.9	V
D+/D- Comparator Threshold for Non-Standard Adaptor Detection (Divider 1, 3)	V_{2P0_VTH}		1.83		2.13	V
D+/D- Comparator Threshold for Non-Standard Adaptor Detection (Divider 2)	V_{1P2_VTH}		1.03		1.45	V
D- Pull-Down for Connection Check	R_{D-_DWN}		14.25		24.8	kΩ
BAT Pin Over-Voltage/Over-Current Protection						
Battery Over-Voltage Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}		104		%
Battery Over-Voltage Hysteresis	$V_{BAT\_OVP\_HYST}$	V_{BAT} falling, as percentage of V_{BAT_REG}		2		%
System Over-Current Threshold	$I_{BAT\_FET\_OCP}$	BATFET_OCP = 1, T_J = +25℃	12.1			A
		BATFET_OCP = 0, T_J = +25℃	8.4			
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Threshold	$T_{JUNCTION\_REG}$	TREG[1:0] = 11		120		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature increasing		160		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}	Temperature falling		30		℃
JEITA Thermistor Comparator (Buck Mode)						
T1 (0℃) Threshold Voltage on TS Pin	V_{T1}	Charge suspends if temperature T is below T1 (T < T1), as percentage of V_{REGN}	72.75	73.25	73.75	%
T1 Falling		As percentage of V_{REGN}	71.35	71.85	72.35	%
T2 (10℃) Threshold Voltage on TS Pin	V_{T2}	Charge sets to I_{CHG}/2 and V_{REG} if T1 < T < T2, as percentage of V_{REGN}	67.75	68.25	68.75	%
T2 Falling		As percentage of V_{REGN}	66.35	66.85	67.35	%
T3 Rising	V_{T3}	As percentage of V_{REGN}	45.25	45.75	46.25	%
T3 (45℃) Threshold Voltage on TS Pin		Charge sets to V_{REG} - 200mV if T3 < T < T4, as percentage of V_{REGN}	44.25	44.75	45.25	%
T4 Rising	V_{T4}	As percentage of V_{REGN}	35.25	35.75	36.25	%
T4 (60℃) Threshold Voltage on TS Pin		Charge suspends if T > T4, as percentage of V_{REGN}	33.75	34.25	34.75	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Cold or Hot Thermistor Comparator (Boost Mode)							
Cold Temperature Threshold (TS Pin Voltage Rising Threshold)	V_{BCOLD}	As percentage to V_{REGN} (approx. -20℃ w/ 103AT)		79.5	80	80.5	%
TS Voltage Falling (Exit Cold Range)	V_{BCOLD_HYS}	As percentage to V_{REGN}			1		%
Hot Temperature Threshold (TS Pin Voltage Falling Threshold)	V_{BHOT}	As percentage to V_{REGN} (approx. 65℃ w/ 103AT)		30.75	31.25	31.75	%
TS Voltage Rising(Exit Hot Range)	V_{BHOT_HYS}	As percentage to V_{REGN}			3		%
PWM							
PWM Switching Frequency, and Digital Clock	f_{SW}	Oscillator frequency		1.35	1.5	1.65	MHz
Maximum PWM Duty Cycle	D_{MAX}				99		%
Boost Mode Operation							
Typical Boost Mode Regulation Voltage Range	$V_{OTG\_REG\_RANGE}$			4.55		5.51	V
Typical Boost Mode Regulation Voltage Step	$V_{OTG\_REG\_STEP}$				64		mV
Boost Mode Regulation Voltage Accuracy	$V_{OTG\_REG\_ACC}$	I_{VBUS} = 0A, BOOSTV[3:0] = 0111 (4.998V)		-2.2		1.2	%
Minimum Battery Voltage to Exit Boost Mode	V_{OTG_BAT1}	V_{BAT} falling	MIN_VBAT_SEL = 0	2.9	3	3.1	V
	V_{OTG_BAT2}		MIN_VBAT_SEL = 1	2.5	2.6	2.7	
Minimum Battery Voltage to Enter Boost Mode	$V_{OTG\_BAT\_EN}$	V_{BAT} rising	MIN_VBAT_SEL = 0	3.1	3.2	3.3	V
			MIN_VBAT_SEL = 1	2.7	2.8	2.9	
Typical Boost Mode Output Current Range	I_{OTG}			0.5		2.45	A
Boost Mode RBFET Over-Current Protection Accuracy	$I_{OTG\_OCP\_ACC}$	BOOST_LIM[2:0] = 010 (1.2A)		1.09	1.28	1.46	A
Boost Mode Over-Voltage Threshold	V_{OTG_OVP}	Rising threshold		5.85	5.975	6.1	V
REGN LDO							
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 5V, I_{REGN} = 20mA		4.36	4.57	4.78	V
		V_{VBUS} = 9V, I_{REGN} = 40mA		4.5	4.9	5.3	
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 5V, V_{REGN} = 3.8V		35	65	95	mA
Analog-to-Digital Converter (ADC)							
Resolution	RES	Rising threshold			7		bits
Typical Battery Voltage Range	V_{BAT_RANGE}	V_{VBUS} > V_{BAT} + V_{SLEEP} or OTG mode is enabled		2.304		4.844	V
		V_{VBUS} < V_{BAT} + V_{SLEEP} and OTG mode is disabled		V_{SYS_MIN}		4.844	
Typical Battery Voltage Resolution	V_{BAT_RES}				20		mV
Typical System Voltage Range	V_{SYS_RANGE}	V_{VBUS} > V_{BAT} + V_{SLEEP} or OTG mode is enabled		2.304		4.844	V
		V_{VBUS} < V_{BAT} + V_{SLEEP} and OTG mode is disabled		V_{SYS_MIN}		4.844	
Typical System Voltage Resolution	V_{SYS_RES}				20		mV
Typical V_{VBUS} Voltage Range	V_{VBUS_RANGE}	V_{VBUS} > V_{BAT} + V_{SLEEP} or OTG mode is enabled		2.6		15.3	V
Typical V_{VBUS} Voltage Resolution	V_{VBUS_RES}				100		mV
Typical Battery Charge Current Range	I_{BAT_RANGE}	V_{VBUS} > V_{BAT} + V_{SLEEP}		0		6.4	A
Typical Battery Charge Current Resolution	I_{BAT_RES}				50		mA
Typical Input Current Range	I_{VBUS_RANGE}	V_{VBUS} > V_{BAT} + V_{SLEEP}		0		3.25	A
Typical Input Current Resolution	I_{VBUS_RES}				50		mA
Typical TS Voltage Range	V_{TS_RANGE}			21		80.055	%
Typical TS Voltage Resolution	V_{TS_RES}				0.47		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic I/O Pin Characteristics (OTG, nCE, nQON)						
Input High Threshold	V_{IH}		0.85			V
Input Low Threshold	V_{IL}				0.4	V
High-Level Leakage Current	I_{IN_BIAS}	Pull up rail 1.8V			1	μA
Internal nQON Pull-Up	V_{QON}	Battery only mode		3.8		V
		V_{VBUS} = 9V		4		
		V_{VBUS} = 5V		4		
Internal nQON Pull-Up Resistance	R_{QON}			200		kΩ
Logic I/O Pin Characteristics (DSEL)						
Output Low Threshold	V_{OL}	I_{OL} = 2mA, C_{DSEL} = 47nF			0.1	V
Output High Threshold	V_{OH}	I_{OH} = 5mA, C_{DSEL} = 47nF, non-switching, I_{REGN} = 30mA	4.5			V
Logic I/O Pin Characteristics (INT, STAT)						
Output Low Threshold	V_{OL}	Sink current = 5mA			0.2	V
High-Level Leakage Current	I_{OUT_BIAS}	Pull up rail 1.8V			1	μA
I^2C Interface (SCL, SDA)						
Input High Threshold	V_{IH}	Pull up rail 1.8V	0.85			V
Input Low Threshold	V_{IL}	Pull up rail 1.8V			0.4	V
Output Low Threshold	V_{OL}	Sink current = 5mA			0.2	V
High-Level Leakage Current	I_{BIAS}	Pull up rail 1.8V			1	μA

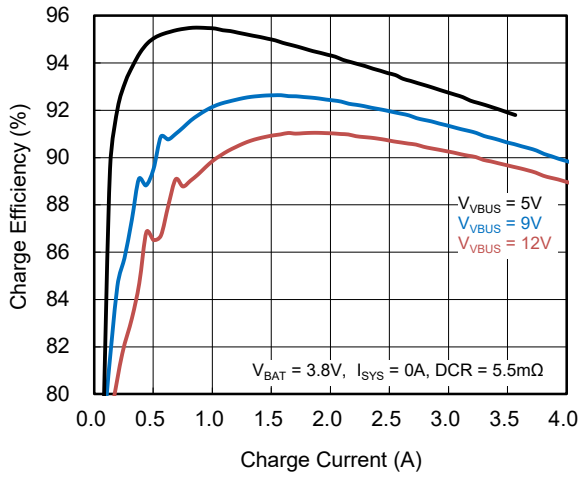
TIMING REQUIREMENTS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

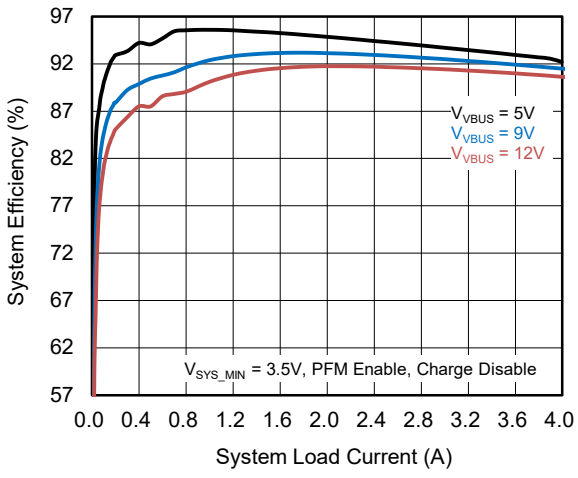
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up						
Wait Window for Bad Adaptor Detection	t_{BAD_SRC}			30		ms
BAT Over-Voltage Protection						
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}			4		ms
Battery Charger						
Recharge Deglitch Time	t_{RECHG}			20		ms
Current Pulse Control						
Current Pulse Control Stop Pulse	t_{PUMPX_STOP}		445		575	ms
Current Pulse Control Long on Pulse	t_{PUMPX_ON1}		295		395	ms
Current Pulse Control Short on Pulse	t_{PUMPX_ON2}		85		145	ms
Current Pulse Control off Pulse	t_{PUMPX_OFF}		85		145	ms
Current Pulse Control Stop Start Delay	t_{PUMPX_DLY}		115		180	ms
Battery Monitor						
Conversion Time	t_{CONV}	CONV_RATE = 0		1	1000	ms
nQON Timing and Ship Mode Timing						
nQON Negative Pulse Low Pulse Width to Turn on BATFET and Exit Ship Mode	$t_{SHIPMODE}$		0.5	1	1.6	s
nQON Low Time to Reset BATFET	t_{QON_RST}		5	10	16	s
BATFET off Time during Full System Reset	t_{BATFET_RST}		160	340	480	ms
Wait Delay for Entering Ship Mode	t_{SM_DLY}		6	13	19	s
I^2C Interface						
SCL Clock Frequency	f_{SCL}			400		kHz
Digital Clock and Watchdog Timer						
Digital Clock Frequency in Low Power	f_{LPDIG}	REGN LDO disabled	20	30	60	kHz
Digital Clock Frequency	f_{DIG}	REGN LDO enabled	1350	1500	1650	kHz
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 11, REGN LDO disabled	80	175		s
		WATCHDOG[1:0] = 11, REGN LDO enabled	140	165		

TYPICAL PERFORMANCE CHARACTERISTICS

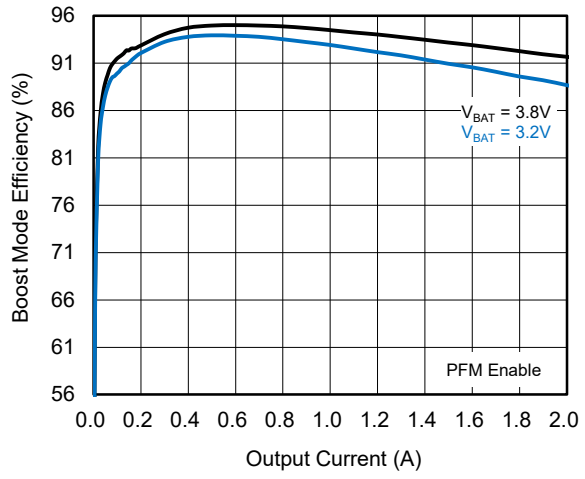
Charge Efficiency vs. Charge Current



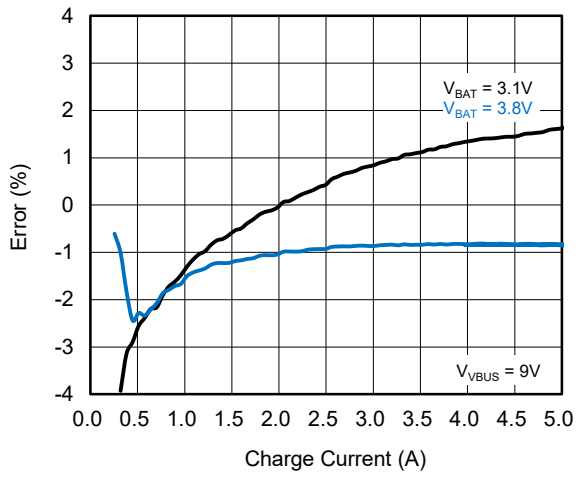
System Efficiency vs. System Load Current



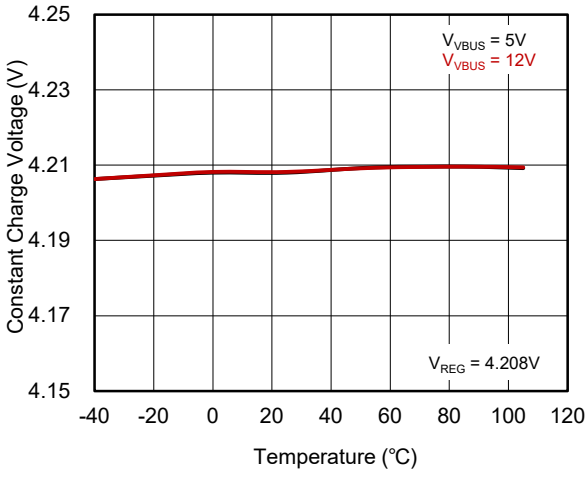
Boost Mode Efficiency vs. Output Current



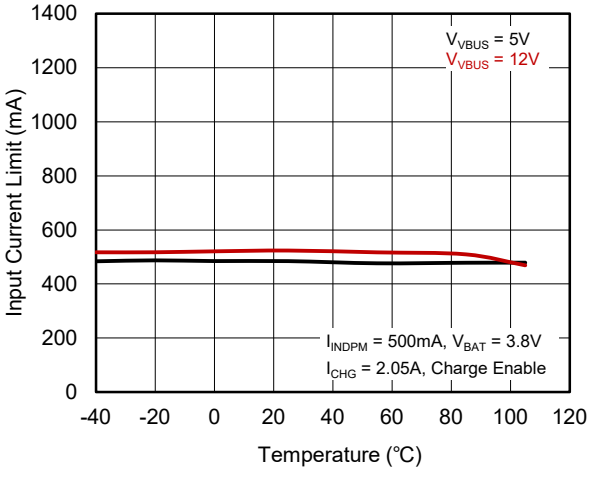
Charge Current Accuracy vs. Charge Current I²C Setting



Constant Charge Voltage vs. Temperature

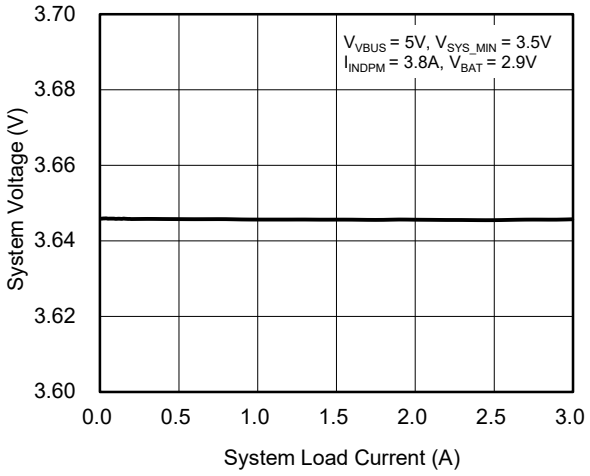


Input Current Limit vs. Temperature

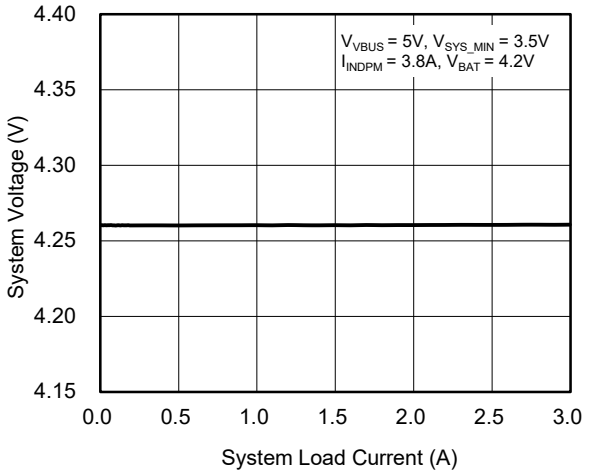


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

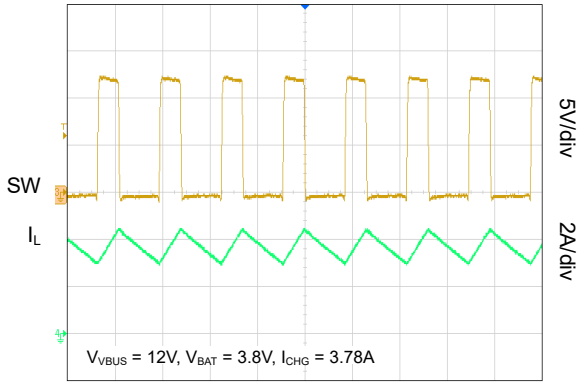
System Voltage vs. System Load Current



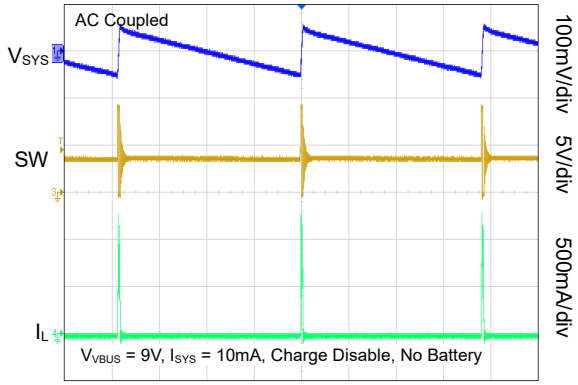
System Voltage vs. System Load Current



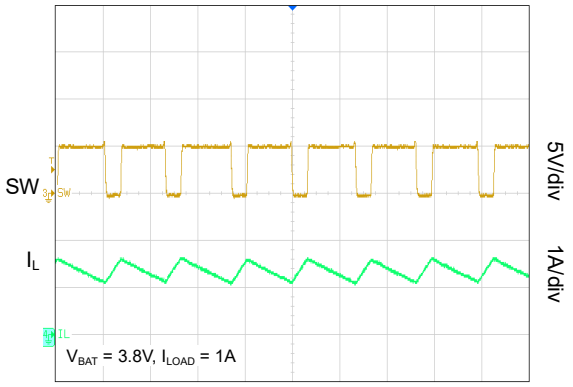
PWM Switching Waveform



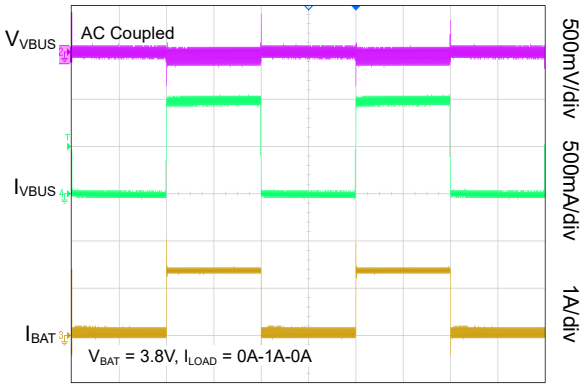
PFM Switching Waveform



Boost Mode Switching Waveform

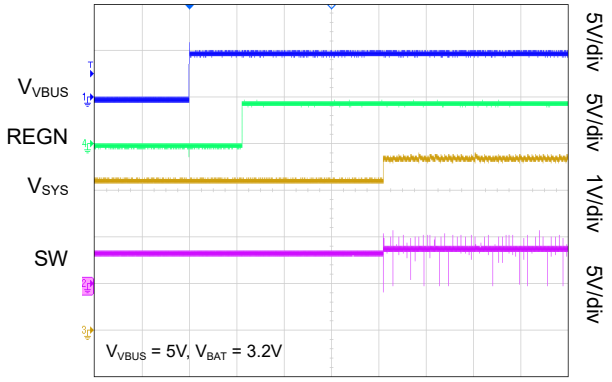


Boost Mode Load Transient



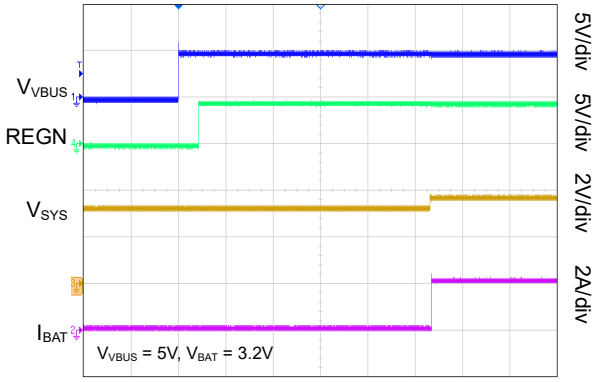
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power-Up with Charge Disable



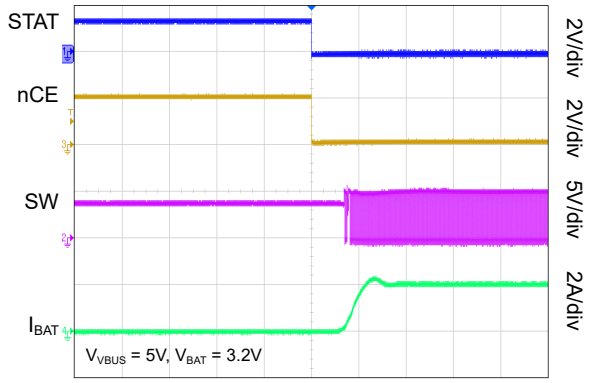
Time (100ms/div)

Power-Up with Charge Enable



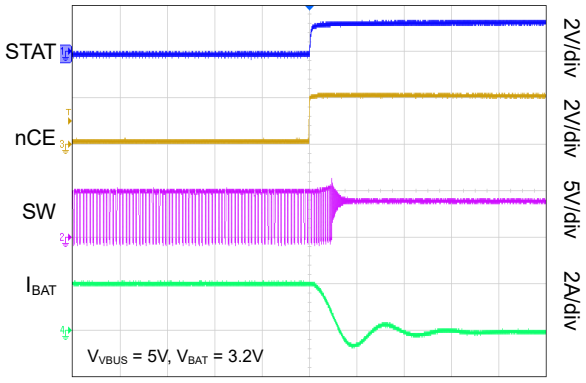
Time (100ms/div)

Charge Enable



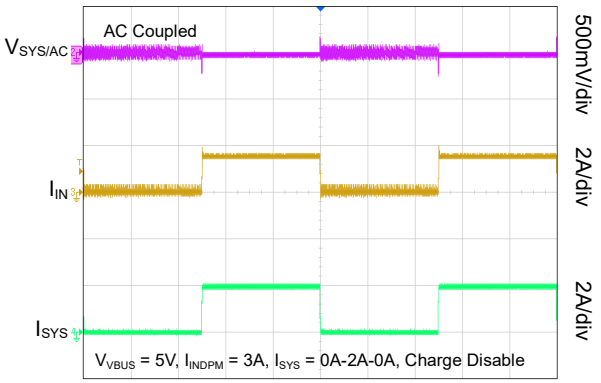
Time (50μs/div)

Charge Disable



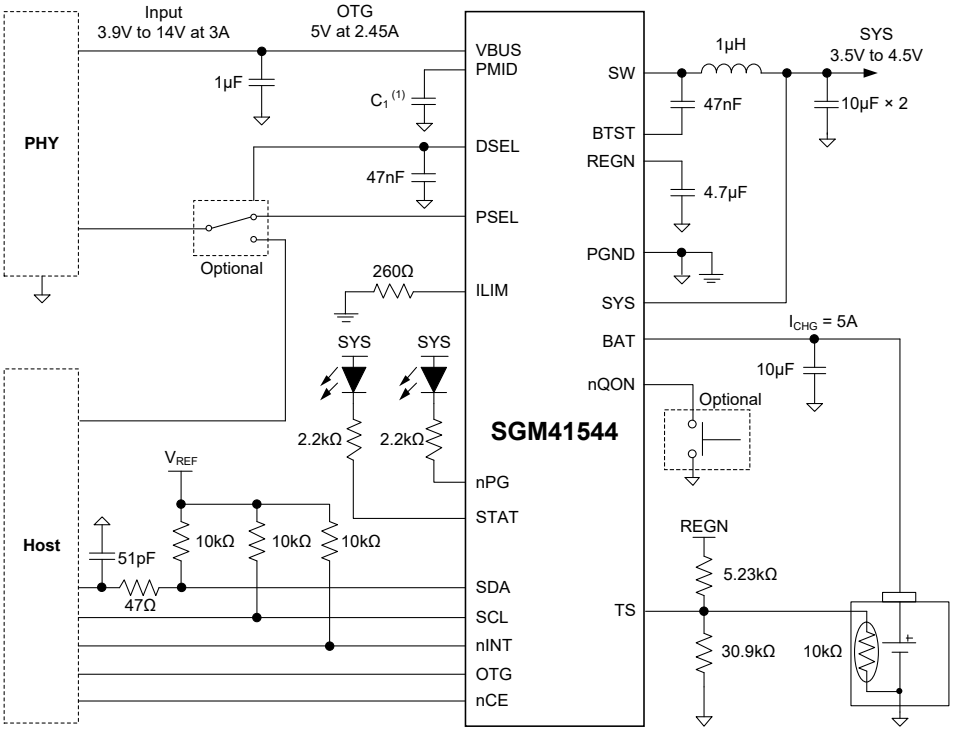
Time (10μs/div)

Input Current DPM Response without Battery



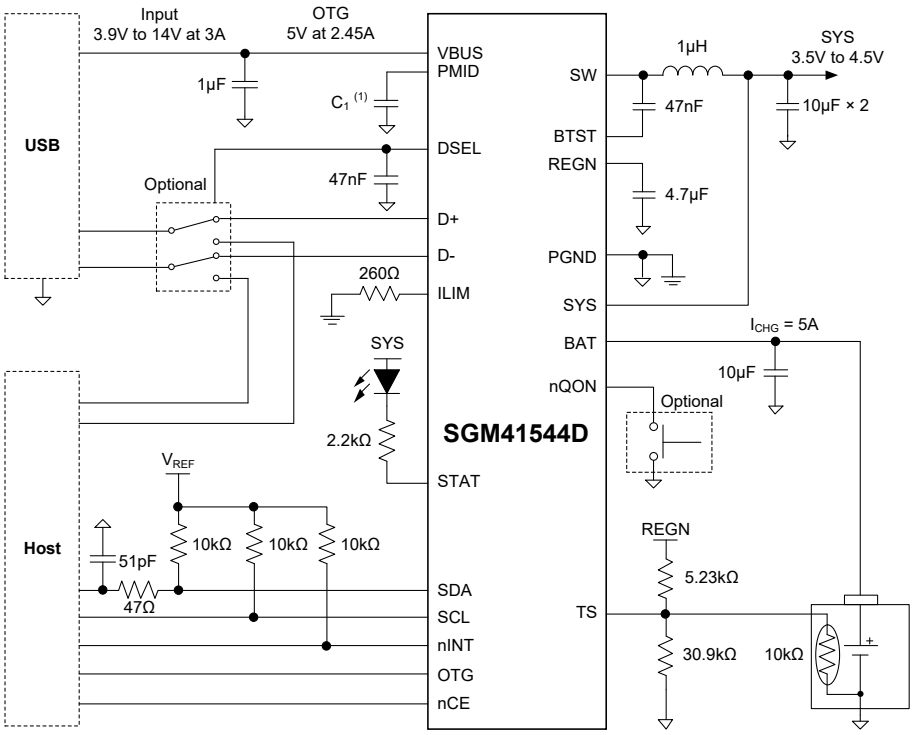
Time (2ms/div)

TYPICAL APPLICATION CIRCUITS



NOTE:
1. It is recommended that C_1 = 8.2μF (OTG ≤ 1.8A) or 20μF (OTG ≤ 2.45A).

Figure 1. SGM41544 Typical Application Circuit



NOTE:
1. It is recommended that C_1 = 8.2μF (OTG ≤ 1.8A) or 20μF (OTG ≤ 2.45A).

Figure 2. SGM41544D Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

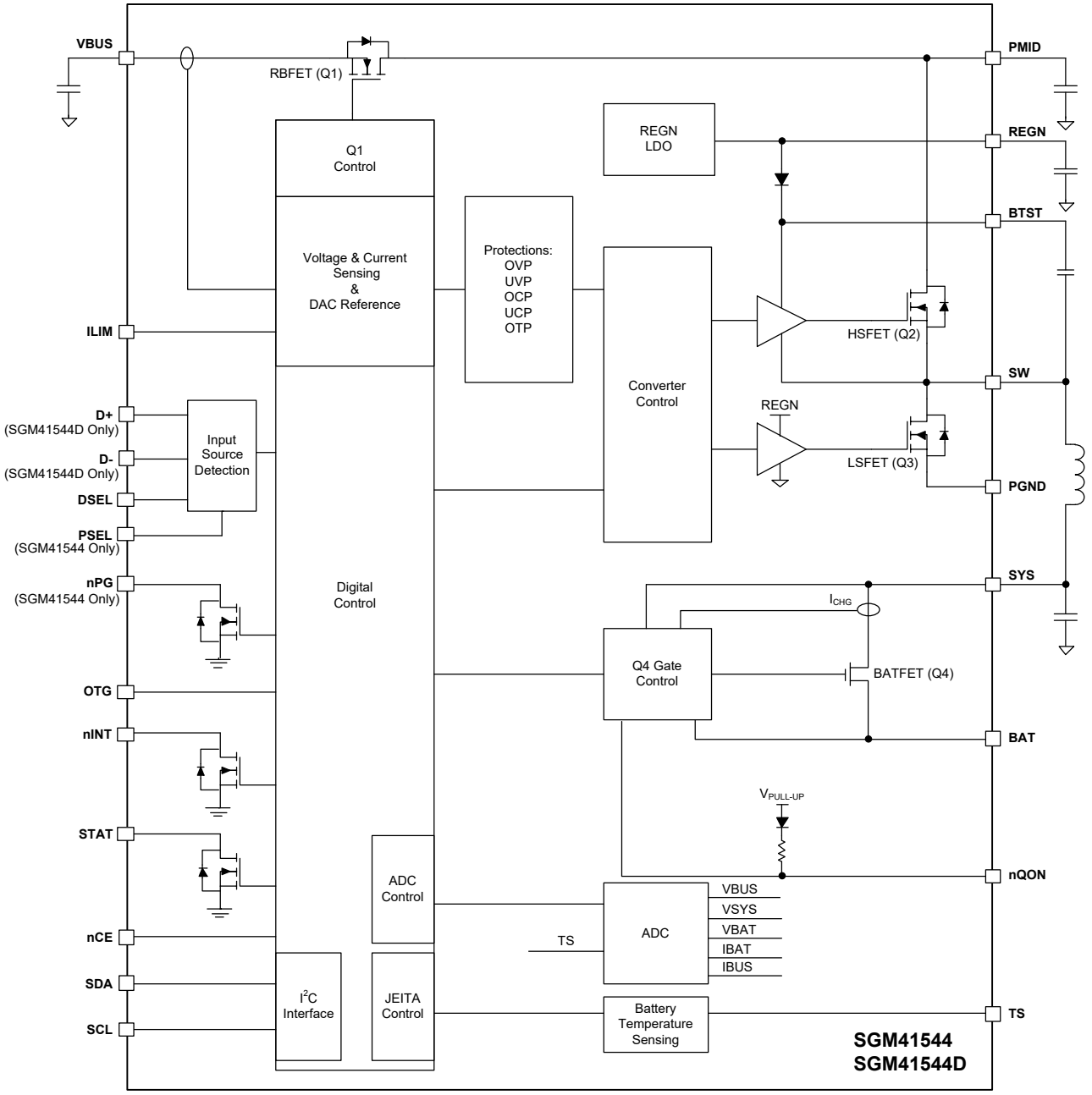


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM41544/SGM41544D are power management and charger devices for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The SGM41544/SGM41544D can accommodate a wide range of input sources including USB, wall adaptor and car chargers. It is optimized for 5V input (USB voltage) but is capable of operating with input voltages from 3.9V to 14V. It also supports JEITA profile for battery charging safety at high or low temperatures. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT) or both is another feature of the device. Battery charge current is programmable and can reach a maximum of 5A (charge). In the Boost mode, the battery voltage is boosted to power the VBUS pin (2.45A MAX) when it is a power receiving node (USB OTG) that is typically regulated to 5V.

The device may operate in several different modes:

In HIZ mode, the reverse blocking FET (Q1), internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it supplies DC power to the system through BATFET.

In the sleep mode, the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VBUS}) is not high enough for charging the battery. In other words, V_{VBUS} is smaller than V_{BAT} + V_{SLEEP} (where V_{SLEEP} is a small threshold) and Buck converter is not able to charge, even at its maximum duty cycle. The Boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VBUS} is almost equal to or smaller than V_{BAT}).

In supplement mode, the input source power is not enough to supply system demanded power and the battery assists by discharging to the system in parallel and providing the deficit.

Power-On Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}), a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I^2C interface will also be ready for communication and all registers reset to their default values.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time.

The discharge current through BATFET is continuously monitored. In the supplement mode, if a system overload (or short) occurs (I_{BAT} > I_{BATFET_OCP}), the BATFET is turned off immediately and BATFET_DIS bit is set to 1. The BATFET will not enable until the input source is applied or one of the BATFET Enable Mode (Exit Ship Mode) methods (explained later) is used to activate the BATFET.

Power-Up Process from the Input Power Source

Upon connection of an input source (VBUS), its voltage sensed from VBUS pin is checked to turn on the internal REGN LDO regulator and the bias circuits (whether the battery is present or not). The input current limit is determined and set before the Buck converter is started. The sequences of actions when VBUS as input source is powered up are:

1. REGN LDO power-up.
2. Poor power source detection (qualification).
3. Input power source type detection. (Based on D+/D- or PSEL input. It is used to set the default input current limit (IINDPM[5:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers and TS rail (thermistor pin). The STAT pin can also be pulled up to REGN. The REGN enables when the following two conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

1. $V_{VBUS} > V_{VBUS\_PRESENT}$.
2. $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ (in Buck mode) or $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in Boost mode).

In HIZ state, the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is powered only by the battery in HIZ mode.

Poor Power Source Detection (Qualification)

When REGN LDO is powered, the input source (adaptor) is checked for its type and current capacity. To start the Buck converter, the input (VBUS) must meet the following conditions:

1. $V_{VBUS} < V_{VBUS\_OV}$
2. $V_{VBUS} > V_{VBUS\_MIN}$ during t_{BAD_SRC} test period (30ms TYP) in which the I_{BAD_SRC} (30mA TYP) current is pulled from VBUS.

If the test is failed, the conditions are repeatedly checked every two seconds. As soon as the input source passes qualification, the VBUS_GD bit in status register is set to 1 and a pulse is sent to the nINT pin to inform the host. Type detection will start as the next step.

Input Power Source Type Detection

When EN_AUTO_INDET bit is set to 1, the input source detection will run through the D+/D- lines or the PSEL pin while REGN LDO is powered and after the VBUS_GD bit is set. The SGM41544D can detect the input source types, which include SDP/CDP/DCP and non-standard adaptor through the D+/D- pins following USB BC1.2 specification. In addition, after DCP is detected, it can detect HVDCP when EN_HVDCP bit is set to 1. The SGM41544 sets the input current limit through PSEL pin. A pulse is sent to nINT pin to inform the host when the input source type detection is completed. Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINDPM[5:0]) is changed to set current limit.
2. PG_STAT (power good) bit is set.
3. VBUS_STAT[2:0] register is updated to indicate USB or adaptor input source types.

The input current is always limited by the IINDPM[5:0] register and the limit can be updated by the host if needed. Regardless of the input current optimizer (ICO) setting, the charger input current is always limited by the lower value of the IINDPM[5:0] register or the current limit set by ILIM pin.

The input power source type detection is ignored if EN_AUTO_INDET = 0. In this case, the IINDPM[5:0] register remains unchanged and the VBUS_STAT[2:0] bits keep 000 (no input).

Input Current Limit by PSEL (SGM41544)

PSEL pin interfaces with USB physical layer (PHY) for input current limit setting. The USB PHY device output is used to detect if the input is a USB host or a charging port. In the host-control mode, the host must enable FORCE_INDET bit for reading the PSEL value and updating the IINDPM[5:0] register. In the default mode, the IINDPM[5:0] register is updated automatically by PSEL value in real-time as given in Table 1.

Table 1. Input Current Limit Setting from PSEL

Input Detection	PSEL Pin	Input Current Limit (I_{LIM})	VBUS_STAT[2:0]
USB Host SDP	High	500mA	001
Adaptor	Low	2400mA	010

Input Current Limit by D+/D- Detection (SGM41544D)

The input current limit of SGM41544D is determined and set by the integrated D+/D- based input power source detection. Five major steps are included in the D+/D- detection: VBUS detection, data contact detect (DCD, detect non-standard adaptor), primary detection (detect SDP adaptor), secondary detection (detect CDP adaptor and DCP adaptor), and high voltage detection (detect HVDCP adaptor). Please refer to Figure 4 and Table 2.

If HVDCP detection is enabled (EN_HVDCP = 1 and EN_12V = 1), the SGM41544D continues to proceed the HVDCP handshakes to adjust the adaptor output voltage to 9V or 12V for fast charging.

After the input power source type detection is completed, the nINT pin sends out a low pulse to notify the host and the VBUS_STAT[2:0] register, IINDPM[5:0] register are updated as Table 3.

DETAILED DESCRIPTION (continued)

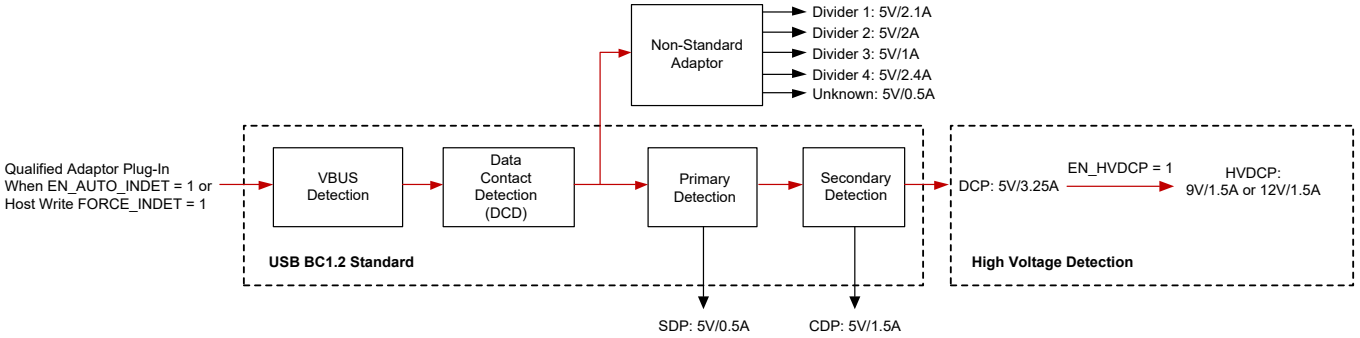


Figure 4. D+/D- Based USB BC1.2 Detection Flow

Table 2. Non-Standard Adaptor Type Detection

Non-Standard Adaptor	D+ Threshold	D- Threshold	Input Current Limit (A)
Divider 1	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P0_VTH}	2.1
Divider 2	V_{D+} within V_{1P2_VTH}	V_{D-} within V_{1P2_VTH}	2
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P7_VTH}	1
Divider 4	V_{D+} within V_{2P7_VTH}	V_{D-} within V_{2P7_VTH}	2.4

Table 3. Input Current Limit Setting from D+/D- Detection

D+/D- Detection	Input Current Limit (IINDPM)	VBUS_STAT[2:0]
USB SDP (USB500)	500mA	001
USB CDP	1.5A	010
USB DCP	3.25A	011
Divider 1	2.1A	110
Divider 2	2A	110
Divider 3	1A	110
Divider 4	2.4A	110
Adjustable High Voltage DCP	1.5A	100
Unknown Adaptor	500mA	101

Some notes for HVDCP detection:

1. The registers do not have the EN_9V bit, so it is enabled by default, and the EN_12V bit has higher priority.

2. If a non-QC adaptor plug-in and the HVDCP related bits are enabled, the HVDCP detection will fail, and the VBUS_STAT[2:0] keeps 011 to indicate the USB DCP adaptor.

3. If a QC adaptor plug-in and the HVDCP related bits are disabled, there is no HVDCP detection and the VBUS_STAT[2:0] also keeps 011 to indicate the USB DCP adaptor.

Force Detection of Input Current Limit

The host can set FORCE_INDET bit to 1 in host mode to force the device to run. And the FORCE_INDET bit returns to 0 by itself and input result is updated after the detection is completed.

D+/D- Output Voltage Setting (SGM41544D)

The host can set different status on SGM41544D D+ or D- pins via DP_DAC[2:0] and DM_DAC[2:0] registers. The D+ pin status can be set to HIZ (default), 0V, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V, and D- pin status can be set to HIZ (default), 0V, 0.6V, 1.2V, 2.0V, 2.7V or 3.3V. But DP_DAC[2:0] and DM_DAC[2:0] will be reset to default value when adaptor plug-in. If D+/D- status change is required for more QC adaptor detection, host should set the DP_DAC[2:0] and DM_DAC[2:0] registers after input source D+/D- detection is done. The D+/D- status change command during D+/D- detection period will be ignored.

DETAILED DESCRIPTION (continued)

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

A wide voltage range (3.9V to 15.3V) is supported for the input voltage limit. When the adaptor plug-in (VBUS_GD bit from 0 to 1), the VINDPM[6:0] register is updated to the value based on VINDPM_OS bit and the FORCE_VINDPM bit is reset to 0 (default) if it is set. If V_{VBUS} < 6V, the VINDPM[6:0] register is updated to (V_{VBUS} - VINDPM_OS), else the VINDPM[6:0] register is updated to (V_{VBUS} - 2 × VINDPM_OS). Then the VINDPM[6:0] register is read only and will keep unchanged regardless of the value of V_{VBUS}. The VINDPM[6:0] register can only be written when FORCE_VINDPM = 1, and the VINDPM[6:0] register will return to the initial value of the adaptor plug-in when set FORCE_VINDPM bit from 1 to 0.

The device supports dynamic tracking of the battery voltage (VINDPM). VDPM_BAT_TRACK[1:0] bits can be used to enable tracking (00 to disable tracking) and set the tracking offset value. When the tracking is enabled, the input voltage limit will be set to the larger value between the VINDPM[6:0] and V_{BAT} + VDPM_BAT_TRACK[1:0]. The VDPM_BAT_TRACK[1:0] tracking offset can be set to 200mV, 250mV or 300mV.

DC/DC Converter Power-Up

The 1.5MHz switching converter composed of LSFET and HSFET is enabled, which can start switching when the input current limit is set. Converter is initiated with a soft-start when the system voltage is ramped up. If SYS voltage is less than 2.2V, the input current is limited to 200mA or IINDPM[5:0], depending on whichever is smaller, otherwise the limit is set to the lower value of ILIM pin and IINDPM[5:0] (EN_ICO = 0) or ICO_ILIM[5:0] (EN_ICO = 1).

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

When converter operates for battery charging, it acts as an efficient, fixed frequency synchronous Buck converter regardless of the input/output voltages and currents. However, it is capable of switching to PFM mode at light load when charging is disabled or when the detected battery voltage is less than minimum system voltage setting. PFM operation can be enabled or prevented in either Buck or Boost mode through using the PFM_DIS bit.

Input Current Optimizer (ICO)

The SGM41544/SGM41544D provide the input current optimizer (ICO) to identify the input adaptor source maximum power point. To avoid the input adaptor source overload and staying in VINDPM, the ICO algorithm identifies maximum input current limit of the adaptor automatically and updates this input current limit to ICO_ILIM[5:0] register.

The ICO function is default enabled, and it can be disabled by the host through setting EN_ICO bit to 0. After a DCP type power source is detected, the ICO algorithm runs automatically when EN_ICO bit is valid. The host can set FORCE_ICO bit to force the ICO algorithm regardless of input source type detected under EN_ICO bit to 1 condition.

The actual input current limit is reported by ICO_ILIM[5:0] register in ICO mode, while it is decided by the IINDPM[5:0] register when out of ICO mode. In addition, the actual input current is also limited by an external resistor at ILIM pin when EN_ILIM = 1.

When the ICO algorithm is activated, it runs to dynamically and continuously adjust the input current limit using ICO_ILIM[5:0] register. During the adjustment, the ICO_OPTIMIZED bit changes until they are finally set. The operation of ICO algorithm depends on the battery voltage as following:

Case 1: When V_{BAT} < V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[5:0] register with an initial value that equals the IINDPM. Where the IINDPM is the maximum input current limit determined by the system.

Case 2: When V_{BAT} > V_{SYS_MIN}, the device starts ICO algorithm by ICO_ILIM[5:0] register with an initial value of 500mA. The 500mA is minimum input current limit which minimizes the input power source overload.

During the optimization, if VINDPM is triggered, the ICO algorithm decreases the input current limit (the dynamic ICO_ILIM[5:0] register) to avoid input source overloading. When the maximum input current limit is detected, the ICO_ILIM[5:0] register reflects the optimal maximum input current limit which does not trigger VINDPM. The ICO_OPTIMIZED bit is updated to 1 to indicate the maximum input current is detected.

In above case 1, if both VINDPM and IINDPM are not triggered at ICO_ILIM[5:0] initial value, the ICO_ILIM[5:0] register keeps the initial value and the ICO_OPTIMIZED = 0 to indicate the ICO optimization is in process. If the load becomes heavy, the VINDPM still not be triggered but IINDPM is triggered, and the ICO algorithm is also completed. The ICO_ILIM[5:0] register keeps the initial value still, and the ICO_OPTIMIZED bit is updated to 1 to indicate the maximum input current detected.

DETAILED DESCRIPTION (continued)

In above case 2, if the VINDPM is not triggered and the converter is under light load condition, the ICO_ILIM[5:0] gives the input current limit a little higher than the actual input current (500mA minimum input current limit). The ICO_OPTIMIZED bit remains 0 to indicate the ICO optimization is in process. If the load becomes heavy, the ICO algorithm automatically runs to set new ICO_ILIM[5:0] register value.

Once the ICO algorithm is completed (ICO_OPTIMIZED = 1), the ICO_ILIM[5:0] register will keep un-change unless one of the following events occurs. Each of the following events can force the ICO algorithm to run again and reset the ICO_OPTIMIZED bit to 0:

1. EN_HIZ bit is toggled or re-plugin the input source.
2. Host changes the IINDPM[5:0] register.
3. Host changes the VINDPM[6:0] register.
4. Host sets the FORCE_ICO bit to 1.
5. Resume from VBUS_OVP.

Boost Mode

The SGM41544/SGM41544D support USB On-The-Go (OTG). When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (Boost mode) with 1.5MHz/500kHz (by setting BOOST_FREQ bit) switching frequency to supply power from the battery to that load. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is invalid when the OTG_CONFIG bit is set. The USB OTG output current limit requirement is achieved by programming. However, the Boost converter can deliver 2.45A to the output (maximum limit). The converter will be set to Boost mode if at least 30ms is passed from enabling this mode (OTG pin HIGH and OTG_CONFIG bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{OTG\_BAT\_EN}$
2. $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in sleep mode).
3. Acceptable voltage range at TS pin ($V_{BHOT} < V_{TS} < V_{BCOLD}$).

The output voltage is set to V_{VBUS} = 5V and is maintained as long as V_{BAT} is above $V_{OTG\_BAT\_EN}$. The output current can reach up to the programmed value by BOOST_LIM[2:0] bits (2.45A MAX). The VBUS_STAT[2:0] status register bits are set to 111 in Boost mode (OTG).

To minimize the output overshoot in Boost mode, the device starts with PFM first and then switches to PWM. As stated before, PFM can be avoided by using PFM_DIS bit in Buck and Boost modes.

Host Mode and Default Mode Operation with Watchdog Timer

After a power-on reset, the device starts in default mode (standalone) with all registers reset as default. If the watchdog timer is expired, the device will also enter default mode with WATCHDOG_FAULT bit set to high. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41544/SGM41544D operate like an autonomous charger. The battery is charged for 12 hours (default value for the fast charging safety timer). Then the charge stops while Buck converter continues to operate to power the system load. In this mode, the WATCHDOG_FAULT bit is high.

Most of the flexibility features of the SGM41544/SGM41544D become available in the host mode when the device is controlled by a host with I^2C. By setting the WD_RST bit to 1, the charger mode changes from default mode to host mode. In this mode, the WATCHDOG_FAULT bit is low and all device parameters can be programmed by the host. To prevent device watchdog from being reset that results in going back to default mode, the host must disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_RST bit to prevent WATCHDOG_FAULT bit from being set. Every time a 1 is written to the WD_RST bit, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to their default values except for IINDPM[5:0], DP_DAC[2:0], DM_DAC[2:0], EN_12V, VINDPM_OS, EN_ICO, EN_HVDCP, EN_MAXDCP, EN_AUTO_INDET, FORCE_DSEL, SYS_MIN[2:0], BATFET_DIS, BATFET_DLY, EN_BATFET_RST, PFM_DIS, FORCE_VINDPM, VINDPM[6:0], EN_ICHG_MON[1:0], OVP[1:0], VDPM_BAT_TRACK[1:0], VINDPM_INT_MASK, IINDPM_INT_MASK bits that keep their values unchanged.

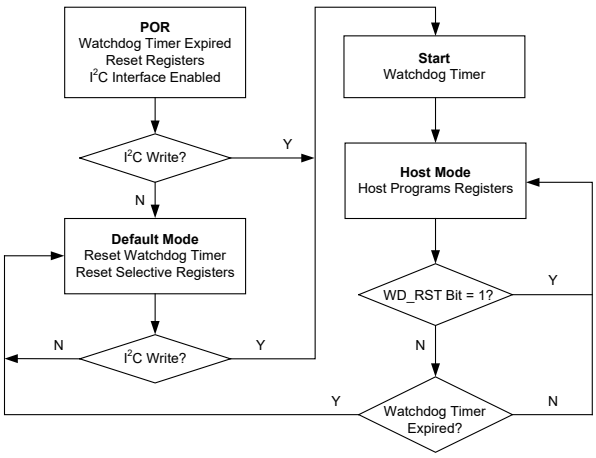


Figure 5. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41544/SGM41544D are designed for charging single-cell Li-Ion or Li-poly batteries with a charge current up to 5A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path and features low on-resistance (17mΩ TYP) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if CHG_CONFIG = 1 and nCE pin is pulled low. In default mode, the SGM41544/SGM41544D run a charge cycle with the default parameters itemized in Table 4. At any moment, the host can control the charging operations by writing the registers.

Table 4. Charging Parameter Default Setting

Default Mode	SGM41544/SGM41544D
Charging Voltage (V_{REG})	4.208V
Charging Current (I_{CHG})	2.048A
Pre-Charge Current (I_{PRECHG})	128mA
Termination Current (I_{TERM})	256mA
Temperature Profile	JEITA
Safety Timer	12h

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied, a new charge cycle starts:

- NTC temperature fault is not asserted (TS pin).
- Safety timer fault is not asserted.
- BATFET is not forced off (BATFET_DIS bit = 0).
- Charging enabled (3 conditions: CHG_CONFIG bit = 1, ICHG[6:0] register is not 0mA and nCE pin is low).
- Battery voltage is below the programmed full charge level (V_{REG}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{REG} - 100mV or V_{REG} - 200mV configured by VRECHG bit). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the nCE pin or CHG_CONFIG bit.

Normally, a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or dynamic power management (DPM) mode.

Charge Status Report

The STAT is an open-drain output pin that reports the status of charge and can drive an LED for indication: a low indicates that charging is in progress, a high shows that charging is completed or disabled and alternating low/high (blinking) show a charging fault. The STAT may be disabled (keep the open-drain switch off) by setting EN_ICHG_MON[1:0] = 10 or 11.

The CHRG_STAT[1:0] status register reports the present charging phase and status by two bits: 00 = charging disabled, 01 = in pre-charge, 10 = in fast charging (constant current mode or constant voltage mode) and 11 = charging completed.

A negative pulse is sent on nINT pin to inform the host when a charging cycle is completed. In addition, the output status of STAT pin can be set by STAT_SET[1:0] bits, 00 = LED off (HIZ), 01 = LED on (low), 10 = LED blinking at 1s on 1s off, 11 = LED blinking at 1s on 3s off. This two bits only take effect when EN_ICHG_MON[1:0] = 01.

Battery Charging Profile

The SGM41544/SGM41544D feature a full battery charging profile with five phases. In the beginning of the cycle, the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 5. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are trickle charge (V_{BAT} < 2.2V), pre-charge and fast-charge (constant current and constant voltage).

Table 5. Charging Current Setting Based on V_{BAT}

V_{BAT} Voltage	Selected Charging Current	Default Value in the Register	CHRG_STAT[1:0]
< 2.2V	I_{SHORT}	90mA	01
2.2V to 3V	I_{PRECHG}	128mA	01
> 3V	I_{CHG}	2048mA	10

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified. The charge current will be less than the value in the register. The termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

DETAILED DESCRIPTION (continued)

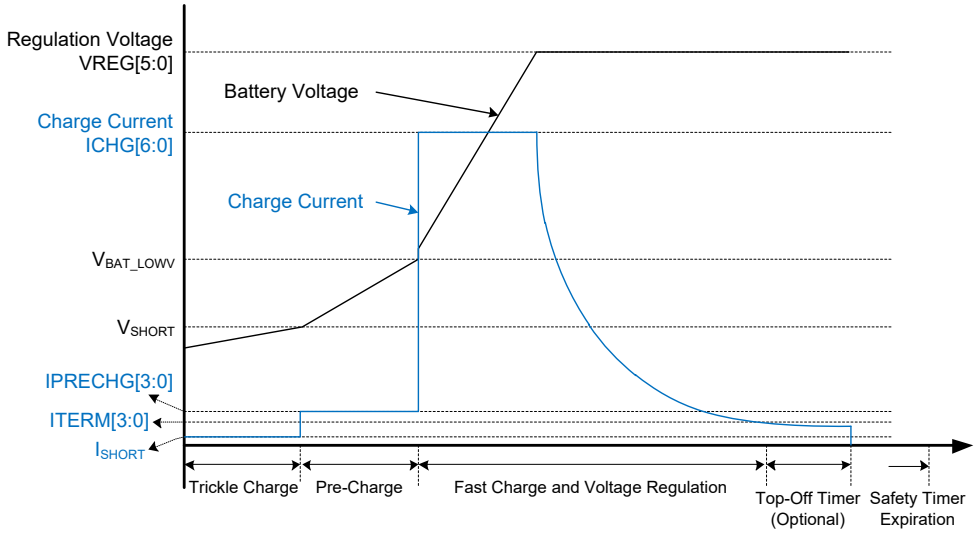


Figure 6. Battery Charging Profile

Charge Termination

A charge cycle is terminated when the battery voltage is higher than the recharge threshold and the charge current falls below the programmed termination current. Unless there is a high power demand for system and it needs to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the Buck converter operates continuously to supply the system.

The CHRG_STAT[1:0] bits are set to 11 and a negative pulse is sent to nINT pin after termination.

If the charger is regulating input current, input voltage or junction temperature instead of charge current, termination will be temporarily prevented. The EN_TERM bit is termination control bit and can be set to 0 to disable termination before it happens.

At low termination currents (256mA TYP), the offset in the internal comparator may give rise to a higher (+10mA to +20mA) actual termination current. A delay in termination can be added (optional) as a compensation for comparator offset using a programmable top-off timer. During the delay, constant voltage charge phase continues and gives the falling charge current a chance to drop closer to the programmed value. The top-off delay timer has the same restrictions of the safety timer. As an example, under some conditions, if the safety timer is suspended, the top-off timer will also be suspended or if the safety timer is slowed down, the termination timer will also be slowed down. The TOPOFF_ACTIVE bit reports the active/inactive status of the top-off timer. The CHRG_STAT[1:0] and TOPOFF_ACTIVE bits can be read to find status of the termination.

Any of the following events resets the top-off timer:

1. Disable to enable transition of nCE (charge enable).
2. A low to high change in the status of termination.
3. Set REG_RST bit to 1.

The setting of the top-off timer is applied at the time of termination detection and unless a new charge cycle is started, modifying the top-off timer parameters after termination has no effect. A negative pulse is sent to nINT when top-off timer is started or ended.

Resistance Compensation (IRCOMP)

When in a high-current charging system, the resistance between the charger output and the battery cell terminals (such as MOSFETs, connectors, circuit board routing, and sense resistors) can force the charging process to change prematurely from constant current to constant voltage and prolong the charging time. The SGM41544/SGM41544D feature resistance compensation (IRCOMP) to speed up charge cycles and extend constant current charge time while providing the maximum power to the battery.

The host can compensate the resistance by increasing the charge voltage set point that is based on the actual charge current and resistance, as shown in the following formula. It is recommended that the host sets the maximum allowed regulation voltage register (VCLAMP[2:0]) and the minimum resistance compensation (BATCOMP) for the safe operation.

$$V_{REG\_ACTUAL} = VREG + \min\left(I_{CHRG\_ACTUAL} \times BATCOMP, V_{CLAMP}\right) \quad (1)$$

DETAILED DESCRIPTION (continued)

Temperature Qualification

The charging current and voltage of the battery must be limited when battery is cold or hot. A thermistor input for battery temperature monitoring is included in the device that can protect the battery based on JEITA guidelines.

Compliance with JEITA Guideline

JEITA guideline (April 20, 2007 release) is implemented in the device for safe charging of the Li-Ion battery. JEITA highlights the considerations and limits that should be considered for charging at cold or hot battery temperatures. High charge current and voltage must be avoided outside the normal operating temperatures (typically 0℃ and 60℃). This functionality can be disabled if not needed. Four temperature levels are defined by JEITA from T1 (minimum) to T4 (maximum). Outside this range, charging should be stopped. The corresponding voltages sensed by NTC are named V_{T1} to V_{T4}. Due to the sensor negative resistance, a higher temperature results in a lower voltage on TS pin. The battery cool range is between T1 and T2, and the warm range is between T3 and T4. Charge must be limited in the cool and warm ranges.

One of the conditions for starting a charge cycle is having the TS voltage within V_{T1} to V_{T4} window limits. If the battery is too cold or too hot during charging and TS voltage exceeds the T1 - T4 limits, charging is suspended (zero charge current) and the controller waits for the battery temperature to come back within the T1 to T4 window.

JEITA recommends reducing charge current to 1/2 of fast charging current or lower at cool temperatures (T1 - T2). For warmer temperature (within T3 - T4 range), charge voltage is recommended to V_{REG} - 200mV.

The SGM41544/SGM41544D exceed the JEITA requirement by their flexible charge parameter settings. At warm temperature range (T3 - T4), the charge voltage is set to V_{REG}, V_{REG} - 100mV, V_{REG} - 200mV, V_{REG} - 300mV by the JEITA_VSET_H[1:0] bits, and the charge current can be reduced down to 0%, 20% or 50% of fast charging current by the JEITA_ISET_H[1:0] bits. At cool temperatures (T1 - T2), the current setting can be reduced down to 50% or 20% of fast charging current selected by the JEITA_ISET_L bit when EN_JEITA_ISET_L = 1, and the charge voltage is set to V_{REG} when JEITA_VSET_L = 0, the charge voltage is set to V_{REG} - 200mV when JEITA_VSET_L = 1. In addition, the cool threshold T2 and warm threshold T3 can be changed through JEITA_VT2[1:0] and JEITA_VT3[1:0], and the charge current can be disabled by setting EN_JEITA_ISET_L = 0.

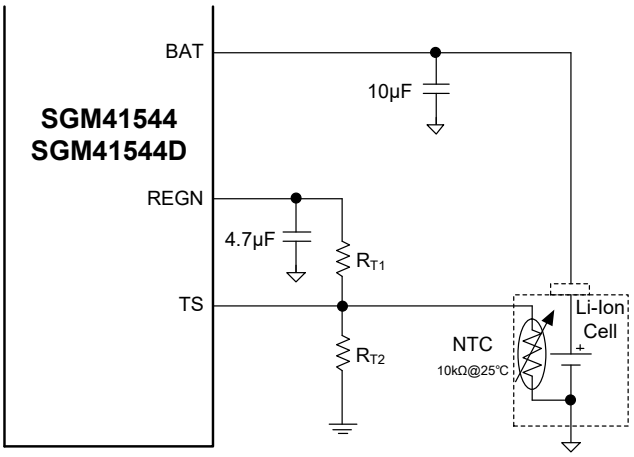


Figure 7. Battery Thermistor Connection and Bias Network

A 103AT-2 type thermistor is recommended to use for the SGM41544/SGM41544D. Other thermistors may be used and bias network (see Figure 7) can be calculated based on the following equations:

$$R_{T2} = \frac{R_{THCOLD} \times R_{THHOT} \times \left(\frac{1}{V_{T1}} - \frac{1}{V_{T4}}\right)}{R_{THHOT} \times \left(\frac{1}{V_{T4}} - 1\right) - R_{THCOLD} \times \left(\frac{1}{V_{T1}} - 1\right)} \quad (2)$$

$$R_{T1} = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{R_{T2}}\right) + \left(\frac{1}{R_{THCOLD}}\right)} \quad (3)$$

Where, V_{T1} and V_{T4} are T_{COLD} and T_{HOT} threshold voltage on TS pin as percentage to V_{REGN}, R_{THCOLD} and R_{THHOT} are thermistor resistances (R_{TH}) at desired T1 (Cold) and T4 (Hot) temperatures. Select T_{COLD} = 0℃ and T_{HOT} = 60℃ for Li-Ion or Li-polymer batteries. For a 103AT-2 type thermistor R_{THCOLD} = 27.28kΩ and R_{THHOT} = 3.02kΩ, the calculation results are: R_{T1} = 5.29kΩ and R_{T2} = 31.17kΩ. The standard value of R_{T1} is 5.23kΩ and that of R_{T2} is 30.9kΩ.

DETAILED DESCRIPTION (continued)

Boost Mode Temperature Monitoring (Battery Discharge)

The device is capable of monitoring the battery temperature for safety during the Boost mode. The temperature must remain within the V_{BCOLD} to V_{BHOT} thresholds, otherwise the Boost mode will be suspended and VBUS_STAT[2:0] bits are set to 000. Moreover, NTC_FAULT[2:0] bits are updated to report Boost mode cold or hot condition. Once the temperature returns within the right window, the Boost mode is resumed and NTC_FAULT[2:0] bits are cleared to 000 (normal).

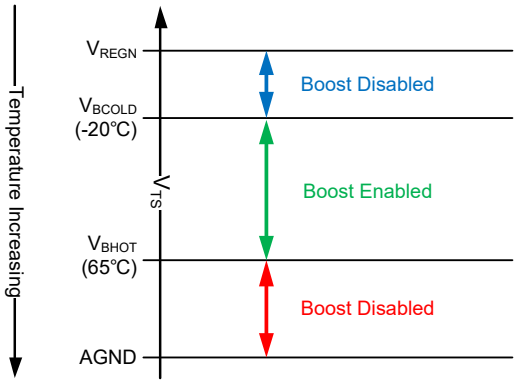


Figure 8. TS Pin Thermistor Temperature Window Settings in Boost Mode

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, CHRG_FAULT[1:0] bits are set to 11 and a negative pulse is sent to nINT pin. By default, the charge time limit is 4.5 hours if the battery voltage does not rise above V_{BAT_LOWV} threshold. And it is 12 hours if it goes above V_{BAT_LOWV}. This feature is optional and can be disabled by clearing EN_TIMER bit. The 12 hours limit can also be changed to 5, 8 or 20 hours by setting CHG_TIMER[1:0] bits.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation, JEITA cool or thermal regulation. Because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 12 hours and the charger is regulating the input current (IINDPM_STAT bit = 1) in the whole charging cycle, the actual safety time will be 24 hours. Clearing the EN_TMR2X bit will disable the half clock rate feature.

The safety timer is paused if a fault occurs or charger is in supplement mode, charging is suspended. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling nCE pin or CHG_CONFIG bit, the timer resets and restarts a new timing.

Narrow Voltage DC (NVDC) Design in SGM41544/SGM41544D

The SGM41544/SGM41544D feature an NVDC design using the BATFET that connects the system to the battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using Buck converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. SYS_MIN[2:0] register sets the minimum system voltage (default 3.5V). If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is below the minimum system voltage setting. The system voltage is regulated to 150mV (TYP) above the minimum system voltage setting. The battery is gradually charged and its voltage rises above the minimum system voltage and lets BATFET change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 60mV (TYP) above the battery voltage if:

1. The charging is terminated.
2. Charging is disabled and the battery voltage is above the minimum system voltage setting.

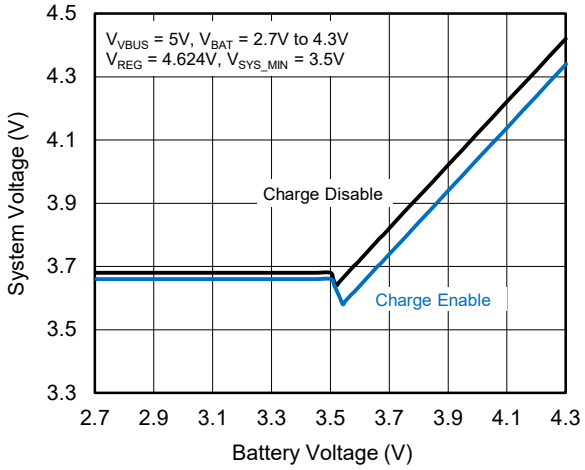


Figure 9. System Voltage vs. Battery Voltage

DETAILED DESCRIPTION (continued)

SGM41544/SGM41544D Dynamic Power Management (DPM)

The SGM41544/SGM41544D feature a dynamic power management (DPM). To implement DPM, the device always monitors the input current and voltage to regulate power demand from the source and avoid input adaptor overloading or to meet the maximum current limits specified in the USB specs. Overloading an input source may result in either current trying to exceed the input current limit (I_{INDPM}) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the VSYS regulating to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduced to satisfy $I_{IN} \le I_{INDPM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINDPM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case, the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINDPM_STAT or VINDPM_STAT status bits are set during an IINDPM or VINDPM respectively. Figure 10 summarizes the DPM behavior (IINDPM type) for a design example with a 9V/1.2A adaptor, 3.2V battery, 2.8A charge current setting and 3.4V minimum system voltage setting.

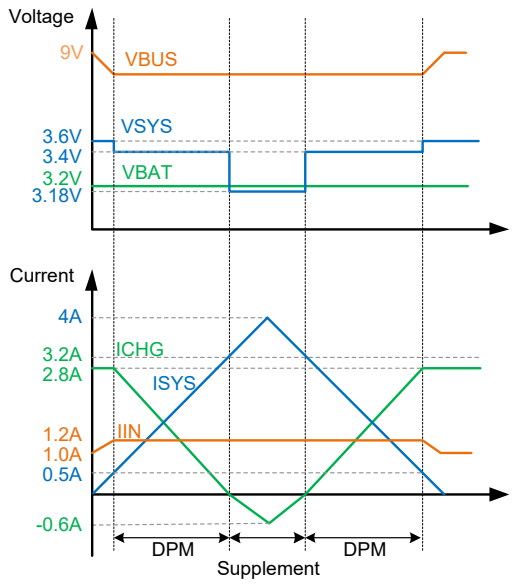


Figure 10. Input, Battery and System Voltage and Currents in DPM

Battery Supplement Mode

If the system voltage drops 45mV below the battery voltage, the BATFET gradually starts to turn on. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation) such that the BATFET V_{DS} stays at 25mV. At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Using the MOSFET linear mode at lower currents prevents swinging oscillation from entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 11. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

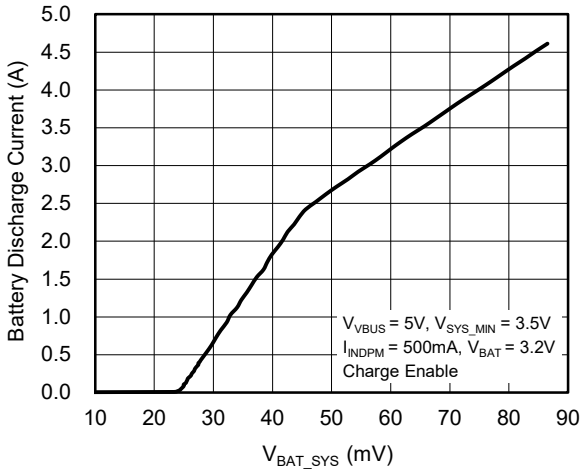


Figure 11. BATFET Gate Regulation V-I Curve

Battery Monitor

The device has a battery monitor that can provide measurements of input voltage, battery voltage, system voltage, thermistor ratio, charging current and input current, based on the device modes of operation and REG0x21 register. The measurements are reported in battery monitor registers (REG0x0E - REG0x12, REG0x20). The battery monitor has two conversion modes by using CONV_RATE bit: one-shot conversion (default) and 1 second continuous conversion.

For the one-shot conversion (CONV_RATE = 0), the conversion will start when the CONV_START bit is set and which conversion is active depends on REG0x21. The CONV_START bit is set during the conversion and cleared by the device when the conversion is completed. The conversion result is provided after t_{CONV} (1s MAX).

DETAILED DESCRIPTION (continued)

For the continuous conversion (CONV_RATE = 1), the conversion will start when the CONV_RATE bit is set and all conversions are active. During an active conversion, setting the CONV_START bit indicates that the conversion is in progress. The conversion result is provided every 1 second automatically. The battery monitor ends continuous conversion when the CONV_RATE bit is cleared.

When the battery monitor is active, the REGN power is enabled, which can increase the quiescent current.

Table 6. Battery Monitor Operation Modes

Parameter	Enable	Register	Operation Modes			
			Charge Mode	Boost Mode	Charge Disable	Battery Only Mode
Battery Voltage (V_{BAT})	REG0x21[4]	REG0x0E	Yes	Yes	Yes	Yes
System Voltage (V_{SYS})	REG0x21[3]	REG0x0F	Yes	Yes	Yes	Yes
Temperature (TS) Voltage (V_{TS})	REG0x21[2]	REG0x10	Yes	Yes	Yes	Yes
VBUS Voltage (V_{VBUS})	REG0x21[5]	REG0x11	Yes	Yes	Yes	N/A
Charge Current (I_{BAT})	REG0x21[6]	REG0x12	Yes	N/A	N/A	N/A
Input Current (I_{VBUS})	REG0x21[7]	REG0x20	Yes	N/A	Yes	N/A

Status Outputs Pins (nPG, STAT, nINT and DSEL)

Power Good Indication (nPG Pin and PG_STAT Bit)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high and the nPG pin goes low. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$.
- Device is not in sleep mode: $V_{VBUS} > V_{BAT} + V_{SLEEP}$.
- Input source is not poor: $V_{VBUS} > V_{VBUS\_MIN}$ (3.8V TYP) when I_{BAD_SRC} (30mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection.

Charge Status (STAT Pin)

Charging state is indicated with the open-drain STAT pin as explained in Table 7. This pin is able to drive an LED (see Figure 1 or Figure 2). The functionality of the STAT pin is disabled if the EN_ICHG_MON[1:0] bits are set to 10 or 11.

Table 7. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charging completed	High (LED OFF)
Charging is disabled or in sleep mode	High (LED OFF)
Charge is suspended due to input over-voltage, TS fault, timer faults or system over-voltage or Boost mode is suspended (TS fault)	1Hz Blinking

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt, it can react and check the charger situation on time.

The following events can generate an interrupt pulse:

1. Faults reflect in REG0x0C register (watchdog, Boost overload, charge faults and battery over-voltage).
2. Charging is completed.
3. PSEL or D+/D- detection identifies a connected source (USB or adaptor).
4. Input source voltage enters the "input good" range:
   a) V_{VBUS} exceeds V_{BAT} (not in sleep mode).
   b) V_{VBUS} comes below V_{VBUS_OV}.
   c) V_{VBUS} remains above V_{VBUS_MIN} (3.8V TYP) when I_{BAD_SRC} (30mA TYP) load current is applied.
5. Input removes or out of the "input good" range.
6. A DPM event (VINDPM or IINDPM) occurs (a maskable interrupt).

Once a fault/flag happens, the nINT pulse is asserted immediately and the fault bits are updated in REG0x0C. Fault status is not reset in the register until the host reads it. A new fault will not assert a new nINT pulse until the host reads REG0x0C and all the previous faults are cleared. Therefore, in order to read the current time faults, the host must read REG0x0C two times consecutively. The first read returns the history of the fault register status (from the time of the last read or reset) and the second one checks the current active faults. As an exception, the NTC_FAULT[2:0] bits report the actual real-time status of TS pin.

DETAILED DESCRIPTION (continued)

D+/D- Multiplexer Selection Control (DSEL Pin)

The DSEL pin is normally grounded and pulled-up by internally to REGN during the D+/D- detection. For SGM41544, the pin is normally low and can be set to high by FORCE_DSEL bit. For SGM41544D, the pin is pulled high during input source type detection (when EN_AUTO_INDET = 1 or FORCE_INDET = 1). After the detection is completed, the pin remains high logic when DCP or HVDCP is detected. The pin returns to logic low when the other input source type is detected and the FORCE_DSEL bit can be set to force the DSEL pin to change from low to high.

For SGM41544/SGM41544D, when in battery only mode (not in OTG), the DSEL pin is always low and when in OTG mode, the DSEL pin can be changed to high by FORCE_DSEL bit.

BATFET Control for System Power Reset and Ship Mode

Ship Mode (BATFET Disable)

Ship mode is usually used when the system is stored or in idle state for a long time or is in shipping. In such conditions, it is better to completely disconnect battery and make system voltage zero to minimize the leakage and extend the battery life. To enter ship mode, the BATFET has to be forced off by setting BATFET_DIS bit. The BATFET turns off immediately if BATFET_DLY bit is 0, or turns off after a t_{SM_DLY} delay (13 seconds) if BATFET_DLY bit is set.

Exit Ship Mode (BATFET Enable)

To exit the ship mode and enable the BATFET, one of the following can be applied:

With the chip no power by VBUS:

1. Connect the adaptor to the input with a valid voltage to the VBUS input.
2. Pull nQON pin from logic high to low to enable BATFET, for example, by shorting nQON to PGND. The negative pulse width should be at least a $t_{SHIPMODE}$ (1s TYP) for deglitching.

With the chip already powered by VBUS:

3. Clear BATFET_DIS bit by using host and I^2C.
4. Set REG_RST bit to 1 to reset all registers.
5. Apply a negative pulse to nQON pin (same as 2).

Full System Reset with BATFET Using nQON

When the input source is not present, the BATFET can act as a load on/off switch between the system and battery. This feature can be used to apply a power-on reset to the system. Host can toggle BATFET_DIS bit to cycle power off/on and reset the system. A push-button connected to nQON pin or a negative pulse can also be used to manually force a system power cycle when BATFET is ON (BATFET_DIS bit = 0). For this function, a negative logic pulse with a minimum width of t_{QON_RST} (10s TYP) must be applied to the nQON pin that results in a temporary BATFET turn-off for t_{BATFET_RST} (340ms TYP) that automatically turns on afterward. This functionality can be disabled by setting EN_BATFET_RST bit to 0.

Current Pulse Control Protocol

The SGM41544/SGM41544D provides the control to generate the VBUS current pulse protocol that communicates with an adjustable high voltage adaptor to inform the adaptor to increase/decrease the output voltage. To enable the interface, the EN_PUMPX bit must be set. The host relies on setting the PUMPX_UP or PUMPX_DN bit to select the increase/decrease voltage pulse to start the VBUS current pulse sequence. When in the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate the pulse sequence in progress, and the device pulses the input current limit between the current limit specified in the IINDPM[5:0] register and the 100mA current limit. When the pulse sequence is completed, the input current limit is returned to the value set by the IINDPM[5:0] register and the PUMPX_UP or PUMPX_DN bit is cleared. Besides, the EN_PUMPX bit can be cleared during the current pulse sequence to terminate the sequence and force the charger to immediately return to the input current limit specified in the IINDPM[5:0] register. When the EN_PUMPX bit is set to low, writes to the PUMPX_UP and PUMPX_DN bits are ignored, which has no effect on VBUS current limit.

Input Current Limit on ILIM Pin

The device has an additional hardware pin on ILIM to clamp input current limit for safe operation. A resistor between ILIM pin and PGND can set the clamped input current limit as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (4)$$

For example, if EN_ILIM = 1 and the IINDPM[5:0] register is 3A , a 260Ω resistor is connected between ILIM and ground, the actual input current limit is clamped to 1.31A (K_{ILIM} = 340 TYP). When ILIM pin voltage is higher than 0.8V, the SGM41544/SGM41544D clamp the input current and enter input current regulation. The same behavior as entering IINDPM through IINDPM[5:0] register, the IINDPM_STAT bit is also set and SGM41544/SGM41544D report a nINT if the IINDPM_INT_MASK bit is 0.

DETAILED DESCRIPTION (continued)

When EN_ILIM = 1 and the input current is not clamped by ILIM pin, the ILIM pin voltage (V_{ILIM}, lower than 0.8V) is proportional to the actual input current. In this case, the input current can be monitored and calculated by:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (5)$$

For example, with a 260Ω ILIM resistor, the 0.4V ILIM voltage corresponds to 0.65A input current. If ILIM pin is shorted to PGND, the ILIM will not help on limiting the input current and the limit is set by the IINDPM[5:0] register. If ILIM pin is open, the ILIM voltage will float above 0.8V, and the input current is limited to zero.

Setting EN_ILIM bit to 0 can disable the ILIM pin clamping function as well as the input current monitoring function. Either enable or disable ILIM pin function operation takes effect immediately.

SGM41544/SGM41544D Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (V_{VBUS} and V_{SYS}) and switch currents are constantly monitored to assure safe operation of the device in both Buck and Boost modes, as described below.

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage (VBUS_OVP)

Converter switching will stop as soon as VBUS voltage exceeds V_{VBUS_OV} over-voltage limit that is programmable by OVP[1:0] in REG0x17. It is selectable among 5.5V, 6.5V, 10.5V and 14V (default) for USB or 5V, 9V or 12V adaptors respectively.

Each time VBUS exceeds the OVP limit, a nINT pulse is asserted. As long as the over-voltage persists, the CHRG_FAULT[1:0] bits are set to 01 in REG0x0C. Fault will be cleared to 00 if the voltage comes back below limit (and a hysteresis threshold) and host reads the fault register. Charger resumes its normal operation when the voltage comes back below OVP limit.

2. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold is 350mV + V_{SYS_REG} (system regulation voltage + 350mV). Once a SYSOVP occurs, switching stops to clamp any overshoot and a 26mA sink current is applied to SYS to pull the voltage down.

Boost Mode Voltage and Current Monitoring

In Boost mode, the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Soft-Start on VBUS

Boost mode begins with a soft-start to prevent large inrush currents when it is enabled.

2. Output Short Protection for VBUS

Short-circuit protection is provided for VBUS output in Boost mode. To accept different types of load connected to VBUS and OTG adaptation, an accurate constant current regulation control is implemented for Boost mode. In case of a short-circuit on VBUS pin, the device operates in Hiccup. When in Hiccup, the Q1 turns off for 60ms and try to restart. Also, a nINT pulse is sent and the BOOST_FAULT bit is set to 1 in REG0x0C. If the short is removed, the device will return to normal operation and the BOOST_FAULT bit will be cleared.

3. Output Over-Voltage Protection for VBUS

In Boost mode, converter stops switching and exits Boost mode (by clearing OTG_CONFIG bit) if VBUS voltage rises above regulation and exceeds the V_{OTG_OVP} over-voltage limit (5.95V TYP). A nINT pulse is sent and the BOOST_FAULT bit is set to 1.

SGM41544/SGM41544D Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of +120℃ is considered for maximum IC surface temperature in Buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to +120℃ (thermal regulation mode) and sets the THERM_STAT bit to 1. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the junction temperature exceeds T_{SHUT} (+160℃), thermal shutdown protection arises in which the converter is turned off, CHRG_FAULT[1:0] bits are set to 10 in the fault register and a nINT pulse is sent.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the converter resumes automatically.

DETAILED DESCRIPTION (continued)

Boost Mode Thermal Protections

Similar to Buck mode, T_J is monitored in Boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (+160 ℃), the Boost mode will be disabled (OTG_CONFIG bit clears). If T_J falls below the hysteresis band of T_{SHUT_HYS} (30℃ under T_{SHUT}), the Boost can recover again by re-enabling OTG_CONFIG bit by host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 4% above the battery regulation voltage setting. In case of a BATOVP, charging or external direct charging stops right away, the BAT_FAULT bit is set to 1 and a nINT pulse is sent.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level ($V_{BAT\_DPL\_FALL}$), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. In such condition, the battery will start charging with the small I_{SHORT} current (90mA TYP) first as long as V_{BAT} < V_{SHORT}. When battery voltage is increased and V_{SHORT} < V_{BAT} < V_{BAT_LOWV}, the charge current will increase to the pre-charge current level programmed in the IPRECHG[3:0] register.

Battery Over-Current Protection for System

The BATFET will latch off, if its current limit is exceeded due to a short or large overload on the system (I_{BAT} > I_{BATFET_OCP}). To reset this latch off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41544/ SGM41544D parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41544/SGM41544D operate as a slave device that address is 0x6A (6AH). It has 28 8-bit registers, numbered from REG0x00 to REG0x21. A register read beyond REG0x21 (0x21) returns 0xFF.

Physical Layer

The standard I²C interface of SGM41544/SGM41544D supports standard mode and fast mode communication speeds. The frequency of standard mode is up to 100kbits/s, while the fast mode is up to 400kbits/s. Bus lines are pulled high by weak current source or pull-up resistors are in logic high state with no clocking when the bus is free. The SDA pin is open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started through taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 12. All transactions are started by master which applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy. By the way, only a master can send out the START and STOP signals.

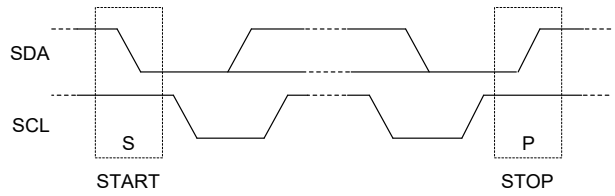


Figure 12. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 13.

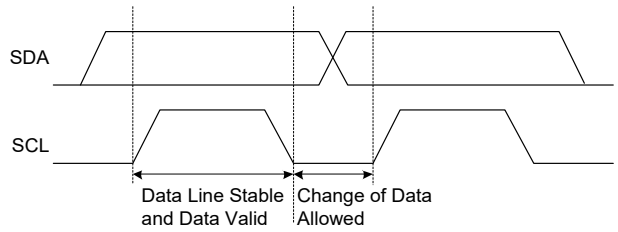


Figure 13. I²C Bus Bit Transfer

DETAILED DESCRIPTION (continued)

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 14 shows the byte transfer process with I^2C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The 7-bit slave address is 1101010b (0x6A). The address bit arrangement is shown in Figure 15 and the data transfer transaction is shown in Figure 16.

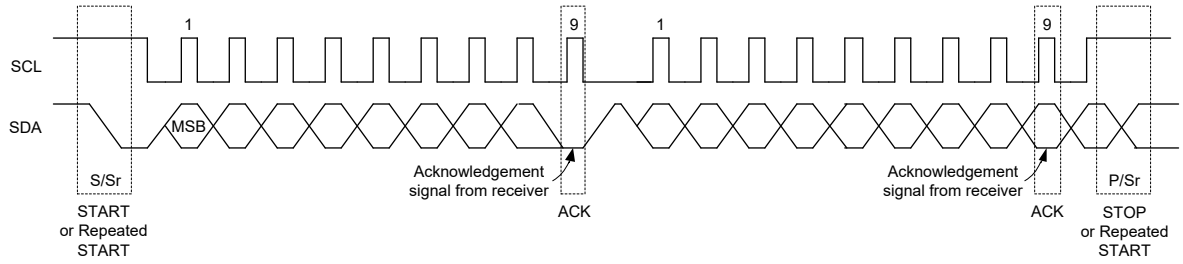


Figure 14. Byte Transfer Process

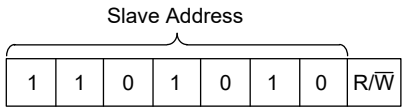


Figure 15. 7-Bit Address Format (0x6A)

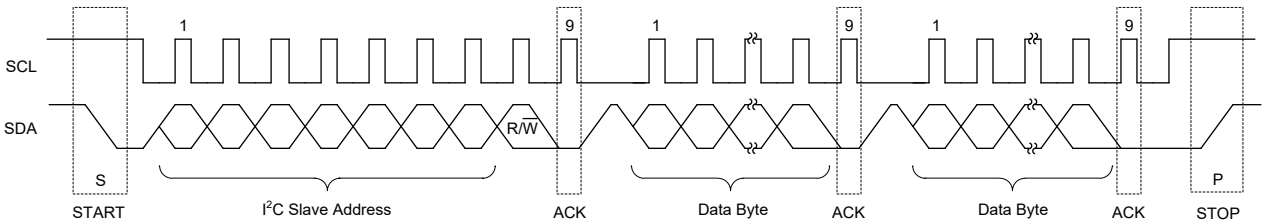


Figure 16. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 17 for a single write data transfer. After receiving the ACK, the master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 18), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, the master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

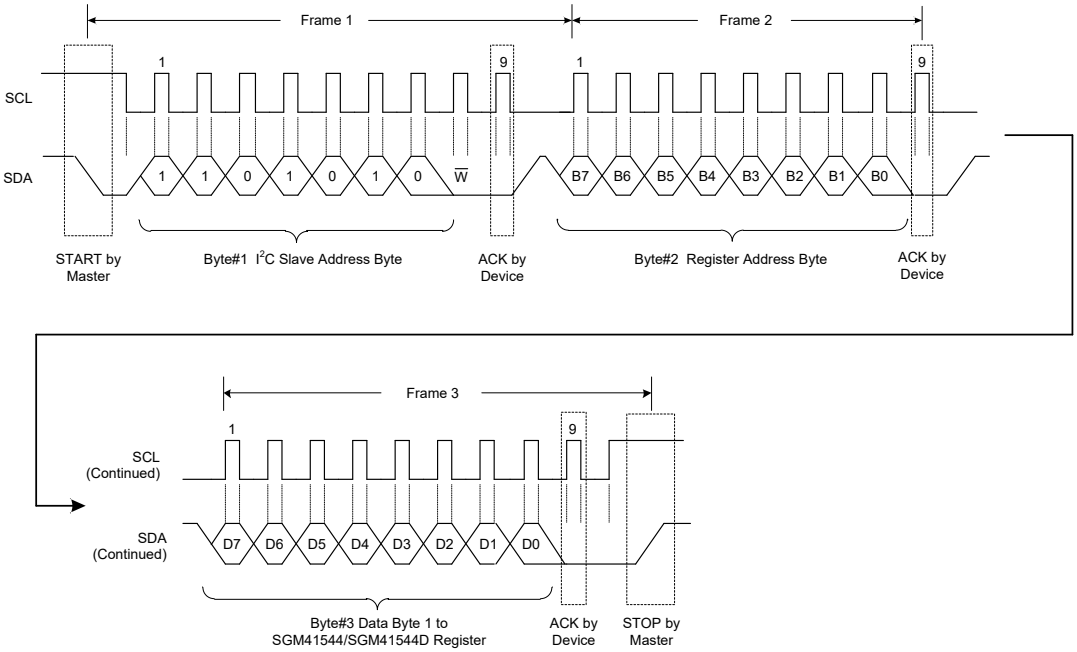


Figure 17. A Single Write Transaction

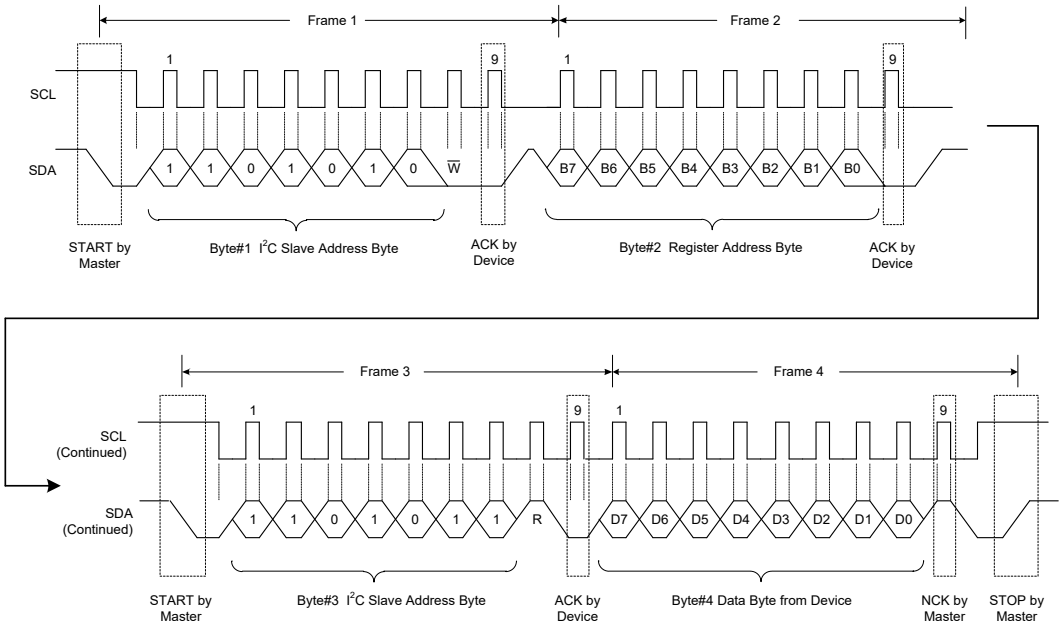


Figure 18. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41544/SGM41544D for REG0x00 through REG0x21 registers, as explained in Figure 19 and Figure 20.

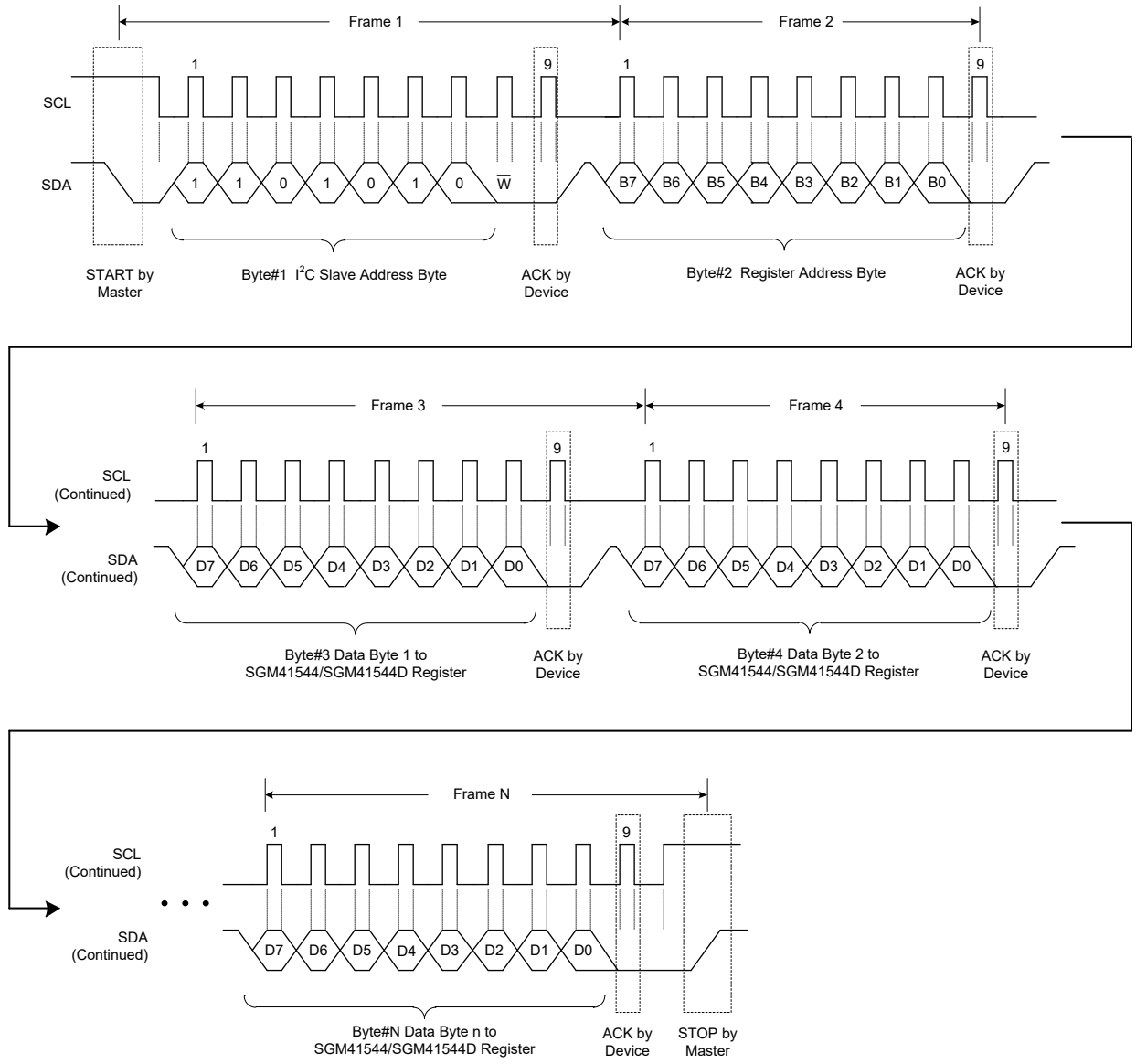


Figure 19. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

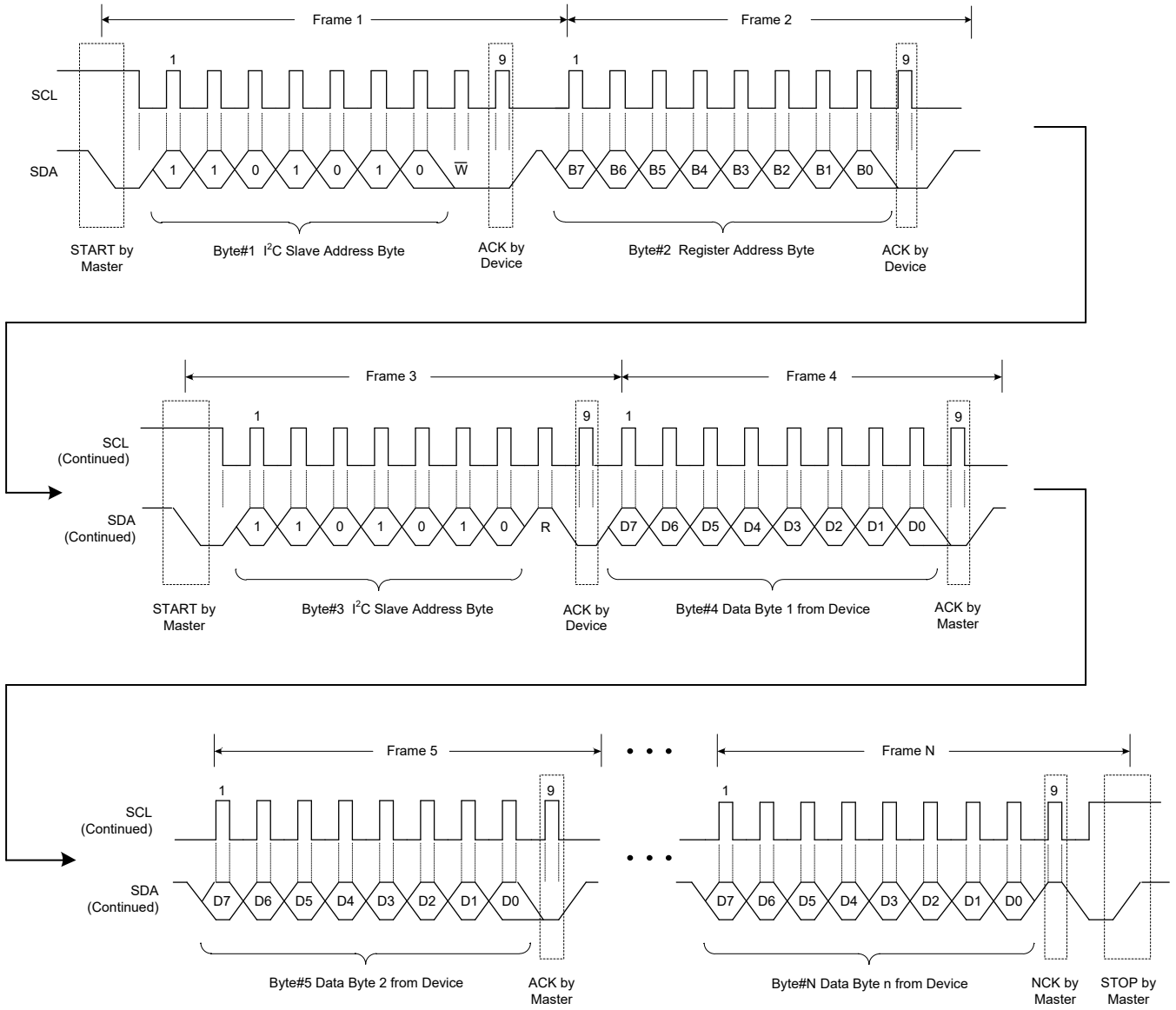


Figure 20. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Register Address Map

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
CHARGE	0x0B[4:3]	—	—	—	0x03[4]
VREG	0x19[7]	—	—	0x06[7:2] + 0x15[5]	—
VREG_FT	—	—	—	0x15[7:6]	0x15[7:6]
ICHG	—	—	—	0x04[6:0]	—
IPRECHG	—	—	—	0x05[7:4]	—
ITERM	—	—	—	0x05[3:0]	0x07[7]
VRECHG	—	—	—	0x06[0]	—
BATLOWV	—	—	—	0x06[1]	—
IRCOMP	—	—	—	0x08[7:5] + 0x08[4:2]	—
CHG_TIMER	0x0C[5:4]	—	—	0x07[2:1]	0x07[3]
TOPOFF_TIMER	0x19[6]	—	—	0x17[5:4]	0x17[5:4]
TMR2X	—	—	—	—	0x09[6]
VINDPM	0x13[7]	—	0x19[5]	0x01[0] 0x0D[7] + 0x0D[6:0]	—
VDPM_BAT_TRACK	—	—	—	0x17[3:2]	0x17[3:2]
IINDPM	0x13[6]	—	0x19[4]	0x00[5:0]	—
ICO_ILIM	0x14[6]	—	—	0x13[5:0]	0x02[4]
FORCE_ICO	—	—	—	0x09[7]	—
EN_ILIM	—	—	—	—	0x00[6]
VBUS_STAT	0x0B[7:5]	—	—	—	—
VBUS_GD	0x11[7]	—	—	—	—
PG_STAT	0x0B[2]	—	—	—	—
EN_AUTO_INDET	—	—	—	—	0x02[0]
FORCE_INDET	—	—	—	—	0x02[1]
HVDCP Adaptor	—	—	—	—	0x02[3]
MaxDCP Adaptor	—	—	—	—	0x02[2]
EN_12V	—	—	—	—	0x01[1]
DP_DAC	—	—	—	0x01[7:5]	—
DM_DAC	—	—	—	0x01[4:2]	—
EN_ICHG_MON	—	—	—	0x16[3:2]	0x16[3:2]
STAT_SET	—	—	—	0x16[1:0]	0x16[1:0]
SYS_MIN	0x0B[0]	—	—	0x03[3:1]	—
HIZ MODE	—	—	—	—	0x00[7]
WATCHDOG	0x0C[7]	—	—	0x07[5:4]	0x07[5:4]
WD_RST	—	—	—	—	0x03[6]
OTG	0x0B[7:5]	—	—	0x0A[7:4]	0x03[5]
BOOST_FREQ	—	—	—	0x02[5]	—
MIN_VBAT_SEL	—	—	—	0x03[0]	—
BOOST_LIM	—	—	—	0x0A[2:0]	—
BOOST_FAULT	0x0C[6]	—	—	—	—
BATFET	—	—	—	0x09[3]	0x09[5]
EN_BATFET_RST	—	—	—	—	0x09[2]
BATFET_OCP	—	—	—	0x21[0] + 0x21[1]	—
PFM	—	—	—	—	0x0A[3]
FORCE_DSEL	—	—	—	—	0x03[7]
PUMPX	—	—	—	0x09[1] 0x09[0]	0x04[7]
NTC_FAULT	0x0C[2:0]	—	—	—	—
JEITA_VT2	—	—	—	0x18[3:2]	—
JEITA_VT3	—	—	—	0x18[1:0]	—
JEITA_VSET_L	—	—	—	0x09[4]	—
JEITA_VSET_H	—	—	—	0x17[1:0]	—
JEITA_ISET_L	—	—	—	0x07[0]	0x18[6]
JEITA_ISET_H	—	—	—	0x18[5:4]	—
TREG	0x0E[7]	—	—	0x08[1:0]	—
TSHUT	0x0C[5:4]	—	—	—	—

REGISTER MAPS (continued)

I²C Register Address Map (continued)

FUNCTION	STAT	FLAG	MASK	THRESHOLD SETTING	ENABLE
BUS OVP	0x0C[5:4]	–	–	0x17[7:6]	–
BUS UVP	0x0C[5:4]	–	–	–	–
BAT OVP	0x0C[3]	–	–	–	–
REG_RST	–	–	–	–	0x14[7]
CONV_START	–	–	–	–	0x02[7]
CONV_RATE	–	–	–	0x02[6]	–
IBUS_ADC	–	–	–	0x20[6:0]	0x21[7]
IBAT_ADC	–	–	–	0x12[6:0]	0x21[6]
VBUS_ADC	–	–	–	0x11[6:0]	0x21[5]
VBAT_ADC	–	–	–	0x0E[6:0]	0x21[4]
VSYS_ADC	–	–	–	0x0F[6:0]	0x21[3]
TS_ADC	–	–	–	0x10[6:0]	0x21[2]
TS_PROFILE	–	–	–	0x14[2]	–
DEV_REV	–	–	–	0x14[1:0]	–
PN	–	–	–	0x16[7:4]	–

I²C Slave Address of SGM41544/SGM41544D: 0x6A

Bit Types:

R/W: Read/Write bit(s)

R: Read only bit(s)

n: Parameter code formed by the bits as an unsigned binary number.

REG0x00: Input Current Limit Register [Reset = 0x48]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	EN_HIZ	0	R/W	Enable HIZ Mode 0 = Disable (default) 1 = Enable		REG_RST or Watchdog
D[6]	EN_ILIM	1	R/W	Enable ILIM Pin 0 = Disable 1 = Enable (Enable ILIM pin) (default)		REG_RST or Watchdog
D[5:0]	IINDPM[5:0]	00 1000	R/W	IINDPM[5] 1 = 1600mA	Input Current Limit (n: 6 bits): = 100 + 50n (mA) Offset: 100mA Range: 100mA (00 0000) - 3.25A (11 1111) Default: 00 1000 (500mA) The actual input current limit is the lower of I²C or ILIM pin. IINDPM[5:0] bits are changed automatically after the input source type detection is completed. USB Host SDP = 500mA USB CDP = 1.5A USB DCP = 3.25A Adjustable High Voltage DCP = 1.5A Unknown Adaptor = 500mA Non-Standard Adaptor = 1A/2A/2.1A/2.4A	REG_RST
				IINDPM[4] 1 = 800mA		
				IINDPM[3] 1 = 400mA		
				IINDPM[2] 1 = 200mA		
				IINDPM[1] 1 = 100mA		
				IINDPM[0] 1 = 50mA		

REGISTER MAPS (continued)

REG0x01: DPDM_Driver Register [Reset = 0x01]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	DP_DAC[2:0]	000	R/W	D+ Pin Output Driver 000 = HIZ mode (default) 001 = 0V (V_{0P0_VSRC}) 010 = 0.6V (V_{0P6_VSRC}) 011 = 1.2V (V_{1P2_VSRC}) 100 = 2.0V (V_{2P0_VSRC}) 101 = 2.7V (V_{2P7_VSRC}) 110 = 3.3V (V_{3P3_VSRC}) 111 = Reserved When the input source is plugged in, the bits are reset to the default value, which can be changed after the D+/D- detection is completed.	REG_RST
D[4:2]	DM_DAC[2:0]	000	R/W	D- Pin Output Driver 000 = HIZ mode (default) 001 = 0V (V_{0P0_VSRC}) 010 = 0.6V (V_{0P6_VSRC}) 011 = 1.2V (V_{1P2_VSRC}) 100 = 2.0V (V_{2P0_VSRC}) 101 = 2.7V (V_{2P7_VSRC}) 110 = 3.3V (V_{3P3_VSRC}) 111 = Reserved When the input source is plugged in, the bits are reset to the default value, which can be changed after the D+/D- detection is completed.	REG_RST
D[1]	EN_12V	0	R/W	Enable 12V Detection for HVDCP 0 = Disable 12V detection (default) 1 = Enable 12V detection	REG_RST
D[0]	VINDPM_OS	1	R/W	Input Voltage Limit Offset 0 = 400mV 1 = 600mV (default) Minimum VINDPM threshold is clamped at 3.9V. Maximum VINDPM threshold is clamped at 15.3V. When VBUS at noLoad is ≤ 6V, the VINDPM_OS is used to calculate VINDPM threshold. When VBUS at noLoad is > 6V, the VINDPM_OS multiple by 2 is used to calculate VINDPM threshold.	REG_RST

REGISTER MAPS (continued)

REG0x02: Charger_Control_0 Register [Reset = 0x3D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CONV_START	0	R/W	ADC Conversion Start Control 0 = ADC conversion not active (default) 1 = Start ADC conversion This bit is read only when CONV_RATE = 1. It remains high during ADC conversion and input source detection.	REG_RST or Watchdog
D[6]	CONV_RATE	0	R/W	ADC Conversion Rate Selection 0 = One-shot ADC conversion (default) 1 = Start 1s continuous conversion When set to 0, which ADC conversion is active depends on REG0x21. When set to 1, all ADC conversions are active.	REG_RST or Watchdog
D[5]	BOOST_FREQ	1	R/W	Boost Mode Frequency Selection 0 = 1.5MHz 1 = 500kHz (default) Note: Write to this bit is invalid when the OTG_CONFIG bit is enabled.	REG_RST or Watchdog
D[4]	EN_ICO	1	R/W	Input Current Optimizer (ICO) Enable 0 = Disable ICO algorithm 1 = Enable ICO algorithm (default)	REG_RST
D[3]	EN_HVDCP	1	R/W	High Voltage DCP Enable 0 = Disable HVDCP handshake 1 = Enable HVDCP handshake (default)	REG_RST
D[2]	EN_MAXDCP	1	R/W	MaxDCP Adaptor Enable 0 = Disable handshake 1 = Enable handshake (default)	REG_RST
D[1]	FORCE_INDET	0	R/W	Force D+/D- or PSEL Detection 0 = Not in D+/D- or PSEL detection (default) 1 = Force D+/D- or PSEL detection	REG_RST or Watchdog
D[0]	EN_AUTO_INDET	1	R/W	Automatic D+/D- or PSEL Detection Enable 0 = Disable D+/D- or PSEL detection when VBUS is plugged in 1 = Enable D+/D- or PSEL detection when VBUS is plugged in (default)	REG_RST

REG0x03: Charger_Control_1 Register [Reset = 0x1A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_DSEL	0	R/W	DSEL Pin Control 0 = Allow DSEL pin output to drive low (default) 1 = Force DSEL pin output to drive high	REG_RST
D[6]	WD_RST	0	R/W	I^2C Watchdog Timer Reset 0 = Normal (default) 1 = Reset Watchdog timer reset control bit. Write 1 to this bit to avoid watchdog expiry. WD_RST bit resets to 0 after watchdog timer reset (expiry).	REG_RST or Watchdog
D[5]	OTG_CONFIG	0	R/W	Boost (OTG) Mode Configuration 0 = OTG disable (default) 1 = OTG enable The OTG is enabled when the OTG_CONFIG bit is 1 and OTG pin is pulled high. This bit has priority over-charge enable in the register.	REG_RST or Watchdog
D[4]	CHG_CONFIG	1	R/W	Charge Enable Configuration 0 = Charge disable 1 = Charge enable (default) Charge is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low.	REG_RST or Watchdog
D[3:1]	SYS_MIN[2:0]	101	R/W	SYS_MIN[2] 1 = 0.4V SYS_MIN[1] 1 = 0.2V SYS_MIN[0] 1 = 0.1V Minimum System Voltage Limit (n: 3 bits): = 3 + 0.1n (V) Offset: 3.0V Range: 3.0V - 3.7V Default: 3.5V (101)	REG_RST
D[0]	MIN_VBAT_SEL	0	R/W	Minimum Battery Voltage (Falling) to Exit Boost Mode 0 = 2.9V (default) 1 = 2.5V	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x04: Charge_Current_Limit Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	EN_PUMPX	0	R/W	Current Pulse Control Enable 0 = Disable current pulse control (default) 1 = Enable current pulse control (PUMPX_UP and PUMPX_DN)		REG_RST or Watchdog
D[6:0]	ICHG[6:0]	010 0000	R/W	ICHG[6] 1 = 4096mA ICHG[5] 1 = 2048mA ICHG[4] 1 = 1024mA ICHG[3] 1 = 512mA ICHG[2] 1 = 256mA ICHG[1] 1 = 128mA ICHG[0] 1 = 64mA	Fast Charge Current Limit (n: 7 bits): = 64n (mA) Offset: 0mA Range: 0mA (000 0000) - 5056mA (100 1111) Default: 2048mA (010 0000) Note: ICHG[6:0] = 000 0000 (0mA) disables charge. ICHG[6:0] > 100 1111 (5056mA) is clamped to register value 100 1111 (5056mA).	REG_RST or Watchdog

REG0x05: Pre-Charge and Termination Current Limit Register [Reset = 0x13]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	IPRECHG[3:0]	0001	R/W	IPRECHG[3] 1 = 512mA IPRECHG[2] 1 = 256mA IPRECHG[1] 1 = 128mA IPRECHG[0] 1 = 64mA	Pre-Charge Current Limit (n: 4 bits): = 64 + 64n (mA) Offset: 64mA Range: 64mA - 1024mA Default: 128mA (0001)	REG_RST or Watchdog
D[3:0]	ITERM[3:0]	0011	R/W	ITERM[3] 1 = 512mA ITERM[2] 1 = 256mA ITERM[1] 1 = 128mA ITERM[0] 1 = 64mA	Termination Current Limit (n: 4 bits): = 64 + 64n (mA) Offset: 64mA Range: 64mA - 1024mA Default: 256mA (0011)	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x06: Battery_Voltage_Limit_0 Register [Reset = 0x5A]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:2]	VREG[5:0]	01 0110	R/W	VREG[5] 1 = 512mV VREG[4] 1 = 256mV VREG[3] 1 = 128mV VREG[2] 1 = 64mV VREG[1] 1 = 32mV VREG[0] 1 = 16mV	Charge Voltage Limit (n: 6 bits): = 3856 + 16n (mV) (n ≤ 48), if VREG_SET = 0 = 3504 + 16n (mV) (n ≤ 48), if VREG_SET = 1 If VREG_SET = 0 Offset: 3.856V Range: 3.856V - 4.624V (11 0000) Default: 4.208V (01 0110) If VREG_SET = 1 Offset: 3.504V Range: 3.504V - 4.272V (11 0000) Default: 3.856V (01 0110) Note: VREG[5:0] > 11 0000 (4.624V or 4.272V) is clamped to register value 11 0000 (4.624V or 4.272V).	REG_RST or Watchdog
D[1]	BATLOWV	1	R/W	Battery Pre-Charge to Fast Charge Threshold 0 = 2.8V 1 = 3.0V (default)		REG_RST or Watchdog
D[0]	VRECHG	0	R/W	Battery Recharge Threshold Offset (below Charge Voltage Limit) 0 = 100mV (VRECHG) below VREG (VREG[5:0]) (default) 1 = 200mV (VRECHG) below VREG (VREG[5:0])		REG_RST or Watchdog

REG0x07: Charger_Control_2 Register [Reset = 0x9D]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	EN_TERM	1	R/W	Charging Termination Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[6]	Reserved	0	R/W	Reserved.	REG_RST or Watchdog
D[5:4]	WATCHDOG[1:0]	01	R/W	I^2C Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s	REG_RST or Watchdog
D[3]	EN_TIMER	1	R/W	Charging Safety Timer Enable 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[2:1]	CHG_TIMER[1:0]	10	R/W	Fast Charge Timer Setting 00 = 5h 01 = 8h 10 = 12h (default) 11 = 20h	REG_RST or Watchdog
D[0]	JEITA_ISET_L (0℃ - 10℃)	1	R/W	JEITA Low Temperature Current Setting 0 = 50% of I_{CHG} (ICHG[6:0]) 1 = 20% of I_{CHG} (ICHG[6:0]) (default) When EN_JEITA_ISET_L = 1.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x08: IRCOMP Register [Reset = 0x03]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:5]	BAT_COMP[2:0]	000	R/W	BAT_COMP[2] 1 = 80mΩ BAT_COMP[1] 1 = 40mΩ BAT_COMP[0] 1 = 20mΩ	IR Compensation Resistor Setting (n: 3 bits): = 20n (mΩ) Range: 0mΩ - 140mΩ Default: 0Ω (000) (i.e. disable IRComp)	REG_RST or Watchdog
D[4:2]	VCLAMP[2:0]	000	R/W	VCLAMP[2] 1 = 128mV VCLAMP[1] 1 = 64mV VCLAMP[0] 1 = 32mV	IR Compensation Voltage Clamp above VREG[5:0] (n: 3 bits): = 32n (mV) Offset: 0mV Range: 0mV - 224mV Default: 0mV (000)	REG_RST or Watchdog
D[1:0]	TREG[1:0]	11	R/W	Thermal Regulation Threshold 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)		REG_RST or Watchdog

REG0x09: Charger_Control_3 Register [Reset = 0x44]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	FORCE_ICO	0	R/W	Force Start Input Current Optimizer (ICO) 0 = Do not force ICO (default) 1 = Force ICO Note: This bit can only be set and always returns to 0 after ICO starts. The bit only valid when EN_ICO = 1.	REG_RST or Watchdog
D[6]	EN_TMR2X	1	R/W	Enable Half Clock Rate Safety Timer 0 = Disable 1 = The safety timer slows down during DPM, JEITA cool, or thermal regulation (default) Slow down by a factor of 2.	REG_RST or Watchdog
D[5]	BATFET_DIS	0	R/W	Force BATFET Off to Enable Ship Mode 0 = Allow BATFET(Q4) to turn on (default) 1 = Turn off BATFET immediately (REG0x09 D[3])	REG_RST
D[4]	JEITA_VSET_L (0℃ - 10℃)	0	R/W	JEITA Low Temperature Voltage Setting 0 = Set charge voltage to V_{REG} (default) 1 = Set charge voltage to V_{REG} - 200mV	REG_RST or Watchdog
D[3]	BATFET_DLY	0	R/W	BATFET Turn Off Delay Control 0 = BATFET is turned off immediately when the BATFET_DIS bit is set (default) 1 = BATFET is turned off delay by t_{SM_DLY} when the BATFET_DIS bit is set	REG_RST
D[2]	EN_BATFET_RST	1	R/W	BATFET Full System Reset Enable 0 = Disable BATFET full system reset 1 = Enable BATFET full system reset (default)	REG_RST
D[1]	PUMPX_UP	0	R/W	Current Pulse Control Voltage Up Enable 0 = Disable (default) 1 = Enable Note: This bit can only be set when setting the EN_PUMPX bit and returns to 0 after the current pulse control sequence is completed.	REG_RST or Watchdog
D[0]	PUMPX_DN	0	R/W	Current Pulse Control Voltage Down Enable 0 = Disable (default) 1 = Enable Note: This bit can only be set when setting the EN_PUMPX bit and returns to 0 after the current pulse control sequence is completed.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x0A: OTG_Regulation Register [Reset = 0x73]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7:4]	BOOSTV[3:0]	0111	R/W	BOOSTV[3] 1 = 512mV BOOSTV[2] 1 = 256mV BOOSTV[1] 1 = 128mV BOOSTV[0] 1 = 64mV	Boost Mode Voltage Regulation (n: 4 bits): = 4550 + 64n (mV) Offset: 4.55V Range: 4.55V - 5.51V Default: 4.998V(0111)	REG_RST or Watchdog
D[3]	PFM_DIS	0	R/W	Enable PFM Mode 0 = Enable (default) 1 = Disable		REG_RST
D[2:0]	BOOST_LIM[2:0]	011	R/W	Boost Mode Current Limit 000 = 0.5A 001 = 0.75A 010 = 1.2A 011 = 1.4A (default) 100 = 1.65A 101 = 1.875A 110 = 2.15A 111 = 2.45A		REG_RST or Watchdog

REG0x0B: Charger_Status_0 Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	VBUS_STAT[2:0]	xxx	R	VBUS Status Register (SGM41544D) 000 = No input 001 = USB host SDP 010 = USB CDP (1.5A) 011 = USB DCP (3.25A) 100 = Adjustable high voltage DCP (1.5A) 101 = Unknown adaptor (500mA) 110 = Non-standard adaptor (1A/2A/2.1A/2.4A) 111 = OTG VBUS Status Register (SGM41544) 000 = No input 001 = USB host SDP (500mA) → PSEL HIGH 010 = Adaptor 2.4A → PSEL LOW 111 = OTG Other values are reserved. Note: The software current limit is reported in IINDPM[5:0] register.	N/A
D[4:3]	CHRG_STAT[1:0]	xx	R	Charging Status 00 = Not charging 01 = Pre-charge (V_{BAT} < V_{BAT_LOWV}) 10 = Fast charging 11 = Charge termination done	N/A
D[2]	PG_STAT	x	R	Power Good Status 0 = Not power good 1 = Power good	N/A
D[1]	Reserved	x	R	Reserved. Always reads 0.	N/A
D[0]	VSYS_STAT	x	R	VSYS Regulation Status 0 = Not in VSYS_MIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In VSYS_MIN regulation (V_{BAT} < V_{SYS_MIN})	N/A

REGISTER MAPS (continued)

REG0x0C: Fault_Status Register [Reset = 0xXX]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	WATCHDOG_FAULT	x	R	Watchdog Fault Status 0 = Normal 1 = Watchdog timer expiration	N/A
D[6]	BOOST_FAULT	x	R	Boost Mode Fault Status 0 = Normal 1 = VBUS is overloaded in OTG, or VBUS OVP, or battery is too low in Boost mode	N/A
D[5:4]	CHRG_FAULT[1:0]	xx	R	Charge Fault Status 00 = Normal 01 = Input fault (V_{BUS} > V_{VBUS_OV} or V_{BAT} < V_{BUS} < V_{VBUS_MIN} (typical 3.8V) 10 = Thermal shutdown 11 = Charge safety timer expiration	N/A
D[3]	BAT_FAULT	x	R	Battery Fault Status 0 = Normal 1 = BATOVP (V_{BAT} > V_{BAT_OVP})	N/A
D[2:0]	NTC_FAULT[2:0]	xxx	R	NTC Fault Status For Buck mode: 000 = Normal 010 = TS warm 011 = TS cool 101 = TS cold 110 = TS hot For Boost mode: 000 = Normal 101 = TS cold 110 = TS hot	N/A

REG0x0D: Input_Voltage_Limit Register [Reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	FORCE_VINDPM	0	R/W	VINDPM Threshold Setting Method 0 = Run relative VINDPM threshold (default) 1 = Run absolute VINDPM threshold Note: When the input source is plugged in, the register is reset to the default value.		REG_RST
D[6:0]	VINDPM[6:0]	001 0010	R/W	VINDPM[6] 1 = 6400mV	Absolute VINDPM Threshold (n: 7 bits): = 2600 + 100n (mV) (n ≥ 13) Offset: 2.6V Range: 3.9V (000 1101) - 15.3V (111 1111) Default: 4.4V (001 0010) Note: Value < 000 1101 is clamped to 3.9V (000 1101). The register is read only when FORCE_VINDPM = 0 and can be written by internal control based on relative VINDPM threshold setting. It can be read/write when FORCE_VINDPM = 1.	REG_RST
				VINDPM[5] 1 = 3200mV		
				VINDPM[4] 1 = 1600mV		
				VINDPM[3] 1 = 800mV		
				VINDPM[2] 1 = 400mV		
				VINDPM[1] 1 = 200mV		
				VINDPM[0] 1 = 100mV		

REGISTER MAPS (continued)

REG0x0E: VBAT_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	THERM_STAT	0	R	Thermal Regulation Status 0 = Normal (default) 1 = In thermal regulation		N/A
D[6:0]	BATV[6:0]	000 0000	R	BATV[6] 1 = 1280mV	ADC Conversion of Battery Voltage (V_{BAT}) (n: 7 bits): = 2304 + 20n (mV) Offset: 2.304V Range: 2.304V (000 0000) - 4.844V (111 1111) Default: 2.304V (000 0000)	N/A
				BATV[5] 1 = 640mV		
				BATV[4] 1 = 320mV		
				BATV[3] 1 = 160mV		
				BATV[2] 1 = 80mV		
				BATV[1] 1 = 40mV		
				BATV[0] 1 = 20mV		

REG0x0F: VSYS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	Reserved	0	R	Reserved. Always reads 0.		N/A
D[6:0]	SYSV[6:0]	000 0000	R	SYSV[6] 1 = 1280mV	ADC Conversion of System Voltage (V_{SYS}) (n: 7 bits): = 2304 + 20n (mV) Offset: 2.304V Range: 2.304V (000 0000) - 4.844V (111 1111) Default: 2.304V (000 0000)	N/A
				SYSV[5] 1 = 640mV		
				SYSV[4] 1 = 320mV		
				SYSV[3] 1 = 160mV		
				SYSV[2] 1 = 80mV		
				SYSV[1] 1 = 40mV		
				SYSV[0] 1 = 20mV		

REG0x10: TS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	Reserved	0	R	Reserved. Always reads 0.		N/A
D[6:0]	TSPCT[6:0]	000 0000	R	TSPCT[6] 1 = 29.76%	ADC Conversion of TS Voltage (TS) as Percentage of REGN (n: 7 bits): = 21% + 0.465%n Offset: 21% Range: 21% (000 0000) - 80.055% (111 1111) Default: 21% (000 0000)	N/A
				TSPCT[5] 1 = 14.88%		
				TSPCT[4] 1 = 7.44%		
				TSPCT[3] 1 = 3.72%		
				TSPCT[2] 1 = 1.86%		
				TSPCT[1] 1 = 0.93%		
				TSPCT[0] 1 = 0.465%		

REGISTER MAPS (continued)

REG0x11: VBUS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	VBUS_GD	0	R	VBUS Good Status 0 = Not VBUS attached (default) 1 = VBUS attached		N/A
D[6:0]	VBUSV[6:0]	000 0000	R	VBUSV[6] 1 = 6400mV VBUSV[5] 1 = 3200mV VBUSV[4] 1 = 1600mV VBUSV[3] 1 = 800mV VBUSV[2] 1 = 400mV VBUSV[1] 1 = 200mV VBUSV[0] 1 = 100mV	ADC Conversion of VBUS Voltage (V_{VBUS}) (n: 7 bits): = 2600 + 100n (mV) Offset: 2.6V Range: 2.6V (000 0000) - 15.3V (111 1111) Default: 2.6V (000 0000)	N/A

REG0x12: IBAT_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	Reserved	0	R	Reserved: Always reads 0.		N/A
D[6:0]	ICHGR[6:0]	000 0000	R	ICHGR[6] 1 =3200mA ICHGR[5] 1 =1600mA ICHGR[4] 1 =800mA ICHGR[3] 1 =400mA ICHGR[2] 1 =200mA ICHGR[1] 1 =100mA ICHGR[0] 1 = 50mA	ADC Conversion of Charge Current (I_{BAT}) when $V_{BAT} > V_{BATSHORT}$ (n: 7 bits): = 50n (mA) Offset: 0mA Range: 0mA (000 0000) - 6350mA (111 1111) Default: 0mA (000 0000) Note: This register returns 000 0000 for $V_{BAT} < V_{SHORT}$.	N/A

REG0x13: Charger_Status_1 Register [Reset = 0xX0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	VINDPM_STAT	x	R	VINDPM Status 0 = Not in VINDPM 1 = VINDPM		N/A
D[6]	IINDPM_STAT	x	R	IINDPM Status 0 = Not in IINDPM 1 = IINDPM		N/A
D[5:0]	ICO_ILIM[5:0]	00 0000	R	ICO_ILIM[5] 1= 1600mA ICO_ILIM[4] 1= 800mA ICO_ILIM[3] 1= 400mA ICO_ILIM[2] 1= 200mA ICO_ILIM[1] 1= 100mA ICO_ILIM[0] 1= 50mA	Input Current Limit in Effect while Input Current Optimizer (ICO) is Enabled (n: 6 bits): = 100 + 50n (mA) Offset: 100mA (default) Range: 100mA (00 0000) - 3.25A (11 1111)	N/A

REGISTER MAPS (continued)

REG0x14: Part_Information Register [Reset = 0x07]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/W	Register Reset 0 = Keep current register setting (default) 1 = Reset to default register value and reset safety timer Note: Reset to 0 after the register reset is completed.	N/A
D[6]	ICO_OPTIMIZED	0	R	Input Current Optimizer (ICO) Status 0 = Optimization is in progress (default) 1 = Maximum input current is detected	N/A
D[5:3]	Reserved	000	R/W	Reserved.	N/A
D[2]	TS_PROFILE	1	R	Temperature Profile 1 = JEITA	N/A
D[1:0]	DEV_REV[1:0]	11	R	Device Revision: 11	N/A

REG0x15: Battery_Voltage_Limit_1 Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	VREG_FT[1:0]	00	R/W	VREG Fine Tuning 00 = Disable (default) 01 = V_{REG} + 8mV 10 = V_{REG} - 8mV 11 = Reserved	REG_RST or Watchdog
D[5]	VREG_SET	0	R/W	VREG Range Selection 0 = 3.856V to 4.624V (default) 1 = 3.504V to 4.272V	REG_RST or Watchdog
D[4:0]	Reserved	0 0000	R/W	Reserved.	REG_RST or Watchdog

REG0x16: Charger_Control_4 Register [Reset = 0xX0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	PN[3:0]	001x	R	Device Configuration 0010 = SGM41544 0011 = SGM41544D	N/A
D[3:2]	EN_ICHG_MON[1:0]	00	R/W	Enable STAT Pin Function 00 = Enable following charging state (default) 01 = Enable following STAT_SET[1:0] bits 10 = Disable (float pin) 11 = Disable (float pin) These bits turn on or off the function of the STAT open-drain output pin (charge status or customer customized indicator).	REG_RST
D[1:0]	STAT_SET[1:0]	00	R/W	STAT Pin Output Setting 00 = LED off (HIZ) (default) 01 = LED on (low) 10 = LED blinking 1s on 1s off 11 = LED blinking 1s on 3s off This bits only takes effect when EN_ICHG_MON[1:0] = 01.	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x17: Charger_Control_5 Register [Reset = 0XC1]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	OVP[1:0]	11	R/W	VBUS Pin OVP Threshold 00 = 5.5V 01 = 6.5V (5V input) 10 = 10.5V (9V input) 11 = 14.3V (12V input) (default)	REG_RST
D[5:4]	TOPOFF_TIMER[1:0]	00	R/W	Top-Off Timer 00 = Disabled (default) 01 = 15 minutes 10 = 35 minutes 11 = 45 minutes The charge extension time is added after the termination condition is detected. If disabled, charging terminates as soon as the termination conditions are met.	REG_RST or Watchdog
D[3:2]	VDPM_BAT_TRACK[1:0]	00	R/W	Dynamic VINDPM Tracking 00 = Disable (V_{INDPM} set by register) (default) 01 = V_{BAT} + 200mV 10 = V_{BAT} + 250mV 11 = V_{BAT} + 300mV Set V_{INDPM} to track V_{BAT} voltage. Actual V_{INDPM} is the larger of VINDPM[6:0] value and this register value.	REG_RST
D[1:0]	JEITA_VSET_H[1:0] (45℃ - 60℃)	01	R/W	JEITA High Temperature Voltage Setting 00 = Set charge voltage to V_{REG} - 300mV 01 = Set charge voltage to V_{REG} - 200mV (default) 10 = Set charge voltage to V_{REG} - 100mV 11 = Set charge voltage to V_{REG}	REG_RST or Watchdog

REG0x18: Charger_Control_6 Register [Reset = 0x75]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R/W	Reserved.	REG_RST or Watchdog
D[6]	EN_JEITA_ISET_L (0℃ - 10℃)	1	R/W	Charge Enable during Cool Temperature 0 = Disable 1 = Enable (default)	REG_RST or Watchdog
D[5:4]	JEITA_ISET_H[1:0] (45℃ - 60℃)	11	R/W	Charge Current Setting during Warm Temperature 00 = 0% of I_{CHG} 01 = 20% of I_{CHG} 10 = 50% of I_{CHG} 11 = 100% of I_{CHG} (default) In warm condition, the safety timer does not become 2X.	REG_RST or Watchdog
D[3:2]	JEITA_VT2[1:0]	01	R/W	JEITA Cool Threshold Setting 00 = V_{T2} = 70.75% (5.5℃) 01 = V_{T2} = 68.25% (10℃) (default) 10 = V_{T2} = 65.25% (15℃) 11 = V_{T2} = 62.25% (20℃)	REG_RST or Watchdog
D[1:0]	JEITA_VT3[1:0]	01	R/W	JEITA Warm Threshold Setting 00 = V_{T3} = 48.25% (40℃) 01 = V_{T3} = 44.75% (45℃) (default) 10 = V_{T3} = 40.75% (50.5℃) 11 = V_{T3} = 37.75% (54.5℃)	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0x19: Charger_Status_2 Register [Reset = 0xX0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	CV_STAT	x	R	CV Mode Status Indicator 0 = V_{BAT} is lower than V_{REG} 1 = V_{BAT} approaches to V_{REG}	N/A
D[6]	TOPOFF_ACTIVE	x	R	Active Top-Off Timer Counting Status 0 = Top-off timer is not counting 1 = Top-off timer is counting	N/A
D[5]	VINDPM_INT_MASK	0	R/W	VINDPM Event Detection Interrupt Mask 0 = Allow VINDPM nINT pulse (default) 1 = Mask VINDPM nINT pulse	REG_RST
D[4]	IINDPM_INT_MASK	0	R/W	IINDPM Event Detection Mask 0 = Allow IINDPM nINT pulse (default) 1 = Mask IINDPM nINT pulse	REG_RST
D[3:0]	Reserved	0000	R/W	Reserved.	REG_RST or Watchdog

REG0x20: IBUS_ADC Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION		RESET BY
D[7]	Reserved	0	R/W	Reserved.		REG_RST or Watchdog
D[6:0]	IBUSR[6:0]	000 0000	R	3200mA 1600mA 800mA 400mA 200mA 100mA 50mA	ADC Conversion of Input Current (I_{VBUS}) Offset: 0mA Range: 0mA (000 0000) - 3.25A (100 0001) Default: 0mA (000 0000) 100 0010 - 111 1111: Reserved	N/A

REGISTER MAPS (continued)

REG0x21: ADC_Function_Disable [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[6]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[4]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[3]	VSYS_ADC_DIS	0	R/W	VSYS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[2]	TS_ADC_DIS	0	R/W	TS ADC Control 0 = Enable (default) 1 = Disable	REG_RST
D[1]	BATFET_OCP_DEG	0	R/W	System Over-Current Deglitch 0 = 128μs (default) 1 = 2ms	REG_RST or Watchdog
D[0]	BATFET_OCP	0	R/W	System Over-Current Threshold (I_{BATFET_OCP}) 0 = 12A (default) 1 = 10.2A	REG_RST or Watchdog

APPLICATION INFORMATION

The SGM41544/SGM41544D are typically used as a charger with power path management in smart phones, tablets and other portable devices. In the design, it comes along with a host controller (a processor with I^2C interface) and a single-cell Li-Ion or Li-polymer battery.

Detailed Design Procedure

Inductor Design

Small energy storage elements (inductor and capacitor) can be used since the high frequency (1.5MHz) switching converter is used in the SGM41544/SGM41544D. Inductor should tolerate current which is higher than the maximum charge current (I_{CHG}) plus half the inductor peak to peak ripple current (ΔI) without saturation:

$$I_{SAT} > I_{CHG} + \frac{\Delta I}{2} \quad (6)$$

The inductor ripple current is determined by the input voltage (V_{VBUS}), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (f_S = 1.5MHz) and the inductance (L). In CCM:

$$\Delta I = \frac{V_{VBUS} \times D \times (1-D)}{f_S \times L} \quad (7)$$

Inductor ripple current is maximum when D ≈ 0.5. In the practical designs, inductor peak to peak current ripple is selected in a range from 20% to 40% of the maximum DC current ΔI = (0.2 ~ 0.4) × I_{CHG} for a good trade-off between inductor size and efficiency. Selecting the higher ripple allows choosing of smaller inductance.

For each application, V_{VBUS} and I_{CHG} are known, so L can be calculated from (4) and current rating of the inductor can be selected from (3). Choose an inductor that has small DCR and core losses at 1.5MHz to have high efficiency and cool operation at full load.

Input Capacitor Design

Select low ESR ceramic input capacitor (X7R or X5R) with sufficient voltage and RMS ripple current rating for decoupling of the input switching ripple current (I_{CIN}). The RMS ripple current in the worst case is around the $I_{CHG}/2$ when D ≈ 0.5. If the converter does not operate at D ≈ 50%, in the worst case, the capacitor RMS current can be estimated from (5) in which D is the closest operating duty cycle to 0.5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (8)$$

For SGM41544/SGM41544D, place C_{IN} across PMID and PGND pins close to the chip. Voltage rating of the capacitor must be at least 25% higher than the normal input voltage to minimize voltage derating. For a 14V input voltage, the preferred rating is 25V or higher.

A C_{IN} = 22μF is suggested.

Output Capacitor Design

The output capacitance (on the system) must have enough RMS (ripple) current rating to carry the inductor switching ripple and provide enough energy for system transient current demands. I_{COUT} (C_{OUT} RMS current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (9)$$

And the output voltage ripple can be calculated by:

$$\Delta V_O = \frac{V_{OUT}}{8LC_{OUT}f_S^2}\left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (10)$$

Increasing L or C_{OUT} (the LC filter) can reduce the ripple.

The internal loop compensation of the device is optimized for > 20μF ceramic output capacitor. 10V, X7R (or X5R) ceramic capacitors are recommended for the output.

Input Power Supply Considerations

To power the system from the SGM41544/SGM41544D, either an input power source with a voltage range from 3.9V to 14V and at least 100mA current rating should power VBUS, or a single-cell Li-Ion battery with voltage higher than V_{BAT_UVLOZ} should be connected to BAT pin of the device. The input source must have enough current rating to allow maximum power delivery through charger (Buck converter) to the system.

APPLICATION INFORMATION (continued)

Layout Guidelines

The switching node (SW) creates very high frequency noises, which are several times higher than f_{SW} (1.5MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation, it is important to design a proper layout for minimizing the current path impedance and loop area. A graphical guideline for the current loops and their frequency content is provided in Figure 21. The following considerations can help to make a better layout.

1. Place the input capacitor between PMID and PGND pins as close as possible to the chip with the shortest copper connections (avoid vias). Choose the smallest capacitor size.

2. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area connected to the SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

3. Place output capacitor PGND pin as close as possible to the PGND pin of the device and the PGND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency current paths short enough and on the same layer. A PGND copper layer under the component layer helps to reduce noise emissions. Note that the DC current and AC current paths are in the layout and keep them short and decoupled as much as possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from PGND pin. To avoid high current flow through the AGND path, it should be connected to PGND only at one point (preferably the PGND pin).

5. Place decoupling capacitors close to the IC pins with the shortest copper connections.

6. Solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

7. Select proper sizes for the vias and ensure that enough copper is available to carry the current for the given current path. Vias usually have some considerable parasitic inductance and resistance.

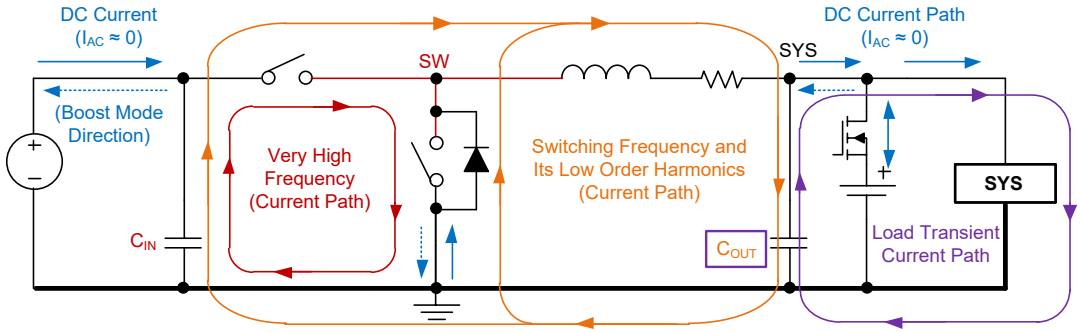


Figure 21. The Paths and Loops Carrying High Frequency, DC Currents and Very High Frequency (for Layout Design Consideration)

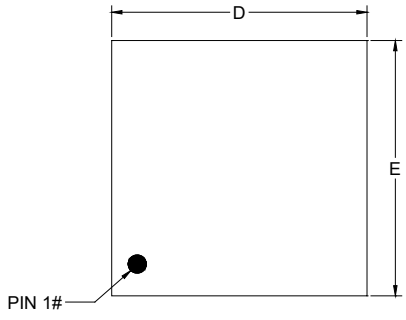
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

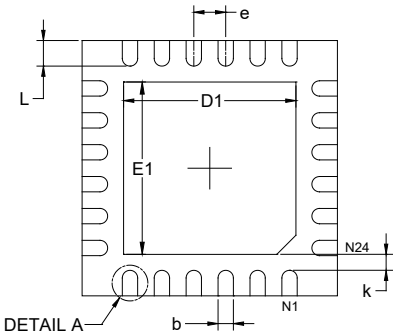
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

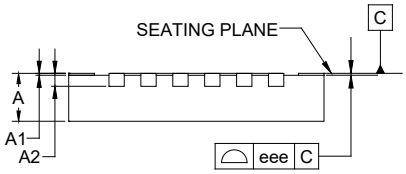
TQFN-4×4-24L



TOP VIEW

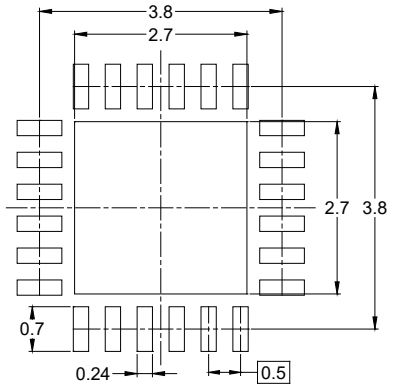


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



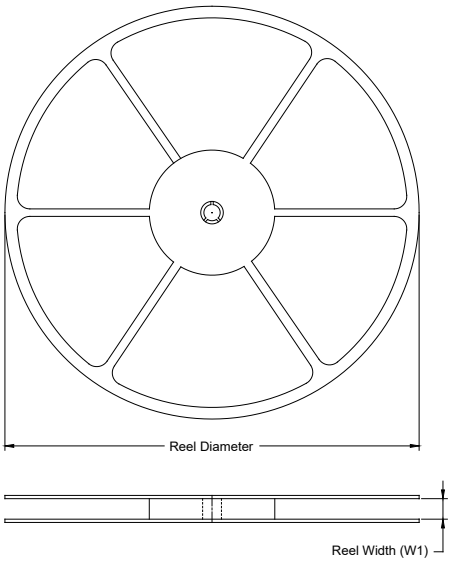
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e		0.500 BSC	
k		0.200 MIN	
L	0.300	-	0.500
eee		0.080	

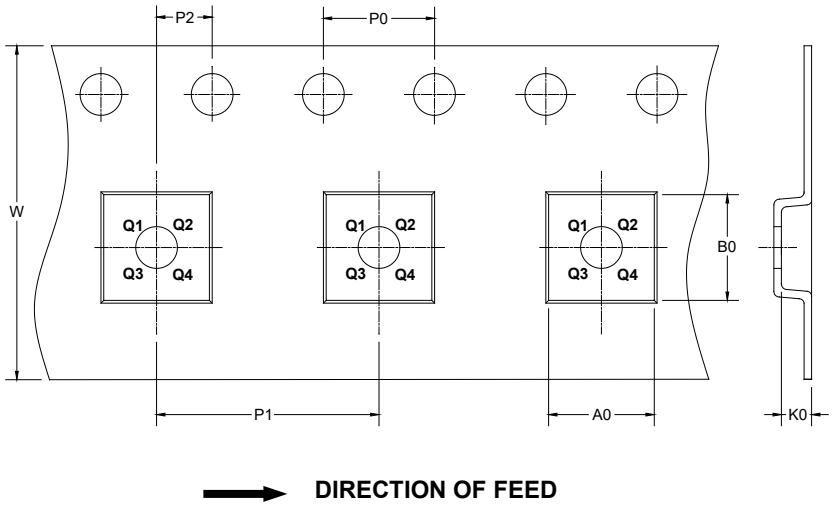
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



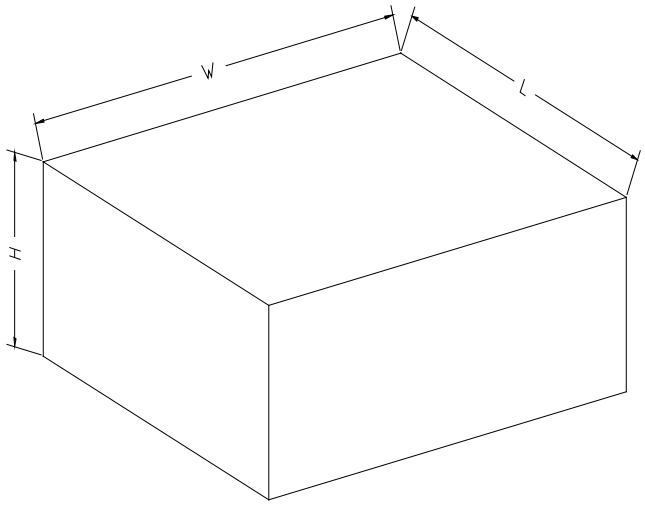
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002