SGM61114
3V to 17V Input, 1A Synchronous Buck Converter with AHP-COT Control

GENERAL DESCRIPTION

The SGM61114 is a high frequency synchronous Buck converter optimized for simple and quick application to high density designs. High output voltage accuracy and fast transient response along with small LC output filter elements are easily achievable with the pin selectable switching frequency and the AHP-COT control.

The 3V to 17V input voltage range makes this device a suitable choice for both 12V input power rails and the battery powered applications including Li-Ion batteries. It supports 100% duty cycle operation and can provide 1A continuous current to its adjustable or fixed output voltage versions. The SGM61114 can operate as a standalone power supply with adjustable soft-start ramp or as a tracking power supply using the SS/TR input pin. The enable input (EN) and power-good output (PG) pins provide power sequencing capability.

In power-save mode (PSM), the VIN quiescent current is reduced to 32μA (TYP). Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. Mode changing is automatically decided based on the load current at the DCM/CCM changeover level.

In the shutdown mode, the device is completely turned off and the current consumption drops to 3μA typically.

The SGM61114 is available in a Green TQFN-3×3-16L package.

FEATURES

- **AHP-COT Topology**
- **3V to 17V Input Voltage Range**
- **Up to 1A Output Current**
- **0.9V to 5.5V Adjustable Output Voltage**
- **Pin Selectable +5% Output Voltage Scaling**
- **Internal Compensation**
- **Adjustable Soft-Start and Tracking Function**
- **Pre-biased Startup**
- **Power-Save Mode with Seamless Transition**
- **32μA (TYP) Quiescent Current**
- **Pin Selectable 1.2MHz/2.1MHz PWM Frequency**
- **Power-Good Output**
- **Power-Good Logic Level (EN = Low)**
  - **SGM61114: High-Impedance**
  - **SGM61114A: Low Level**
- **100% Duty Cycle Mode**
- **Under-Voltage Lockout (UVLO)**
- **Current Limit Protection**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Available in a Green TQFN-3×3-16L Package**

APPLICATIONS

12V Rail Supplies
POL Supply from Single or Multi-Cell Li-Ion Battery
Solid-State Disk Drives
Embedded Systems
LDO Replacement
Mobile PCs, Tablets, Modems, Cameras
Servers, Micro Servers
Data Terminal, Point of Sales (ePOS)

TYPICAL APPLICATION

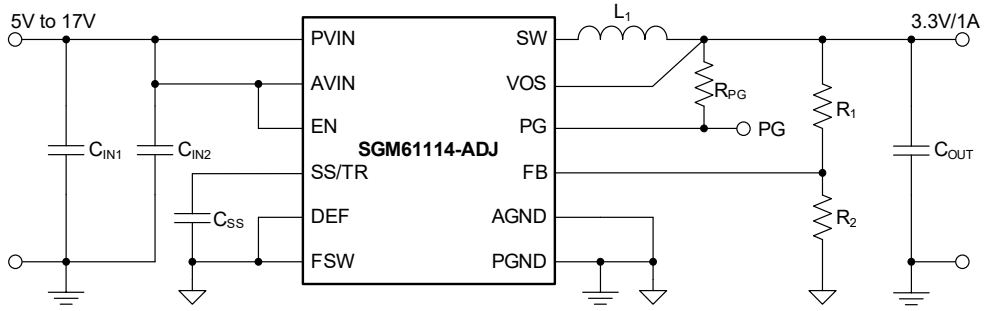


Figure 1. Typical Application Circuit

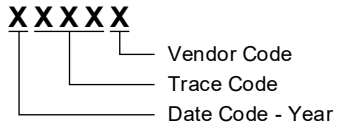
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61114-ADJ	TQFN-3×3-16L	-40℃ to +125℃	SGM61114-ADJXTQ16G/TR	0XYTQ XXXXX	Tape and Reel, 4000
SGM61114A-ADJ	TQFN-3×3-16L	-40℃ to +125℃	SGM61114A-ADJXTQ16G/TR	0Z8TQ XXXXX	Tape and Reel, 4000
SGM61114-1.8	TQFN-3×3-16L	-40℃ to +125℃	SGM61114-1.8XTQ16G/TR	0Z9TQ XXXXX	Tape and Reel, 4000
SGM61114-3.3	TQFN-3×3-16L	-40℃ to +125℃	SGM61114-3.3XTQ16G/TR	0ZATQ XXXXX	Tape and Reel, 4000
SGM61114-5.0	TQFN-3×3-16L	-40℃ to +125℃	SGM61114-5.0XTQ16G/TR	0ZBTQ XXXXX	Tape and Reel, 4000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



ABSOLUTE MAXIMUM RATINGS

Pin Voltage Range
AVIN, PVIN ..... -0.3V to 20V
EN, SS/TR, SW ..... -0.3V to V_{IN} + 0.3V
DEF, FSW, FB, PG, VOS ..... -0.3V to 6V
Power-Good Sink Current, PG 10mA
Package Thermal Resistance
TQFN-3×3-16L, θ_{JA} ..... 41.5℃/W
TQFN-3×3-16L, θ_{JB} ..... 16.7℃/W
TQFN-3×3-16L, $\theta_{JC\ (TOP)}$ ..... 51.2℃/W
TQFN-3×3-16L, $\theta_{JC\ (BOT)}$ ..... 6.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} (at AVIN and PVIN) ..... 3V to 17V
Operating Junction Temperature, T_J ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

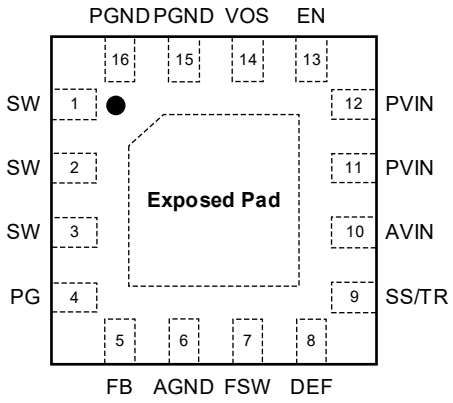
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1, 2, 3	SW	O	Switching Node of the Converter. Connect it to one terminal of the output inductor.
4	PG	O	Open-Drain Power-Good Output. A pull-up resistor to a logic high rail is needed. The PG pin goes low when the output voltage is below regulation and will be in high-impedance state when the output is in regulation.
5	FB	I	Voltage Feedback of Adjustable Output Voltage. Connect an external resistor divider from the output to this pin to program the desired output voltage. Connect to the AGND pin for fixed output voltage versions.
6	AGND	G	Analog Ground. Connect this pin to the exposed pad and the system ground plane.
7	FSW	I	Switching Frequency Select Pin. The normal operation switching frequency will be 2.1MHz (TYP) if this pin is pulled low and set to 1.2MHz (TYP) if it is pulled high. This pin is pulled low internally at low state and will be set to low if it is left floating.
8	DEF	I	Output Voltage Scaling Input Pin. It is with an internal pull-down resistor. If DEF is pulled low, the output voltage will be set to its nominal value (V_{NOM}) but if it is pulled high, the output will be scaled to 5% higher (1.05 × V_{NOM}). It is internally pulled low at low state and will be set to low if it is left floating.
9	SS/TR	I	Soft-Start/Tracking Input Pin. A minimum 1nF capacitor is required for this pin to avoid overshoot during the charge of soft-start capacitor. To set the soft-start ramp, place a capacitor (C_{SS}) between this pin and AGND. If an external voltage is applied to this pin, the output voltage will track it. This feature is useful for voltage tracking and ratiometric sequencing.
10	AVIN	P	Supply Voltage Input for the Internal Control Circuitry. Connect to the same source as the PVIN, but be decoupled separately to reduce input noise from the control circuit.
11, 12	PVIN	P	Supply Voltage for Power Stage. Connects to the same source as AVIN.
13	EN	I	Active High Enable Input. Connect a temporary internal pull-down resistor. Applying a logic high voltage to this pin enables the chip. Pulling EN low will shut down the device.
14	VOS	I	Output Voltage Sense Input Pin. Connect this pin to sense the output ripple that is needed for the internal control loop. It is recommended to connect it directly to the output capacitor with a separate track.
15, 16	PGND	G	Power Ground. The PGND, exposed thermal pad and the common system ground plane must be connected directly.
Exposed Pad	-	G	Exposed Thermal Pad. It must be directly connected to AGND, PGND and the PCB common ground plane. Solder this pad such that a good heat transfer path is created from the junction to the ambient. Thermal vias will help.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, T_J = -40°C to +125°C, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Input Voltage Range	V_{IN}	Device is functional (Not in UVLO)		3		17	V
Quiescent Current	I_Q	V_{IN} = 3V to 17V, EN = High, no load, device not switching	T_J = +25℃		32	42	μA
			T_J = -40℃ to +85℃		32	45	
Shutdown Current (I_{AVIN} + I_{PVIN})	I_{SD}	V_{IN} = 3V to 17V, EN = Low	T_J = +25℃		3	3.9	μA
			T_J = -40℃ to +85℃		3	4.2	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling (PWM mode)		2.62	2.73	2.84	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}				160		mV
Thermal Shutdown Temperature	T_{SD}	Temperature rising			160		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}				16		℃
Input and Output Signals (EN, DEF, FSW, SS/TR and PG)							
High Level Input Threshold Voltage for Logic Inputs (EN, DEF, FSW)	V_H			0.9	0.66		V
Low Level Input Threshold Voltage for Logic Inputs (EN, DEF, FSW)	V_L				0.44	0.25	V
Input Leakage Current (EN, DEF, FSW)	I_{LKG}	EN = V_{IN} or GND; DEF, FSW = V_{OUT} or GND			0.01	0.8	μA
Power-Good Threshold Voltage	V_{TH_PG}	V_{PG} rising, V_{FB} referenced to V_{REF}		91	95	98	%
		V_{PG} falling, V_{FB} referenced to V_{REF}		85	89	92	
Power-Good Output Low	V_{OL_PG}	I_{PG} = -2mA			0.095	0.3	V
PG Input Leakage Current	I_{LKG_PG}	V_{PG} = 1.8V			10	800	nA
SS/TR Pin Source Current	$I_{SS/TR}$			2.1	2.5	2.9	μA
Power Switch							
High-side MOSFET On-Resistance	R_{DSON}	V_{IN} ≥ 6V			90	155	mΩ
		V_{IN} = 3V			110		
Low-side MOSFET On-Resistance		V_{IN} ≥ 6V			35	64	mΩ
		V_{IN} = 3V			40		
High-side MOSFET Current Limit (1)	I_{LIMF}	V_{IN} = 12V		1.8	2.2	2.5	A
Low-side MOSFET Current Limit (1)	I_{LIML}	V_{IN} = 12V		1.1	1.4	4.3	A
Output (V_{OUT})							
FB Input Leakage Current	I_{LKG_FB}	SGM61114-ADJ, V_{FB} = 0.8V			1	10	nA
Output Voltage Range	V_{OUT}	SGM61114-ADJ, V_{IN} ≥ V_{OUT}		0.9		5.5	V
V_{OUT} Scaling		DEF = 0 (GND)			V_{NOM}		-
		DEF = 1 (V_{OUT})			1.05 × V_{NOM}		-
Initial Output Voltage Accuracy (2)		PWM mode, V_{IN} ≥ V_{OUT} + 1V, T_J = +25℃		791	800	809	mV
		PWM mode, V_{IN} ≥ V_{OUT} + 1V		789	800	811	
Tracking Feedback Voltage		SGM61114-ADJ, $V_{SS/TR}$ = 350mV		208	223	238	mV
Load Regulation (3)	$\Delta V_{OUT}/I_{OUT}$	V_{IN} = 12V, V_{OUT} = 3.3V, PWM mode			0.05		%/A
Line Regulation (3)	$\Delta V_{OUT}/V_{IN}$	V_{IN} = 3V to 17V, V_{OUT} = 3.3V, I_{OUT} = 1A, PWM mode			0.02		%/V

NOTES:

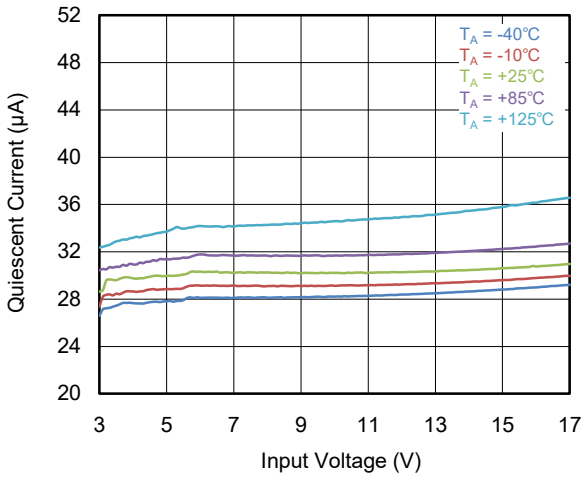
1. It is the static current limit in static conditions. In the dynamic conditions, the propagation delays may increase this limit temporary.

2. Measured at the FB input (Adjustable Version). The impact of the line and load regulation is not included.

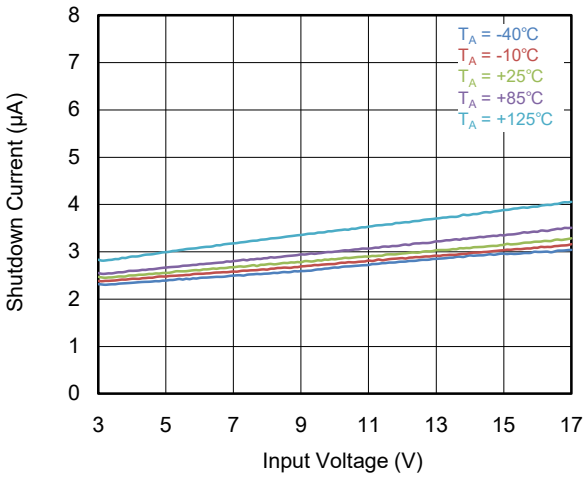
3. Line and load regulations are affected by the application design and circuit layout.

TYPICAL PERFORMANCE CHARACTERISTICS

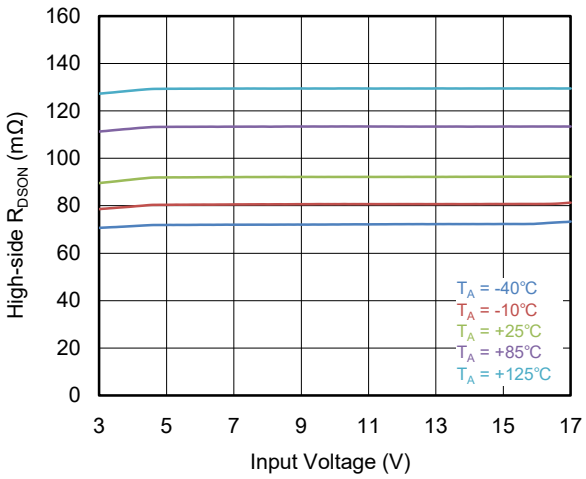
Quiescent Current vs. Input Voltage



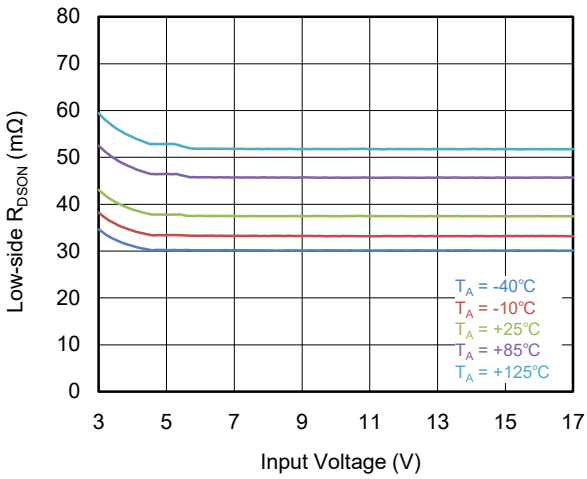
Shutdown Current vs. Input Voltage



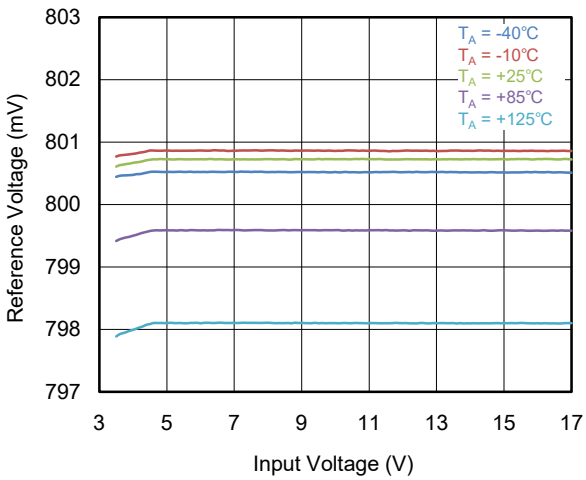
High-side R_{DSON} vs. Input Voltage



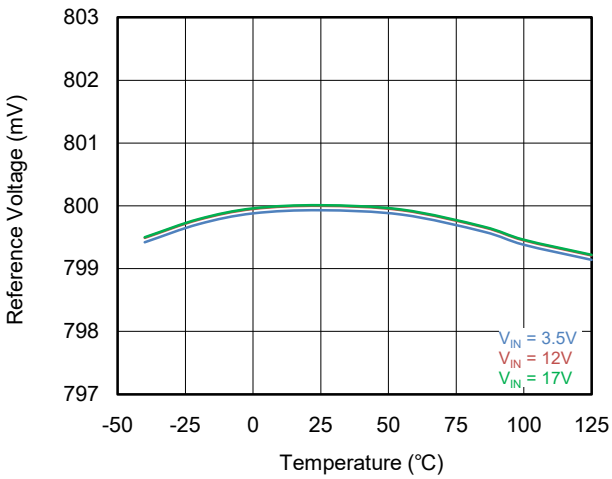
Low-side R_{DSON} vs. Input Voltage



Reference Voltage vs. Input Voltage



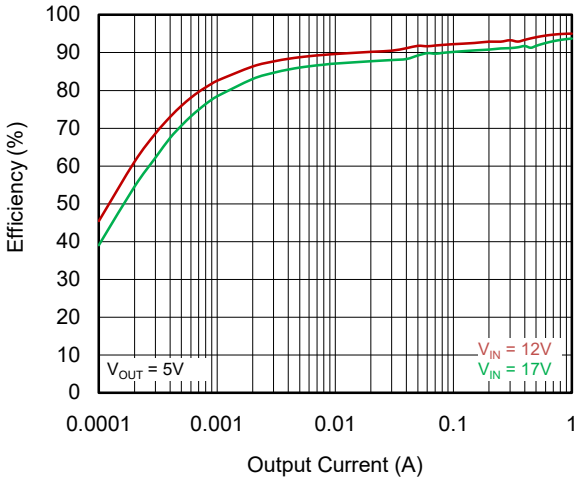
Reference Voltage vs. Temperature



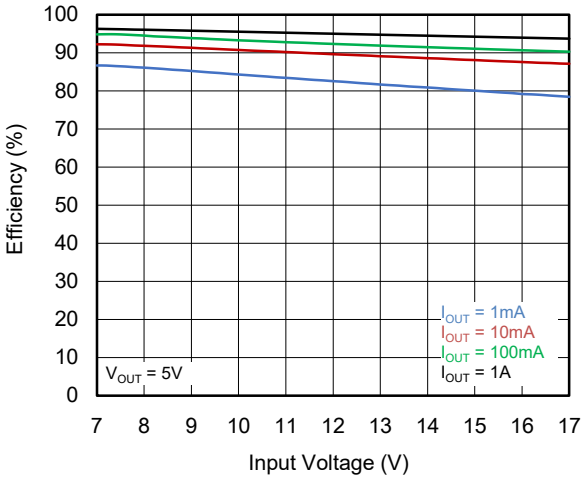
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

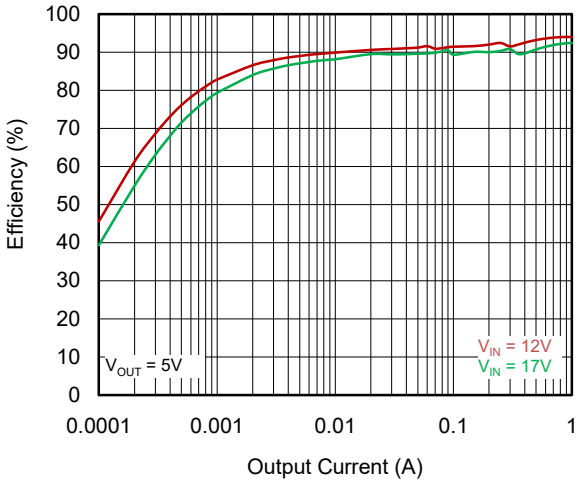
Efficiency vs. Output Current with 1.2MHz



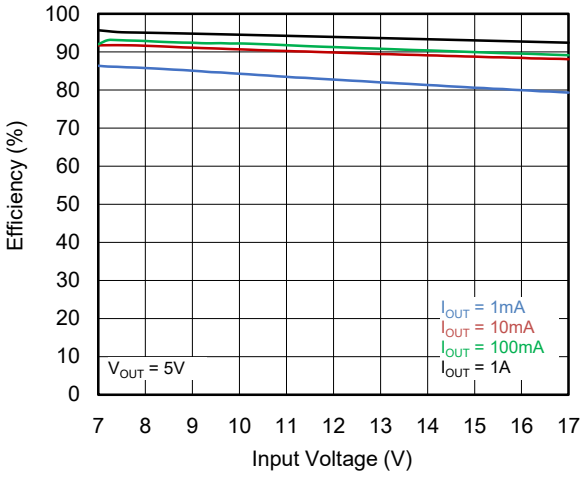
Efficiency vs. Input Voltage with 1.2MHz



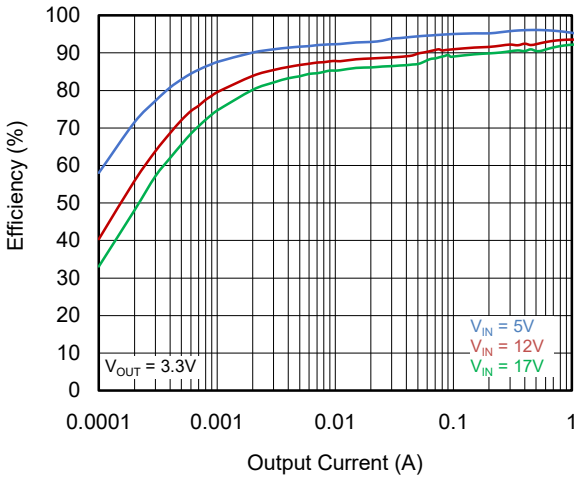
Efficiency vs. Output Current with 2.1MHz



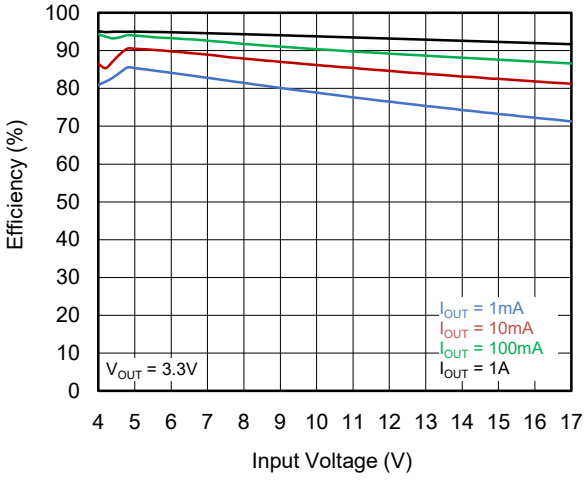
Efficiency vs. Input Voltage with 2.1MHz



Efficiency vs. Output Current with 1.2MHz



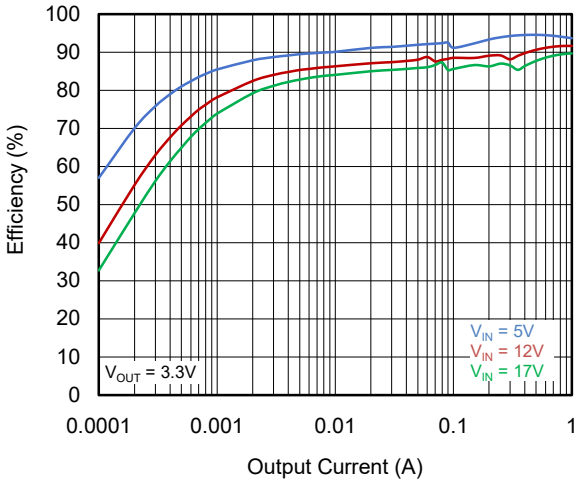
Efficiency vs. Input Voltage with 1.2MHz



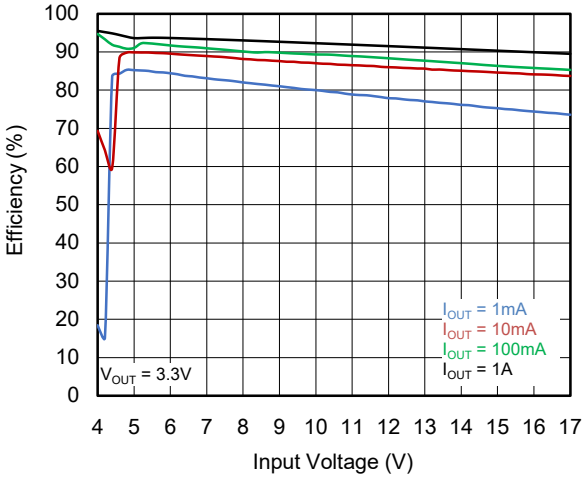
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

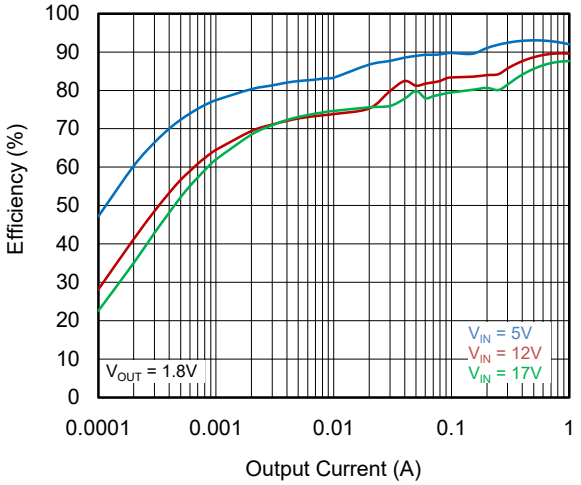
Efficiency vs. Output Current with 2.1MHz



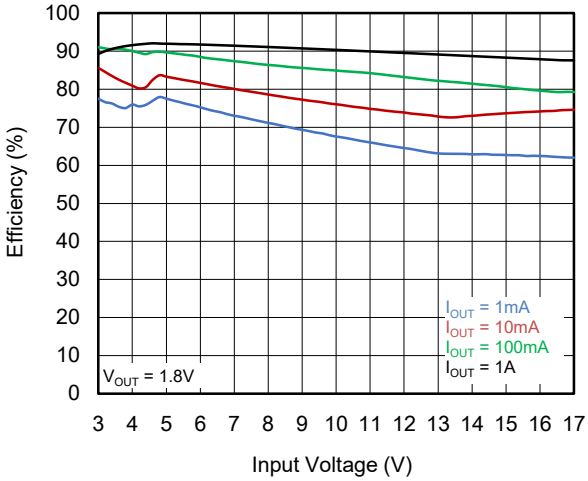
Efficiency vs. Input Voltage with 2.1MHz



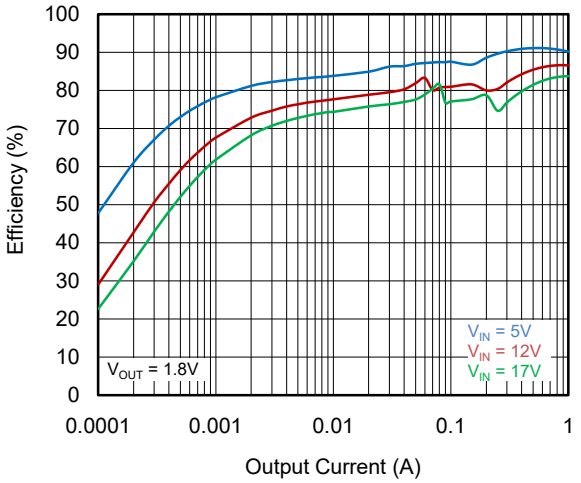
Efficiency vs. Output Current with 1.2MHz



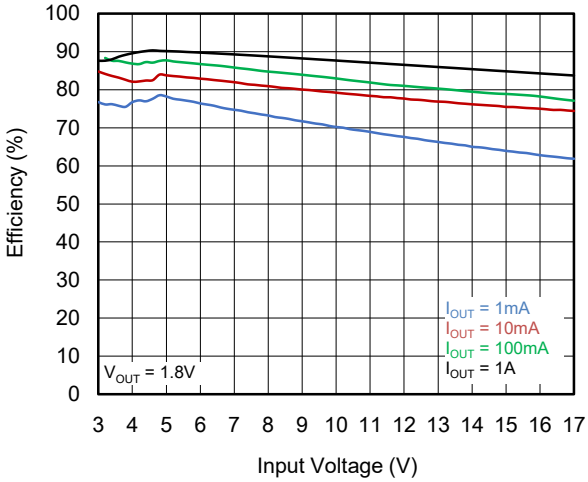
Efficiency vs. Input Voltage with 1.2MHz



Efficiency vs. Output Current with 2.1MHz



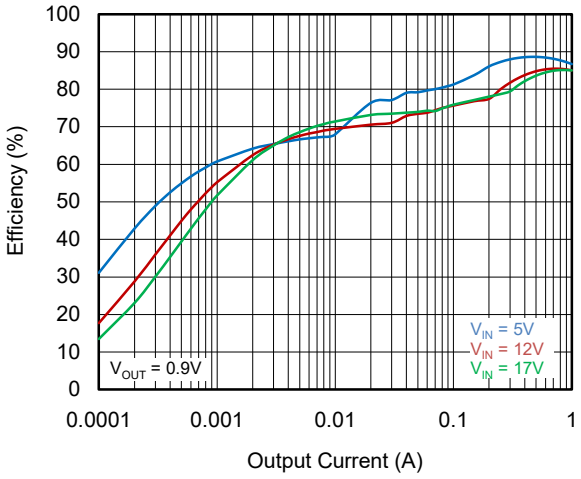
Efficiency vs. Input Voltage with 2.1MHz



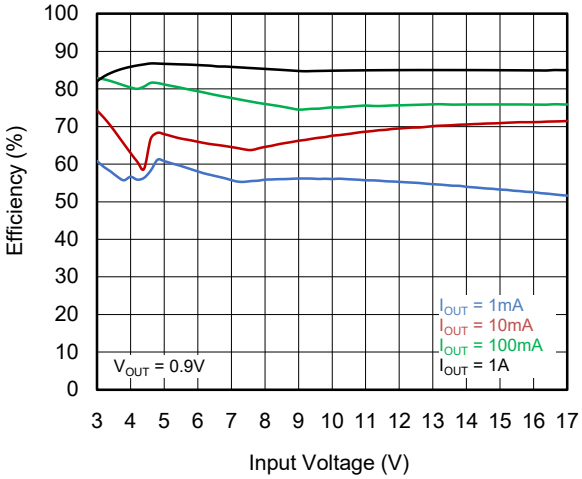
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

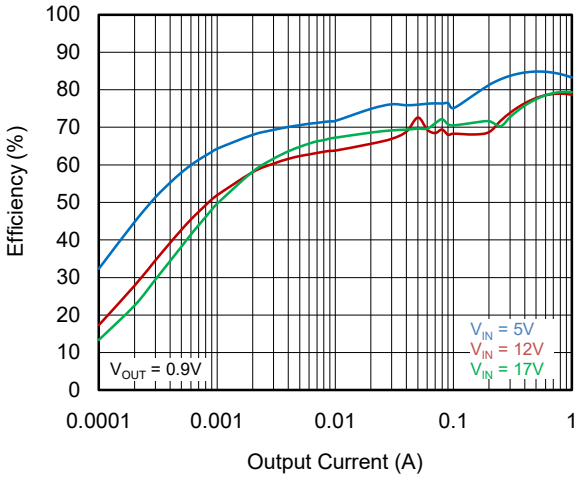
Efficiency vs. Output Current with 1.2MHz



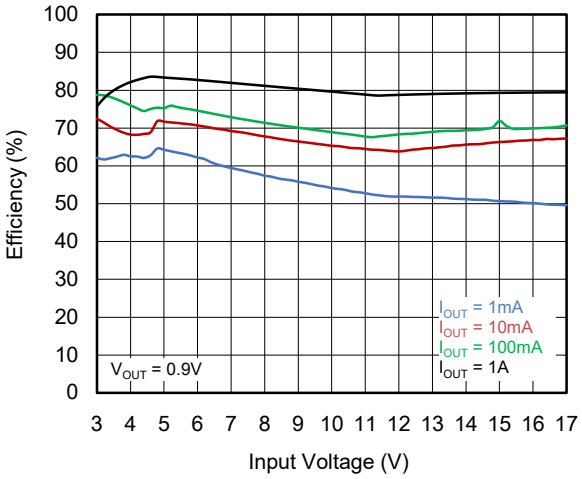
Efficiency vs. Input Voltage with 1.2MHz



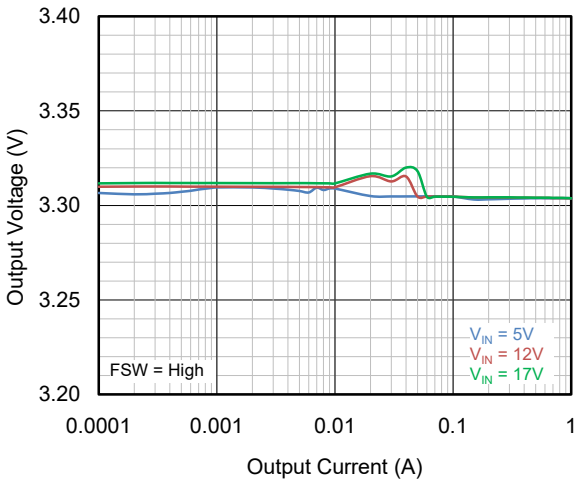
Efficiency vs. Output Current with 2.1MHz



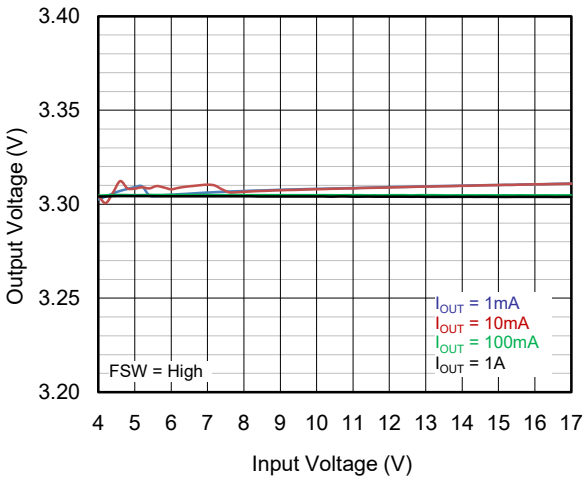
Efficiency vs. Input Voltage with 2.1MHz



Output Voltage Accuracy (Load Regulation)



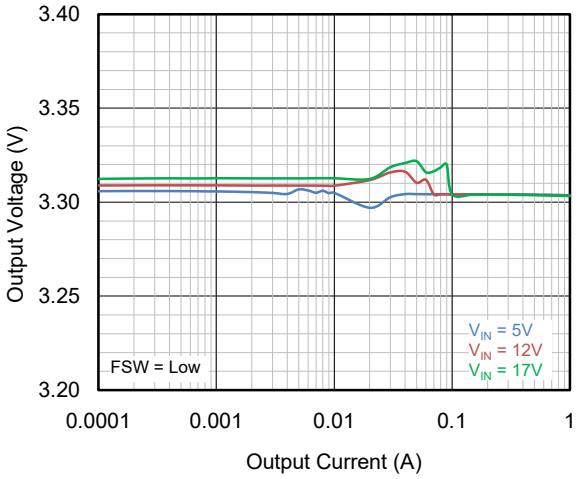
Output Voltage Accuracy (Line Regulation)



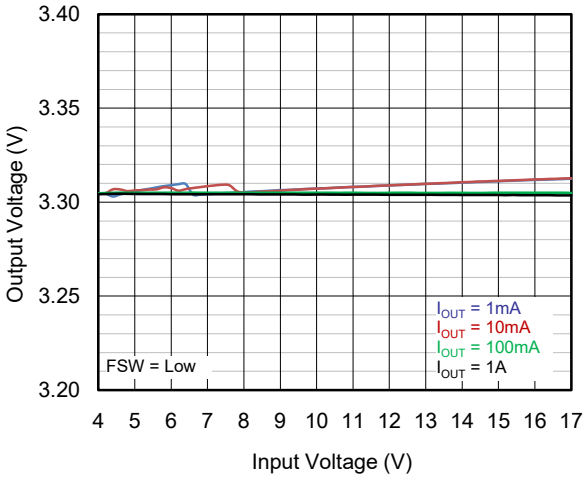
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

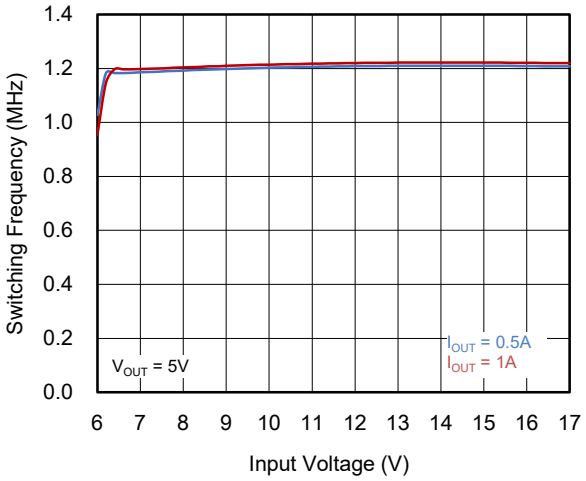
Output Voltage Accuracy (Load Regulation)



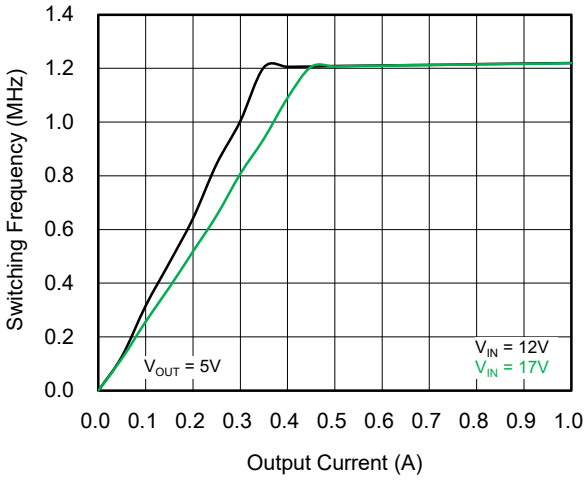
Output Voltage Accuracy (Line Regulation)



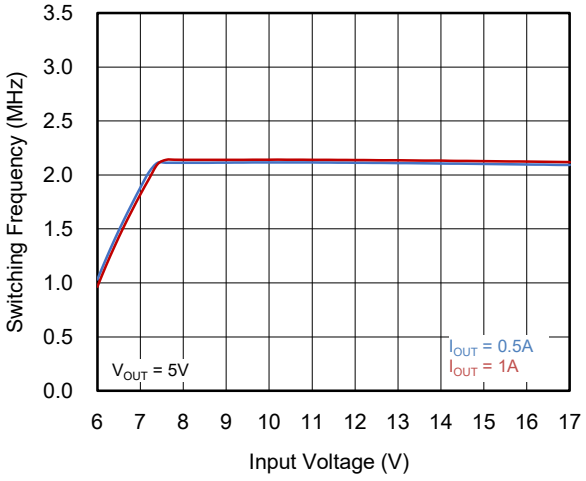
Switching Frequency vs. Input Voltage with 1.2MHz



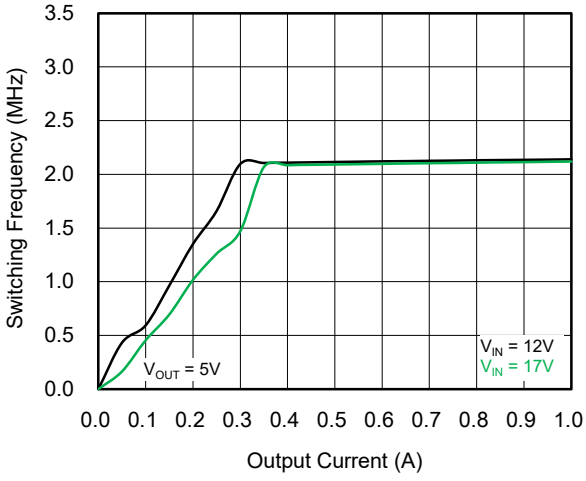
Switching Frequency vs. Output Current with 1.2MHz



Switching Frequency vs. Input Voltage with 2.1MHz



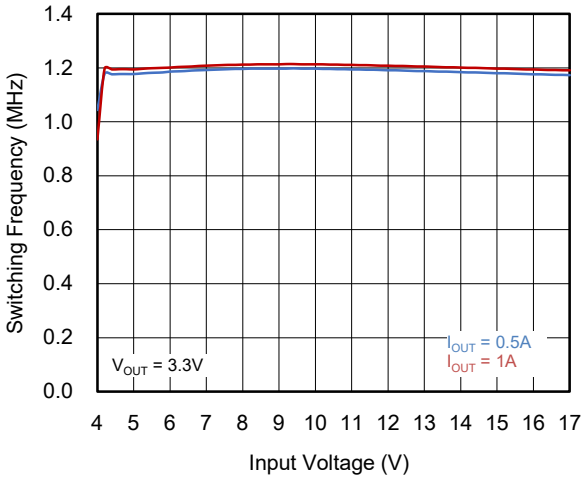
Switching Frequency vs. Output Current with 2.1MHz



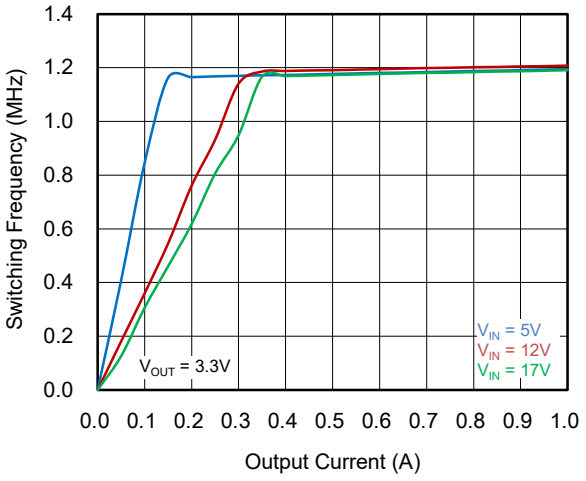
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

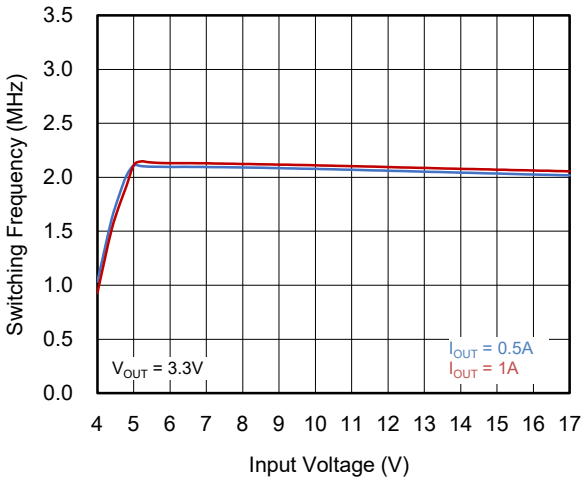
Switching Frequency vs. Input Voltage with 1.2MHz



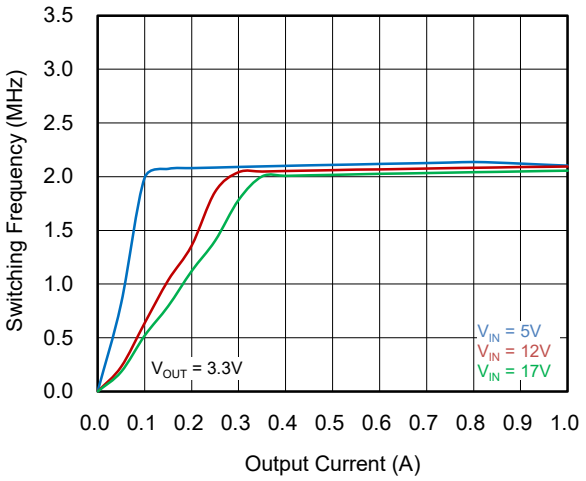
Switching Frequency vs. Output Current with 1.2MHz



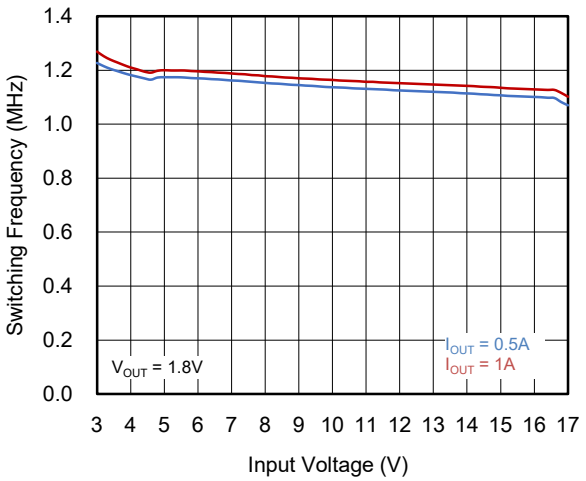
Switching Frequency vs. Input Voltage with 2.1MHz



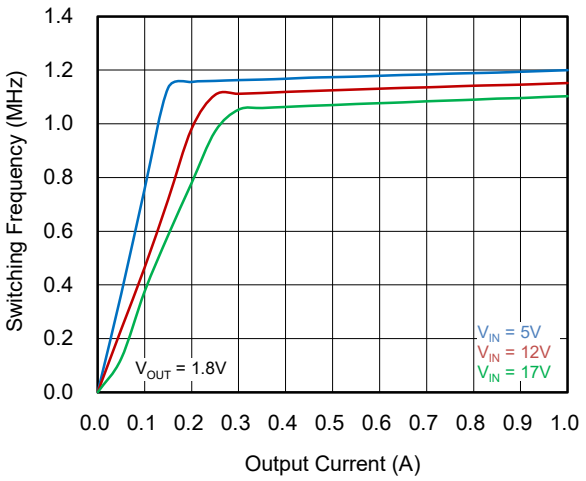
Switching Frequency vs. Output Current with 2.1MHz



Switching Frequency vs. Input Voltage with 1.2MHz



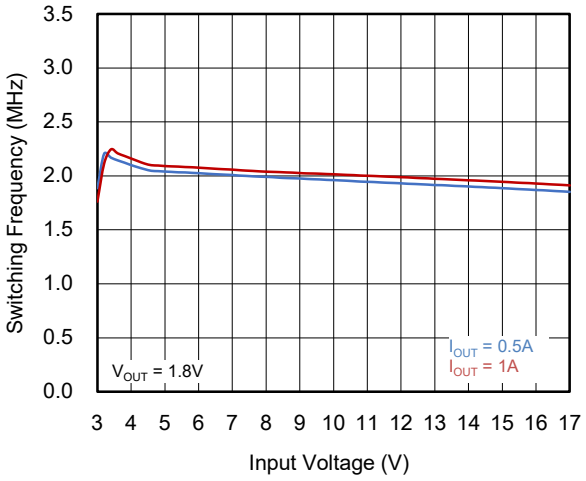
Switching Frequency vs. Output Current with 1.2MHz



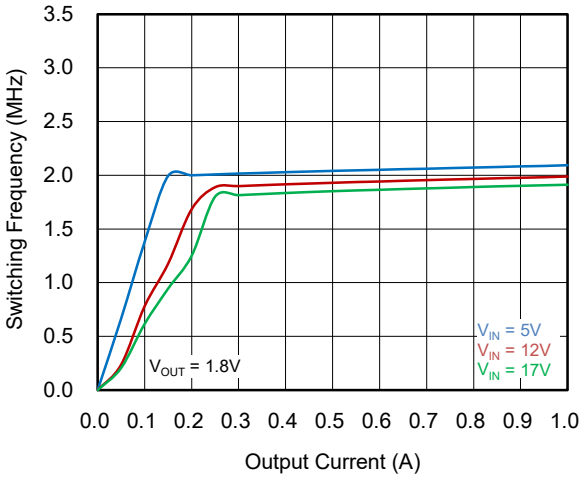
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

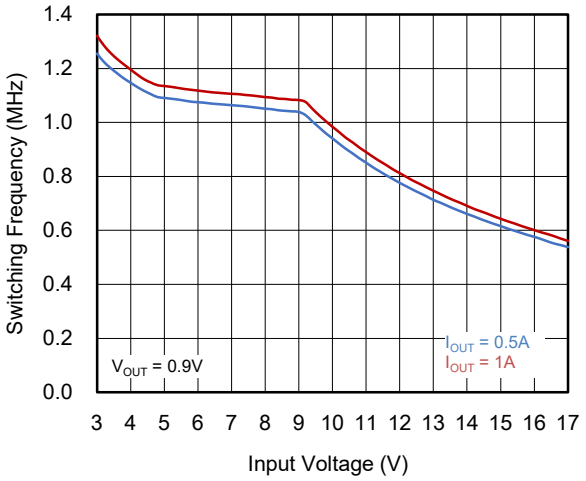
Switching Frequency vs. Input Voltage with 2.1MHz



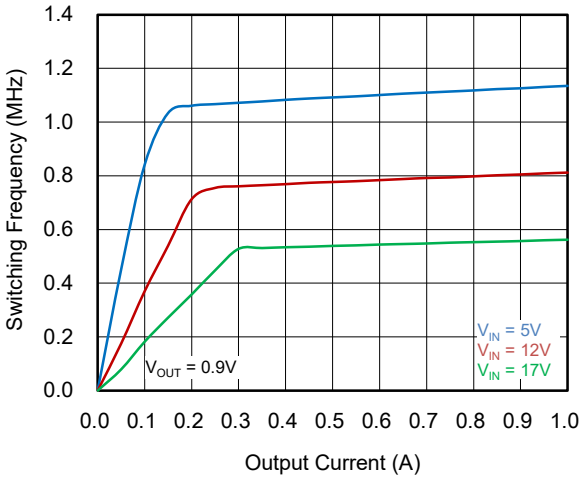
Switching Frequency vs. Output Current with 2.1MHz



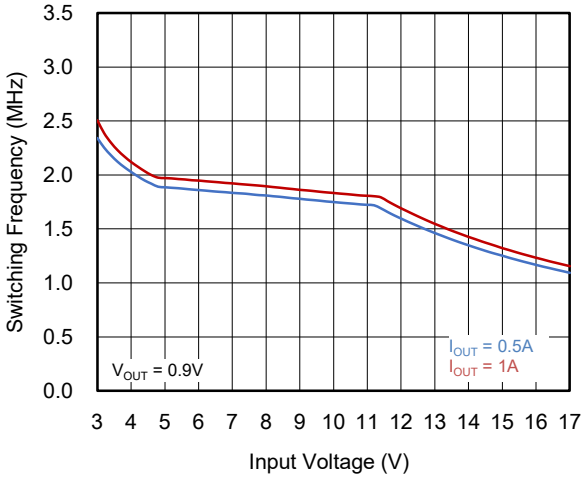
Switching Frequency vs. Input Voltage with 1.2MHz



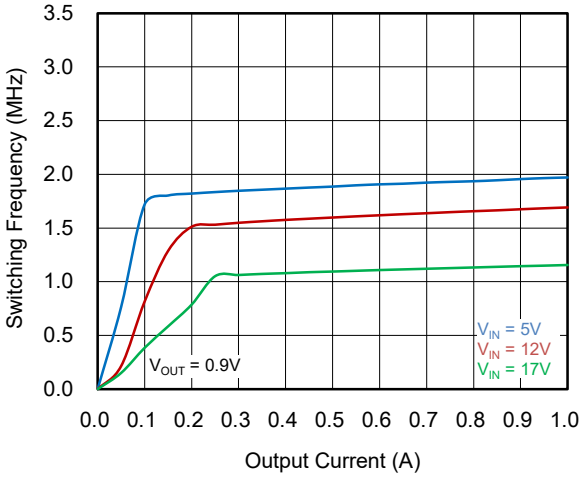
Switching Frequency vs. Output Current with 1.2MHz



Switching Frequency vs. Input Voltage with 2.1MHz



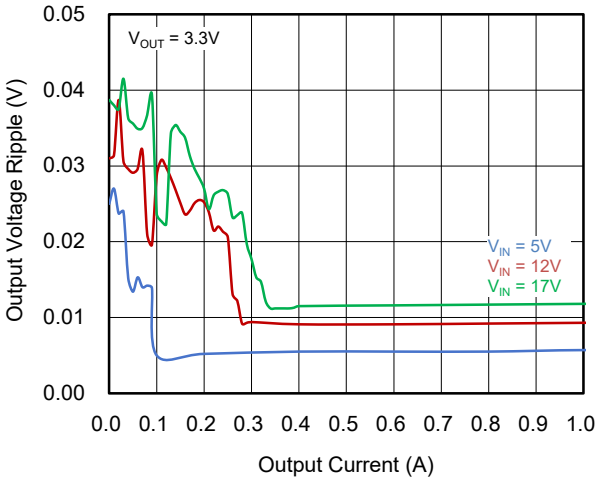
Switching Frequency vs. Output Current with 2.1MHz



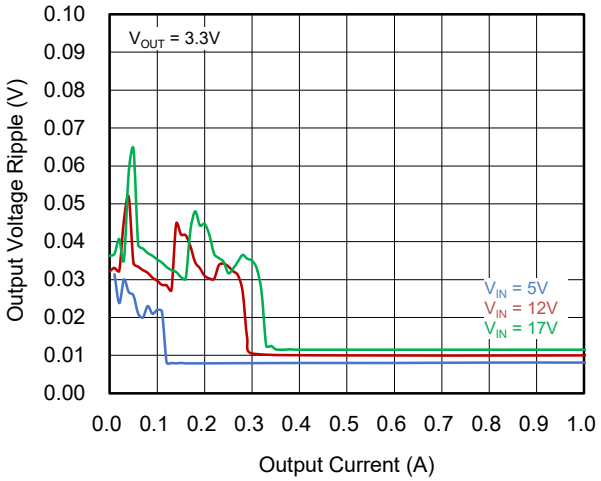
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ at FSW = low and L_1 = 3.3μH, DCR_{TYP} = 16.1mΩ at FSW = high, unless otherwise noted.

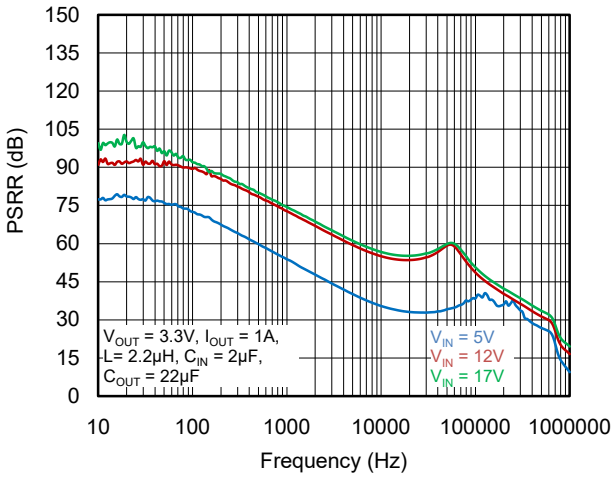
Output Voltage Ripple with 2.1MHz



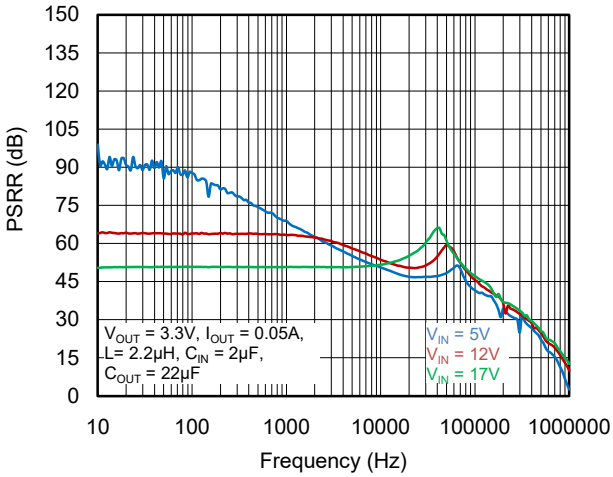
Output Voltage Ripple with 1.2MHz



Power-Supply Rejection Ratio



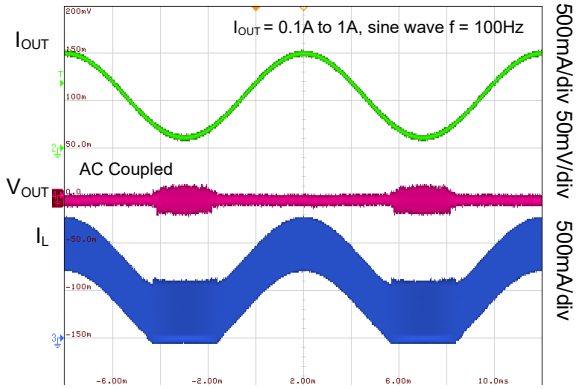
Power-Supply Rejection Ratio



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

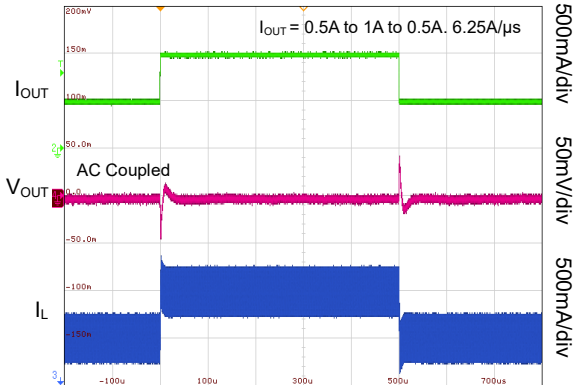
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ and FSW = low, unless otherwise noted.

PWM-to-PSM Transition



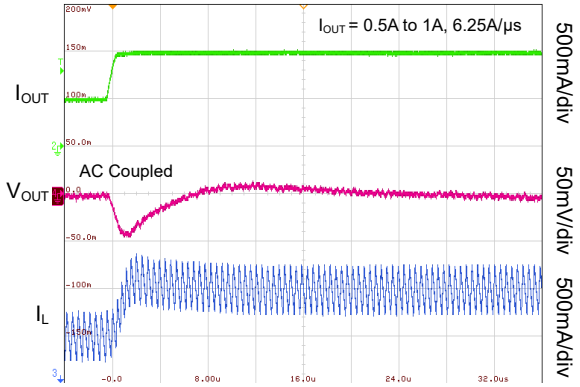
Time (2ms/div)

Load Transient Response



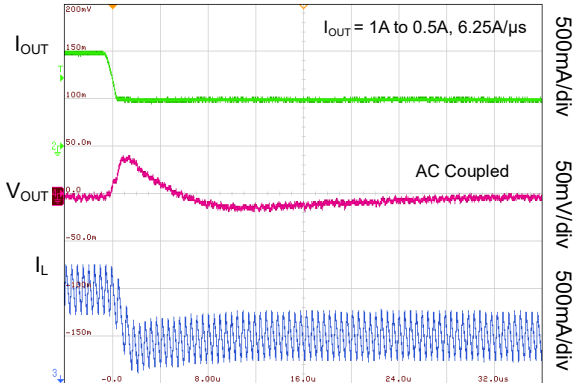
Time (100μs/div)

Load Transient Response of Rising Edge



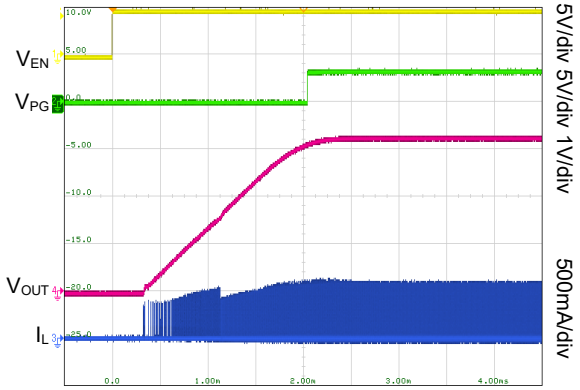
Time (4μs/div)

Load Transient Response of Falling Edge



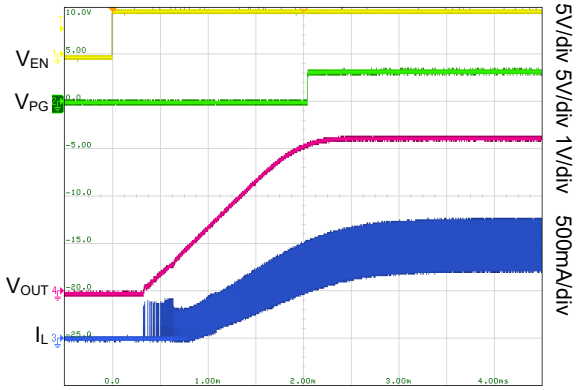
Time (4μs/div)

Startup with 100mA



Time (500μs/div)

Startup with 1A

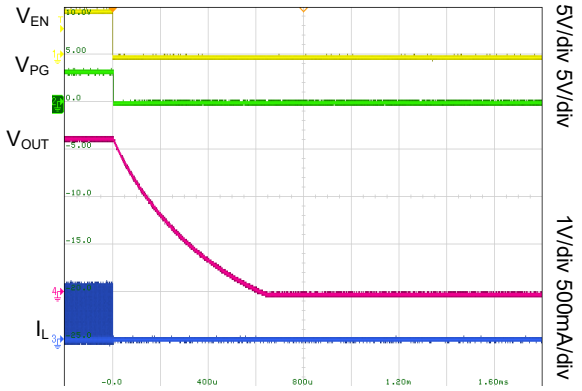


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

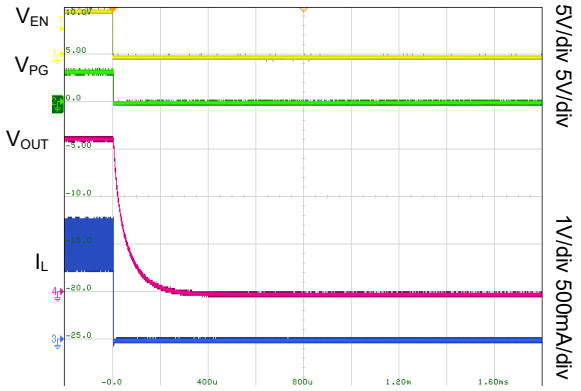
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 3.3V, L_1 = 2.2μH, DCR_{TYP} = 10.7mΩ and FSW = low, unless otherwise noted.

Shutdown with 100mA



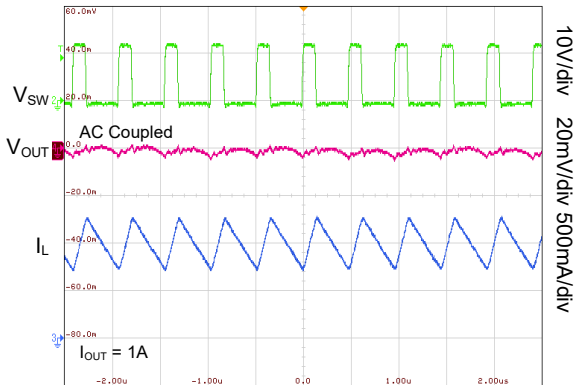
Time (200μs/div)

Shutdown with 1A



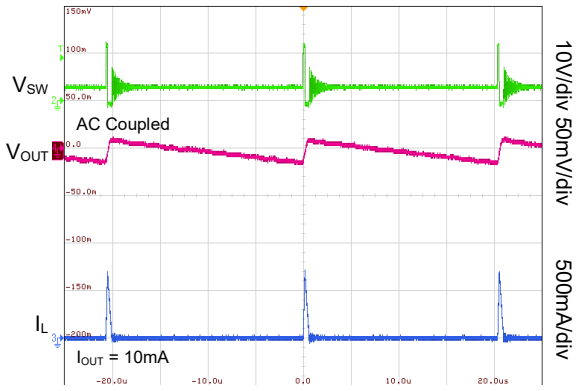
Time (200μs/div)

Typical Operation in PWM Mode



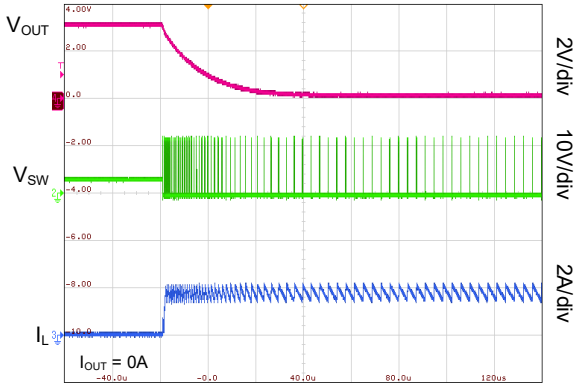
Time (500ns/div)

Typical Operation in Power-Save Mode



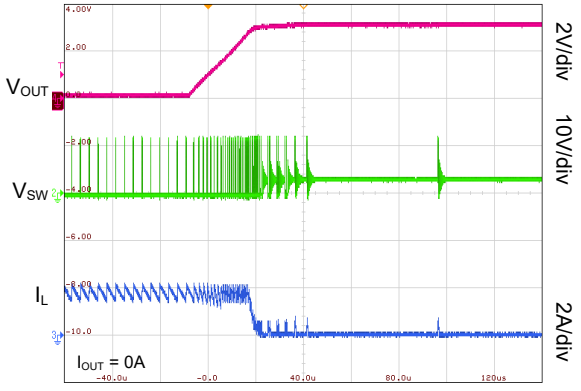
Time (5μs/div)

Current Limit with Output Short



Time (20μs/div)

Recover form Output Short



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

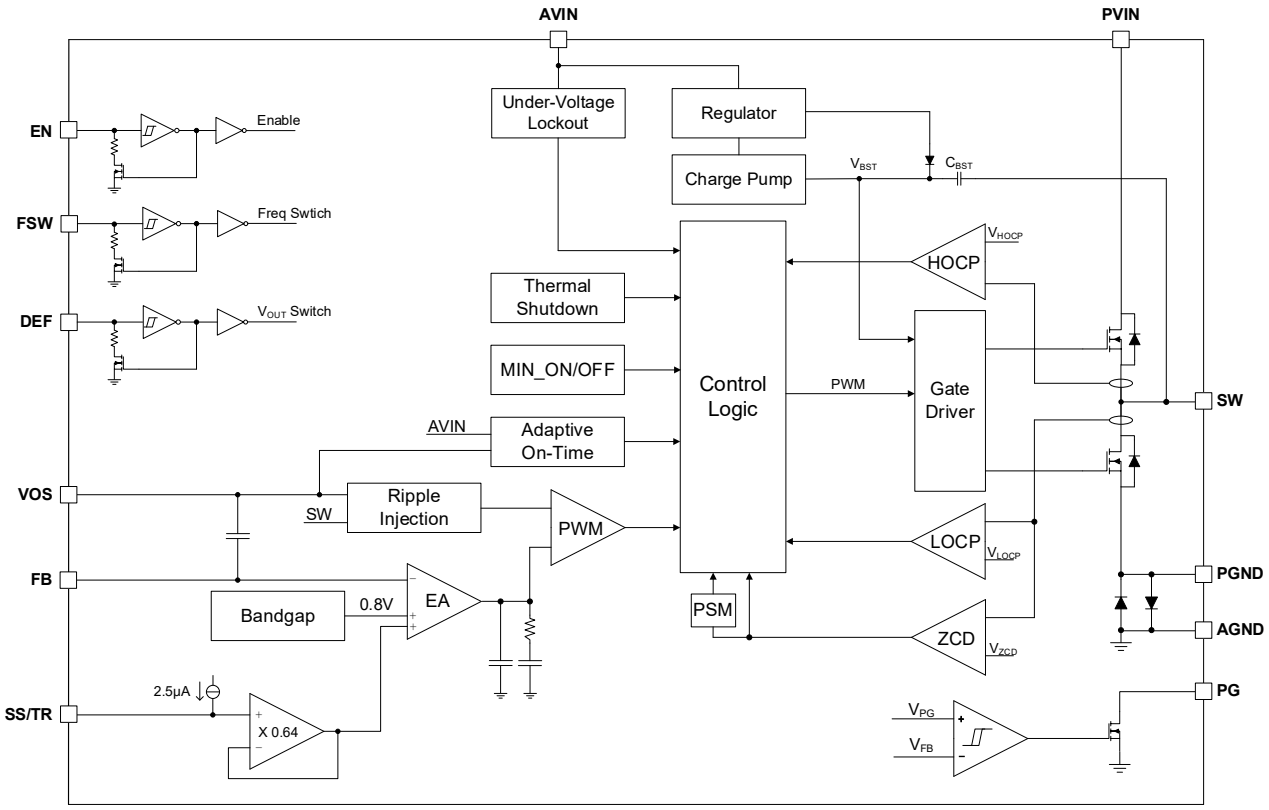


Figure 2. SGM61114-ADJ and SGM61114A-ADJ (Adjustable Output Voltage) Block Diagram

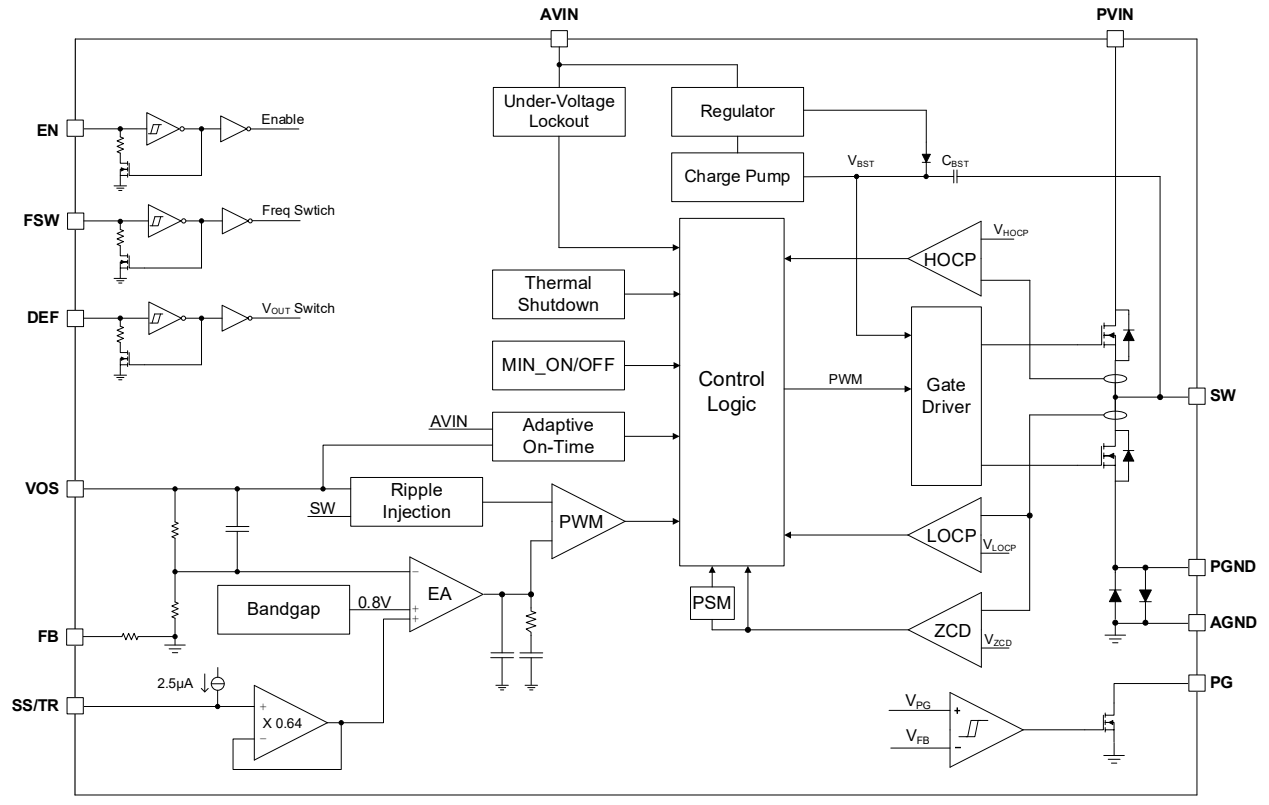


Figure 3. SGM61114-1.8/3.3/5.0 (Fixed Output Voltage) Block Diagram

DETAILED DESCRIPTION

Overview

SGM61114 is a series of high-frequency synchronous Buck converters with AHP-COT architecture and advanced regulation topology. The device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, it goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. Operation mode is seamlessly changed between PWM and PSM to keep the efficiency high in entire load range. In PWM mode, the device operates at a typical 2.1MHz or 1.2MHz switching frequency which depends on frequency selection input voltage.

Under-Voltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, under-voltage lockout is implemented to shut down the device when input voltage is lower than V_{UVLO} (when V_{IN} voltage falls). When the input voltage is higher than V_{UVLO}, the device will recover to normal operation with a 160mV hysteresis.

Device Enable and Disable (EN)

The SGM61114 is enabled by setting the EN pin input to higher than 0.66V. It is disabled when EN pin falls lower than 0.44V. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the setting point voltage. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off to reduce the device current to 3μA. The EN pin is connected with a pull-down resistor to ensure that it remains at the appropriate level. When the EN is connected to a high level, the pull-down circuit is disconnected. If it keeps floating after a low level is connected, the internal pull-down resistance will remain low until the pin is connected to a high level, so the EN pin must be reliably connected to a high or low level.

Soft-Start and Tracking (SS/TR)

A internal soft-start circuit is included to prevent input inrush current and input voltage drops during startup. This circuit slowly ramps up to the error amplifier reference voltage (V_{REF} = 0.8V) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The slope of output voltage is controlled by the external capacitor (C_{SS}) connected to the SS/TR pin, and the starting waveform is shown in Figure 4. Reducing the capacitor will obtain a faster starting speed. In order to avoid capacitor voltage overshoot, it is recommended that the C_{SS} capacitor is not less than 1nF. If the device is set to shutdown (EN = GND), UVLO, or thermal shut down, the SS/TR pin is grounded through a pull-down resistor. The SS/TR connection will restart after exiting the above states.

If an external voltage is applied to the SS/TR pin, the output voltage tracking function can be achieved. This feature is useful for voltage tracking and ratio sequencing. If the given voltage is between 0.2V (TYP) and 1V (TYP), the following relationship exists between the FB pin voltage and the tracking voltage:

$$V_{FB} \approx 0.64 \times V_{SS/TR} \quad (1)$$

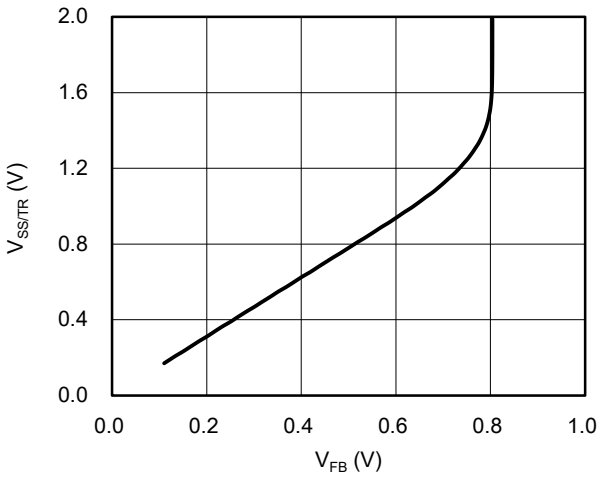


Figure 4. Voltage Tracking Curve

NOTES:

1. When $V_{SS/TR}$ exceeds 1.6V, V_{FB} is clamped to the internal feedback voltage and no longer tracks the given voltage.

2. When the tracking voltage is for external power supply, the voltage value cannot exceed V_{IN} + 0.3V.

DETAILED DESCRIPTION (continued)

The SGM61114 is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turning on, a bias on the output is likely to exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output voltage cannot drop too much during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. During the pre-biased start, when the internal set ramp voltage is higher than the pre-biased voltage, the switch is allowed to operate, and then start normally until the output voltage reaches the given value.

Power-Good (PG)

The device has PG function inside. PG is an open-drain output with a maximum sinking capacity of 2mA. Connect the pin to GND or keep it floating when it is not in use, otherwise this pin should be pulled to a logical high rail not exceeding 5.5V with an external resistor.

For the SGM61114, the PG pin is driven to a low level, when the device is started until the output voltage reaches 95% of the set value; otherwise it is in a high impedance state. For the SGM61114A, the PG pin is driven to a low level during shutdown, UVLO, and thermal shutdown states. At this time, the PG circuit can be used as an active discharge circuit of V_{OUT} in the presence of power supply voltage. Table 1 and Table 2 respectively show the PG state changes of SGM61114 and SGM61114A under different conditions. By connecting the PG signal to the EN pins of other converters, it can be used for sequencing of multiple tracks.

Table 1. PG Output State in Different Conditions (SGM61114)

Device Information		PG State	
		High-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown by EN (EN = Low)		√	
Thermal Shutdown	$T_J > T_{SD}$	√	
UVLO	$0.85V < V_{IN} < V_{UVLO}$	√	
Power Supply Removal	$V_{IN} < 0.85V$	√	

Table 2. PG Output State in Different Conditions (SGM61114A)

Device Information		PG State	
		High-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown by EN (EN = Low)			√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO	$0.85V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.85V$	√	

Selectable Output Voltage Scaling (DEF)

DEF is the input pin of the output voltage scaling function, which can achieve a +5% increase in output voltage. There is an internal pull-down resistor. When the DEF is in low state, it is pulled down internally, and the output voltage will be set to its nominal value (V_{NOM}). Otherwise, when it is pulled up (maximum voltage no higher than 5.5V, it can be connected to V_{OUT} or PG), the output will be scaled to +5% ($1.05 \times V_{NOM}$). If it is in high-impedance or floating, it will be set to low. The output voltage scaling function enhances device adaptability.

Selectable Frequency (FSW)

The SGM61114 can be switched frequency by FSW pin setting. If the pin is pulled down, the normal operating switching frequency will be 2.1MHz (TYP), if the pin is pulled up, set to 1.2MHz (TYP) respectively. This pin is pulled down internally in the low state and will be set to low if it is floating. There is a pull-down resistor inside the pin, which acts in the same way as the DEF pin.

High switching frequency has the advantage of high power density and low voltage ripple, but it brings higher switching loss. On the contrary, low switching frequency has higher efficiency, but will have higher voltage ripple and surge current. In practical applications, the appropriate switching frequency should be selected according to the requirements of key parameters.

DETAILED DESCRIPTION (continued)

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM) which occurs at medium to heavy loads, the device works in pulse width modulation (PWM) operation. Then a fixed on-time architecture is activated. The device operates at a nominal switching frequency of 2.1MHz or 1.2MHz, depending on the setting of the FSW pin.

Power-Save Mode (PSM)

As the load current decreases, the inductor current will change from continuous mode (CCM) to discontinuous mode (DCM). At this time, the on-time t_{ON} of the switch in COT mode is unchanged, and the turn-off time becomes longer, so the switching frequency decreases. When the load current is further reduced, the SGM61114 series will enter the power saving mode. The device then maintains high efficiency by reducing the switching frequency and operating at a minimum static current. In PSM mode, the inductor current is discontinuous and the output voltage is slightly higher than the nominal output voltage. This effect can be mitigated by a larger output capacitance. The switching frequency is greatly reduced as the load current decreases in PSM mode.

When the duty cycle is small, the minimum on-time is set to limit the switching loss, in which case the circuit frequency is below the nominal value. When the input and output voltages are close, the device will remain in CCM, no matter how the load changes, and no longer enter PSM mode.

100% Duty Cycle

When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 2:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (2)$$

where:

V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is the maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection

Limiting switch current protects the switch itself and also prevents over-current sources and the inductor. When the high-side (HS) switch current exceeds high-side MOSFET current limit (2.2A), the HS switch is off and the low-side (LS) switch is on to reduce the inductive current and limit the peak current. The switch on the high-side (HS) can be turned on again only when the switch current on the low-side (LS) is lower than low-side MOSFET current limit (1.4A).

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 16℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGM61114 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

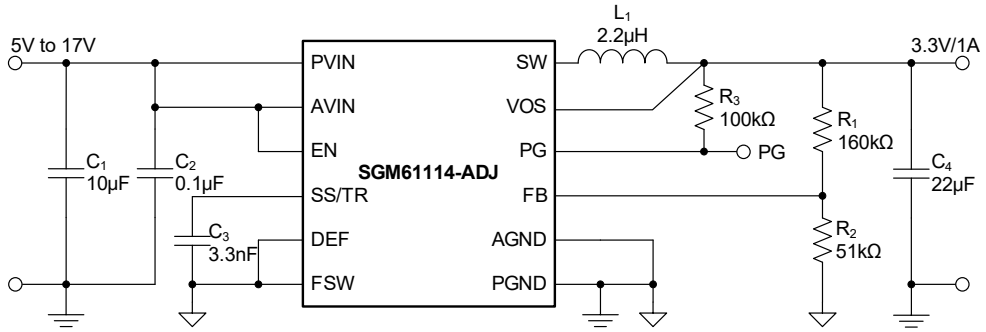


Figure 5. 3.3V Output Voltage Application of SGM61114-ADJ/SGM61114A-ADJ

Design Requirements

Table 3 summarizes the requirements for this example as shown in Figure 5. The selected components are given in Table 4.

Table 3. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage (SGM61114/SGM61114A)	5V to 17V
Output Voltage	3.3V
Maximum Output Current	1A
Switching Frequency	2.1MHz

Table 4. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	10μF,Ceramic Capacitor, 25V, Size1210	Standard
C_2	0.1μF, Ceramic Capacitor, 25V, Size 0603	Standard
C_3	3.3nF, Ceramic capacitor, 25V, Size 0603	Standard
C_4	22μF, Ceramic Capacitor, 6.3V, Size 0805	Standard
L_1	2.2μH, Power Inductor, DCR_{TYP} = 10.7mΩ, I_{SAT} = 7.1A, I_{RMS} = 9A	Sunlord
R_1	160kΩ, Chip Resistor,1/16W, 1%, Size 0603	Standard
R_2	51kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Input Capacitor Selection (C_{IN})

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. In most cases, a 10μF input capacitor is recommended, a larger value reduces input voltage ripple and improves system stability. Usually a 0.1μF low ESR ceramic capacitor is recommended to be connected between the AVIN and AGND pins as closely as possible.

Inductor Selection

The important factors for inductor selection are inductance (L), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equation 3 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

Typically, the peak-to-peak inductor current is selected between 10% and 40% of the maximum output current. The inductor of that the saturation current is 20% higher than I_{L_MAX} is recommended. The inductor initial tolerance can be as high as -20% to +20% of the nominal value and proper current derating is usually required. More generally, choosing the saturation current above high-side limit is enough. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Larger inductance values reduce the ripple current but lead to sluggish transient response. 2.2μH is the recommended value for the typical application. If FSW pin is pulled high, 3.3μH is recommended.

APPLICATION INFORMATION (continued)

Output Capacitor Selection (C_{OUT})

The architecture of the SGM61114 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors are recommended due to the low output voltage ripple. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. The bias voltage can cause the capacitance of the ceramic capacitor to decrease significantly, and the degree of decrease depends on the specification of the capacitor (size, nominal voltage, temperature standard).

The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. C_{OUT} = 22μF is the recommended values for the typical application. If the switching frequency is seriously reduced due to the decrease of the input voltage, it is recommended to increase the output capacitance to ensure system stability.

Soft-Start Capacitor Selection (C_{SS})

The slope of soft-start output voltage can be changed through the selection of SS/TR external capacitor, and the external capacitor can be charged through 2.5μA (TYP) constant current source inside the chip. The relationship between soft-start time and capacitance is shown in the following Equation 4:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{1.25V} \quad (4)$$

where:

C_{SS} is the capacitance (F) required at the SS/TR pin.

t_{SS} is the desired soft-start ramp time (s).

Output Voltage Adjustment

Use Equation 5 for selecting the feedback resistors (R_1 and R_2) in Figure 5 to set the desired output voltage. There is a 20pF capacitance between the VOS pin and the FB pin inside the device. It forms a set of zero-pole pair with R_1 and R_2. The position of the zero-pole pair will affect the dynamic characteristics and stability of the system. Therefore, for different output voltages please refer to the R_1/R_2 values of similar output voltages in Figure 5 to Figure 8.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (5)$$

APPLICATION INFORMATION (continued)

Various Output Voltages

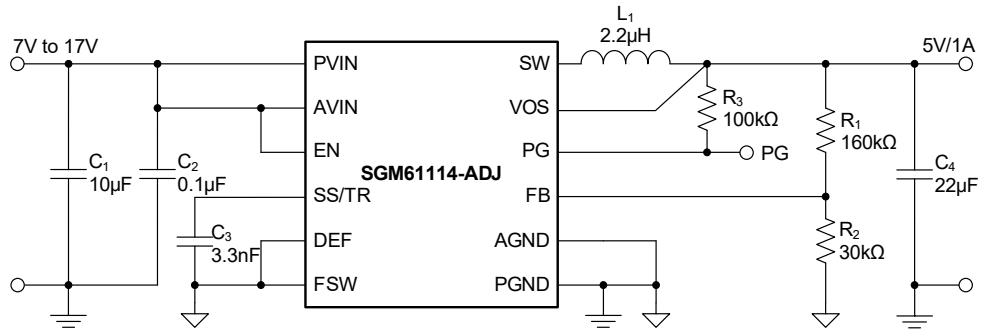


Figure 6. 5V Output Voltage Application of SGM61114-ADJ/SGM61114A-ADJ

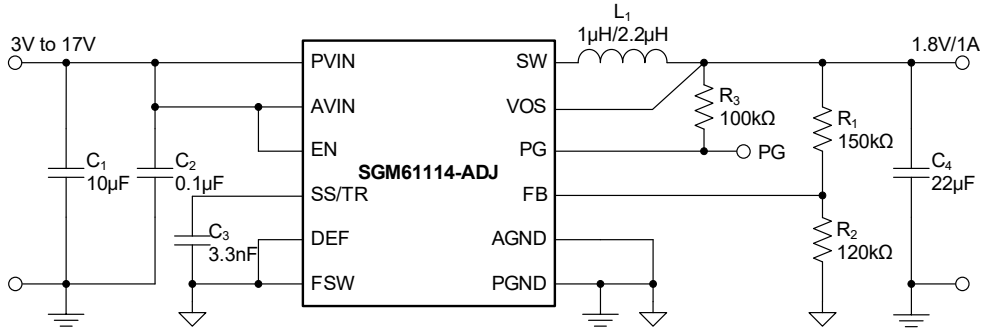


Figure 7. 1.8V Output Voltage Application of SGM61114-ADJ/SGM61114A-ADJ

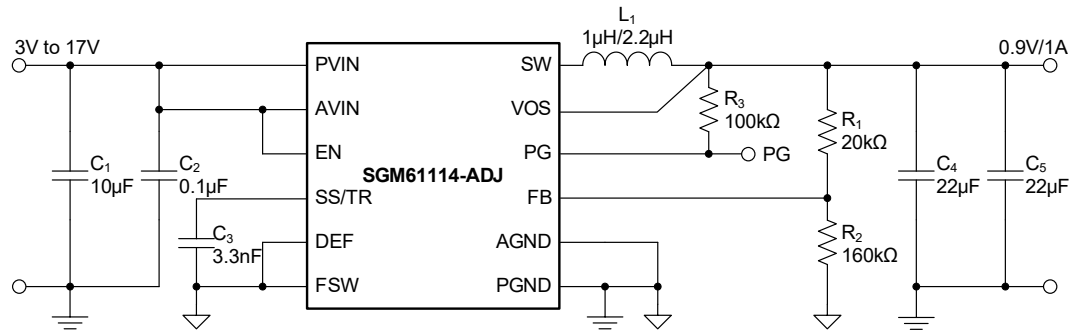


Figure 8. 0.9V Output Voltage Application of SGM61114-ADJ/SGM61114A-ADJ

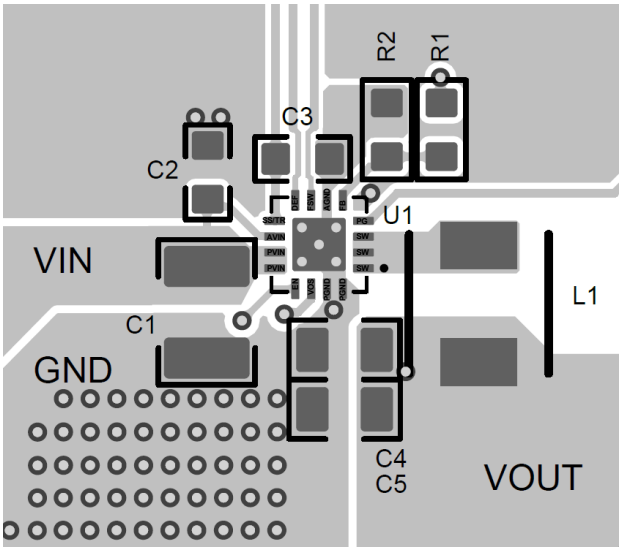
APPLICATION INFORMATION (continued)

Layout Guidelines

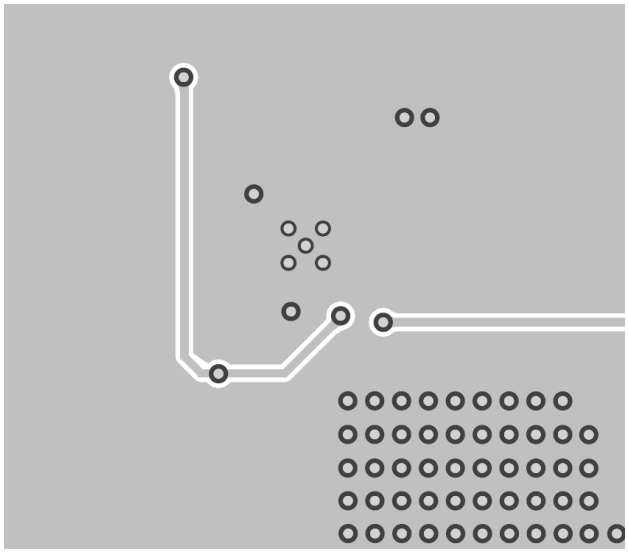
A good printed-circuit-board (PCB) layout is a critical element of any high-performance design. Follow the guidelines below for designing a good layout for the SGM61114.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device PGND pin to minimize the AC current loops.
- Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep signal traces such as FB and VOS sensing lines away from SW or other noise sources. Both of them need to be connected to VOUT by the shortest path and near the output capacitor.
- Divider resistors and C_{SS} are placed close to the IC and connect to the AGND, FB and SS/TR pins directly.
- AGND pin and PGND pin need to be connected through the exposed pad for single-point grounding. In order to ensure mechanical reliability and good heat dissipation, the exposed pad must be fully welded to the circuit board.
- Use GND planes in middle layers for shielding and minimizing the ground potential drifts.

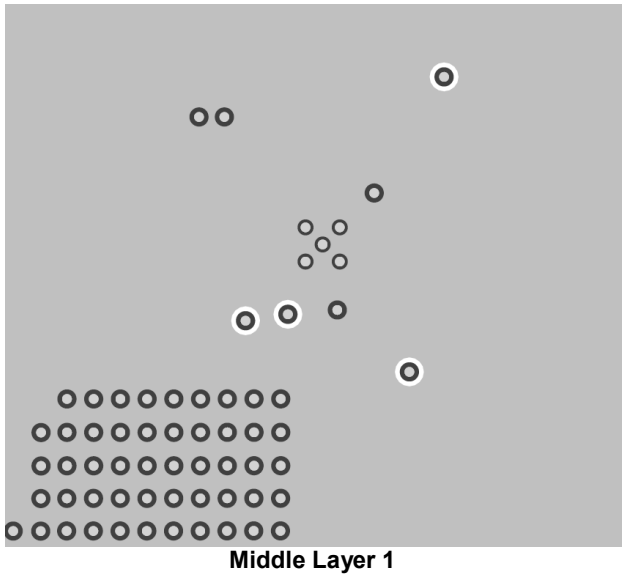
Refer to Figure 9 for a recommended PCB layout.



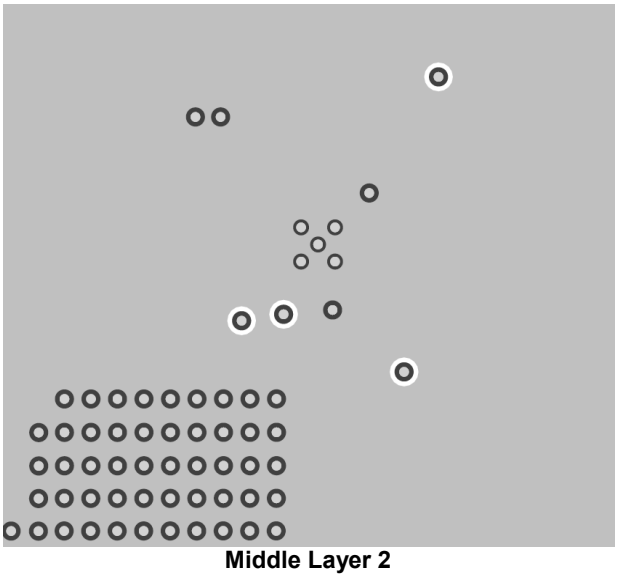
Top Layer



Bottom Layer



Middle Layer 1



Middle Layer 2

Figure 9. PCB Layout

REVISION HISTORY

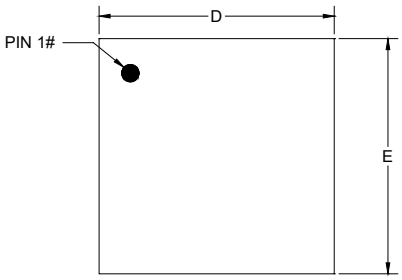
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2024 – REV.A to REV.A.1	Page
Updated Switch Current Limits and Short-Circuit Protection section	18

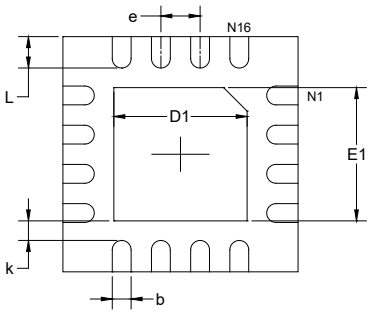
Changes from Original (SEPTEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

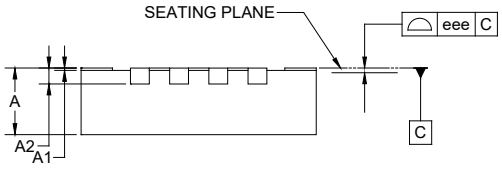
TQFN-3×3-16L



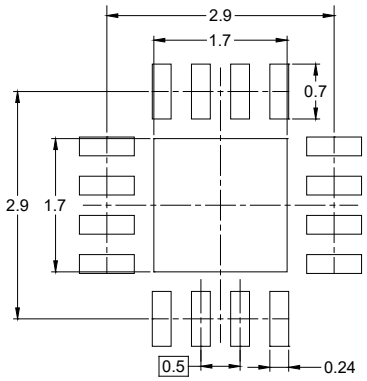
TOP VIEW



BOTTOM VIEW



SIDE VIEW



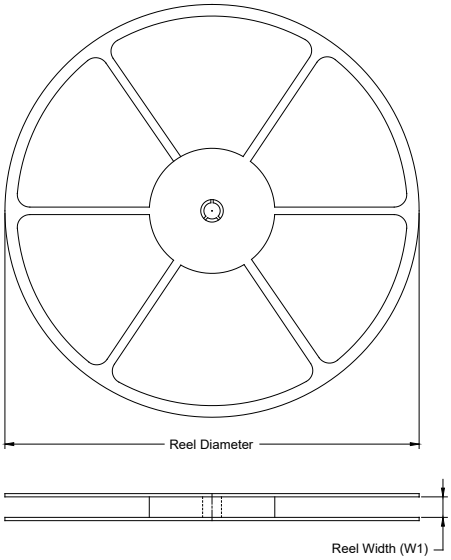
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.800	-	0.900
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	2.900	-	3.100
D1	1.600	-	1.800
E	2.900	-	3.100
E1	1.600	-	1.800
e	0.500 BSC		
L	0.300	-	0.500
k	0.200 MIN		
eee	0.080		

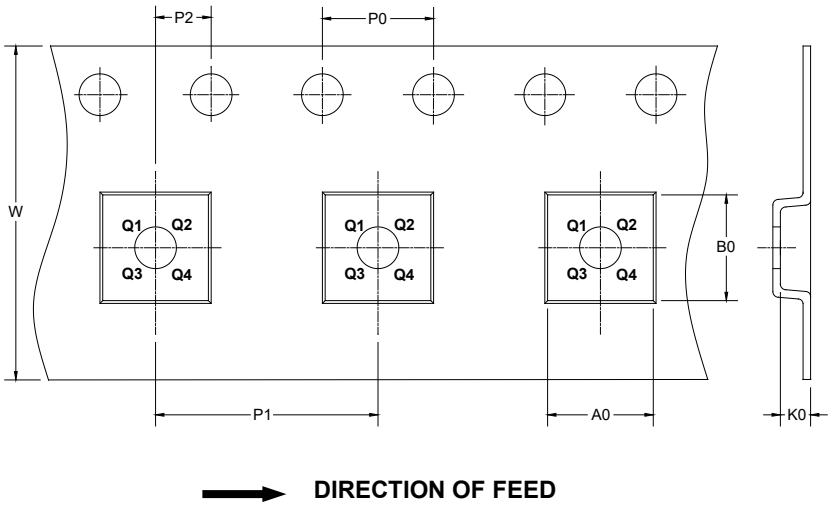
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



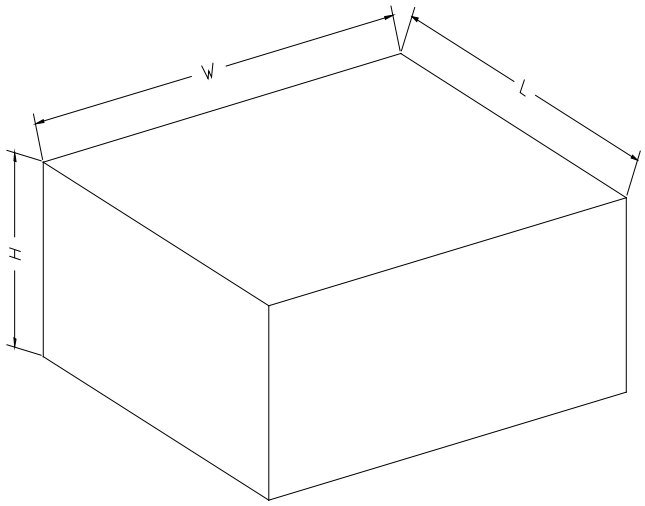
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002