SGM61032SD
2.5V to 5.5V, 3A High Efficiency, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61032SD is a high efficiency and miniature size synchronous Buck converter for low input voltage applications. It is a perfect solution for compact designs. The 2.5V to 5.5V input voltage range is suitable for almost all available battery-powered applications. It operates in PWM mode at 1.5MHz (TYP) in the medium to heavy load range and automatically enters or exits the power-save mode (PSM) at light loads to maintain its high efficiency. During shutdown, the quiescent current is 0.32μA (TYP).

This device is based on adaptive off-time architecture, but still allows a wide range of output capacitors. This flexibility makes the device a good choice for system power rails supply. The adaptive off-time architecture provides excellent output voltage accuracy and superb load transient response. Only external feed-forward compensation capacitor is needed to obtain faster response.

The SGM61032SD is available in a Green SOT-563-6 package.

FEATURES

- **Support 1.2V GPIO**
- **2.5V to 5.5V Input Voltage Range**
- **Adjustable Output Voltage from 0.6V to V_{IN}**
- **Adaptive Off-Time Architecture**
- **Up to 95% Efficiency**
- **Low R_{DSON} Internal Switches: 53mΩ/28mΩ**
- **48μA (TYP) Quiescent Current**
- **Power-Save Mode at Light Loads**
- **Low Dropout with 100% Duty Cycle**
- **PG Output**
- **Fast Load Response**
- **Internal Soft-Start with Pre-biased Startup**
- **Output Discharge at Shutdown**
- **Hiccup Mode OCP/Short-Circuit Protection**
- **Thermal Shutdown Protection**
- **Available in a Green SOT-563-6 Package**

APPLICATIONS

Industrial and Commercial Applications
General Purpose Point-of-Load Power Supplies
Potable Battery-Powered Applications
Wireless Routers, Solid State Drives
Set-Top Boxes, Multi-Function Printers

TYPICAL APPLICATION

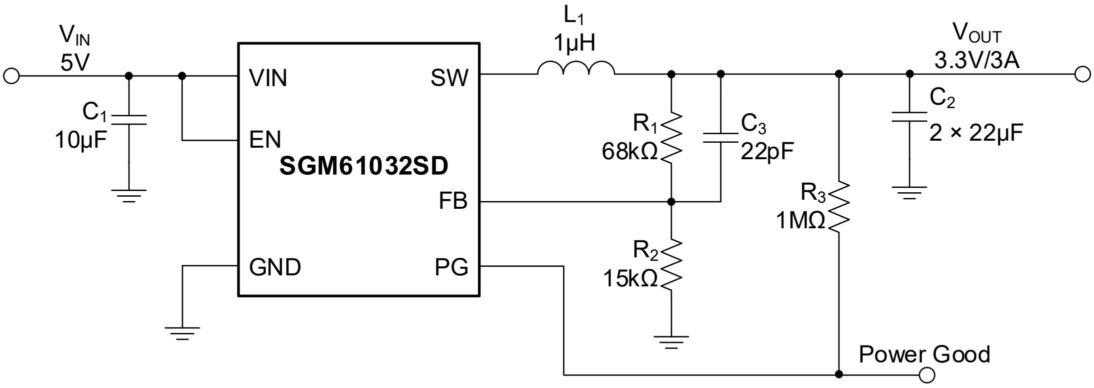


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61032SD	SOT-563-6	-40℃ to +125℃	SGM61032SDXKB6G/TR	0RXX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XX = Date Code.

YY X X

- Date Code - Week
- Date Code - Year
- Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, EN, PG Voltages (1) .... -0.3V to 6V
FB Voltage (1) .... -0.3V to 3V
SW Voltage
DC (1) .... -0.3V to V_{IN} + 0.3V
While Switching, Less than 10ns (1) .... -3.0V to 9V
Package Thermal Resistance
SOT-563-6, θ_{JA} .... 123.9℃/W
SOT-563-6, θ_{JB} .... 24.8℃/W
SOT-563-6, θ_{JC} .... 69.4℃/W
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility (2) (3)
HBM .... ±2000V
CDM .... ±1000V

NOTES:

1. All voltages are referred to the ground terminal.
2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .... 2.5V to 5.5V
Output Voltage Range, V_{OUT} .... 0.6V to V_{IN}
Sink Current at PG Pin, I_{SINK_PG} .... 1mA (MAX)
Output Current .... 0A to 3A
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

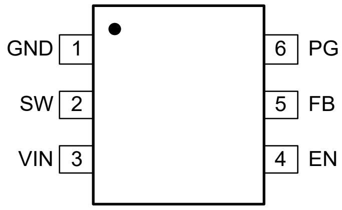
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOT-563-6

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	GND	G	Ground Pin.
2	SW	P	Converter Switching Node Output Pin. Connect to the switching terminal of the output inductor.
3	VIN	P	Power Supply Input Pin.
4	EN	I	Enable Input pin. Pull this pin to logic high to enable the device and pull it low to disable it. Do not leave this pin floating.
5	FB	I	Feedback Input Pin for the Control Loop. Connect this pin to the output feedback resistor divider.
6	PG	O	Power Good Open-Drain Output Pin. Pull this pin up with a resistor to a voltage below 5.5V. If not used, leave it open or connect to GND.

NOTE: I = input, O = output, P = power, G = ground.

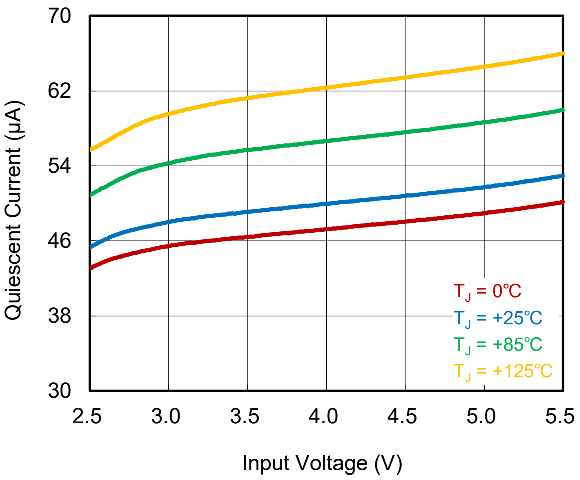
ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

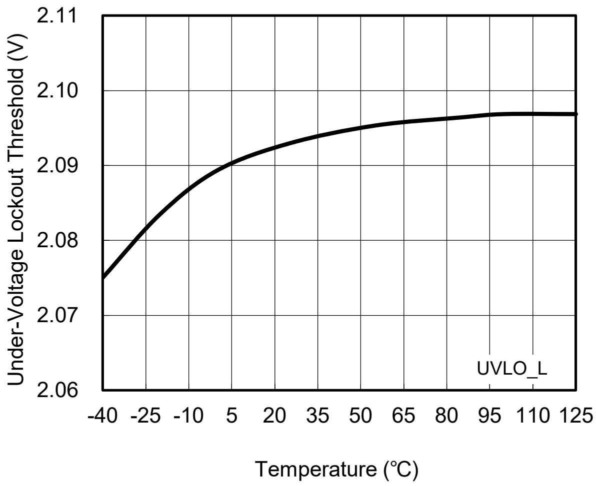
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
Input Voltage Range	V_{IN}		2.5		5.5	V
Quiescent Current into VIN	I_Q	No load, V_{IN} = 2.5V to 5.5V		48	78	μA
Shutdown Current into VIN	I_{SD}	EN = low, V_{IN} = 2.5V to 5.5V, T_J = +25℃		0.32	1.3	μA
		EN = low, V_{IN} = 2.5V to 5.5V, T_J = -40℃ to +25℃			4.5	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling	2	2.1	2.2	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			200		mV
Thermal Shutdown Threshold	T_{SD}	T_J rising		150		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			25		℃
EN Logic Levels						
High-Level Input Voltage	V_{IH}	V_{IN} = 2.5V to 5.5V	0.8			V
Low-Level Input Voltage	V_{IL}	V_{IN} = 2.5V to 5.5V			0.4	V
Input Leakage Current into EN Pin	I_{EN_LKG}	V_{IN} = V_{EN} = 5.5V		0.01	0.55	μA
Soft-Start						
Soft-Start Time	t_{SS}	Measure from 0 to 95% × V_{OUT} (set)		970		μs
Power Good						
Power Good Threshold	V_{PG}	V_{OUT} rising		95% × V_{REF}		V
		V_{OUT} falling		90% × V_{REF}		V
Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA		0.13	0.3	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01	0.5	μA
Power Good Delay	t_{PG_DLY}	V_{FB} falling		45		μs
Output						
Feedback Regulation Voltage	V_{FB}	PWM mode, V_{IN} = 2.5V to 5.5V	594	600	606	mV
Feedback Input Leakage Current	I_{FB_LKG}	V_{FB} = 1V		0.01	0.1	μA
Output Discharge FET On-Resistance	R_{DIS}	EN = low, V_{OUT} = 1.8V		16		Ω
Power Switch						
High-side FET On-Resistance	R_{DSON}	I_{SW} = 500mA		53	82	mΩ
Low-side FET On-Resistance	R_{DSON}	I_{SW} = 500mA		28	45	mΩ
High-side FET Switch Current Limit	I_{LIM}		3.90	5	6.30	A
PWM Switching Frequency	f_{SW}	V_{OUT} = 1.8V, I_{OUT} = 1A		1.5		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

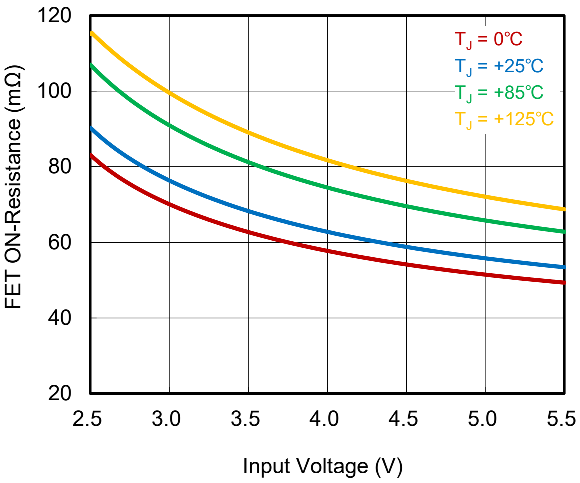
Quiescent Current vs. Input Voltage



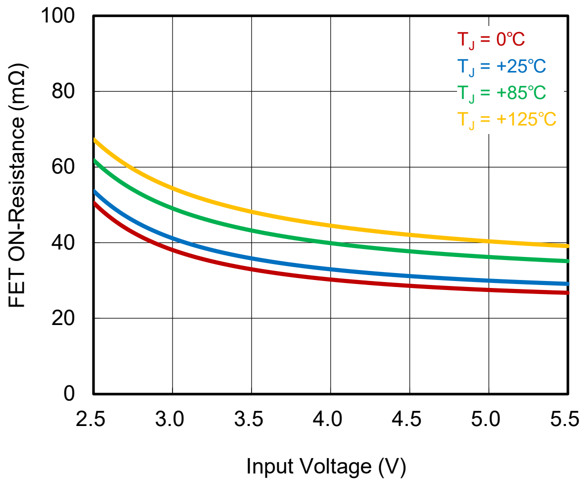
Under-Voltage Lockout Threshold vs. Temperature



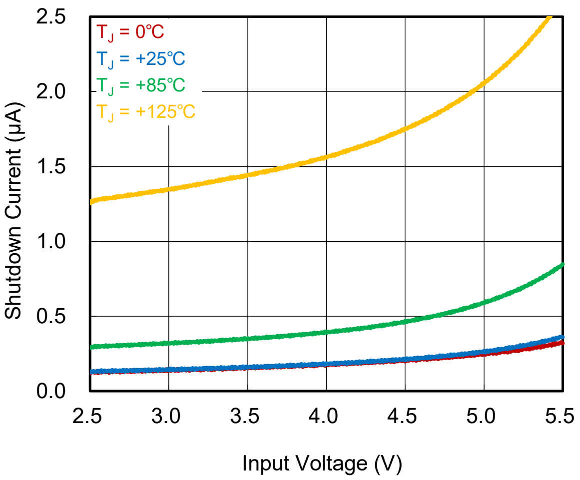
FET ON-Resistance vs. Input Voltage (High)



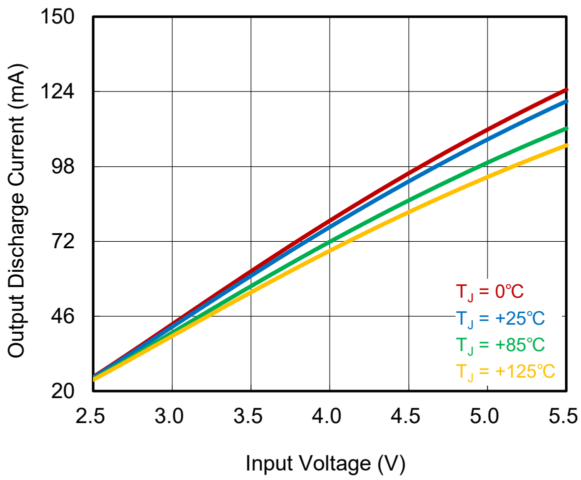
FET ON-Resistance vs. Input Voltage (Low)



Shutdown Current vs. Input Voltage

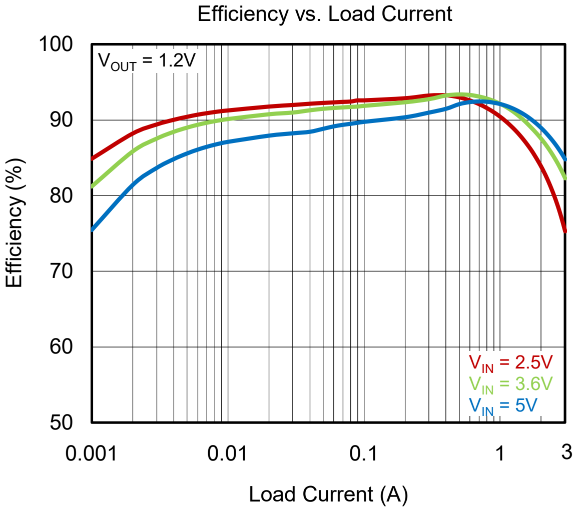


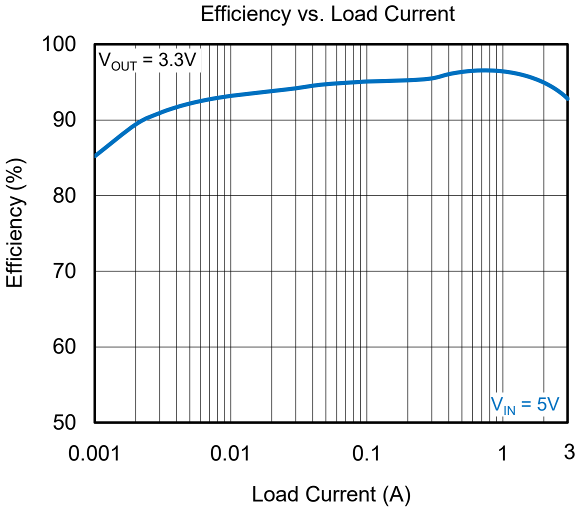
Output Discharge Current vs. Input Voltage

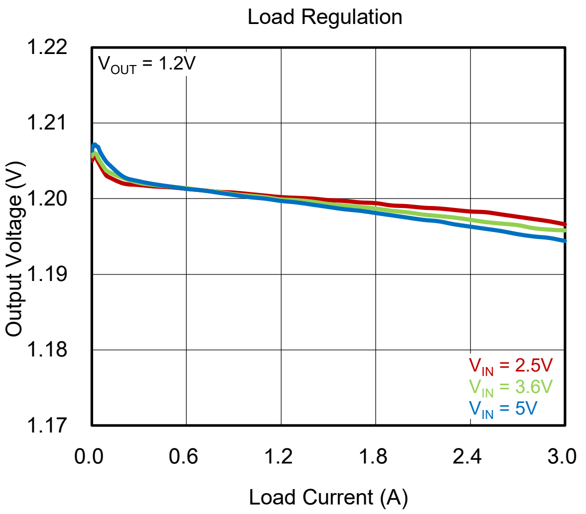


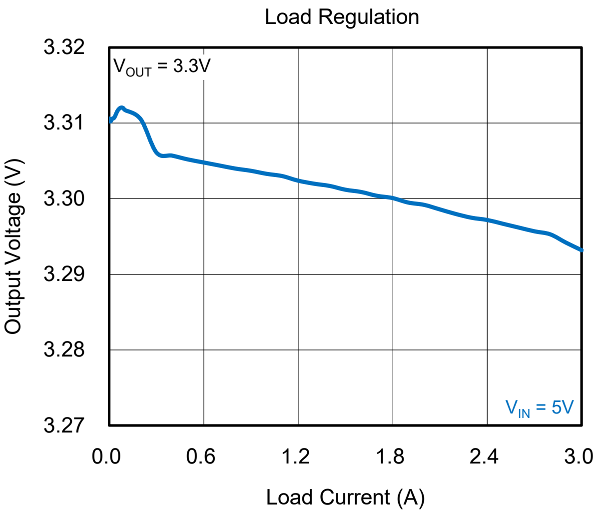
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

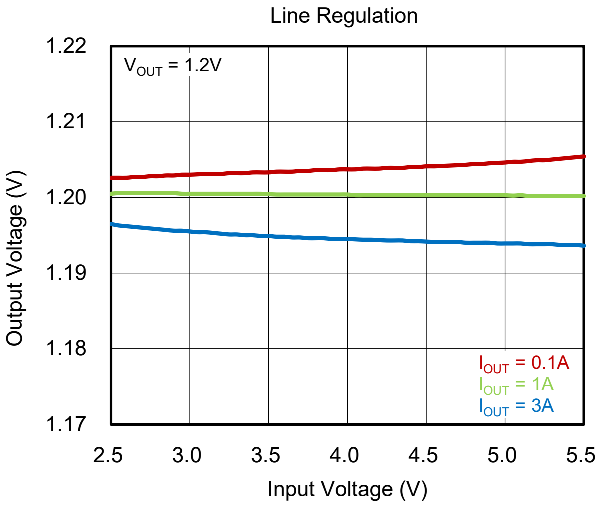
T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH, C_{OUT} = 2 × 22μF and C_3 = 150pF, unless otherwise noted.

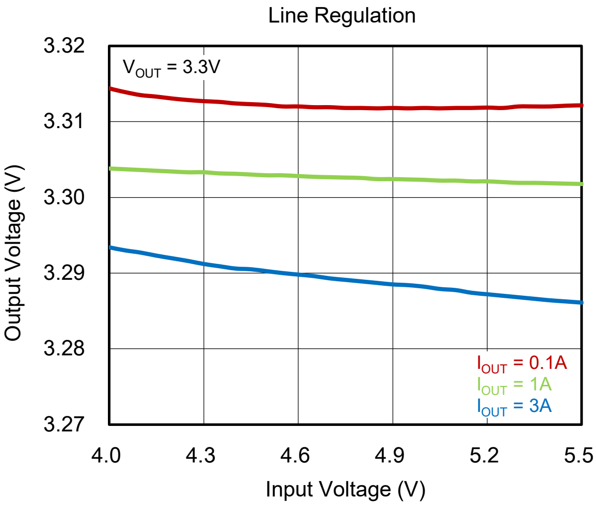








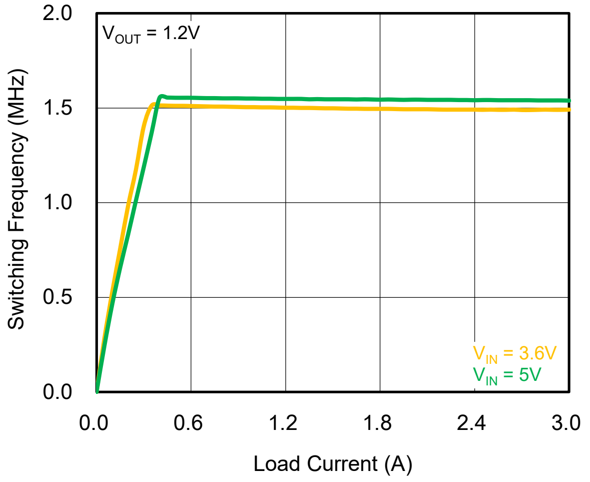




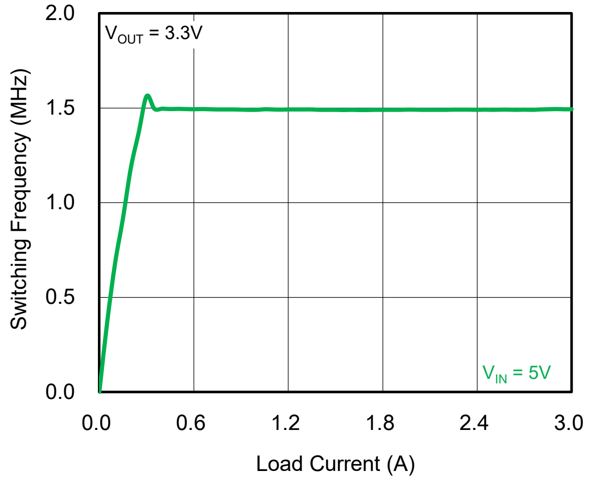
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH, C_{OUT} = 2 × 22μF and C_3 = 150pF, unless otherwise noted.

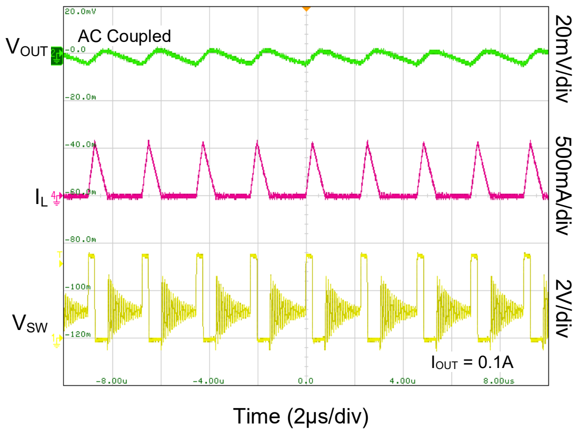
Switching Frequency vs. Load Current



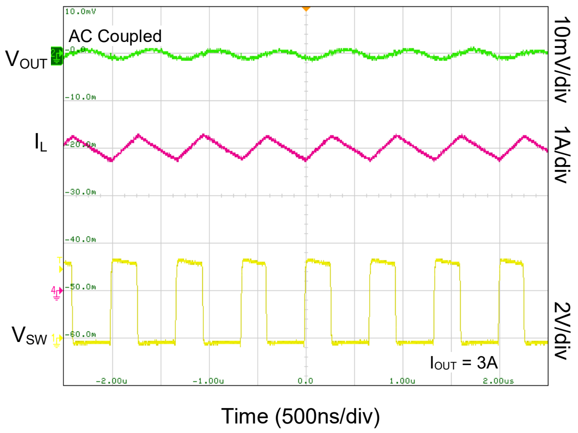
Switching Frequency vs. Load Current



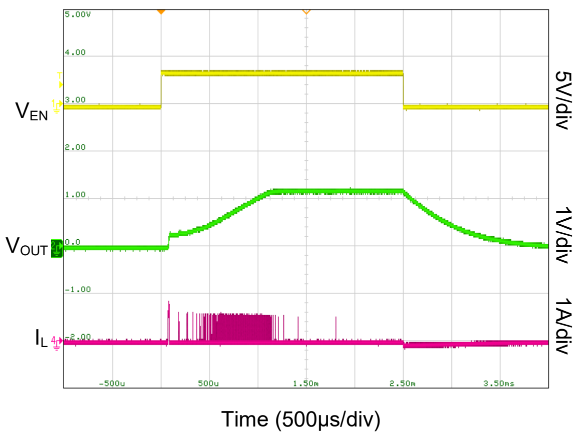
Power-Save Mode Operation (V_{OUT} = 1.2V)



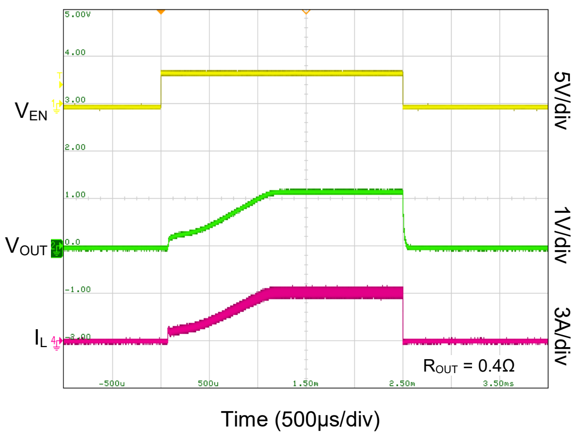
PWM Operation (V_{OUT} = 1.2V)



Startup and Shutdown without Load (V_{OUT} = 1.2V)



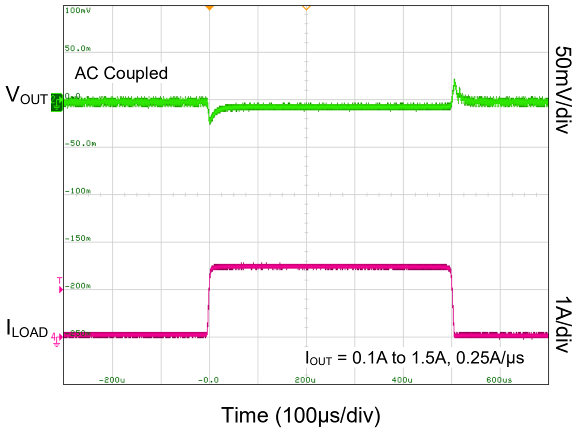
Startup and Shutdown with Load (V_{OUT} = 1.2V)



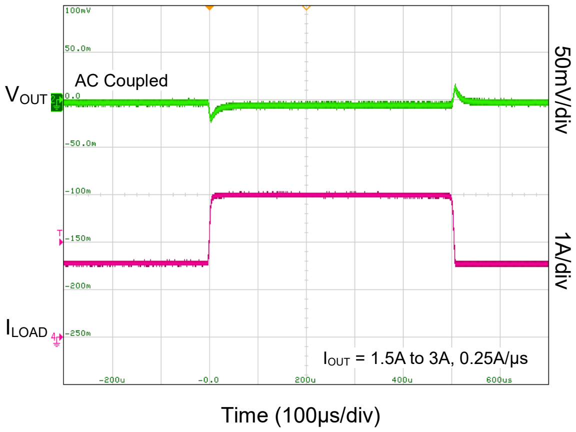
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 3.6V, V_{OUT} = 1.2V, L_1 = 1μH, C_{OUT} = 2 × 22μF and C_3 = 150pF, unless otherwise noted.

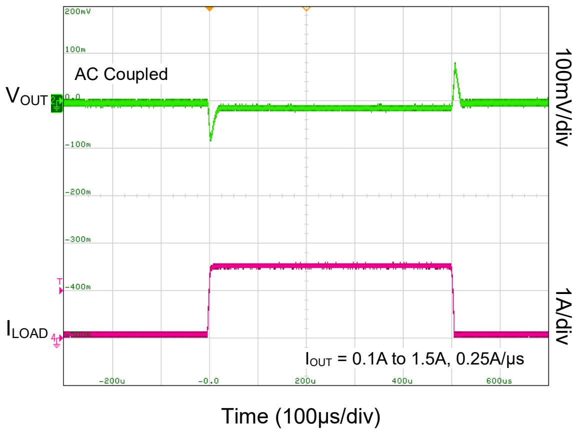
Load Transient (V_{OUT} = 1.2V)



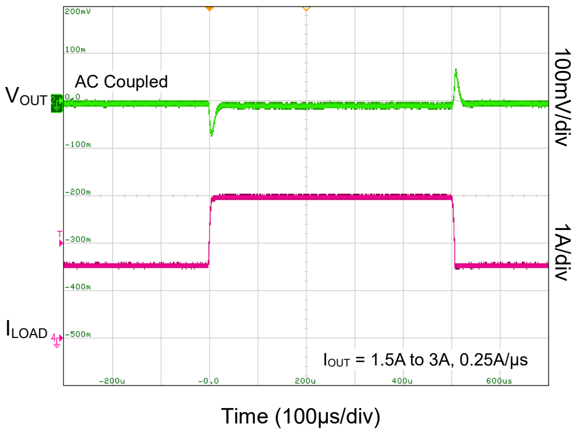
Load Transient (V_{OUT} = 1.2V)



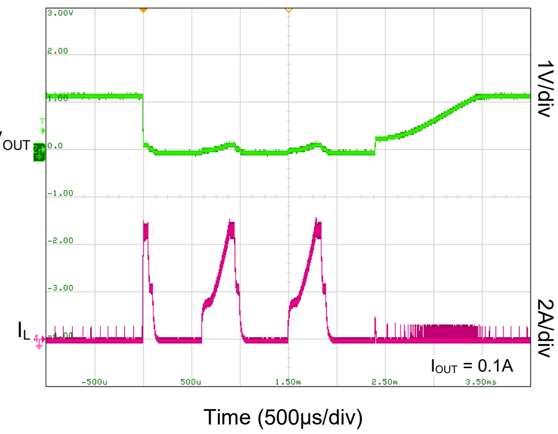
Load Transient (V_{IN} = 5V, V_{OUT} = 3.3V)



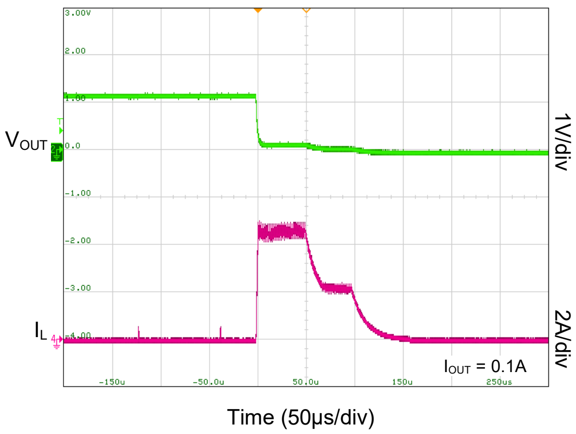
Load Transient (V_{IN} = 5V, V_{OUT} = 3.3V)



Output Short Protection (Hiccup, V_{OUT} = 1.2V)



Output Short Protection (Hiccup) - Zoom In (V_{OUT} = 1.2V)



FUNCTIONAL BLOCK DIAGRAM

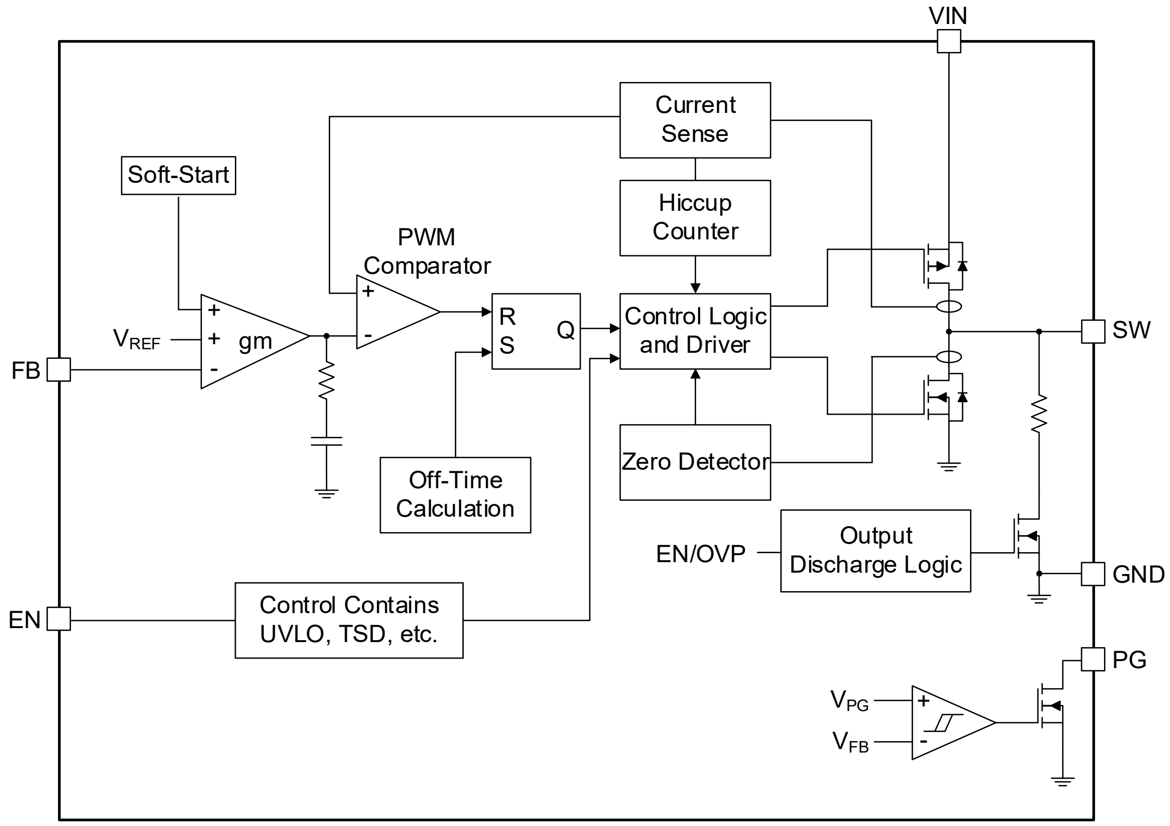


Figure 2. SGM61032SD Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61032SD is a high efficiency Buck switching converter optimized for handheld battery-powered applications. It operates at a quasi-fixed frequency of 1.5MHz and uses adaptive off-time PWM control for the moderate to heavy load range. This allows using a small inductor and small capacitors for compact designs.

At light load conditions, SGM61032SD operates in power-save mode to reduce the switching frequency and losses for longer battery life. The power-save mode quiescent current is 48μA (TYP).

Under-Voltage Lockout (UVLO)

Operating with insufficient supply voltage can cause device malfunction or failure. The UVLO protection shuts down the device if the input voltage is below the V_{UVLO} threshold. The V_{UVLO} hysteresis is 200mV. When the input voltage exceeds the rising UVLO threshold, the device restarts with a fresh soft startup sequence.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.32μA (TYP). During shutdown, an internal FET (16Ω typical on-resistance) is turned on and connects the SW pin to the GND for smooth discharge of the output. This discharge function is also activated when the shutdown is caused by UVLO (V_{IN} < 1.4V, uncertain), output OVP (V_{OVP_RISING} = 110% (TYP) × V_{REF}, $V_{OVP\_FALLING}$ = 105% (TYP) × V_{REF}) or short-circuit protection.

Power Good (PG)

PG is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail which is no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. PG remains low until V_{OUT} exceeds 95% of its nominal (set) value and goes low if V_{OUT} drops below 90% of its nominal value. Table 1 shows how the PG state is changed in different conditions. V_{PG} is the threshold of the PG hysteretic comparator. It has a 5% hysteresis band and goes high when V_{FB} rises above 95% of the V_{REF}.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing.

Table 1. PG Output State in Different Conditions

Reason	Condition(s)	PG State	
		High-Z	Low
Output Voltage	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO	1.4V < V_{IN} < V_{UVLO}		√
Power Supply Removal	V_{IN} ≤ 1.4V	Uncertain	

Soft-Start and Pre-biased Startup

When the device is enabled, the output voltage is ramped up towards its nominal value by an internal soft-start circuit with a rate determined by the startup time (t_{SS}). This circuit slowly ramps up the error amplifier reference voltage (V_{REF} = 0.6V) after exiting the shutdown state or under-voltage lockout (UVLO). The soft-start is critical to prevent excessive inrush currents and to avoid triggering of the output over-current protection to provide a smooth output rise. It also prevents extreme input voltage drops due to large inrush current over the high-impedance batteries and input sources that can interrupt the power-up.

The SGM61032SD is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turned on, a bias on the output can exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output cannot drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device cannot be able to start up properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

DETAILED DESCRIPTION (continued)

Power-Save Mode (PSM)

At light load conditions, the SGM61032SD shifts to the power-save mode to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output goes slightly higher than normal again and the switches are turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation with 100% Duty Cycle

When the input voltage gradually drops to the regulation output voltage, the SGM61032SD can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off. In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \tag{1}$$

where:

V_{IN_MIN} is minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is maximum output current.

R_{DSON} is high-side MOSFET on-resistance.

R_L is inductor DC resistance (DCR).

Switch Current Limits and Short-Circuit Protection (Hiccup)

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak.

If 32 cycles consecutive repetition of this event occurs, the current limit is half reduced for the next 32 cycles and then if the over-current continues, the device stops switching and turns the output discharge circuit on. A new startup is initiated automatically (hiccup) after 500μs (TYP). The hiccup repeats until the overload or short-circuit fault is cleared.

Thermal Protection and Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 25℃ below the T_{SD} limit.

APPLICATION INFORMATION

In this section, power supply design with the SGM61032SD synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

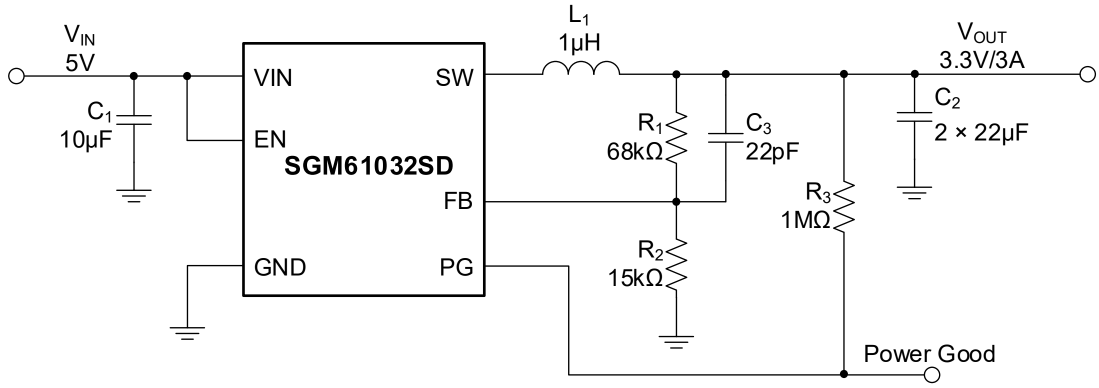


Figure 3. 3.3V Output Voltage Application

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	5V
Output Voltage	3.3V
Output Current	≤ 3A

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C_1	10μF, 10V, X5R, 0603	Standard
C_2, C_3	22μF, 10V, X5R, 0603	Standard
L_1	1μH, Wire Wound, DCR_{TYP} = 11.6mΩ, $I_{SAT(30\%)}$ = 12.5A, $I_{RMS(+40℃)}$ = 10.25A, SRF = 59MHz, 4mm × 4mm × 3mm, P/N: 74438357010	Würth
R_1	68kΩ, depending on the Output Voltage, 1%, size 0603	Standard
R_2	15kΩ, depending on the output voltage, 1%, size 0603	Standard
R_3	1MΩ, depending on the output voltage, 1%, size 0603	Standard

Input Capacitor Selection

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 10μF ceramic capacitor with X5R or better dielectric and 0603 or smaller size is sufficient in most cases. A larger value can be selected to reduce the input current ripple.

Inductor Selection

The inductor current ripple is determined by the inductance value (L). A lower inductance results in higher peak-to-peak current that increases the converter conduction losses. On the other hand, a large inductance results in slower transient response and larger size. I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough. Typically, the peak-to-peak inductor current is selected between 20% and 40% of the maximum output current. Equation 2 can be used to choose the inductance value based on ΔI_L.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \tag{2}$$

where:

I_{OUT_MAX} is the maximum output DC current.

ΔI_L is the inductor current ripple (peak-to-peak).

f_{SW} is switching frequency (MHz).

L is the inductance value (μH).

APPLICATION INFORMATION (continued)

Output Voltage Adjustment

Use Equation 3 for selecting the feedback resistors (R_1 and R_2) in Figure 3 to set the desired output voltage (V_{OUT}):

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

First choose R_2 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_2 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

LC Filter

The inductor (L) and the output capacitor (C) form a low-pass filter for removing switching AC components and passing the DC voltage to the output. Note that variations as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the C_{OUT}, due to tolerances and bias voltage derating the effective capacitance can vary by +20% to -50%.

A feed-forward capacitor improves transient response to the load steps and reduces the output ripple in PSM. A 22pF capacitor is recommended for the 3.3V output in the typical application.

Thermal Considerations

Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGM61032SD is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself has a significant role and to help transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

Layout Guidelines

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGM61032SD.

- Place the input/output capacitors and the inductor as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.
- Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.
- Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy conductors such as power traces and SW node to avoid magnetic and electric noise coupling.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

APPLICATION INFORMATION (continued)

Layout Example

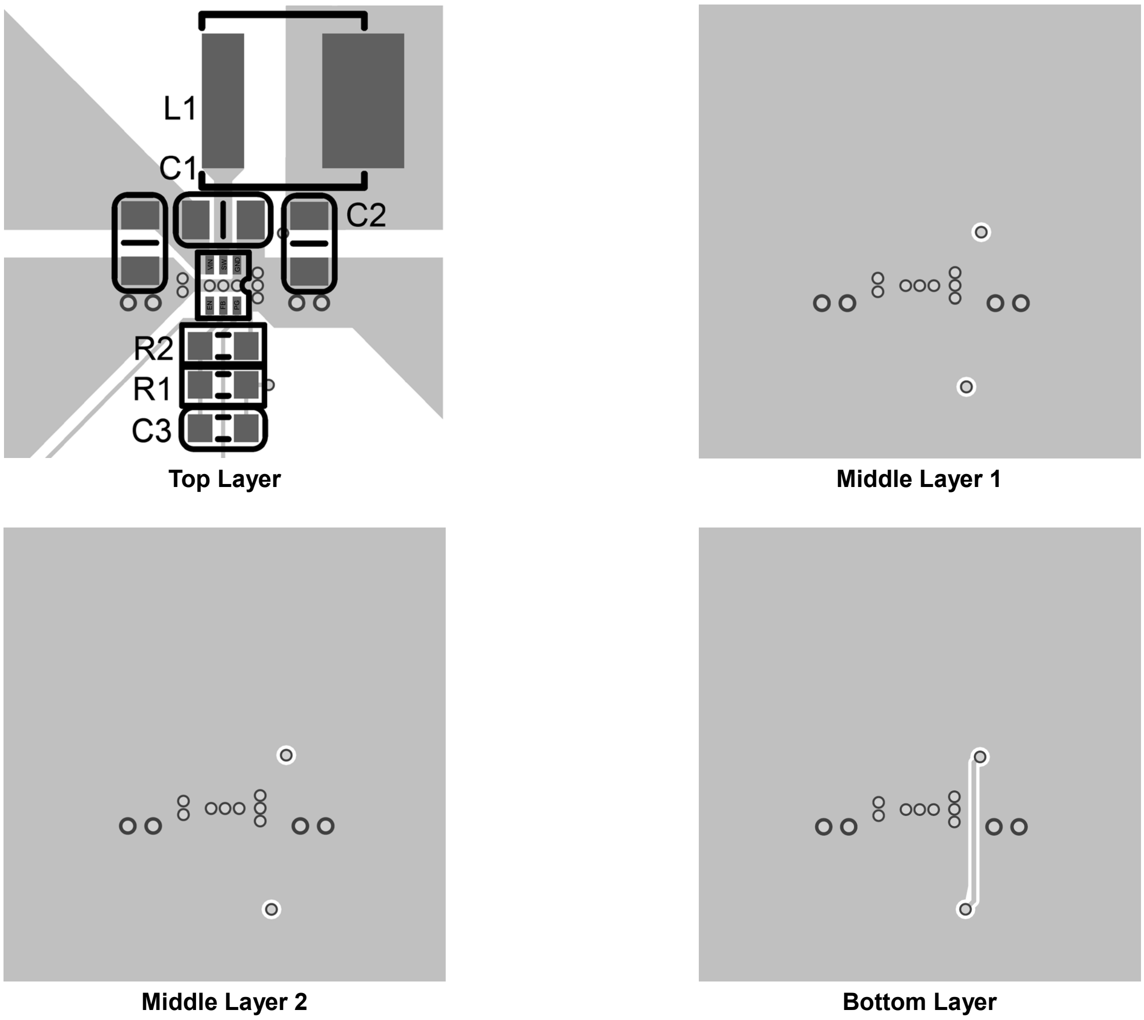


Figure 4. PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

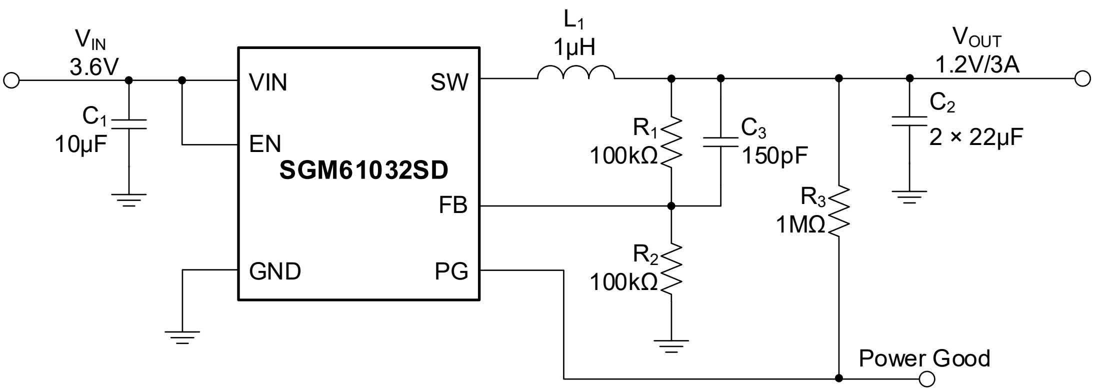


Figure 5. 1.2V Output Voltage Application of SGM61032SD

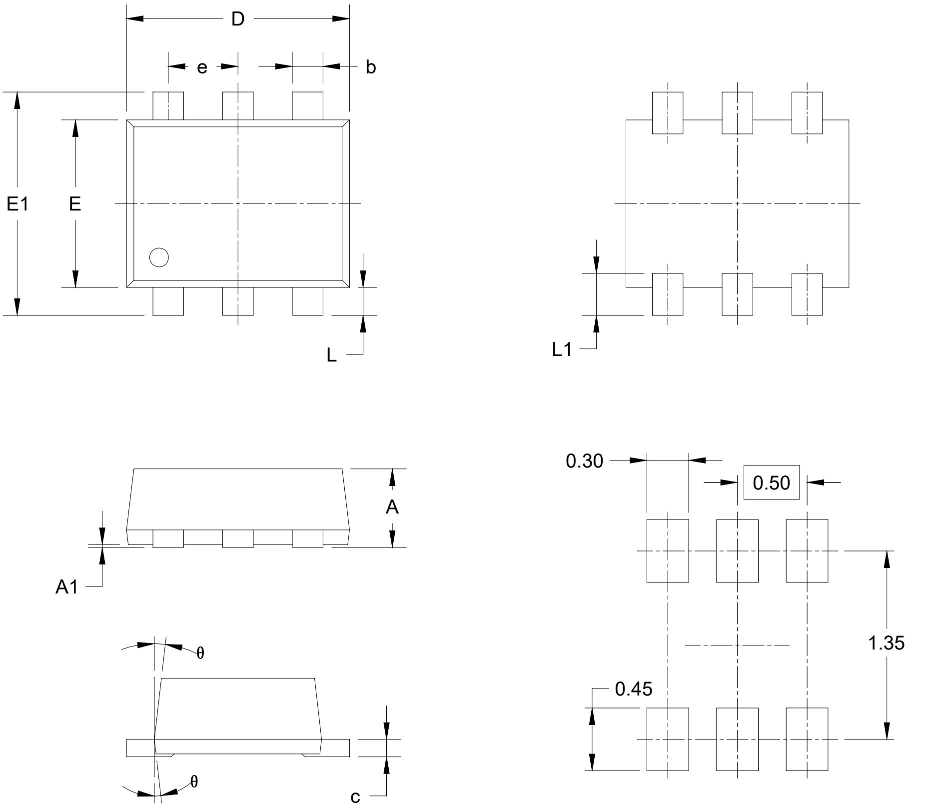
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MAY 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

SOT-563-6



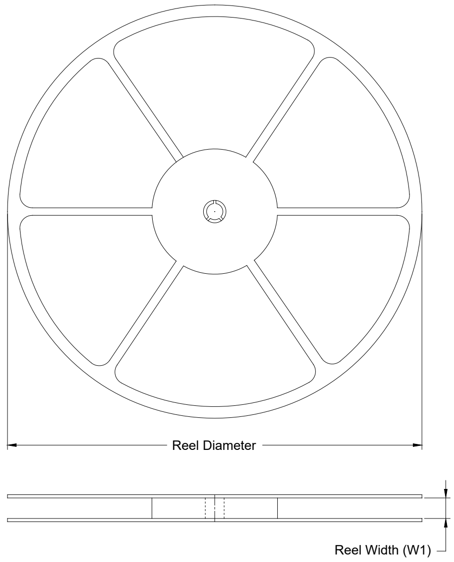
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

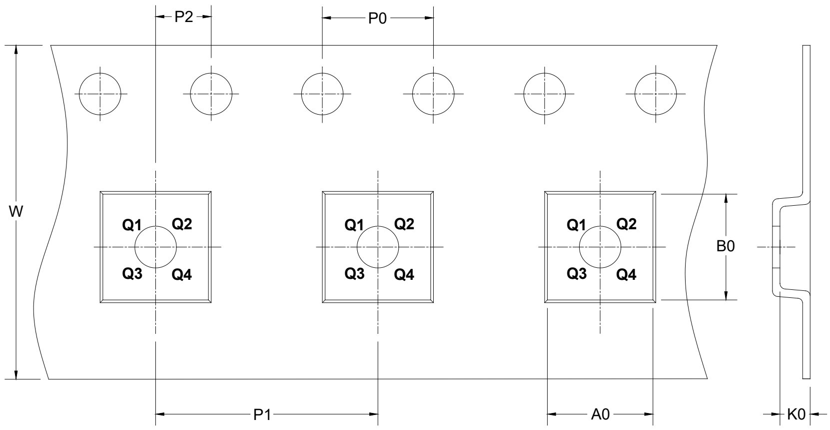
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



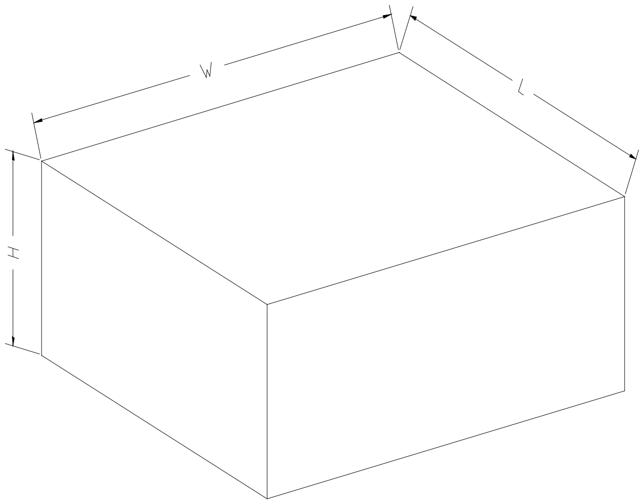
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-563-6	7″	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002