SGM61031S
3A High Efficiency Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61031SH and SGM61031SL are efficient high frequency synchronous Buck converter with an input voltage range of 2.5V to 5.5V and a wide output current range that is optimized for compact solutions. It operates in PWM mode at heavy loads and automatically enters power-save mode (PSM) at light loads to maintain its high efficiency.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

The SGM61031SH and SGM61031SL guarantee robustness by full protection function including input under-voltage lockout, cycle-by-cycle current limit and over-temperature protection. SGM61031SH integrates hiccup output under-voltage protection. SGM61031SL integrates latch-off output over-voltage protection and hiccup output under-voltage protection.

The SGM61031SH and SGM61031SL are available in a Green TDFN-2×2-8AL package.

FEATURES

- **AHP-COT Architecture for Fast Transient Regulation**
- **2.5V to 5.5V Input Voltage Range**
- **3A Output Current**
- **24μA Quiescent Current**
- **1MHz Switching Frequency**
- **0.8ms of Internal Soft-Start Time**
- **100% Duty Cycle for Low Dropout**
- **Power-Save Mode for Light Load Efficiency**
- **Power Good Output**
- **Output Discharge Function**
- **Protection for Output Under-Voltage and Over-Voltage:**
  - **SGM61031SH: Hiccup Protection, UVP**
  - **SGM61031SL: Latch-Off Protection, UVP/OVP**
- **Over-Temperature Protection**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

Battery-Powered Applications
Portable Electronic Devices
Personal Computer, Notebook
Data Storage

TYPICAL APPLICATION

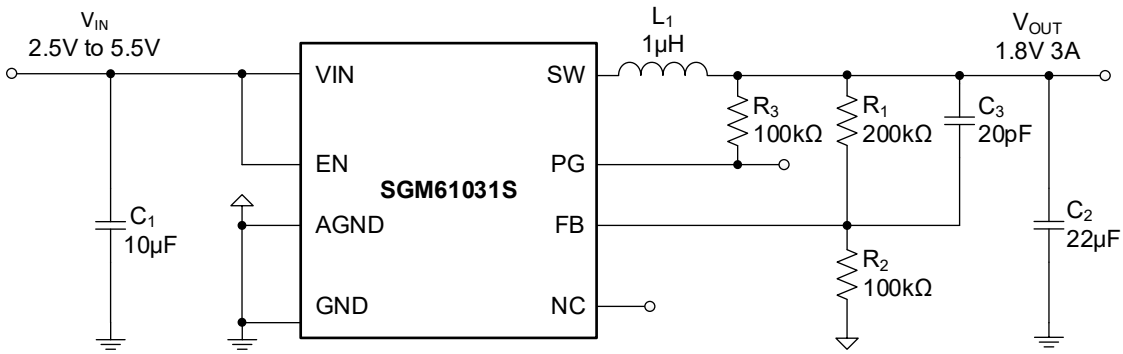


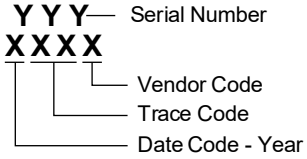
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61031SH	TDFN-2×2-8AL	-40℃ to +125℃	SGM61031SHXTDE8G/TR	1F4 XXXX	Tape and Reel, 3000
SGM61031SL	TDFN-2×2-8AL	-40℃ to +125℃	SGM61031SLXTDE8G/TR	1F5 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 6V
SW, EN, FB, PG Voltages ..... -0.3V to V_{IN} + 0.3V
SW (AC, Less than 10ns) Voltage ..... -3V to 10V
Power Good Sink Current 1mA
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... 57.3℃/W
TDFN-2×2-8AL, θ_{JB} ..... 22.5℃/W
TDFN-2×2-8AL, $\theta_{JC\ (TOP)}$ ..... 75.7℃/W
TDFN-2×2-8AL, $\theta_{JC\ (BOT)}$ ..... 9.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.5V to 5.5V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

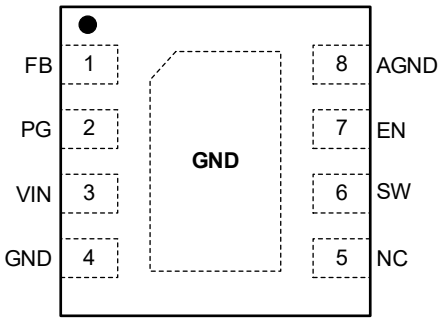
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
2	PG	O	Power Good Open-Drain Output. Connect an external pulled-up resistor to this pin. Leave this pin floating when not in use.
3	VIN	P	Power Supply Voltage Input.
4	GND	G	Power Ground.
5	NC	—	No Connection.
6	SW	P	Switching Node. Connect power inductor to this pin.
7	EN	I	Active-High Enable Input. Logic high sets the device active. Logic low disables it and turns it into shutdown mode. Do not leave this pin floating.
8	AGND	G	Analog Ground.
Exposed Pad	GND	—	Connect it to GND. The thermal pad must be soldered to improve heat dissipation.

NOTE: I = input, O = output, P = power, G = ground.

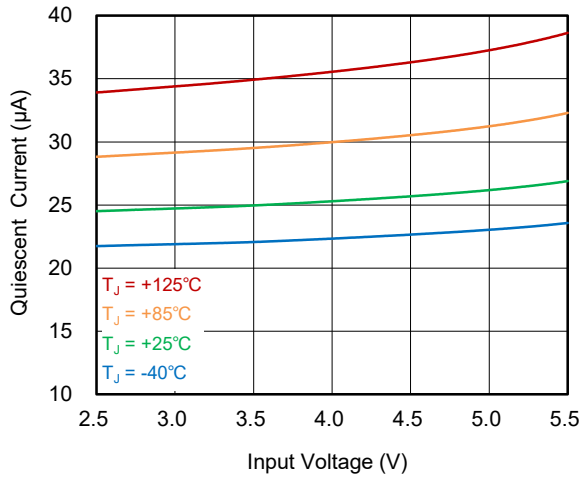
ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃. Typical values are at T_J = +25℃, unless otherwise noted.)

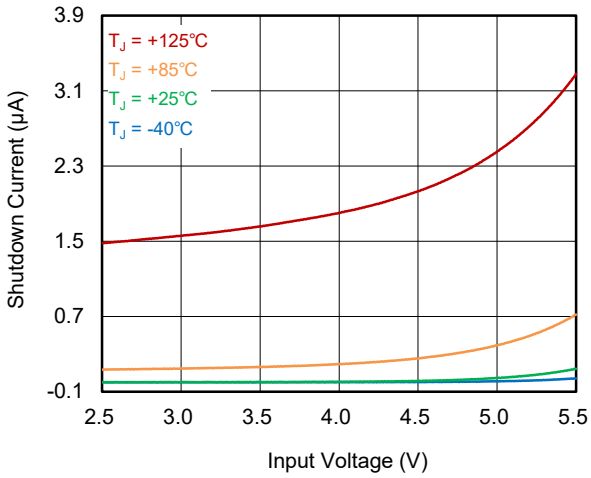
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Input Voltage Range	V_{IN}			2.5		5.5	V
Quiescent Current into VIN	I_Q	V_{IN} = 2.5V to 5.5V, I_{OUT} = 0mA, device not switching			24	48	μA
Shutdown Current into VIN	I_{SD}	V_{IN} = 2.5V to 5.5V, V_{EN} = 0V	T_J = +25℃		0.01	0.8	μA
			T_J = -40℃ to +125℃			4.7	
Under-Voltage Lockout	V_{UVLO}	Input voltage falling		2	2.1	2.2	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	Rising above V_{UVLO}			210		mV
Over-Temperature Protection(OTP)							
Thermal Shutdown	T_{SD}	Temperature rising			147		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}	Temperature falling below T_{SD}			27		℃
Logic Interface (EN)							
High-Level Input Voltage	V_{IH}	V_{IN} = 2.5V to 5.5V		1.2			V
Low-Level Input Voltage	V_{IL}	V_{IN} = 2.5V to 5.5V				0.4	V
Input Leakage Current	I_{LKG}				0.01	0.3	μA
Power Good							
Power Good Threshold	V_{PG_UV}	V_{FB} falling, V_{FB} referenced to V_{REF}		85	90	95	%
		Power good hysteresis, V_{FB} referenced to V_{REF}			5		
PG Leakage Current	I_{PG_LKG}				0.01	0.3	μA
Output							
Internal Reference Voltage	V_{REF}	V_{IN} = 2.5V to 5.5V, PWM	T_J = +25℃	594	600	606	mV
				591	600	609	
Feedback Input Bias Current	I_{FB}	V_{FB} = 0.6V			1	20	nA
Output Discharge Resistor	R_{DIS}	EN = low, V_{OUT} = 1.8V			50		Ω
MOSFETs							
High-side FET On-Resistance	R_{DSON_H}	I_{SW} = 500mA			78		mΩ
Low-side FET On-Resistance	R_{DSON_L}	I_{SW} = 500mA			54		mΩ
High-side FET Switch Current Limit	I_{LIM_H}	Rising inductor current		3.8	5	6.1	A
Protections							
Under-Voltage Protection	V_{UVP}	V_{FB} falling, V_{FB} referenced to V_{REF}			40		%
UVP Deglitch Time	t_{UVP_DLY}	V_{FB} < 40% V_{REF} to UVP trigger			10		us
Hiccup Time	t_{HICCUP}	SGM61031SH, SW pulses stop to a new startup			4		ms
Over-Voltage Protection	V_{OVP}	V_{FB} rising, V_{FB} referenced to V_{REF}			120		%
OVP Deglitch Time	t_{OVP_DLY}	V_{FB} > 120% V_{REF} to OVP trigger, SGM61031SL			10		μs
Time							
Soft-Start Time	t_{SS}	V_{OUT} from 0% to 95%			0.8		ms
ON Time	t_{ON}	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 1A, CCM		420	508	575	ns

TYPICAL PERFORMANCE CHARACTERISTICS

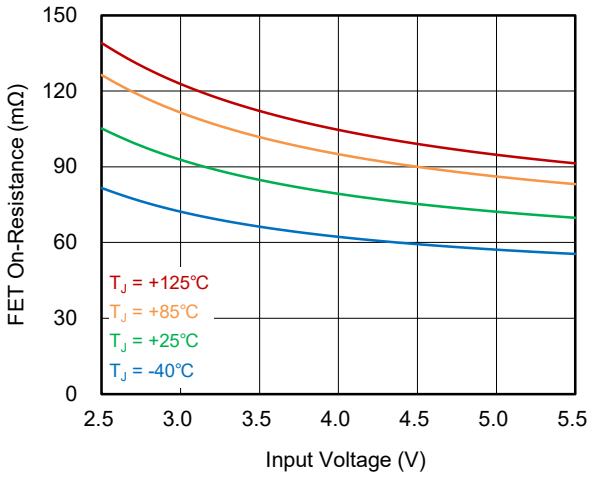
Quiescent Current vs. Input Voltage



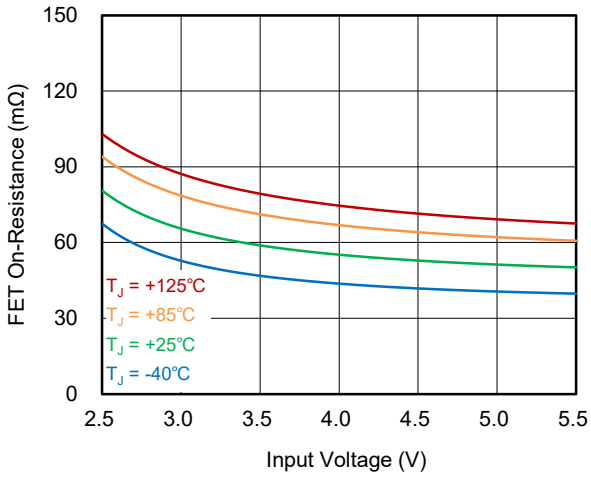
Shutdown Current vs. Input Voltage



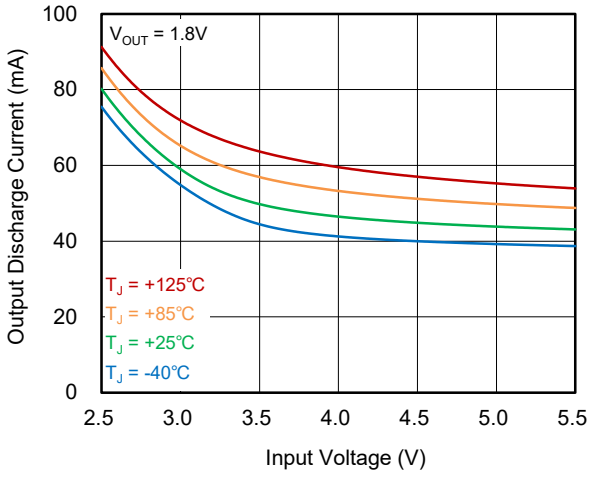
High-side FET R_{DS_ON} vs. Input Voltage



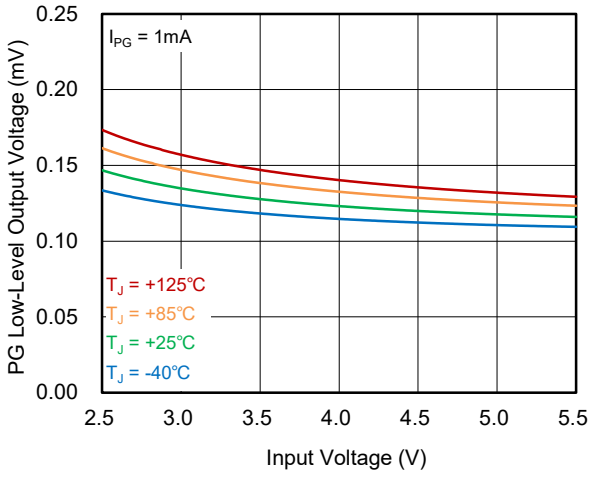
Low-side FET R_{DS_ON} vs. Input Voltage



Output Discharge Current vs. Input Voltage



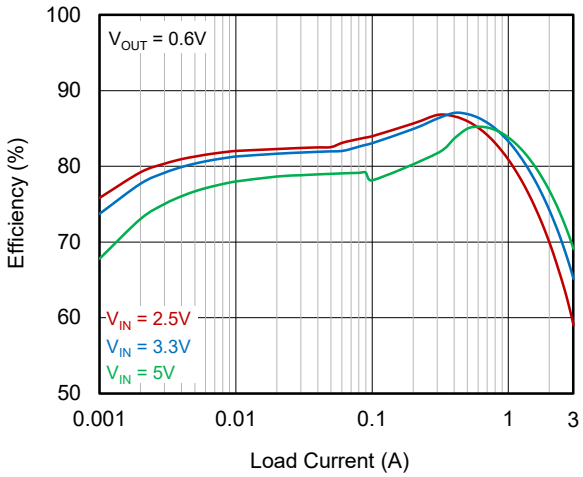
PG Low-Level Output Voltage vs. Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH (DCR = 13mΩ), C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

Efficiency vs. Load Current



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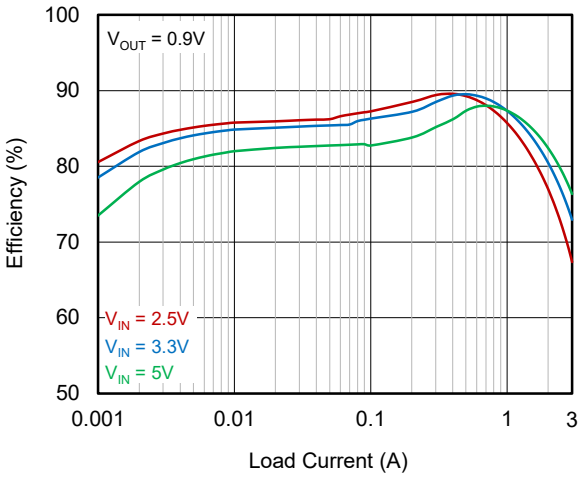

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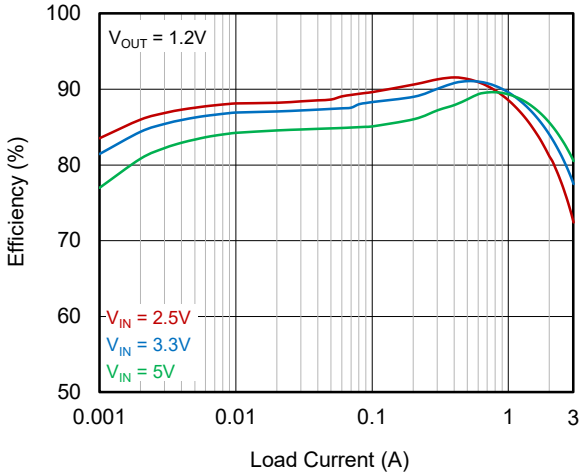

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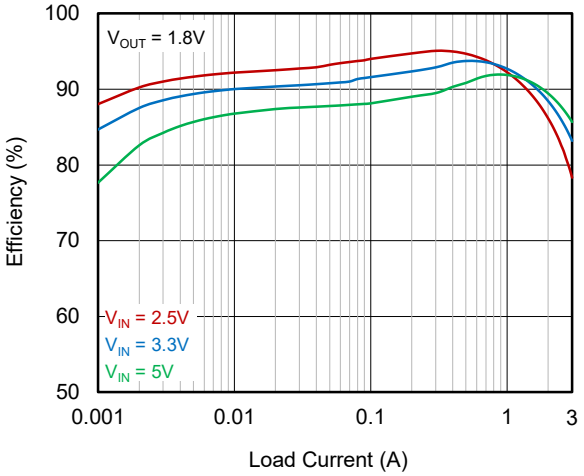

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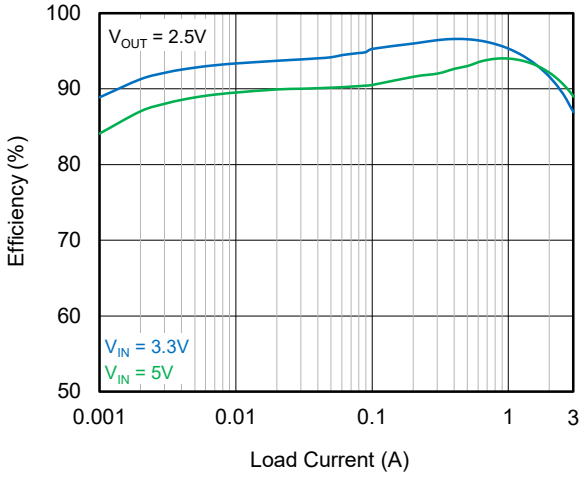

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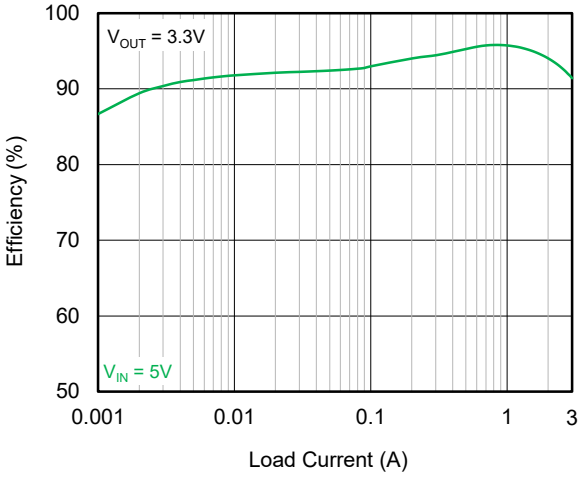
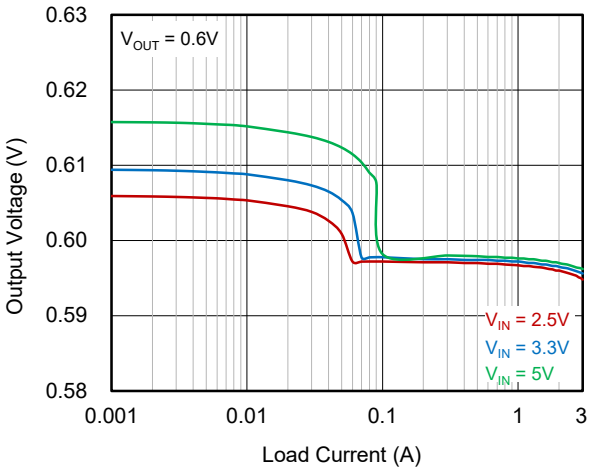


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH (DCR = 13mΩ), C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

Output Voltage vs. Load Current



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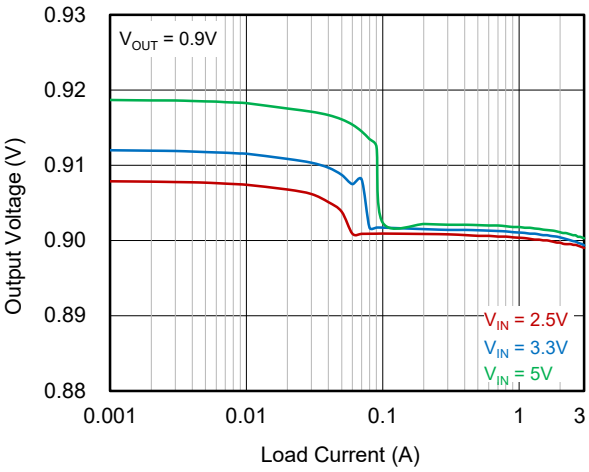

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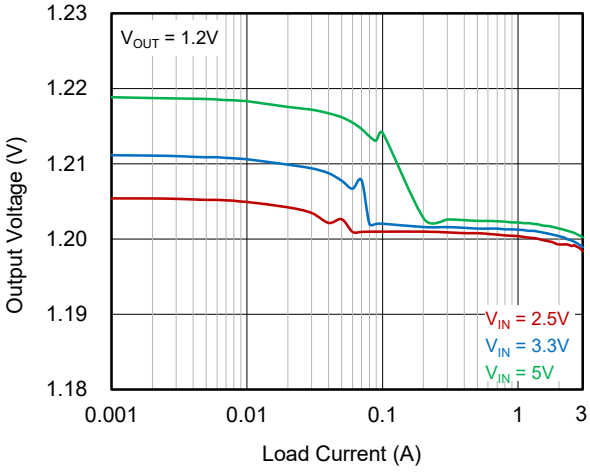

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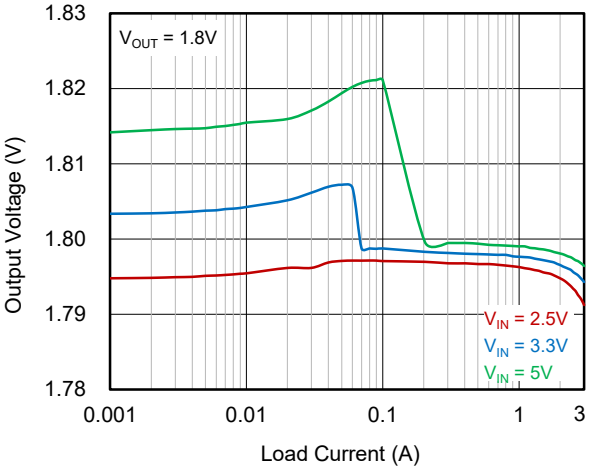

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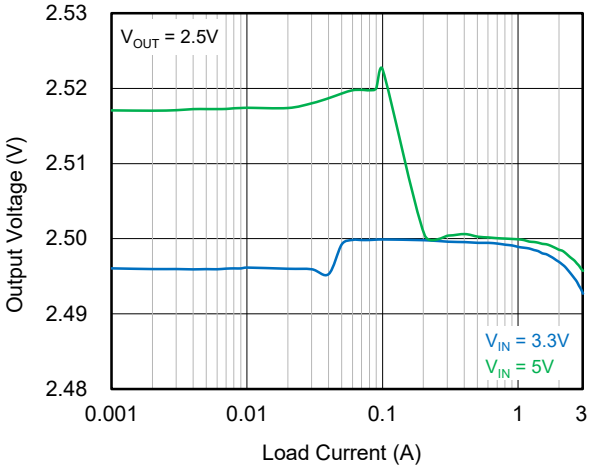

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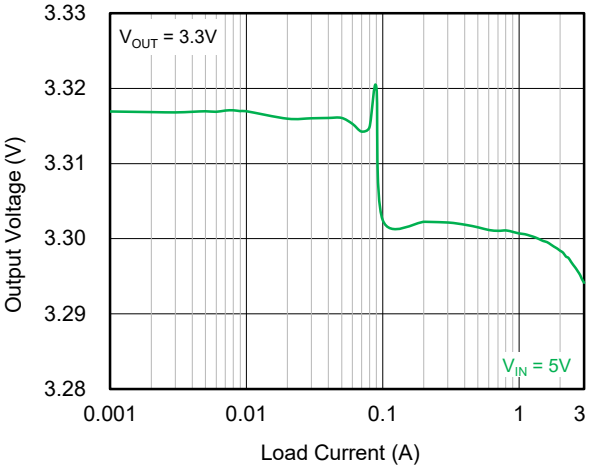
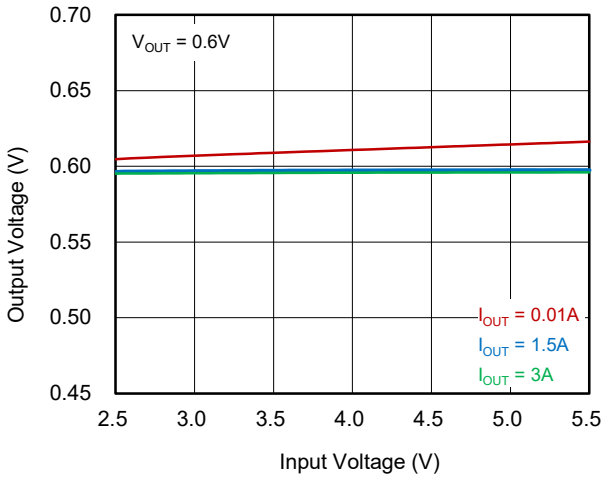


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH (DCR = 13mΩ), C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

Output Voltage vs. Input Voltage



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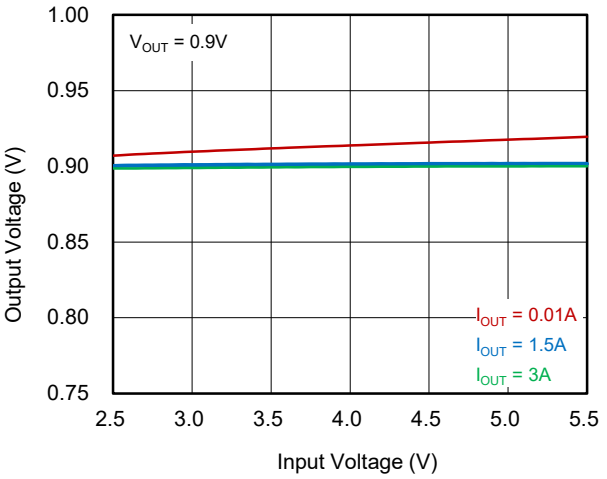

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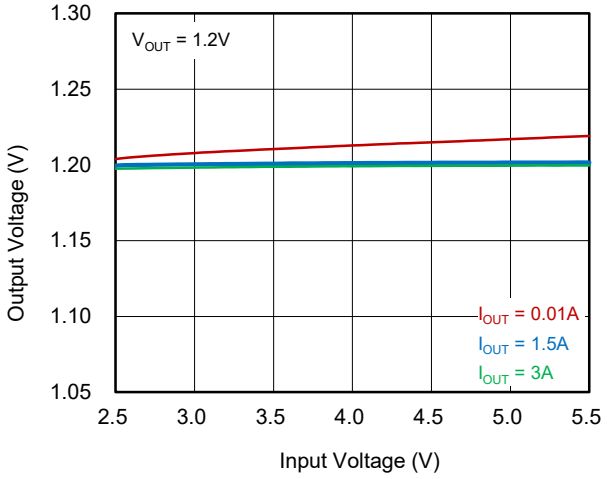

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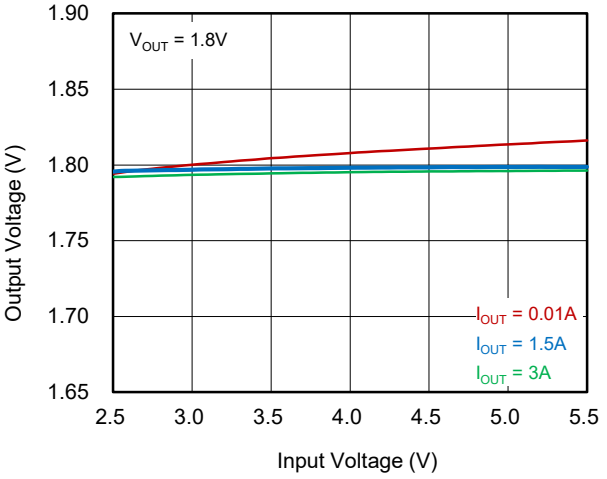
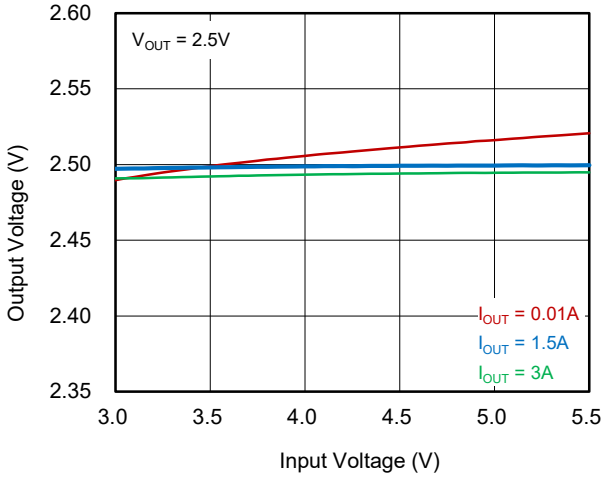


Output Voltage vs. Input Voltage



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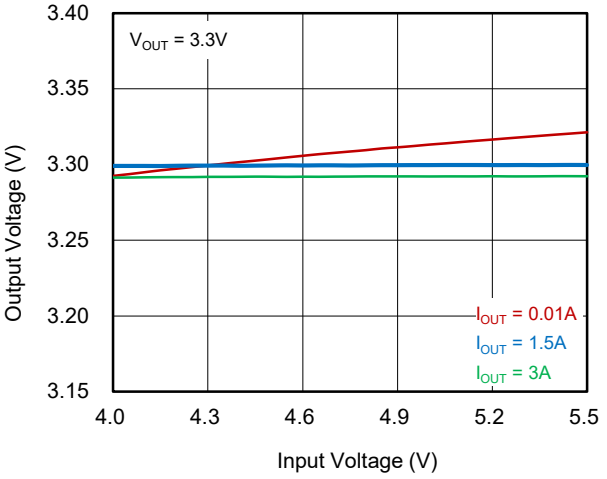
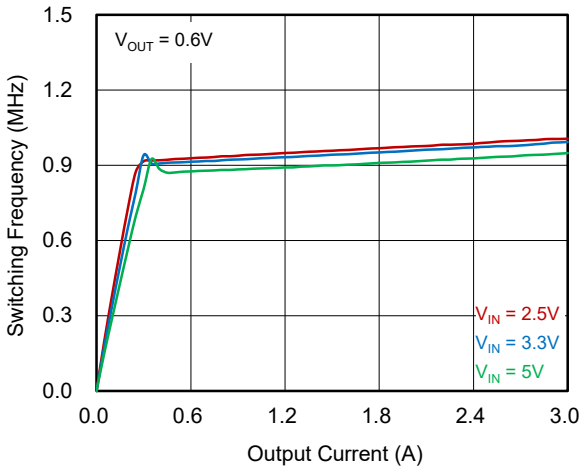


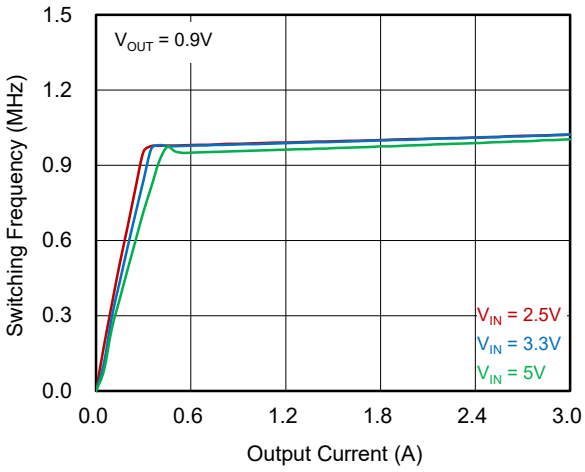
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH (DCR = 13mΩ), C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

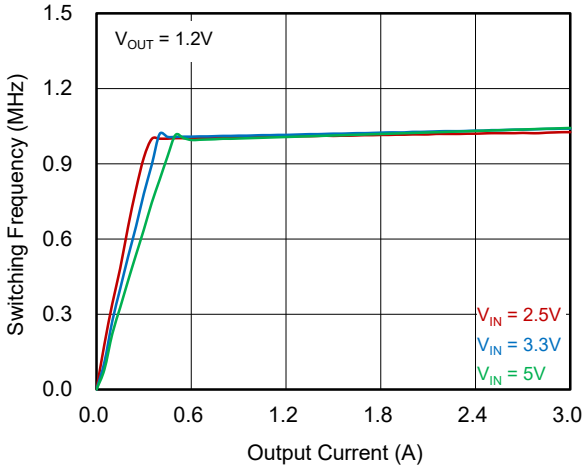
Switching Frequency vs. Output Current



Switching Frequency vs. Output Current



Switching Frequency vs. Output Current



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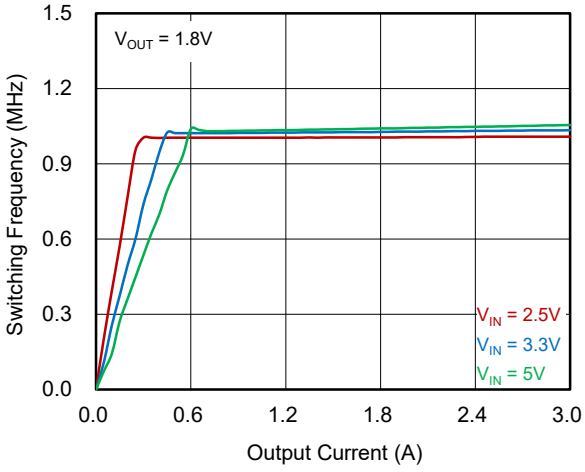
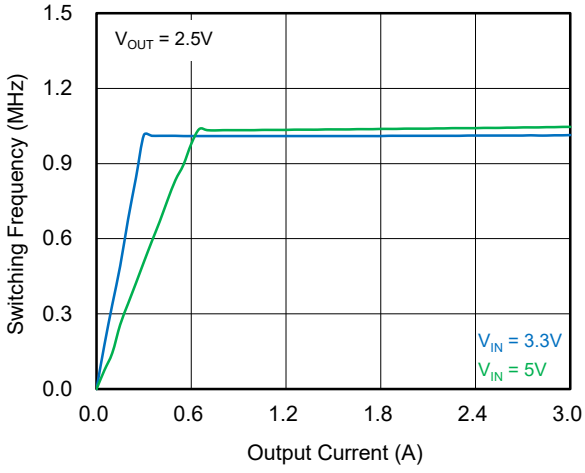
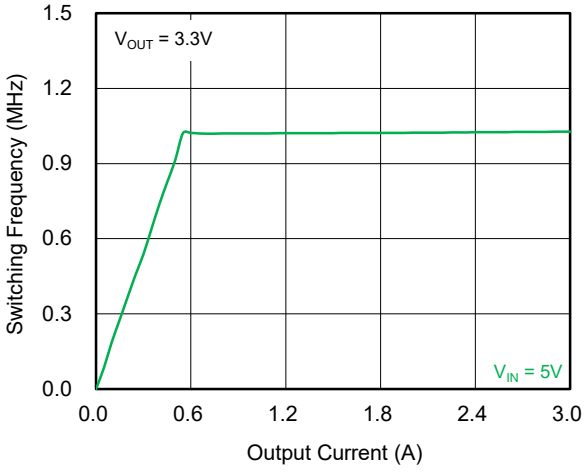


Switching Frequency vs. Output Current



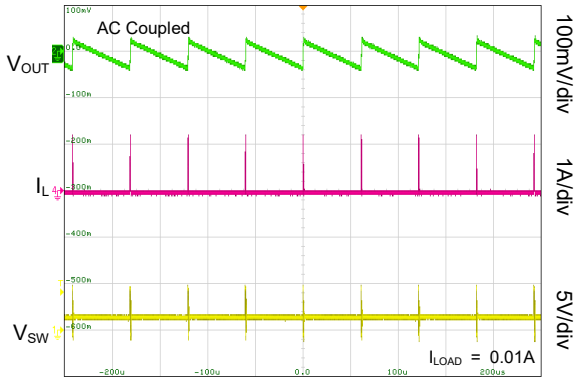
Switching Frequency vs. Output Current



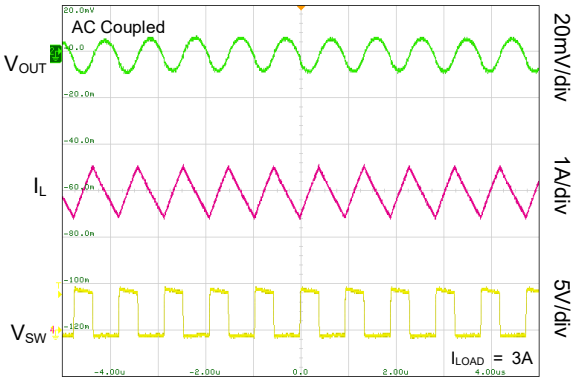
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH, C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

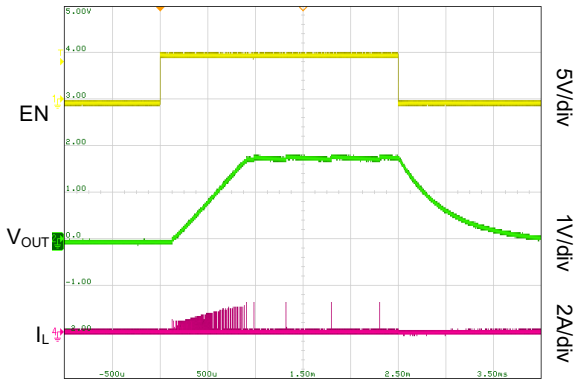
PSM Operation



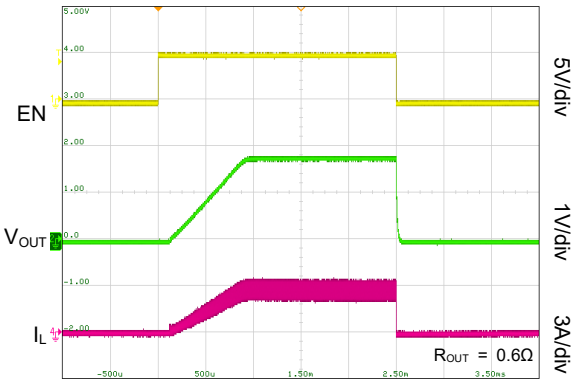
PWM Operation



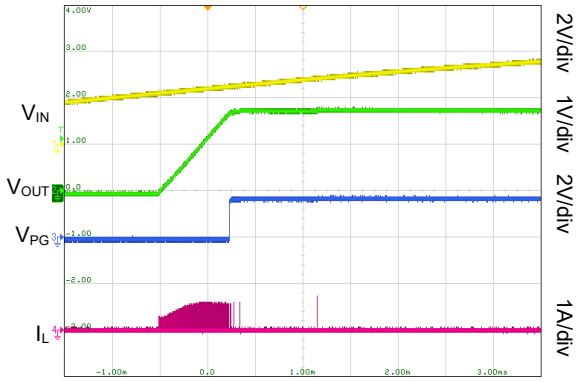
EN Startup and Shutdown without Load



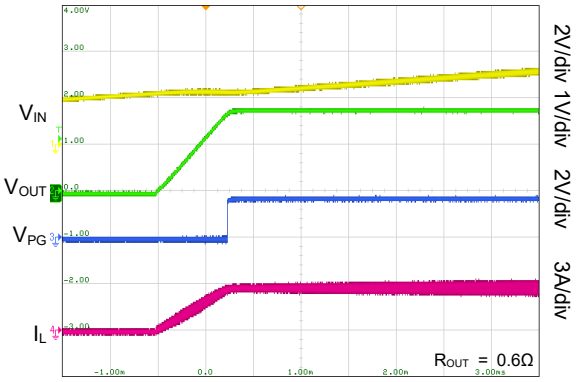
EN Startup and Shutdown with Load



VIN Startup without Load



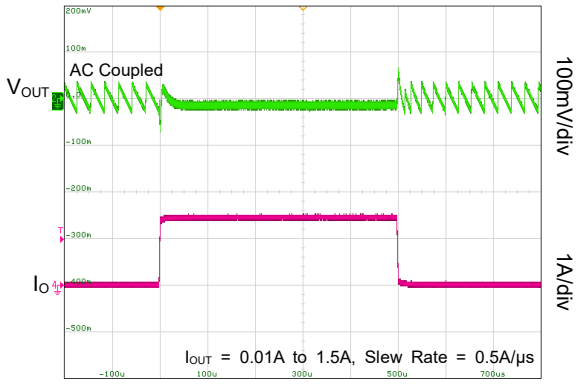
VIN Startup with Load



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

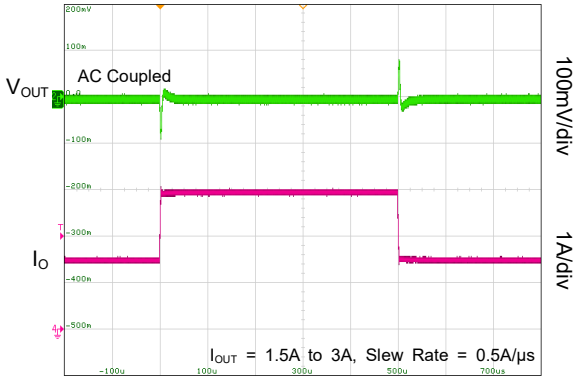
V_{IN} = 5V, V_{OUT} = 1.8V, L_1 = 1μH, C_{OUT} = 22μF and C_{FF} = 20pF, unless otherwise noted.

Load Transient



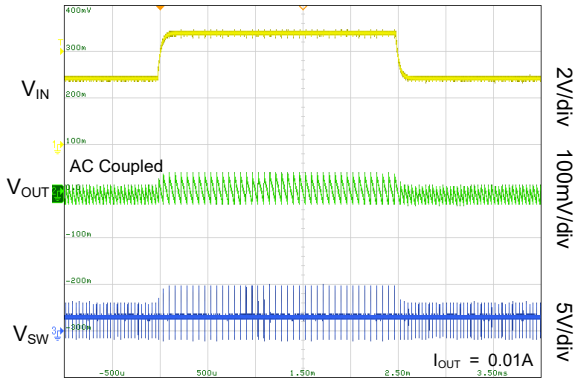
Time (100μs/div)

Load Transient



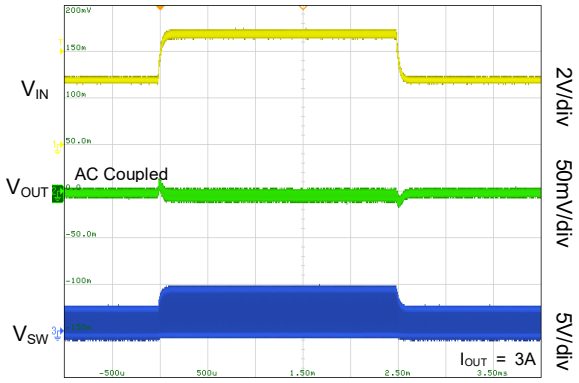
Time (100μs/div)

Line Transient



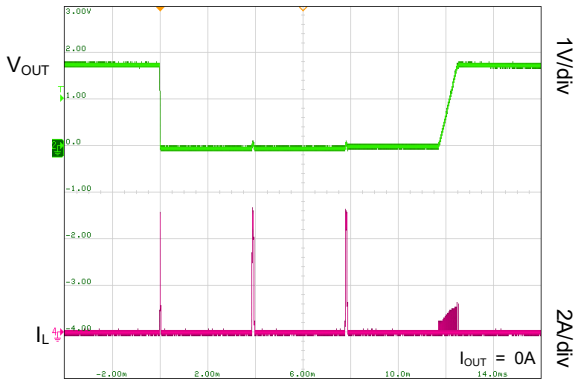
Time (500μs/div)

Line Transient



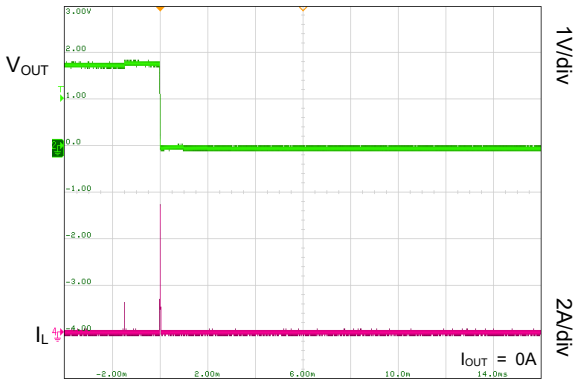
Time (500μs/div)

Output Short Protection and Recover (SGM61031SH)



Time (2ms/div)

Output Short and Protection (SGM61031SL)



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

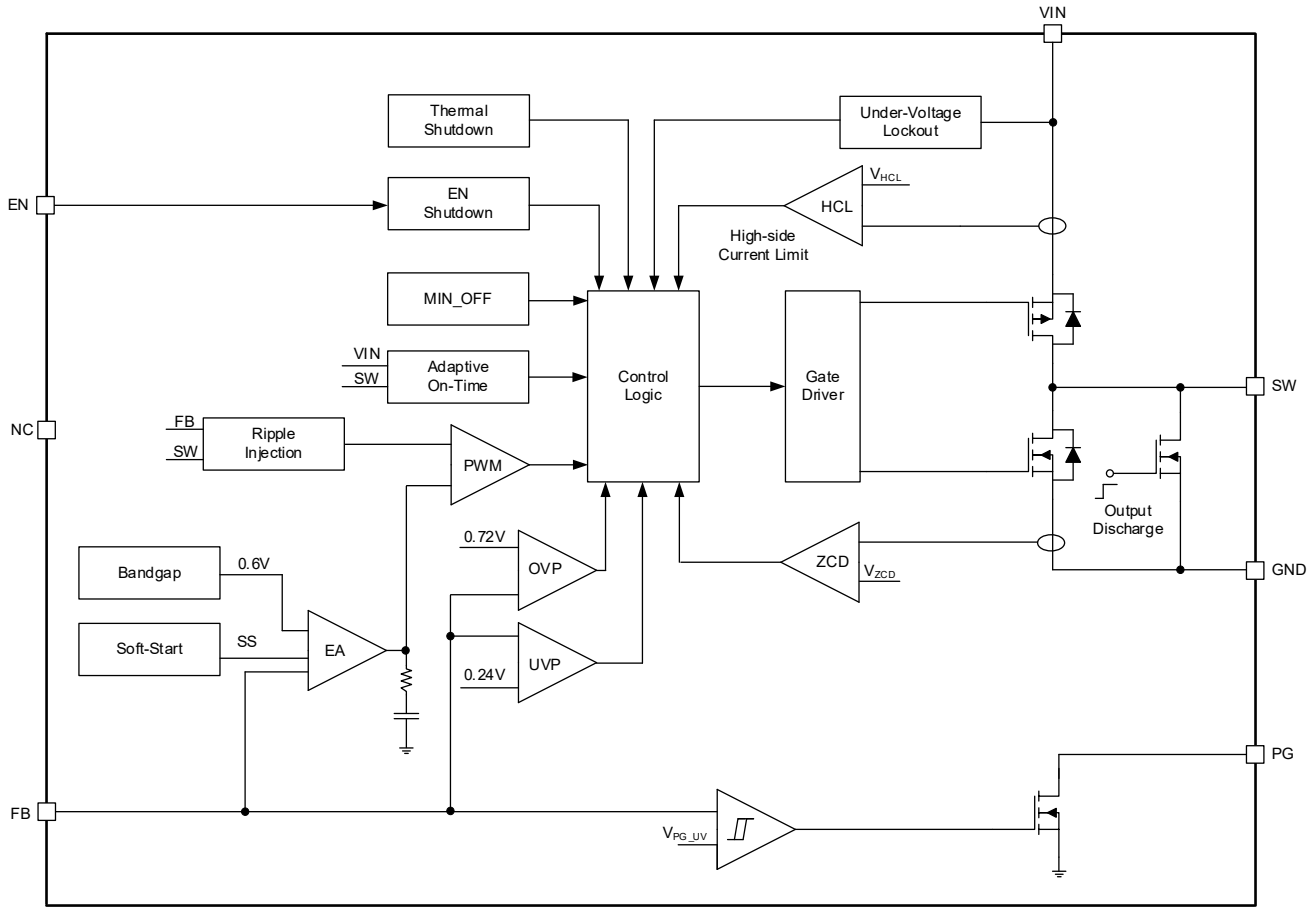


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61031S is a high-efficient Buck converter with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light loads, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 1MHz. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 210mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Device Enable and Disable

A logic high input to EN pin activates the device, and a logic low disables the device. Do not leave it floating.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout (V_{IN} < 1.4V, uncertain), the output is discharged by the SW pin through a typical discharge resistor of R_{DIS}.

Soft-Start

When EN pin is set to logic high and after about 150μs delay, the device starts switching and V_{OUT} increases with 0.8ms (TYP) internal soft-start circuit.

Power Good (PG)

The power good output of SGM61031S will be low in the condition that the output voltage is less than its nominal value. If the output exceeds 95% of the regulated voltage, the power good is in high-impedance state. If the output voltage is less than 90% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum of 1mA sink current. A pull-up resistor connecting to power good output is required. When the device is disabled, under-voltage lockout, or thermal shutdown, the PG pin is driven to Low (see Table 1). The PG signal connected to the EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		PG Logic Status	
		Hi-Z	Low
Enable (EN = High)	$V_{FB} \geq V_{PG\_UV}$	√	
	$V_{FB} \leq V_{PG\_UV}$		√
Shutdown (EN = Low)			√
Thermal Shutdown	$T_J > T_{SD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4V$	Undefined	

Low Dropout Operation (100% Duty Cycle)

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Power-Save Mode

Once the load current decreases, the SGM61031S will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous.

Over-Current Protection

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM_H} threshold, HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak.

For SGM61031SH, if 32 cycles consecutive repetition of this event occurs, the device stops switching and hiccup. A new startup is initiated automatically (hiccup) after 4ms (TYP). The hiccup repeats until the current-limit condition is removed.

DETAILED DESCRIPTION (continued)

Hiccup Short-Circuit Protection (SGM61031SH Only)

If overload or output short-circuits condition continues and output voltage drops below 40% of the set voltage, the device stops switching, after a hiccup time (4ms, TYP), a new startup is initialed automatically. The hiccup repeats until the overload or short-circuit fault is cleared.

Latch-off Output Under-Voltage and Over-Voltage Protection (SGM61031SL Only)

SGM61031SL includes output over-voltage protection and output under-voltage protection circuits to limit output voltage. If the V_{FB} goes above the 120% or below 40% of the reference voltage, the high-side MOSFET will be forced off to limit the output voltage then the IC will be into latch-off mode. Repowering on VIN or re-enabling EN can make the device work again.

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{SD} (+147℃, TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

The SGM61031S is a synchronous Buck converter with output voltage adjusted by feedback dividers. Taking SGM61031S typical application as a reference, the following sections discuss the design of external components and the way to achieve the application.

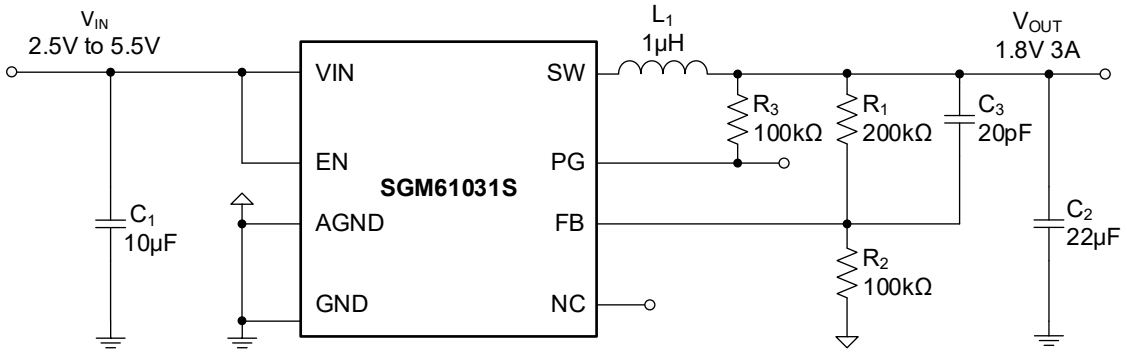


Figure 3. Typical Application Schematic

Design Requirements

For this design example, use Table 2 as the input parameters.

Table 2. Design Parameters

Design Parameters	Example Values
Input Voltage Range	2.5V to 5.5V
Output Voltage	1.8V
Output Current Rating	3A
Operating Frequency	1MHz

Design Details

Table 3 shows the components included in this example.

Table 3. Components List

Ref	Description	Manufacturer
C_1	10μF, Ceramic Capacitor, 10V, X7R, 0603, P/N: GRM188Z71A106KA73	muRata
C_2	22μF, Ceramic Capacitor, 10V, X5R, 0603, P/N: GRM188R61A226ME15	muRata
C_3	20pF, Ceramic Capacitor, 50V, C0G, Size 0603	Std
L_1	1μH Wire Wound, DCR_{TYP} = 12mΩ, $I_{SAT(30\%)}$ = 11.5A, $I_{RMS(+40℃)}$ = 10.1A,SRF = 55MHz, 4mm × 4mm × 2mm, P/N: 74438356010	Würth
R_1	200kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_2	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_3	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std

Capacitor Selection

For input capacitor design, a X5R/X7R dielectric ceramic capacitor should be selected for its low ESR and high frequency performance. 10μF is enough for most applications. The voltage rating of input capacitor must be considered for its significant bias effect. The input ripple voltage can be calculated from Equation 2.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (2)$$

The ripple current rating of input capacitor should be greater than I_{CIN_RMS} in Equation 3 and the maximum value occurs at 50% duty cycle.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN}-V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (3)$$

For output capacitor design, output ripple, transient response and loop stability should be considered. Minimum capacitance of output ripple criteria can be calculated from Equation 4.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (4)$$

Both the input and output capacitors should be placed as close to VIN, SENSE and GND pins as possible to reduce noise caused by PCB parasitic parameters.

APPLICATION INFORMATION (continued)

Inductor Selection

Equation 5 is conventionally used to calculate the output inductance of a Buck converter. The inductor should be selected by its value and the saturation current. The saturation current of inductor should be higher than I_{L_MAX} in Equation 5, and sufficient margin should be reserved. Generally, the saturation current above high-side current limit is enough, and a 20% to 40% ripple current is selected to calculate the inductance. Larger inductor can reduce the ripple current, but with an increasing response time.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (5)$$

where:

- I_{OUT_MAX} is the maximum output current.
- ΔI_L is the inductor current ripple.
- f_{SW} is the switching frequency.
- L is the inductor value.

LC Filter

The inductor (L) and the output capacitor (C) form a low-pass filter for removing switching AC components and passing the DC voltage to the output. Note that variations as high as +20% to -30% in the effective inductance due to tolerances. Similarly, for the C_{OUT}, due to tolerances and bias voltage de-rating the effective capacitance can vary by +20% to -50%.

A feed-forward capacitor improves transient response to the load steps and reduces the output ripple in PSM. A 20pF capacitor is recommended for the 1.8V output in the typical application.

Adjustable Output Voltage

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R_1 and R_2, the output voltage can be programmed to the desired value. Calculate R_1 and R_2 with Equation 6.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (6)$$

First choose R_2 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_2, otherwise, the loss will be increased on this resistor that reduces the light load efficiency.

LAYOUT GUIDELINES

Good PCB layout is the key factor for high performance operation of a device regarding the stability, regulation, efficiency and other performance measures.

A list of guidelines for designing the PCB layout of SGM61031S is provided below:

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device PGND pin to minimize the AC current loops.
- Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep signal traces such as FB and VOUT sensing lines away from SW or other noise sources. Both of them need to be connected to VOUT by the shortest path and near the output capacitor.
- Divider resistors are placed close to the IC and connect to the AGND and FB pins directly.
- AGND pin and PGND pin need to be connected through the exposed pad for single-point grounding. In order to ensure mechanical reliability and good heat dissipation, the exposed pad must be fully welded to the circuit board.
- Use GND planes in middle layers (if used) for shielding and minimizing the ground potential drifts.

Typical suggested layout is provided in Figure 4.

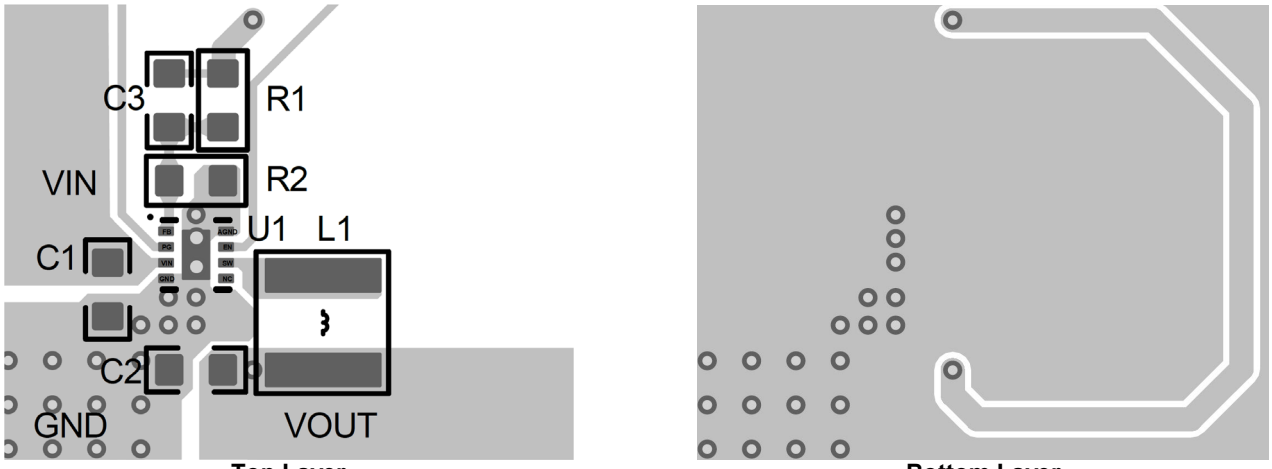


Figure 4. PCB Layout

ADDITIONAL TYPICAL APPLICATION CIRCUITS

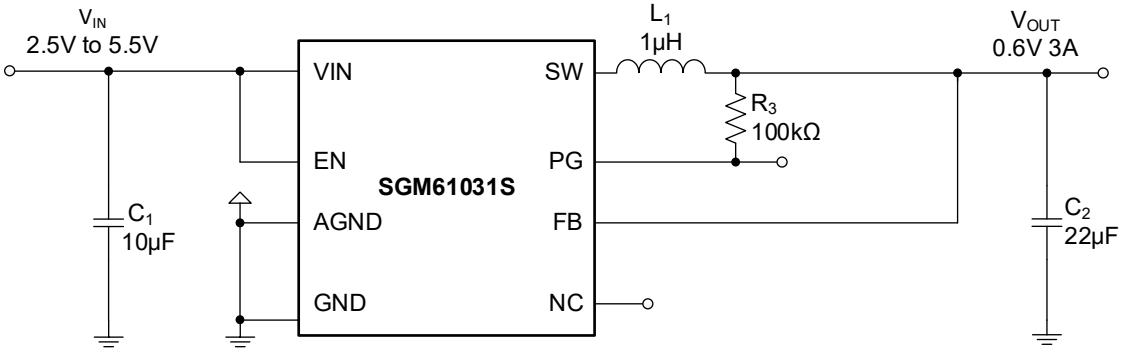


Figure 5. 0.6V Output Voltage Application

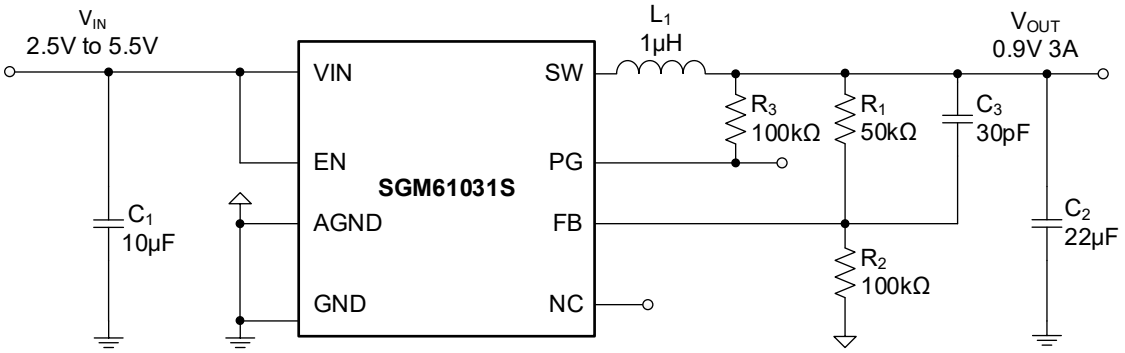


Figure 6. 0.9V Output Voltage Application

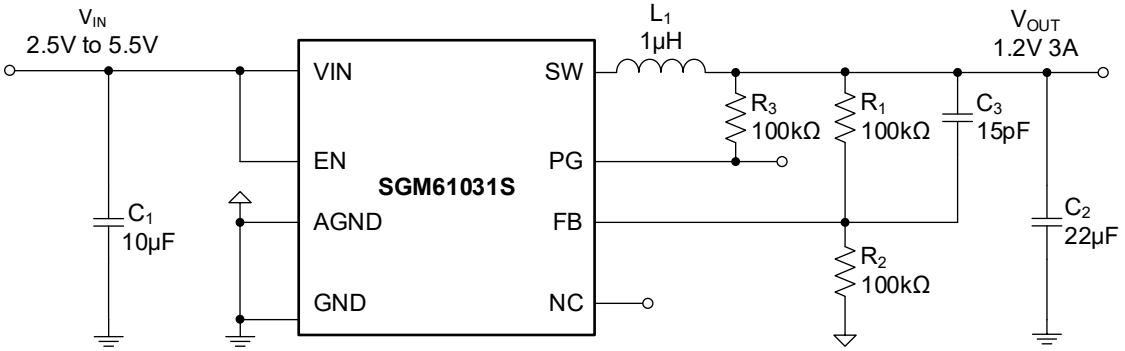


Figure 7. 1.2V Output Voltage Application

ADDITIONAL TYPICAL APPLICATION CIRCUITS (continued)

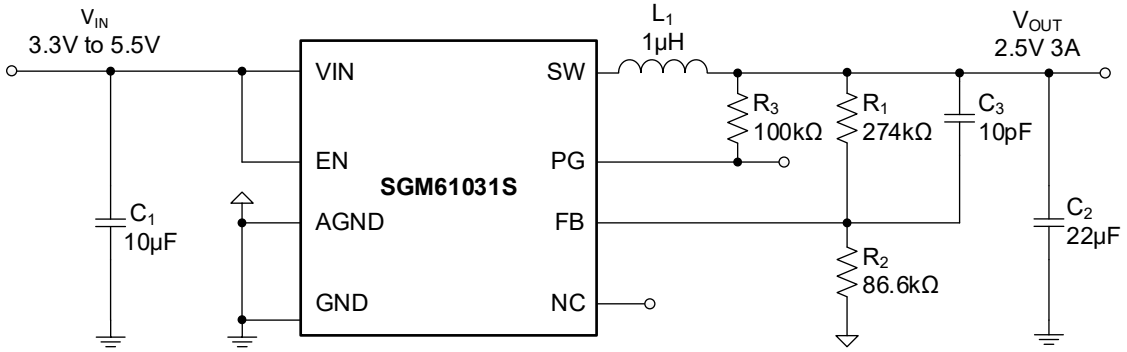


Figure 8. 2.5V Output Voltage Application

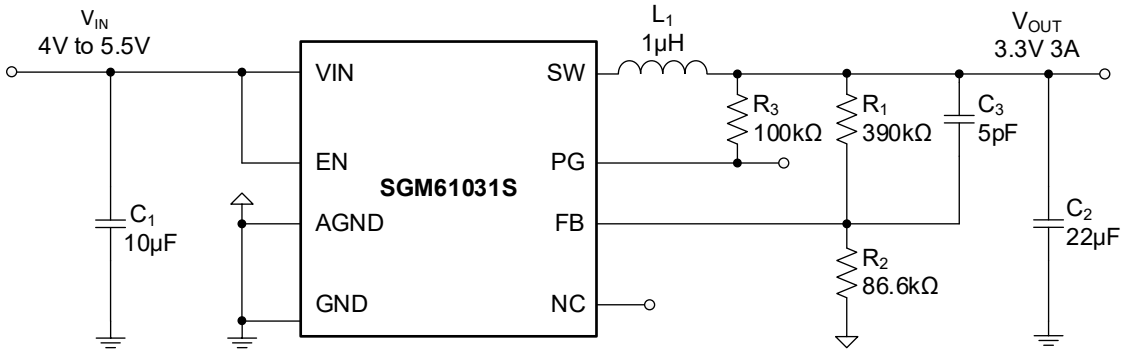


Figure 9. 3.3V Output Voltage Application

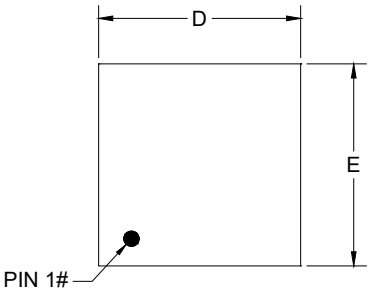
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

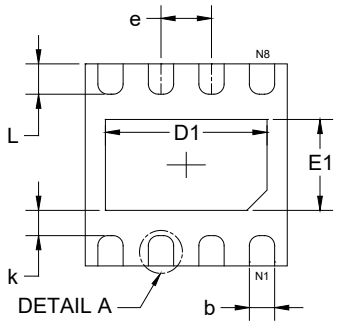
Changes from Original (APRIL 2025) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

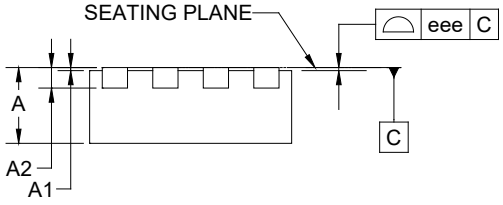
TDFN-2×2-8AL



TOP VIEW

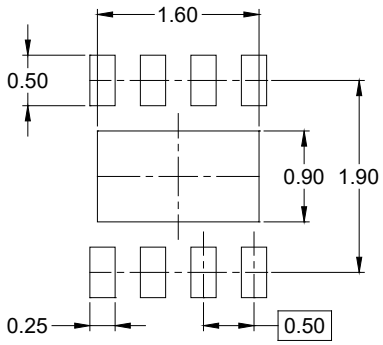


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



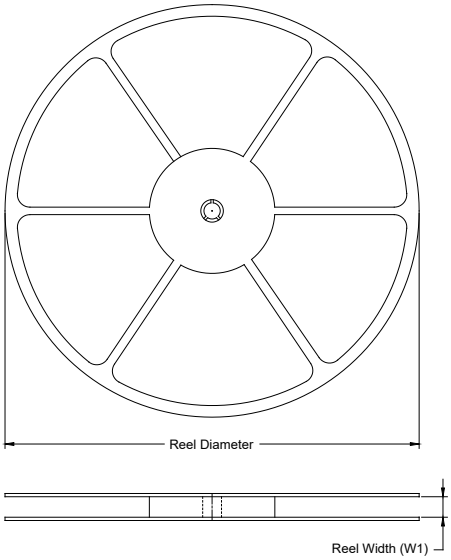
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
D1	1.450	-	1.700
E	1.900	-	2.100
E1	0.750	-	1.000
k	0.200	-	-
e	0.500 BSC		
L	0.200	-	0.400
eee	0.080		

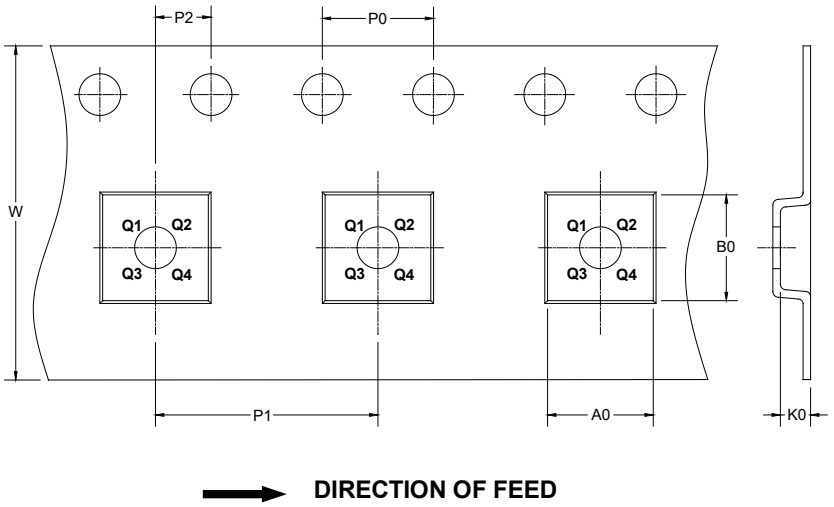
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



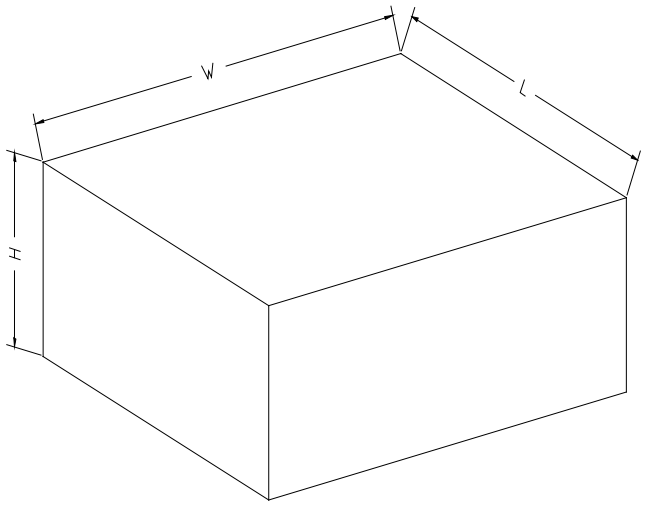
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002