SGM5102
14-Bit, 25MSPS, Low Power Dual Analog-to-Digital Converter Cores

GENERAL DESCRIPTION

The SGM5102 is a 14-bit, 2 channels simultaneous sampling pipeline analog-to-digital converter (ADC). Its good DC and AC performances are designed for low power high-speed control application.

It supports both oversampling and undersampling of IF frequencies.

The SGM5102 offers series LVDS interface. Each ADC channel output can be shifted out by 2-lane mode (2 bits at a time) or 1-lane mode (1 bit at a time). The LVDS drivers have internal optional termination resistors and they are turned off by default.

The SGM5102 supports either differential or single-ended clock signal. Clock signals with PECL, TTL, CMOS or LVDS format can be provided to ENC+ and ENC- pins. The device has internal clock duty cycle stabilizer, which allows a wide range clock duty cycles and keeps high ADC performance at the same time.

The SGM5102 is available in a Green TQFN-6×6-40AL package. It operates over an ambient temperature range -40℃ to +125℃.

FEATURES

- **2-Channel Simultaneous Sampling**
- **INL: ±1.5LSB (TYP), DNL: ±0.6LSB (TYP)**
- **Typical SNR: 71dB (TYP)**
- **Typical SFDR: 93dB (TYP)**
- **Low Power:**
  - **128mW (TYP) Total**
  - **64mW per Channel**
- **Single Supply: 1.8V**
- **Digital Outputs: Serial LVDS with 1 or 2 Bits per Channel**
- **Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$**
- **Full Power Bandwidth S/H: 800MHz**
- **Sleep and Nap Modes**
- **Serial SPI Port for Configuration**
- **Available in a Green TQFN-6×6-40AL Package**

APPLICATIONS

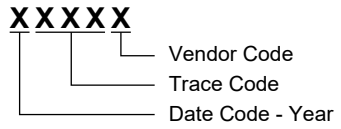
Security Monitoring Equipment
Communication Systems
Medical Imaging Systems
Testing and Measurement Instruments

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5102	TQFN-6×6-40AL	-40℃ to +125℃	SGM5102XTSQ40G/TR	1RX XTSQ40 XXXXX	Tape and Reel, 3000
			SGM5102XTSQ40SG/TR	1RX XTSQ40 XXXXX	Tape and Reel, 250

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range
V_{DD}, OV_{DD} ..... -0.3V to 2V
Analog Input Voltage Range (2)
AIN+, AIN-, PAR/nSER, SENSE ..... -0.3V to (V_{DD} + 0.2V)
Digital Input Voltage Range (3)
ENC+, ENC-, CS, SDI, SCLK ..... -0.3V to 3.9V
SDO (3) ..... -0.3V to 3.9V
Digital Output Voltage Range..... -0.3V to (OV_{DD} + 0.3V)
Package Thermal Resistance
TQFN-6×6-40AL, θ_{JA}..... 26.8℃/W
TQFN-6×6-40AL, θ_{JB}..... 8.6℃/W
TQFN-6×6-40AL, $\theta_{JC\ (TOP)}$ ..... 15.6℃/W
TQFN-6×6-40AL, $\theta_{JC\ (BOT)}$ ..... 2.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....3000V
CDM 1000V

NOTES:

1. All voltage values are referenced to GND and assume that GND and OGND are shorted, unless otherwise stated.

2. Internal protection circuits help clamp these pin voltages when they are driven below GND or beyond V_{DD}. The device is designed to handle more than 100mA input currents below GND or beyond V_{DD} without the risk of latch-up.

3. Internal protection circuits help clamp these pin voltages when they are driven below GND. These pin voltages won't be clamped when these pin voltages are beyond V_{DD}. The device is designed to handle more than 100mA input currents below GND without the risk of latch-up.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

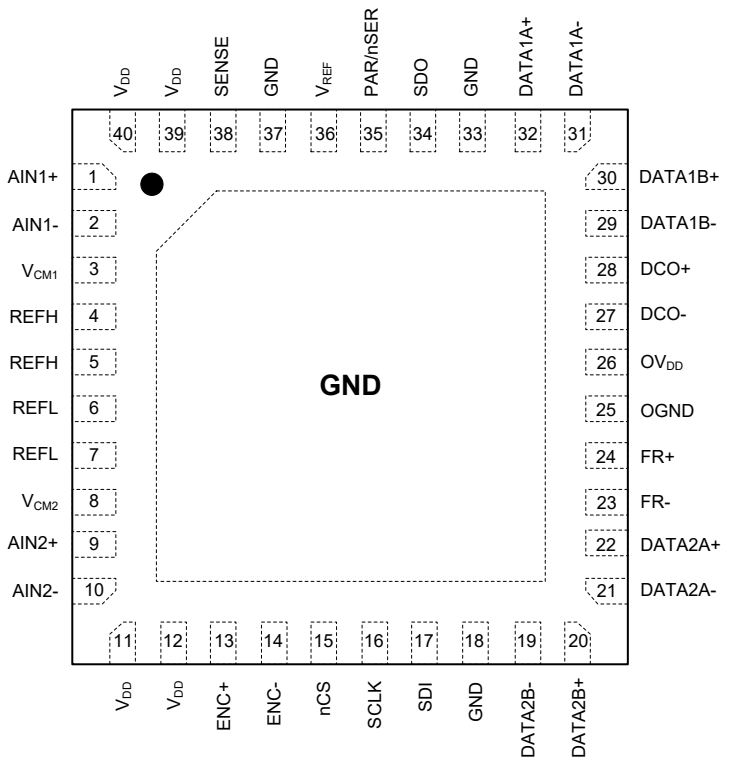
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-6×6-40AL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	AIN1+	Channel 1 Positive Differential Analog Input.
2	AIN1-	Channel 1 Negative Differential Analog Input.
3	V_{CM1}	Common Mode Bias Voltage Output, nominally equal to 0.85V. V_{CM1} is suggested to be used as the bias voltage of input channel 1. A 0.1μF bypass capacitor is suggested to connect between this pin and ground.
4, 5	REFH	ADC High Reference. At least a 2.2μF capacitor coupled with a 0.1μF capacitor is suggested to connect between REFH and REFL.
6, 7	REFL	ADC Low Reference. At least a 2.2μF capacitor coupled with a 0.1μF capacitor is suggested to connect between REFH and REFL.
8	V_{CM2}	Common Mode Bias Voltage Output, nominally equal to 0.85V. V_{CM2} is suggested to be used as the bias voltage of input channel 2. A 0.1μF bypass capacitor is suggested to connect between this pin and ground.
9	AIN2+	Channel 2 Positive Differential Analog Input.
10	AIN2-	Channel 2 Negative Differential Analog Input.
11, 12, 39, 40	V_{DD}	1.8V Analog Power Supply. A 0.1μF bypass ceramic capacitors is suggested to connect between this pin and Ground.
13	ENC+	Encode Positive Input. The input sample starts on the positive edge.
14	ENC-	Encode Negative Input. The input sample starts on the negative edge.
15	nCS	When PAR/nSER = 0V (The device works in serial programming mode.), nCS goes to logic low which means the data on SDI is being shifted into the mode control registers. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), nCS is used to select 2-lane output mode or 1-lane output mode. nCS supports the driven voltage from 1.8V to 3.3V.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
16	SCLK	When PAR/nSER = 0V (The device works in serial programming mode.), SCLK is the serial interface clock input. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), SCLK is used to select 3.5mA or 1.75mA LVDS output current. SCLK supports the driven voltage from 1.8V to 3.3V.
17	SDI	When PAR/nSER = 0V (The device works in serial programming mode.), SDI is the serial interface data input. Data is locked in at the rising edge of SCLK. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), SDI is used to power down the part. SDI supports the driven voltage from 1.8V to 3.3V.
18, 33, 37	GND	ADC Power Ground.
19	DATA2B-	Serial LVDS Outputs for Channel 2. Only OUT2A-/OUT2A+ are used in 1-lane output mode. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
20	DATA2B+	
21	DATA2A-	
22	DATA2A+	
23	FR-	Frame Start Output. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
24	FR+	
25	OGND	Output Driver Ground. Connect directly to the ground plane. Multiple vias close to the pin in the layout is strongly recommended.
26	OV_{DD}	Output Driver Supply. A 0.1μF bypass ceramic capacitors is suggested to connect between this pin and Ground.
27	DCO-	Data Clock Output. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
28	DCO+	
29	DATA1B-	Serial LVDS Outputs for Channel 1. Only OUT1A-/OUT1A+ are used in 1-lane output mode. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
30	DATA1B+	
31	DATA1A-	
32	DATA1A+	
34	SDO	In serial programming mode (PAR/nSER = 0V), if SDO is used as data output pin, as SDO pin is an open-drain output, it must be pulled up to OV_{DD} by an external resistor (suggest 2kΩ). If data output is not needed, it can be left floated. In parallel programming mode (PAR/nSER = V_{DD}), SDO is an input which enables an internal 100Ω termination resistor on the pin connection, SDO can be driven through a 1kΩ series resistor from the interface logic.
35	PAR/nSER	Programming Mode Selection Pin. This pin must be connected to GND or V_{DD} directly. If this pin is connected to GND, nCS, SCLK, SDI and SDO are packaged to serial interface to configure ADC working mode. If this pin is connected to V_{DD}, nCS, SCLK, SDI and SDO are packaged as logic inputs to setting the ADC working mode.
36	V_{REF}	Reference Voltage Output. Voltage nominally 1.25V. A 1μF bypass ceramic capacitors is suggested to connect between this pin and ground.
38	SENSE	Internal reference and a ±1V input range is selected if SENSE is connected to V_{DD}. Similarly, Internal reference and a ±0.5V input range is selected if SENSE is connected to ground. External reference and an input range of ±0.8 • V_{SENSE} is selected if SENSE is connected to a voltage from 0.625V to 1.3V.
Exposed Pad	GND	Must be connected to the PCB ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 25MHz, 2-lane output mode, differential ENC+/ENC- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter Characteristics						
Resolution (No Missing Codes)			14			Bits
Integral Nonlinearity	INL	Differential analog input	-3	±1.5	3	LSB
Differential Nonlinearity	DNL	Differential analog input	-1.0	±0.6	1.2	LSB
Offset Error (1)	E_O		-14	±3	14	mV
Gain Error	E_G	Internal reference		0.1		%FS
		External reference	-2.5	0.1	2.5	
Offset Drift				±20		μV/℃
Full-Scale Drift		Internal reference		±30		ppm/℃
		External reference		±10		
Gain Matching		External reference		±0.2		%FS
Offset Matching				±1		mV
Transition Noise		External reference		1.2		LSB_{RMS}
Analog Input						
Analog Input Range (AIN+ - AIN-)	V_{IN}	1.7V < V_{DD} < 1.9V		1 to 2		V_{P-P}
Analog Input Common Mode (AIN+ + AIN-)/2	$V_{IN(CM)}$	Differential analog input (5)	V_{CM} - 100mV	V_{CM}	V_{CM} + 100mV	V
External Voltage Reference Applied to SENSE	V_{SENSE}	External reference mode	0.625	1.25	1.3	V
Analog Input Common Mode Current	$I_{IN(CM)}$	Per pin, 65MSPS		81		μA
		Per pin, 40MSPS		50		
		Per pin, 25MSPS		31		
Analog Input Leakage Current (No Encode)	I_{IN1}	0 < AIN+, AIN- < V_{DD}	-1		1	μA
PAR/nSER Input Leakage Current	I_{IN2}	0 < PAR/nSER < V_{DD}	-3		3	μA
SENSE Input Leakage Current	I_{IN3}	0.625 < SENSE < 1.3V	-6		6	μA
Sample-and-Hold Acquisition Delay Time	t_{AP}			0		ns
Sample-and-Hold Acquisition Delay Jitter	t_{JITTER}			0.15		ps_{RMS}
Analog Input Common Mode Rejection Ratio	CMRR			60		dB
Full-Power Bandwidth	BW_{-3B}			800		MHz
Dynamic Accuracy (A_{IN} = -1dBFS)						
Signal-to-Noise Ratio	SNR	5MHz input		71		dBFS
		30MHz input	67	71		
		70MHz input		71		
Spurious Free Dynamic Range (2nd or 3rd Harmonic)	SFDR	5MHz input		93		dBFS
		30MHz input	82	92		
		70MHz input		86		
Spurious Free Dynamic Range (4th Harmonic or Higher)		5MHz input		97		dBFS
		30MHz input	82	96		
		70MHz input		90		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 25MHz, 2-lane output mode, differential ENC+/ENC- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise + Distortion	SINAD	5MHz input		71		dBFS
		30MHz input	67	71		
		70MHz input		71		
Crosstalk		10MHz input		-105		dBc
Internal Reference Characteristics (A_{IN} = -1dBFS)						
V_{CM} Output Voltage		I_{OUT} = 0mA	0.83	0.85	0.88	V
V_{CM} Output Temperature Drift				±25		ppm/℃
V_{CM} Output Resistance		-600μA < I_{OUT} < 1mA		3		Ω
V_{REF} Output Voltage		I_{OUT} = 0mA	1.225	1.25	1.290	V
V_{REF} Output Temperature Drift				±25		ppm/℃
V_{REF} Output Resistance		-400μA < I_{OUT} < 1mA		5		Ω
V_{REF} Line Regulation		1.7V < V_{DD} < 1.9V		0.4		mV/V
Digital Inputs and Outputs						
Encode Inputs (ENC+/ENC-): Differential Encode Mode (ENC- Not Tied to GND)						
Differential Input Voltage (2)	V_{ID}		0.2			V
Common Mode Input Voltage	V_{ICM}	Internally set		1.2		V
		Externally set (2)	1.1		1.6	
Input Voltage Range	V_{IN}	ENC+, ENC- to GND	0.2		3.6	V
Input Resistance	R_{IN}	See Figure 16		10		kΩ
Input Capacitance	C_{IN}			3.5		pF
Encode Inputs (ENC+/ENC-): Single-Ended Encode Mode (ENC- Tied to GND)						
High-Level Input Voltage	V_{IH}	V_{DD} = 1.8V	1.2			V
Low-Level Input Voltage	V_{IL}	V_{DD} = 1.8V			0.6	V
Input Voltage Range	V_{IN}	ENC+ to GND	0		3.6	V
Input Resistance	R_{IN}	See Figure 17		30		kΩ
Input Capacitance	C_{IN}			3.5		pF
Digital Inputs (nCS, SDI, SCLK in Serial or Parallel Programming Mode. SDO in Parallel Programming Mode)						
High-Level Input Voltage	V_{IH}	V_{DD} = 1.8V	1.3			V
Low-Level Input Voltage	V_{IL}	V_{DD} = 1.8V			0.6	V
Input Current	I_{IN}	V_{IN} = 0V to 3.6V	-10		10	μA
Input Capacitance	C_{IN}			3		pF
SDO Output (Serial Programming Mode. Open-Drain Output. Requires 2kΩ Pull-Up Resistor if SDO is Used)						
Logic Low Output Resistance to GND	R_{OL}	V_{DD} = 1.8V, SDO = 0V		50		Ω
Logic High Output Leakage Current	I_{OH}	SDO = 0V to 3.6V	-10		10	μA
Output Capacitance	C_{OUT}			3		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 25MHz, 2-lane output mode, differential ENC+/ENC- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs							
Differential Output Voltage	V_{OD}	100Ω differential load	3.5mA mode	247	350	454	mV
			1.75mA mode	125	185	250	
Common Mode Output Voltage	V_{OS}	100Ω differential load	3.5mA mode	1.125	1.23	1.375	V
			1.75mA mode	1.125	1.23	1.375	
On-Chip Termination Resistance	R_{TERM}				100		Ω
Power Requirements (3)							
Analog Supply Voltage (4)	V_{DD}			1.7	1.8	1.9	V
Output Supply Voltage (4)	OV_{DD}			1.7	1.8	1.9	V
Analog Supply Current	I_{VDD}	Sine wave input			76	110	mA
Digital Supply Current	I_{OVDD}	1-lane mode, 1.75mA mode			14		mA
		1-lane mode, 3.5mA mode			21		
		2-lane mode, 1.75mA mode			16	20	
		2-lane mode, 3.5mA mode			27	32	
Power Dissipation	P_{DISS}	1-lane mode, 1.75mA mode			128		mW
		1-lane mode, 3.5mA mode			140		
		2-lane mode, 1.75mA mode			131	155	
		2-lane mode, 3.5mA mode			151	175	
LPM Mode Power Dissipation (6)	P_{DISS_LPM}	1-lane mode, 1.75mA mode			77		mW
		1-lane mode, 3.5mA mode			90		
		2-lane mode, 1.75mA mode			83		
		2-lane mode, 3.5mA mode			102		
Sleep Mode Power	P_{SLEEP}				1		mW
Nap Mode Power	P_{NAP}				40		mW
Power Increase with Differential Encode Mode Enabled (No Increase for Sleep Mode)	$P_{DIFFCLK}$				25		mW

NOTES:

1. The offset error refers to the voltage offset that is measured when the output code alternates between code equals all 0s and all 1s in two's complement output mode, with -0.5LSB being the starting point.

2. Guaranteed by design.

3. V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 25MHz, 2-lane output mode, ENC+ = single-ended 1.8V square wave, ENC- = 0V, input range = $2V_{P-P}$ with differential drive, unless otherwise noted. The supply current and power consumptions are specified by whole chip.

4. Suggested operating conditions.

5. The maximum sampling frequency is determined by the serialization mode. The maximum output data rate is 400Mbps, so t_{SER} must be no less than 2.5ns.

6. f_{SAMPLE} = 10MHz, ENC+ = single-ended 1.8V square wave, LPM mode.

TIMING CHARACTERISTICS

(V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 25MHz, 2-lane output mode, differential ENC+/ENC- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sampling Frequency (2) (3)	f_S		5		25	MHz
ENC Low Time (1)	t_{ENCL}	Duty cycle stabilizer off	19	20	100	ns
		Duty cycle stabilizer on	6	20	100	
ENC High Time (1)	t_{ENCH}	Duty cycle stabilizer off	19	20	100	ns
		Duty cycle stabilizer on	6	20	100	
Sample-and-Hold Acquisition Delay Time	t_{AP}			0		ns
Digital Data Outputs (R_{TERM} = 100Ω Differential, C_L = 2pF to GND on Each Output)						
Serial Data Bit Period	t_{SER}	Two lanes, 16-bit serialization		$1/(8 \times f_S)$		s
		Two lanes, 14-bit serialization		$1/(7 \times f_S)$		
		Two lanes, 12-bit serialization		$1/(6 \times f_S)$		
		One lane, 16-bit serialization		$1/(16 \times f_S)$		
		One lane, 14-bit serialization		$1/(14 \times f_S)$		
		One lane, 12-bit serialization		$1/(12 \times f_S)$		
FR to DCO Delay (1)	t_{FRAME}		$0.35 \times t_{SER}$	$0.5 \times t_{SER}$	$0.65 \times t_{SER}$	s
DATA to DCO Delay (1)	t_{DATA}		$0.35 \times t_{SER}$	$0.5 \times t_{SER}$	$0.65 \times t_{SER}$	s
Propagation Delay (1)	t_{PD}		$0.7n + 2 \times t_{SER}$	$1.1n + 2 \times t_{SER}$	$1.5n + 2 \times t_{SER}$	s
Output Rise Time	t_R	Data, DCO, FR, 20% to 80%		0.17		ns
Output Fall Time	t_F	Data, DCO, FR, 20% to 80%		0.17		ns
DCO Cycle-to-Cycle Jitter		t_{SER} = 1ns		60		ps_{P-P}
Pipeline Latency				6		Cycles
SPI Port Timing (1)						
SCLK Period	t_{SCLK}	Write mode	40			ns
		Readback mode, C_{SDO} = 20pF, $R_{PULL-UP}$ = 2kΩ	250			
nCS to SCLK Set-Up Time	t_S		5			ns
SCLK to nCS Set-Up Time	t_H		5			ns
SDI Set-Up Time	t_{DS}		5			ns
SDI Hold Time	t_{DH}		5			ns
SCLK Falling to SDO Valid	t_{DO}	Readback mode, C_{SDO} = 20pF, $R_{PULL-UP}$ = 2kΩ			125	ns

NOTES:

1. Guaranteed by design.

2. Suggested operating conditions.

3. The maximum sampling frequency is determined by the serialization mode. The maximum output data rate is 400Mbps, so t_{SER} must be no less than 2.5ns.

TIMING DIAGRAMS

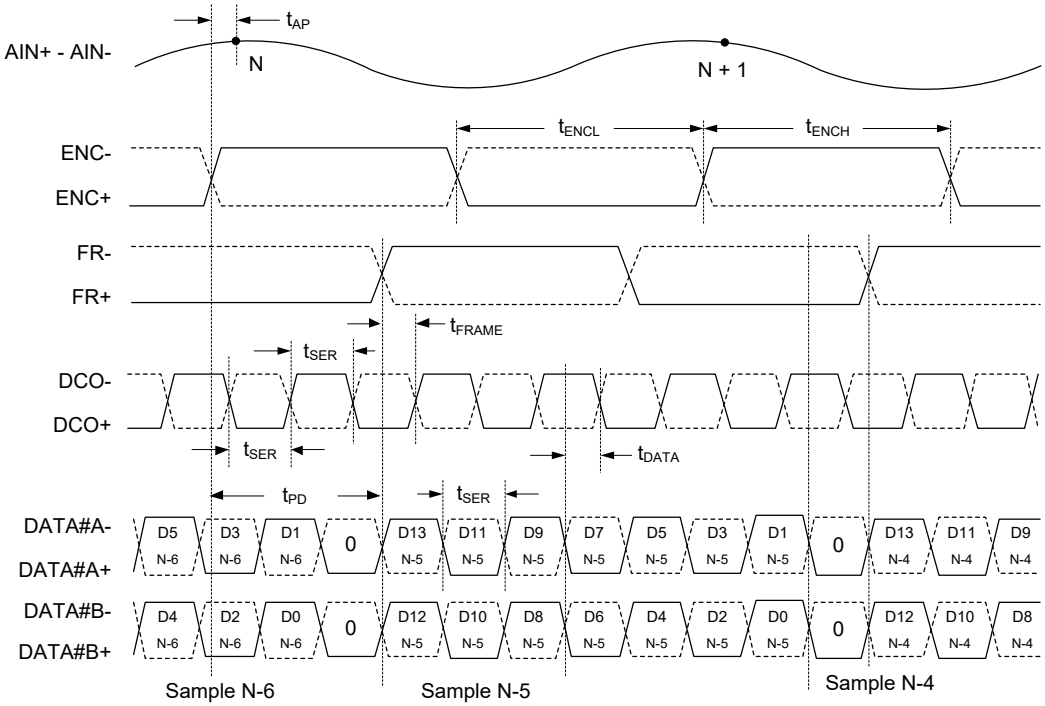
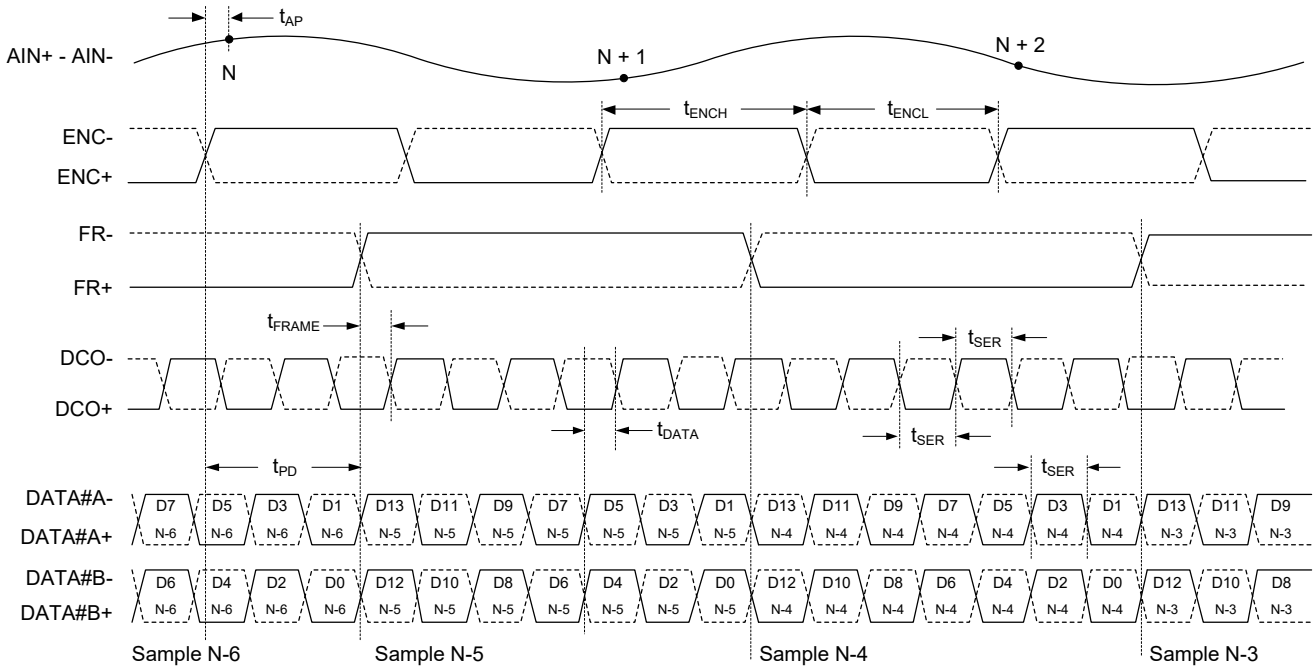


Figure 1. 2-Lane Output Mode, 16-Bit Serialization



NOTE:
During this mode, FR+/FR- has two times the period of ENC+/ENC-.

Figure 2. 2-Lane Output Mode, 14-Bit Serialization

TIMING DIAGRAMS (continued)

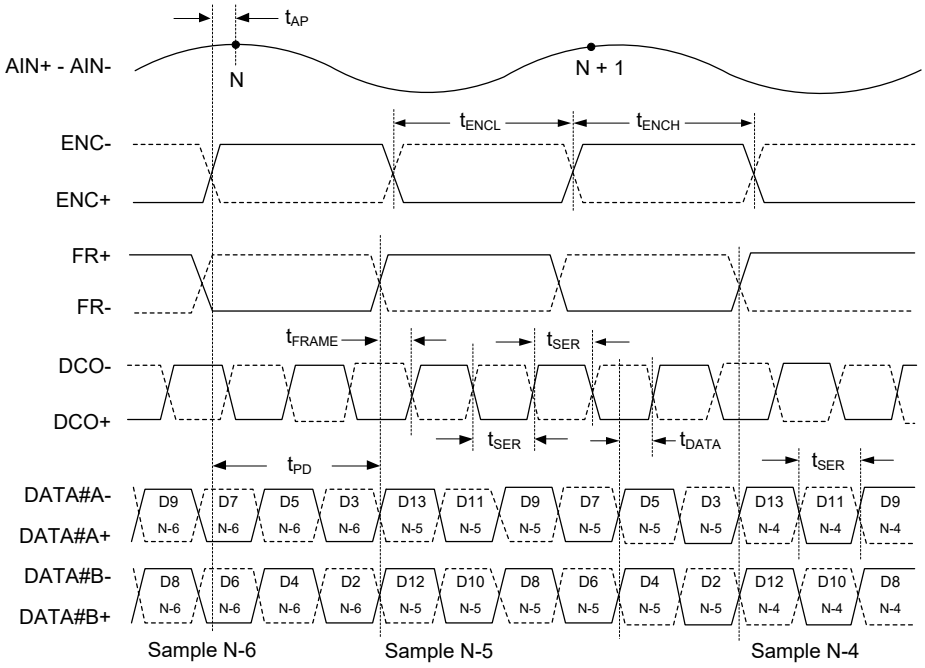
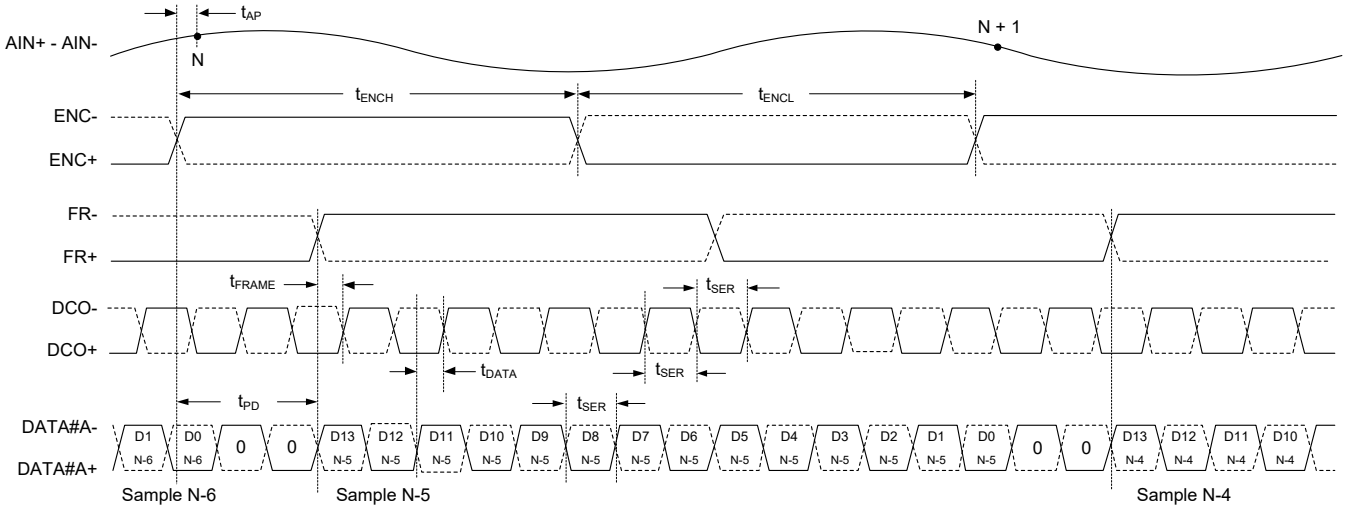


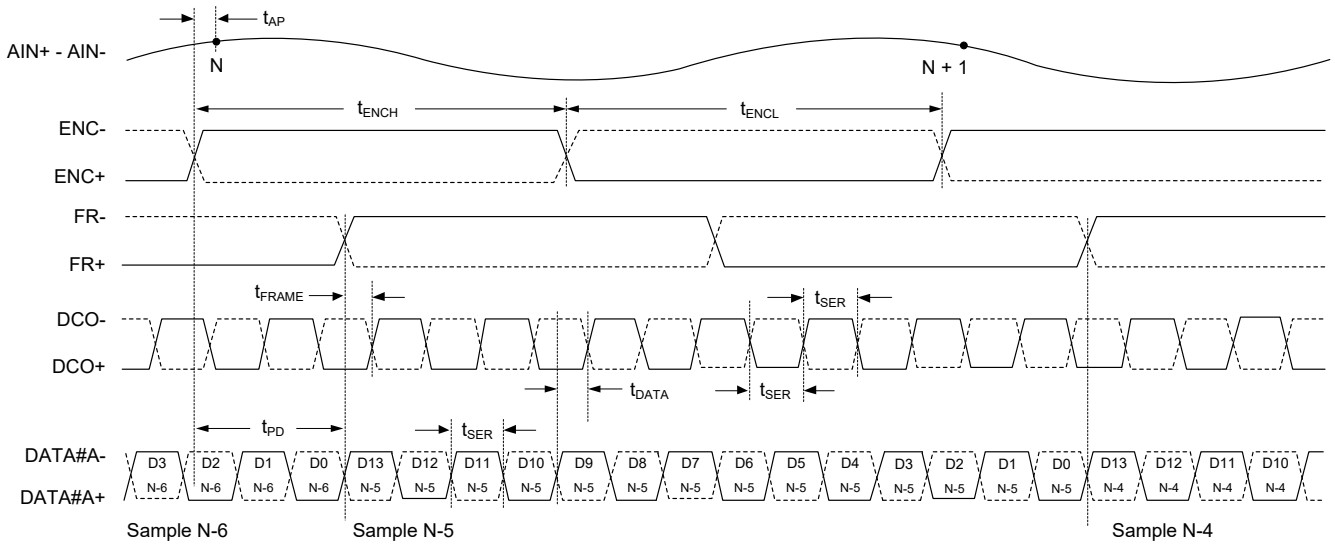
Figure 3. 2-Lane Output Mode, 12-Bit Serialization



NOTE:
DATA#B+, DATA#B- are disabled.

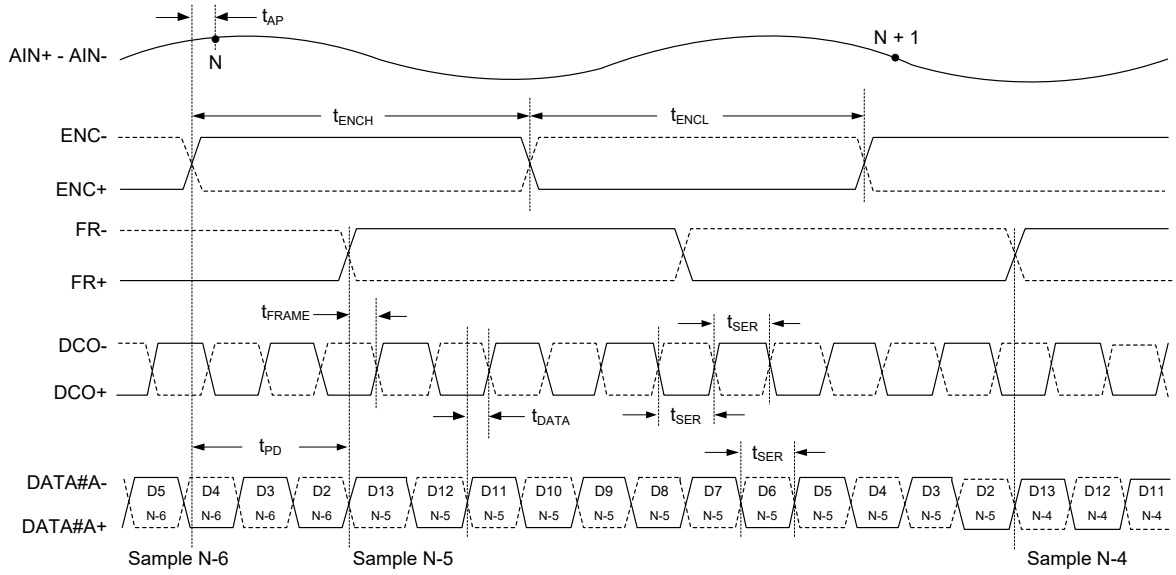
Figure 4. 1-Lane Output Mode, 16-Bit Serialization

TIMING DIAGRAMS (continued)



NOTE:
DATA#B+, DATA#B- are disabled.

Figure 5. 1-Lane Output Mode, 14-Bit Serialization



NOTE:
DATA#B+, DATA#B- are disabled.

Figure 6. 1-Lane Output Mode, 12-Bit Serialization

TIMING DIAGRAMS (continued)

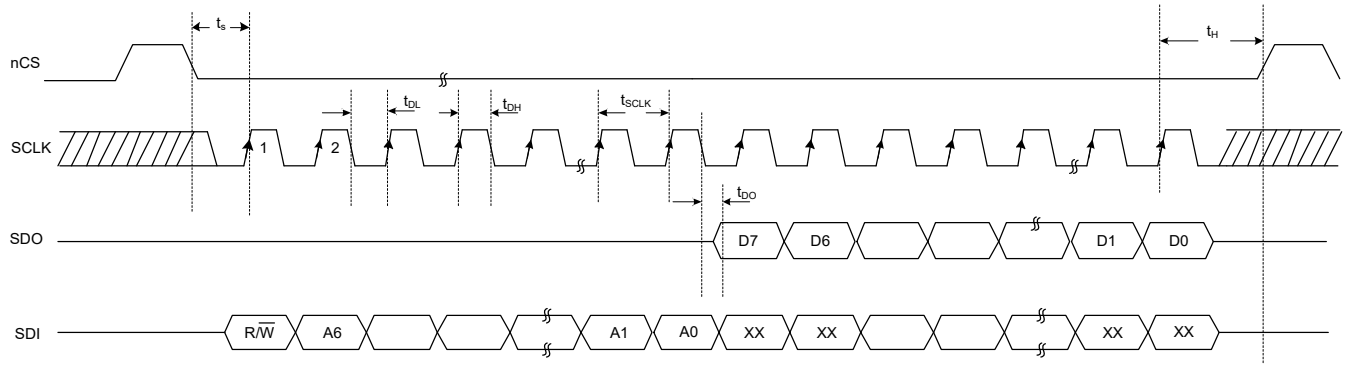


Figure 7. SPI Port Timing (Readback Mode)

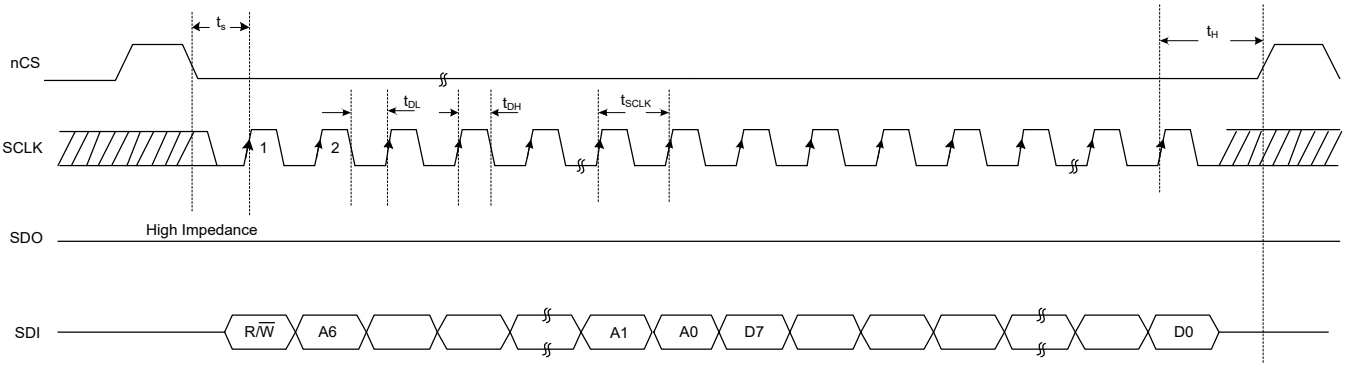
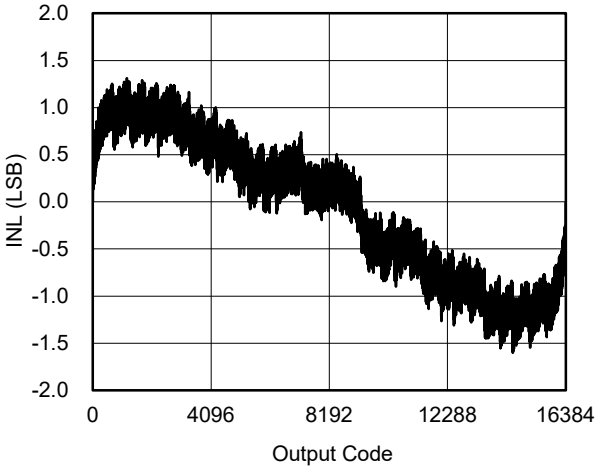


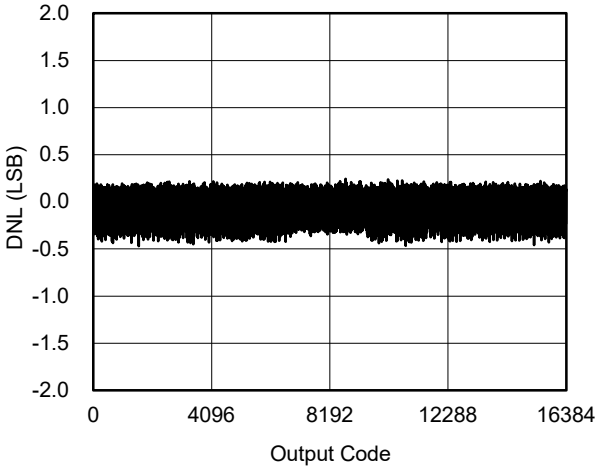
Figure 8. SPI Port Timing (Write Mode)

TYPICAL PERFORMANCE CHARACTERISTICS

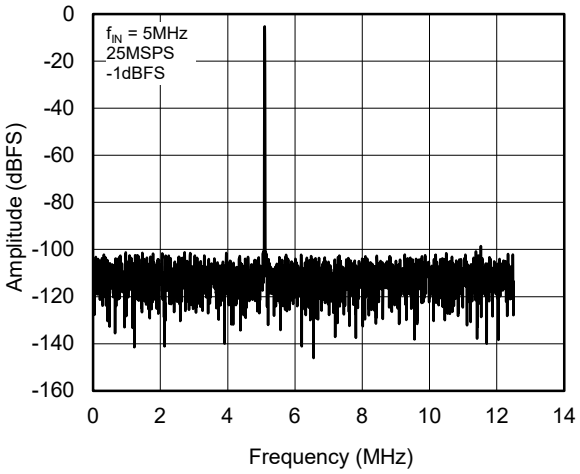
Integral Nonlinearity vs. Output Code



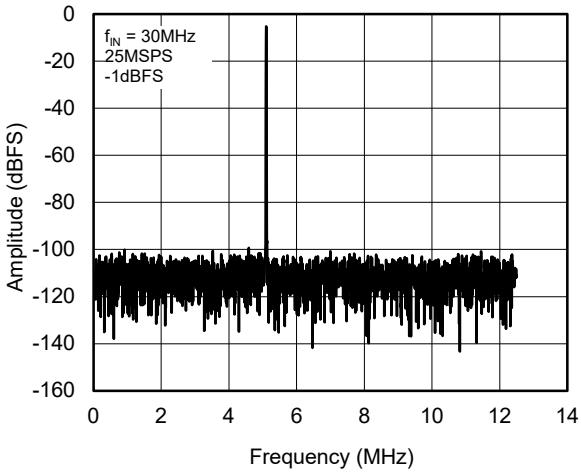
Differential Nonlinearity vs. Output Code



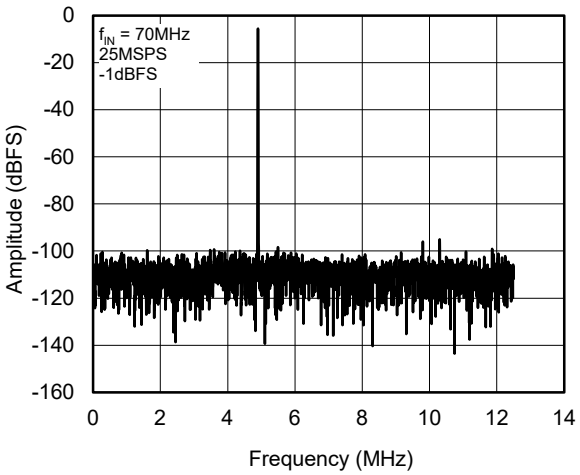
FFT with 5MHz Input Signal



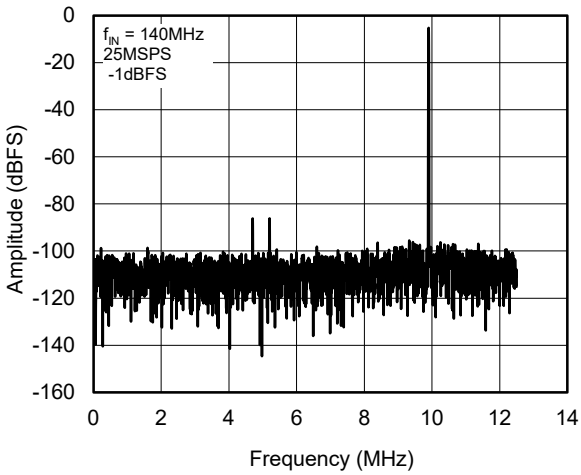
FFT with 30MHz Input Signal



FFT with 70MHz Input Signal

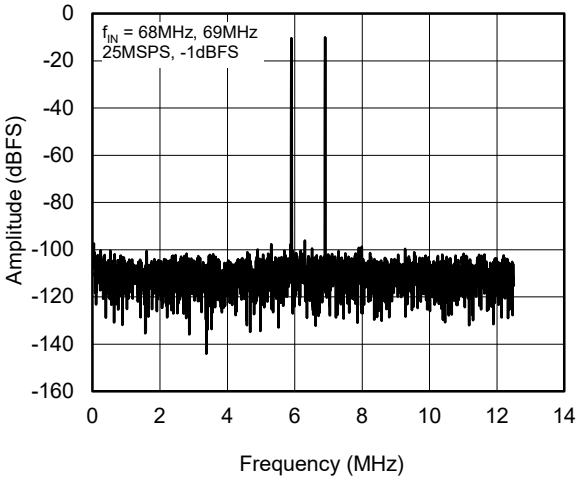


FFT with 140MHz Input Signal

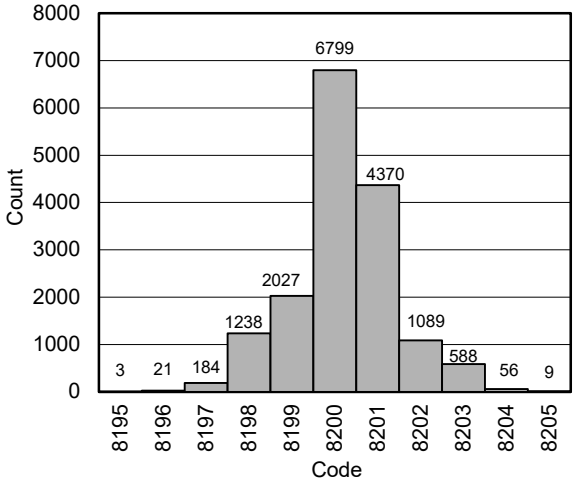


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

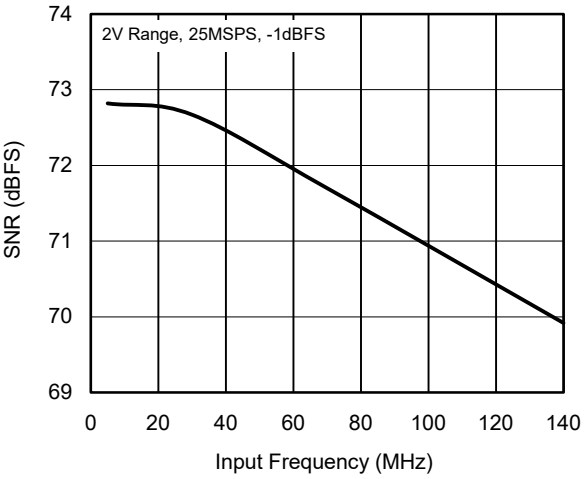
FFT with 2-Tone input Signal



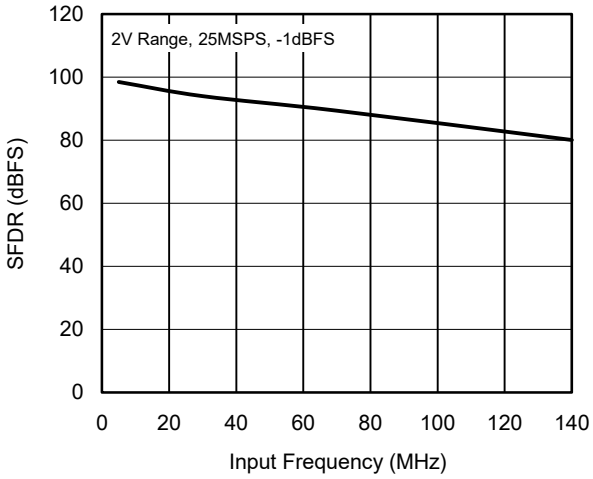
Shorted Input Histogram



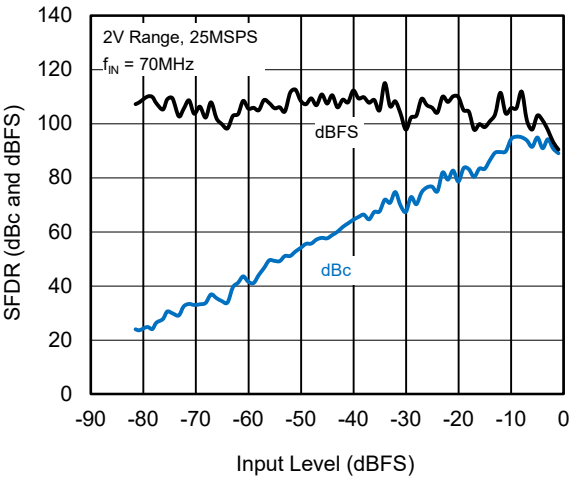
SNR vs. Input Frequency



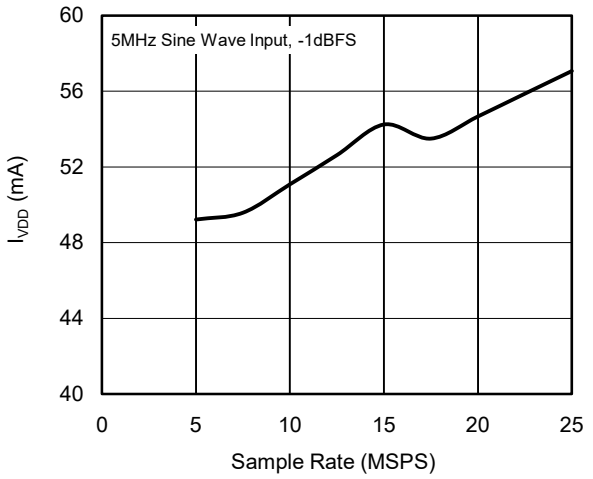
SFDR vs. Input Frequency



SFDR vs. Input Level

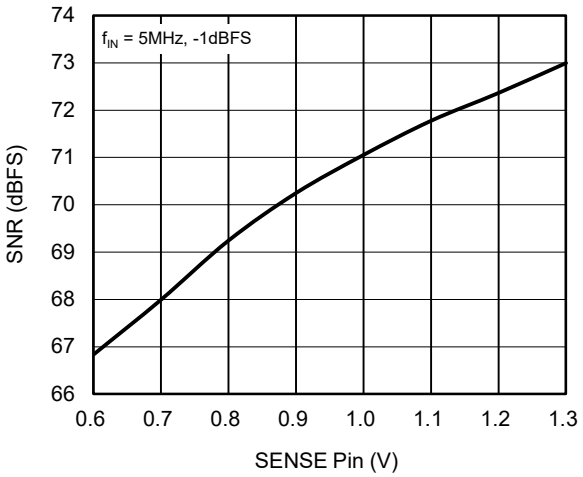


I_{VDD} vs. Sample Rate

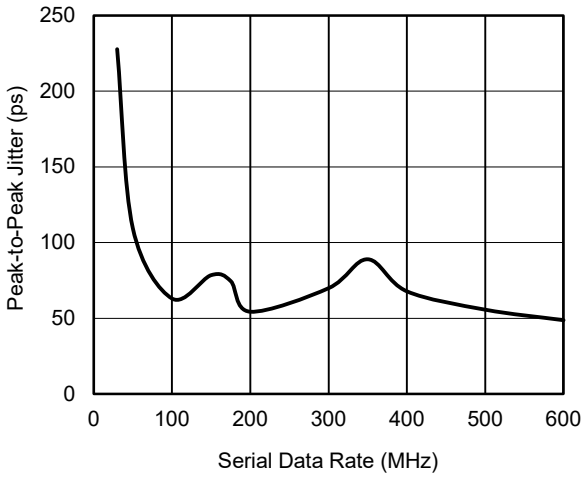


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

SNR vs. SENSE Pin



DCO Cycle-Cycle Jitter vs. Serial Data Rate



TYPICAL APPLICATION CIRCUIT

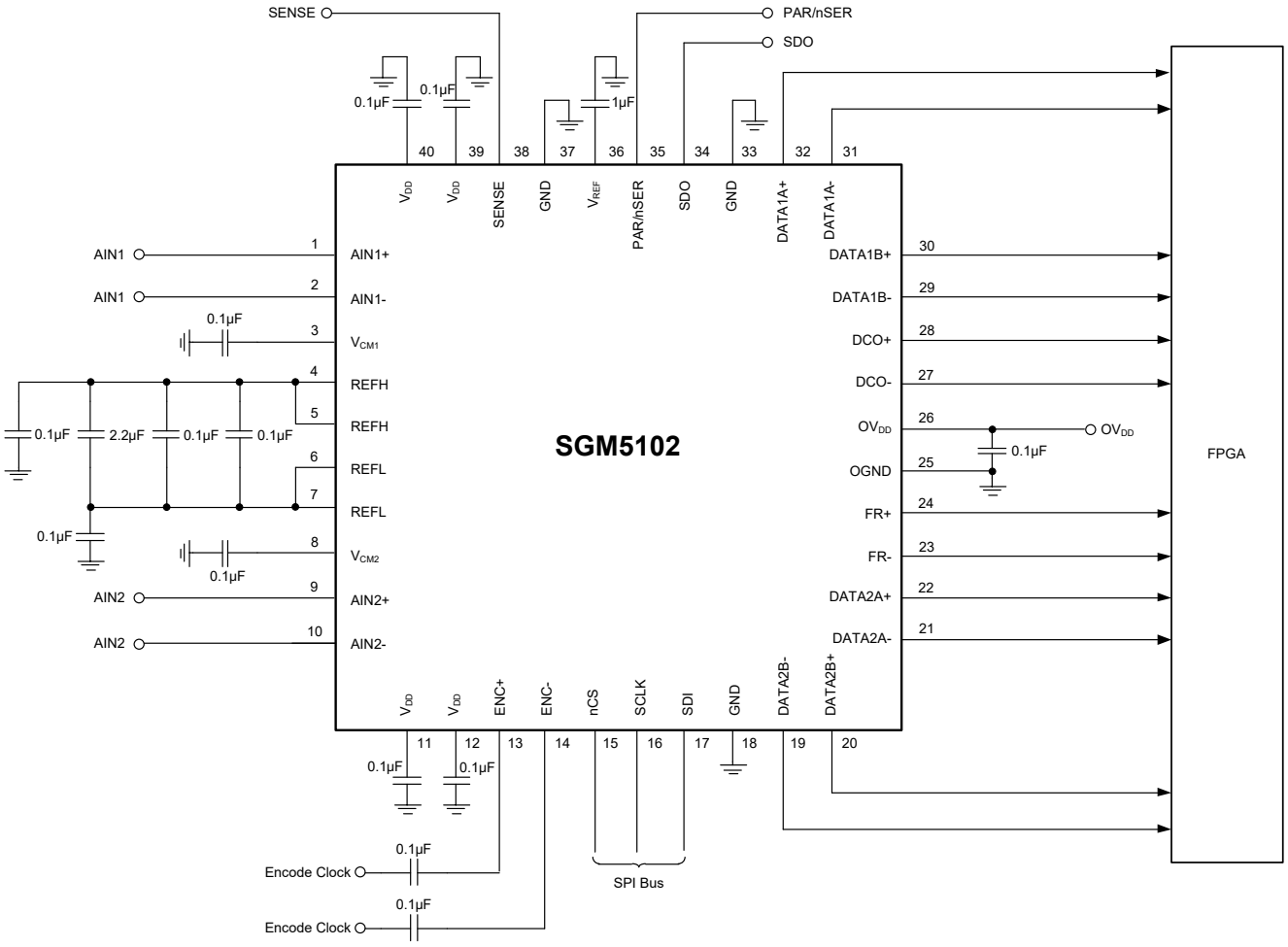


Figure 9. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

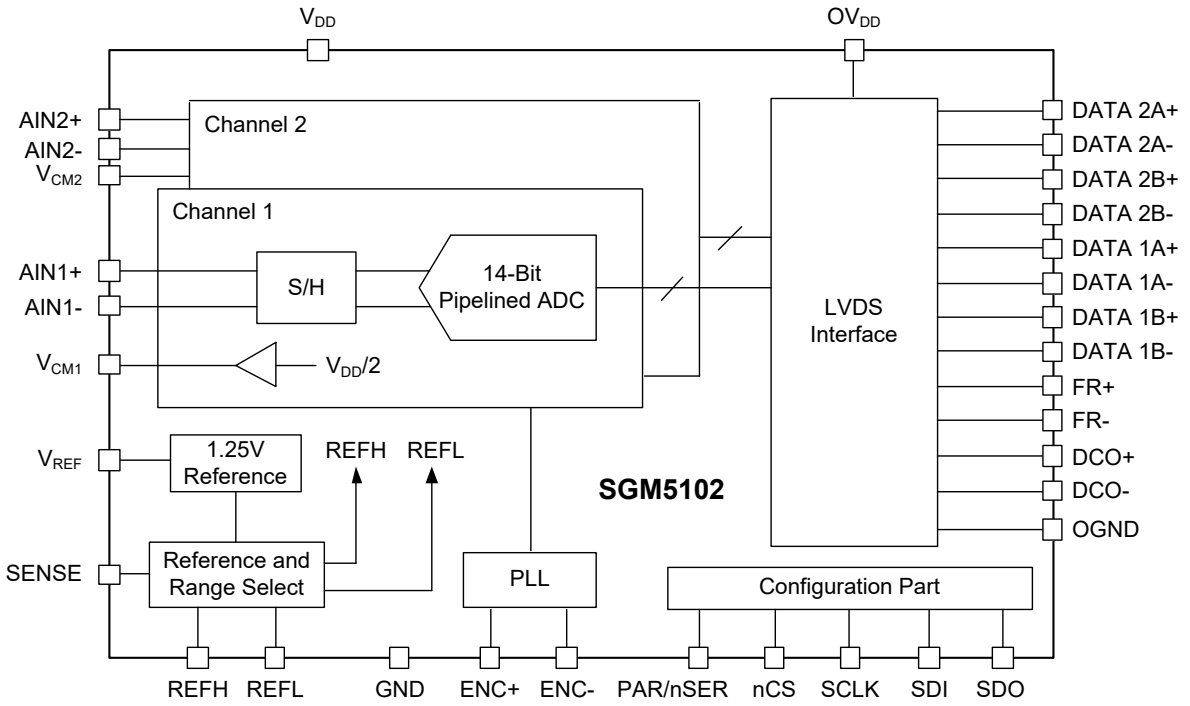


Figure 10. Block Diagram

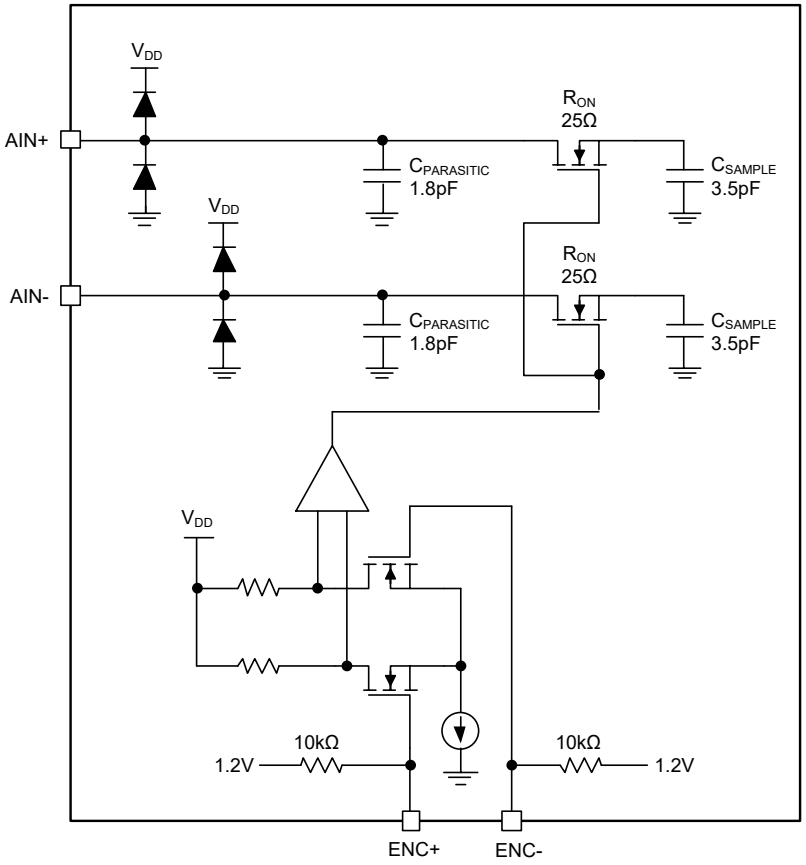
APPLICATION INFORMATION

Converter Operation

The SGM5102 is a dual, 14-bit, low power, 25MSPS analog-to-digital converter (ADC). Each ADC core is based on a multistage, differential pipelined architecture with differential input analog signal. This device supports serial low-voltage differential signaling (LVDS) to minimize the number of interface lines. The output LVDS interface can be set as two-wire mode or one-wire mode. To get optimal jitter performance, the encode input can be driven differentially, or the single-ended mode can be selected to get lower power consumption. There are two programming modes: parallel programming mode and serial programming mode. All the programming modes are set by a SPI port.

Analog Input

In the SGM5102, the differential CMOS sample-and-hold circuits are used for analog inputs, which are shown in Figure 11. The common-mode voltage, which is usually equal to 0.85V and set by the V_{CM1} or V_{CM2} output pins, can be used to properly bias the analog inputs. When the 2V input range is programmed, the analog input voltage should swing from V_{CM} - 0.5V to V_{CM} + 0.5V. A 180° phase difference between AIN+ and AIN- exists. With a shared encode circuit, the input of these two ADC channels should be synchronously sampled.



NOTE: Only one of the two analog channels is shown.

Figure 11. Equivalent Input Circuit

APPLICATION INFORMATION (continued)

Input Drive Circuits

Input Filtering

To isolate the drive circuitry from the ADC S/H switching and optimize wideband SNR level, it is advisable to add an RC low pass filter at the analog inputs. Figure 12 is an example which shows the input RC filter circuit application for SGM5102. Due to the different applications, the RC component values should be calculated and chosen.

Transformer Coupled Circuits

The analog inputs of SGM5102 are not internally DC biased. For the AC-coupled applications, SGM5102 could provide the common mode voltage by the two V_{CM} pins. There are also two RF transformers with a center-tapped secondary in Figure 12 and the ADC input DC level is set with V_{CM} of SGM5102. Transformers, especially the transmission line balun transformer, have the excellent performance for driving high-speed ADC with higher input frequencies.

Amplifier Circuits

Except for transformer, the high-speed differential amplifier can be used to drive the ADC input as Figure 13. To get minimum distortion, it is an excellent choice to set the output common mode voltage of the differential amplifier with V_{CM} pin because of the AC coupling mode.

Differential amplifiers are often used at lower frequencies, but for the very high frequencies, an RF gain block is preferred driving ADC for the optimal distortion. The single-ended signal from gain block is converted to differential with a transformer circuit at the front of analog input of A/D.

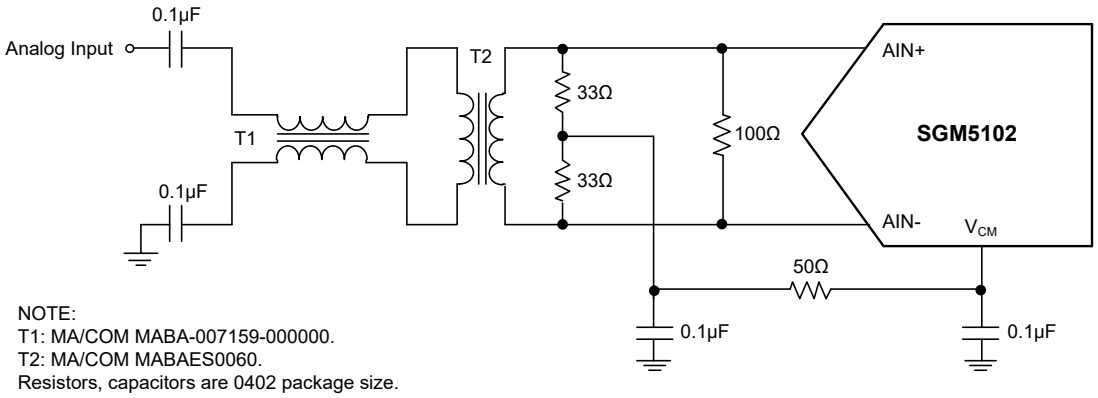


Figure 12. Analog Input Circuit Using Two RF Transformers

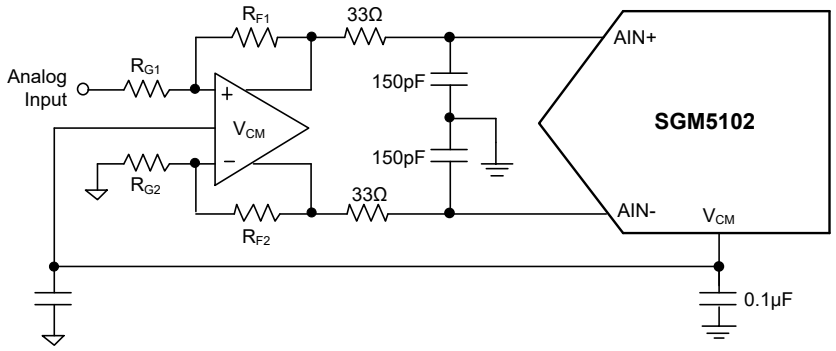


Figure 13. Analog Input Circuit Using a High-Speed Differential Amplifier

APPLICATION INFORMATION (continued)

Reference

There is an internal 1.25V voltage reference in the SGM5102. The SENSE pin is used to set analog input range. Connect SENSE to V_{DD} to get a 2V input range based on the internal reference. If the input range is 1V, the SENSE should be connected to ground. The SGM5102 also supports external reference input through SENSE and a 1.25V reference voltage can be used to set a 2V input range (refer to Figure 14). The external reference voltage can vary from 0.625V to 1.30V, which will set the input range to 1.6 × V_{SENSE}. Having only one reference means that the two ADC channels cannot independently adjust their input voltage ranges.

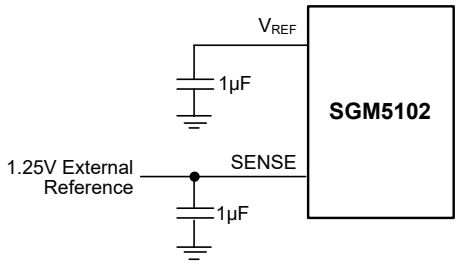


Figure 14. Using an External 1.25V Reference

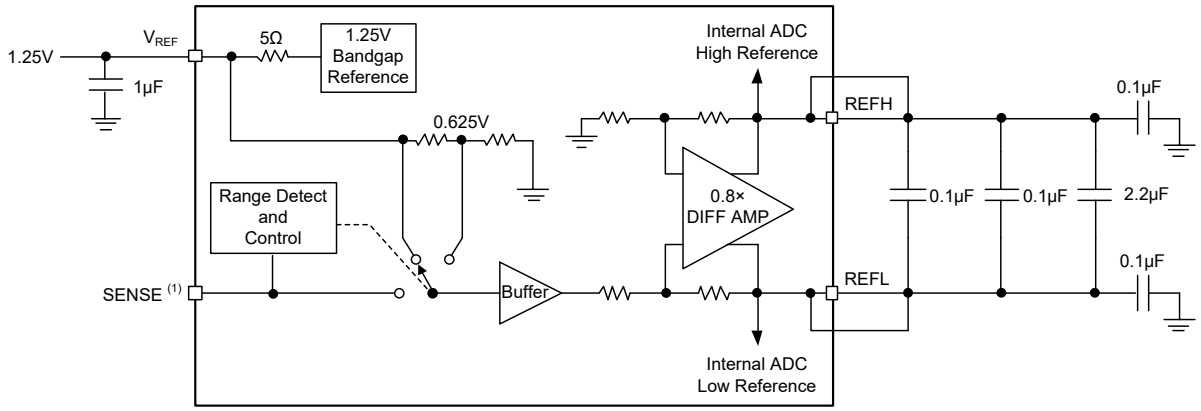
The bypass capacitors are necessary for VREF, REFH, REFL pins of the SGM5102. There is the reference design as shown in Figure 15. What calls for special attention is that the 0.1μF capacitor between REFH and REFL is necessary to be placed at the shorted distance from the pins at the same circuit board.

Encode Input

The noise performance of ADC is closely related to the encode inputs quality. Usually, the clock input of ADC is treated as digital signals to route, but for this encode inputs with high frequencies, it is important to route them away from digital traces when designing the application circuit board. Both the differential encode mode and the single-ended encode mode are supported at the SGM5102, as shown in Figure 16 and Figure 17.

LVDS, PECL or sinusoidal (Figure 18 and Figure 19) encode inputs are recommended to use for the differential encode mode. In the internal circuit, the encode inputs are biased to 1.2V with a 10K equivalent resistance. The maximal voltage level of encode inputs is 3.6V, so it is permitted to set encode input above V_{DD}. Fast rise and fall times of ENC+ is helpful for improving jitter performance. To minimize the probability of false triggering at the differential encode mode, ENC- ought to be set at least 200mV above ground. In the differential encode mode, the common mode voltage can vary from 1.1V to 1.6V.

CMOS encode inputs are used to drive single-ended encode mode. When using single-ended encode mode, the ENC+ and ENC- pins are driven with DC coupling. A square wave should be connected to ENC+ and ENC- should be connected to ground. Like to differential mode, the CMOS logic levels of ENC+ can support from 1.8V to 3.3V and can even go up to 3.6V. The input voltage level threshold of ENC+ is 0.9V. There should be fast rise and fall times of ENC+ in the single-ended mode, which will lead to good jitter performance.



NOTE:
1. Tie to V_{DD} for 2V range, tie to GND for 1V range. Range = 1.6 × V_{SENSE} for 0.625V < V_{SENSE} < 1.300V.

Figure 15. Reference Circuit

APPLICATION INFORMATION (continued)

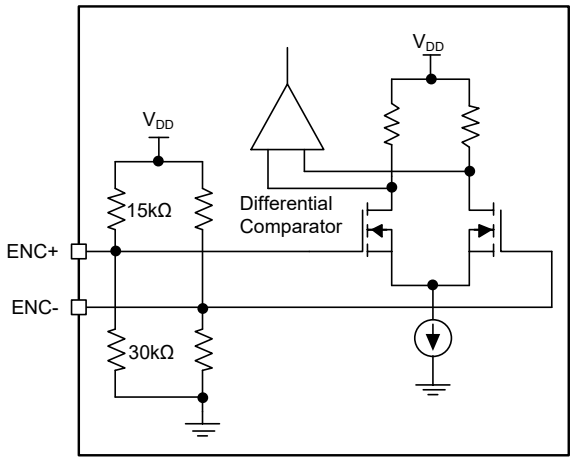


Figure 16. Equivalent Encode Input Circuit for Differential Encode Mode

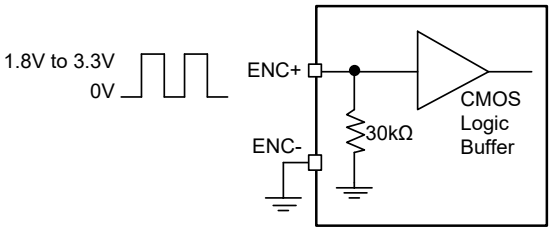
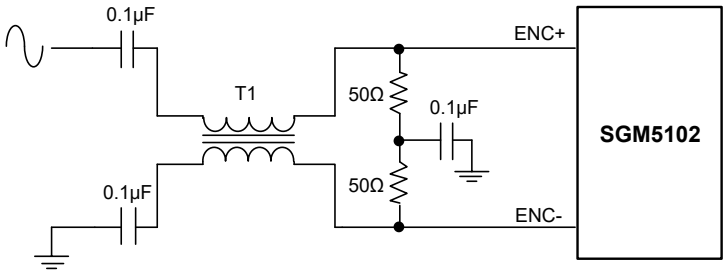


Figure 17. Equivalent Encode Input Circuit for Single-Ended Encode Mode



NOTE:
T1: MA/COM MABA-007159-000000.
Resistors, capacitors are 0402 package size.

Figure 18. Sinusoidal Encode Drive

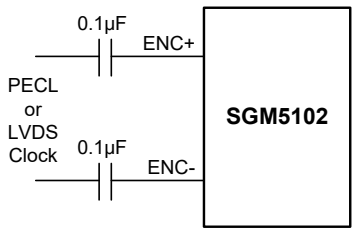


Figure 19. PECL or LVDS Encode Drive

APPLICATION INFORMATION (continued)

Clock PLL and Duty Cycle Stabilizer

In the SGM5102, there is an internal phase-locked loop (PLL), which is used to produce the serial digital output data by multiplying with the encode clock. The PLL would cost 25μs to lock onto the input clock again after the encode signal frequency is changed or switched off.

The duty cycle range of the input encode signal is up to 30% - 70% with the help of a clock duty cycle stabilizer circuit. The duty cycle stabilizer is enabled by default after powering on SGM5102. Although the SGM5102 provides the SPI interface to disable this duty cycle stabilizer in the serial programming mode, it is not recommended. It is not allowed to disable the duty cycle stabilizer at parallel programming mode.

In serial programming mode, the value of register A5 should be varied with the different frequency ENC, which is related to the PLL work mode. So, the user must set register A5 at first. If the ENC frequency is between 5MHz to 8MHz, set the register A5 to 00h. If the ENC frequency is between 8MHz to 16MHz, set the register A5 to 01h. If the ENC frequency is between 16MHz to 25MHz, set the register A5 to 02h.

In parallel programming mode, the input frequency range is 8MHz - 10MHz, and the device is operating in LPM mode.

Digital Outputs

The digital data output interfaces of the two ADC core are LVDS. 2-lane mode or 1-lane mode are supported by each ADC channel. For 2-lane mode, the digital data outputs two bits at a time, and for 1-lane mode, the digital data outputs one bit at a time. In addition, the interfaces support 12-, 14-, 16-bit serialization mode, which can be selected by register A2. It should be noted that the 12-bit serialization mode could result in 12-bit resolution instead of 14-bit resolution.

At the falling and rising edges of the data clock out (DCO), the output data bit would be latched. The rising edges of data frame output (FR) indicate the new conversion result begins. The frequency of FR is usually equal to sampling frequency, but for 2-lane, 14-bit serialization mode, the frequency of FR is equal to half of sampling frequency.

The maximum sample rate of ADC is decided by the serialization mode and the maximum sampling rate. Table 1 shows the maximum serial data rate at the different serialization modes. For 1-lane, 16-bit serialization mode, the data output rate can be up to 400MSPS.

After powering on the SGM5102, the LVDS interfaces would work at the standard levels: a 1.25V output common mode voltage and a 3.5mA output current. Each LVDS data output pair needs an external 100Ω differential termination resistor to convert current to voltage. The termination resistors can be configured to use the internal integrated resistors or added by the side of each LVDS pair. Note that the external termination resistors should be placed as close as possible to the LVDS interface pins.

OV_{DD} and OGND are isolated from the V_{DD} and GND, which are the ADC core power and ground.

Programmable LVDS Output Current

By default, the output driver current of LVDS interfaces is 3.5mA. In serial programming mode, the register A2 can be used to adjust the output current. There are six current levels to set: 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA. In parallel mode, the output driver current can be set to 1.75mA or 3.5mA by the SCLK pin.

Optional LVDS Driver Internal Termination

Usually, an external 100Ω termination resistor will help to optimize the LVDS signal integrity a lot. There is an optional internal 100Ω termination resistor, which can be enabled by setting bit 4 of control register A2 at serial programming mode or by setting SDO to high-level at parallel mode. To keep the same output voltage swing, the LVDS output driver current is doubled when enabling the 100Ω termination, so the internal termination can only be used with 1.75mA, 2.1mA or 2.5mA output current modes due to the current limits.

Table 1. Maximum Sampling Frequency for All Serialization Modes

Serialization Mode		Maximum Sampling Frequency, f_S (MHz)	DCO Frequency	FR Frequency	Serial Data Rate
2-Lane	16-Bit Serialization	25	4 • f_S	f_S	8 • f_S
2-Lane	14-Bit Serialization	25	3.5 • f_S	0.5 • f_S	7 • f_S
2-Lane	12-Bit Serialization	25	3 • f_S	f_S	6 • f_S
1-Lane	16-Bit Serialization	25	8 • f_S	f_S	16 • f_S
1-Lane	14-Bit Serialization	25	7 • f_S	f_S	14 • f_S
1-Lane	12-Bit Serialization	25	6 • f_S	f_S	12 • f_S

NOTE: The sampling frequency for the slower speed grades cannot exceed 25MHz for SGM5102.

APPLICATION INFORMATION (continued)

Data Format

In SGM5102, there are two different digital output code formats. The default format is offset binary, and the two's complement format can be selected by setting the control register A1 in serial programming mode. Below Table 2 describes the relationship between the analog input voltage and digital code.

Table 2. Output Codes vs. Input Voltage

AIN+ - AIN- (2V Range)	D13 - D0 (Offset Binary)	D13 - D0 (Two's Complement)
> 1.000000V	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	10 0000 0000 0001	00 0000 0000 0001
+0.000000V	10 0000 0000 0000	00 0000 0000 0000
-0.000122V	01 1111 1111 1111	11 1111 1111 1111
-0.000244V	01 1111 1111 1110	11 1111 1111 1110
-0.999878V	00 0000 0000 0001	10 0000 0000 0001
-1.000000V	00 0000 0000 0000	10 0000 0000 0000
≤ -1.000000V	00 0000 0000 0000	10 0000 0000 0000

Digital Output Randomizer

The A/D digital outputs are not always stable, which will be influenced by some interference from inductive or capacitive coupling or coupling through the ground plane. Dynamic parameters such as SFDR will become worse even if there exists one small digital interference. To reduce the amplitude of the harmful tone from digital interference, the SGM5102 supports the randomization of the digital output before it is transferred from the ADC.

When setting bit 6 of control register A1 at serial programming mode, the LVDS digital output codes would be randomized. The randomized data would be generated by applying an exclusive-OR logic operation between the LSB and all other data output bits. The FR and DCO are normal outputs. Inversely, the real output code can be decoded by applying an exclusive-OR operation between the LSB and all other bits again.

Digital Output Test Pattern

The SGM5102 provides a test mode for user to test the LVDS digital interface, which can be implemented by writing a known value to the control registers A3 and A4 at the serial programing mode, and then the A/D data outputs (D13-D0) would be forced to the test pattern code. In addition, when this test mode is enabled, the priority of test patterns is higher than all other LVDS formatting modes: two's complement and randomizer.

Output Disable

When working at the serial programming mode, the digital outputs of LVDS can be disabled with setting the control register A2. To save power or enable in-circuit testing, every digital output would be disabled. Besides, those differential impedance of every output pair may stay low, but the common mode becomes high impedance.

Sleep and Nap Modes

In addition to disable digital outputs, the A/D converter can also be set to work in sleep or nap modes to reduce power consumption. The sleep mode is used to power down the entire device, and the total power dissipation will downgrade to only 1mW. When connecting SDI to high-level in parallel programming mode or setting control register A1 in serial programming mode, the sleep mode of SGM5102 will be enabled. However, the size of the bypass capacitors on VREF, REFH and REFL decide the recovery time from power-down mode to normal work mode. Refer to Figure 14, the recovery time is around 2ms with this circuit.

For the SGM5102, there are four combinations of the two A/D channels to be powered down at nap mode. The internal reference circuit model and PLL circuit model will always stay active so that the chip can wake up quickly. Normally, it takes at least 100 clock cycles to recover from nap mode. Otherwise, an additional 50μs is also needed to get a high accurate DC setting, because the internal references would have to become stable from the sight temperature shift due to some supply current change as the A/D is away from nap mode. By setting control register A1 in the serial programming mode, the nap mode is enabled.

APPLICATION INFORMATION (continued)

Device Programming Modes

A simple parallel interface or a serial interface is allowed to program the control registers in the SGM5102. With the parallel interface, only a part of operating mode can be programmed. All the available modes can be programmed by the serial interface because of its greater flexibility. The PAR/nSER pin is used to select parallel interface or parallel interface.

Parallel Programming Mode

Connect PAR/nSER with V_{DD} to enable the parallel programming interface. The nCS, SCLK, SDI and SDO pins are tied to V_{DD} or ground, which are recognized as binary logic inputs to set certain operating modes of the SGM5102. These control pins are also driven by 1.8V, 2.5V or 3.3V CMOS logic. The SDO should be driven with a 1kΩ series resistor as an input pin. The detail operating modes set by nCS, SCLK, SDI and SDO are described as Table 3. Note that the parallel programming mode only supports 10MSPS.

Table 3. Parallel Programming Mode Control Bits (PAR/nSER = V_{DD})

PIN	DESCRIPTION
nCS	2-Lane/1-Lane Selection Bit 0 = 2-lane, 16-bit serialization output mode 1 = 1-lane, 14-bit serialization output mode
SCLK	LVDS Current Selection Bit 0 = 3.5mA LVDS current mode 1 = 1.75mA LVDS current mode
SDI	Power-Down Control Bit 0 = Normal operation 1 = Sleep mode
SDO	Internal Termination Selection Bit 0 = Internal termination disabled 1 = Internal termination enabled

Serial Programming Mode

Connect PAR/nSER with ground to enable the serial programming mode. For this programming interface, the nCS, SCLK, SDI and SDO pins are the normal SPI interface pins and can be used to program all the A/D mode control registers. The 16-bit data can be written by this interface and the registers data can also be read to check the value.

To start a serial data transfer, the nCS pin is taken low. At every rising edge of the first 16 SCLK cycles, the data bit is latched. Except for the first 16 SCLK rising edges, the other will be ignored. When nCS is taken high again, this data transfer ends.

The first transfer bit is the read/write (R/W) bit and the next seven bits are the register address (A[6:0]). The register data (D[7:0]) is the last eight bits. When writing the serial data to the register, the R/W bit is set to low logic. To read the data from one register address, the R/W bit should be set to high logic, and the data will be read back by the SDO pin. Refer to the Timing Diagrams section for the detail control timing logic.

Open-drain output is applied to SDO pin which is pulled to ground through a 200Ω impedance. An external 2kΩ pull-up resistor should be added when the register data is read back by SDO. However, the SDO can also be left floating if the serial data is just written. All the mode control registers are shown in Serial Programming Mode Register Map section.

For serial programming mode, the mode control registers are required to be programmed as soon as possible in case that the SGM5102 works unstably. Before configuring those control registers, the first serial command must be 0x0080, which will reset the device and all the register data will become 0. The bit D7 of register A0 will automatically become to logic 0 again after software reset.

APPLICATION INFORMATION (continued)

Serial Programming Mode Register Map (PAR/nSER = GND)

Register A0: Reset Register (Address = 00h, Default Value = 00h)

BITS	BIT NAME	DESCRIPTION
D[7]	RESET	Software Reset Bit 0 = Not used 1 = Software reset. All mode control registers are reset to 00h. The ADC is momentarily placed in sleep mode This bit is automatically set back to zero at the end of the SPI write command. The reset register is write only.
D[6:0]	Reserved	Unused. Don't care bits.

Register A1: Format and Power-Down Register (Address = 01h, Default Value = 00h)

BITS	BIT NAME	DESCRIPTION
D[7]	DCSOFF	Clock Duty Cycle Stabilizer Bit 0 = Clock duty cycle stabilizer on 1 = Clock duty cycle stabilizer off. This is not recommended
D[6]	RAND	Data Output Randomizer Mode Control Bit 0 = Data output randomizer mode off 1 = Data output randomizer mode on
D[5]	TWOSCOMP	Two's Complement Mode Control Bit 0 = Offset binary data format 1 = Two's complement data format
D[4] D[3] D[0]	SLEEP	Sleep Mode Control Bits 000 = Normal operation 0X1 = Channel 1 in nap mode 01X = Channel 2 in nap mode 1XX = Sleep mode. Both channels are disabled
D[2:1]	Reserved	Unused. Don't care bits.

Register A2: Output Mode Register (Address = 02h, Default Value = 00h)

BITS	BIT NAME	DESCRIPTION
D[7:5]	ILVDS[2:0]	LVDS Output Current Bits 000 = 3.5mA LVDS output driver current 001 = 4.0mA LVDS output driver current 010 = 4.5mA LVDS output driver current 011 = Not used 100 = 3.0mA LVDS output driver current 101 = 2.5mA LVDS output driver current 110 = 2.1mA LVDS output driver current 111 = 1.75mA LVDS output driver current
D[4]	TERMON	LVDS Internal Termination Bit 0 = Internal termination off 1 = Internal termination on. LVDS output driver current is 2× the Current Set by ILVDS[2:0]. Internal termination should only be used with 1.75mA, 2.1mA or 2.5mA LVDS output current modes
D[3]	OUTOFF	Output Disable Bit 0 = Digital outputs are enabled 1 = Digital outputs are disabled
D[2:0]	OUTMODE[2:0]	Digital Output Mode Control Bits 000 = 2-lanes, 16-bit serialization 001 = 2-lanes, 14-bit serialization 010 = 2-lanes, 12-bit serialization 011 = Not used 100 = Not used 101 = 1-lane, 14-bit serialization 110 = 1-lane, 12-bit serialization 111 = 1-lane, 16-bit serialization

APPLICATION INFORMATION (continued)

Register A3: Test Pattern MSB Register (Address = 03h, Default Value = 00h)

BITS	BIT NAME	DESCRIPTION
D[7]	OUTTEST	Digital Output Test Pattern Control Bit 0 = Digital output test pattern off 1 = Digital output test pattern on
D[6]	Reserved	Unused. Don't care bit.
D[5:0]	TP[13:8]	Test Pattern Data Bits (MSB) TP[13:8] set the test pattern for data bit 13 (MSB) through data bit 8.

Register A4: Test Pattern LSB Register (Address = 04h, Default Value = 00h)

BITS	BIT NAME	DESCRIPTION
D[7:0]	TP[7:0]	Test Pattern Data Bits (LSB) TP[7:0] set the test pattern for data bit 7 through data bit 0 (LSB).

Register A5: ENC Control Register (Address = 05h, Default Value = 15h)

BITS	BIT NAME	DESCRIPTION
D[7]	Reserved	Unused. Don't care bit.
D[6]	LPM	ADC LPM Mode for Conversion Clock ≤ 10MHz 0 = Disable ADC LPM mode for conversion clock ≤ 10MHz 1 = Enable ADC LPM mode for conversion clock ≤ 10MHz
D[5:2]	Reserved	Unused. Don't care bit.
D[1:0]	ENCFREQ	ENC Frequency Selection Bit 00 = ENC frequency 5MHz - 8MHz 01 = ENC frequency 8MHz - 16MHz 10 = ENC frequency 16MHz - 25MHz 11 = Forbidden

Grounding and Bypassing

The ground plane is very important for this high-speed ADC, so it is necessary to place a clean unbroken ground plane underneath the first layer with digital outputs layout on a printed circuit board. The separation of the analog and digital section of the PCB is required to reduce the interference from each other. It should be noted that any digital track alongside an analog signal or underneath the ADC is not allowed.

Bypass capacitors, especially high quality ceramic bypass capacitors, are essential for V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Place the bypass capacitors close to those pins as possible, which will help to reduce the noise from pins. For REFH and REFL, a 0.1μF capacitor is required to be placed between them and as close to the chip as possible (1.5mm or less). The size 0402 ceramic capacitors are preferred. A little further away, it is necessary to place a larger 2.2μF between REFH and REFL. To optimize the better current path, make the traces between the bypass capacitors and their respective pins as short and wide as possible.

Don't route the analog inputs, digital outputs and encode signals adjacent to each other. To avoid the interference from those signals, it is necessary to use the ground fill and grounded vias suitably.

Heat Transfer

For the SGM5102, the package leads and the bottom-side exposed pad can be directly soldered onto the printed circuit board, which will help to transfer most of the heat generated by the chip. For enhanced thermal, electrical and board level performance, the exposed pad must be soldered to the board using a large thermal grounded pad on the PCB. Moreover, it is necessary to place an array of vias at these internal ground planes.

REVISION HISTORY

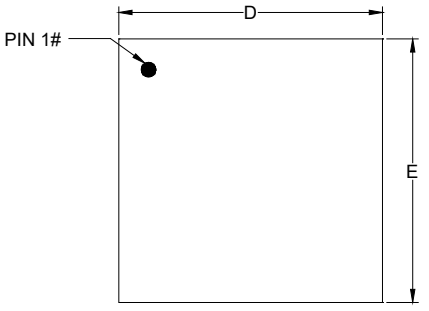
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2024 – REV.A to REV.A.1	Page
Updated Package/Ordering Information section	2

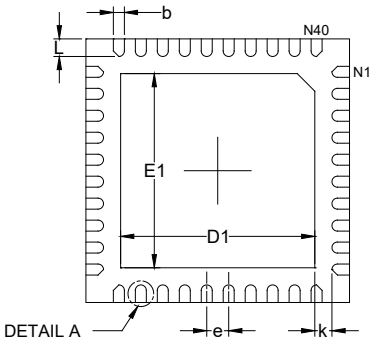
Changes from Original (JULY 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

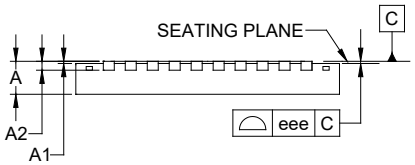
TQFN-6×6-40AL



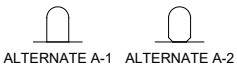
TOP VIEW



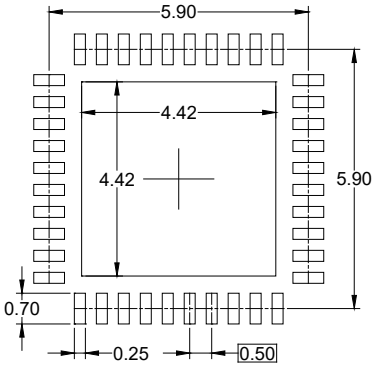
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



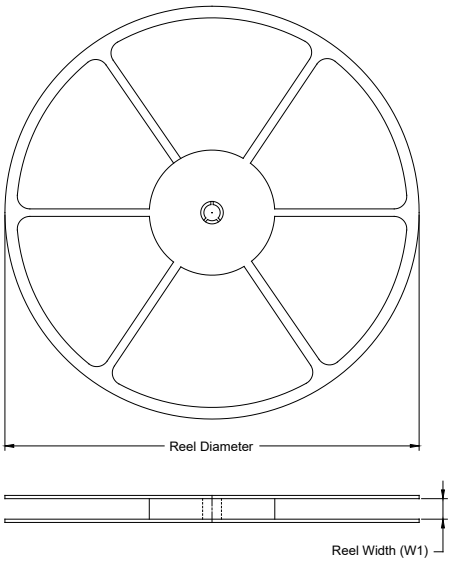
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	5.900	-	6.100
E	5.900	-	6.100
D1	4.320	-	4.520
E1	4.320	-	4.520
e	0.500 BSC		
k	0.390 REF		
L	0.300	-	0.500
eee	0.080		

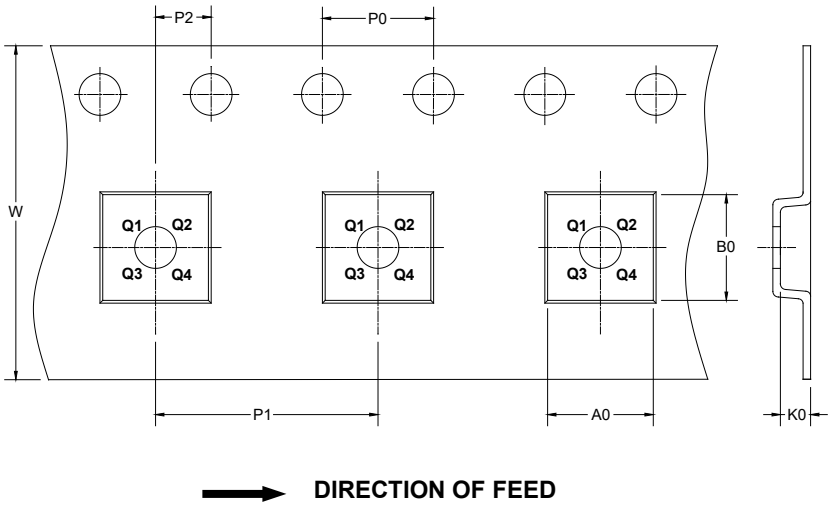
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



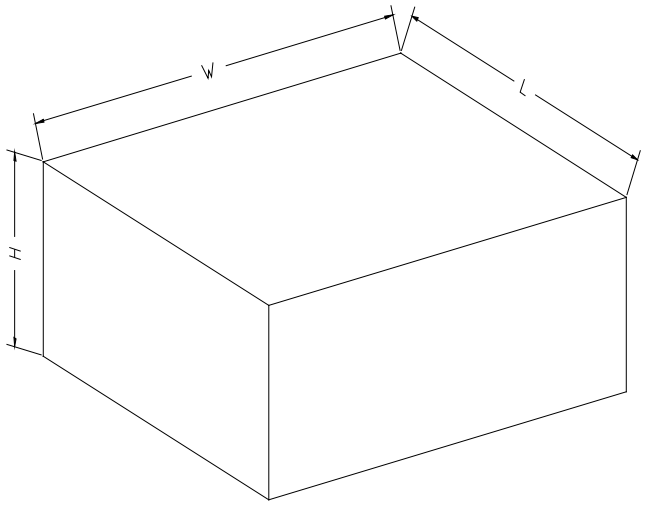
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-6×6-40AL	13″	16.4	6.40	6.40	1.40	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002